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MAX14588

1A Adjustable Overcurrent and Overvoltage Protector with High Accuracy

General Description

The MAX14588 adjustable overvoltage and overcurrent protection device is ideal for protecting systems against positive and negative input voltage faults up to ±40V, and feature low 190mΩ (typ) R_{ON} integrated FETs.

The adjustable overvoltage range is between 6V and 36V, while the adjustable undervoltage range is between 4.5V and 24V. The overvoltage lockout (OVLO) and undervoltage lockout (UVLO) thresholds are set using optional external resistors. The factory preset internal OVLO threshold is 33V (typ), and the preset internal UVLO threshold is 19V (typ).

The MAX14588 also features programmable current-limit protection up to 1A. The device can be set for autoretry, latch-off, or continuous fault response when an overcurrent event occurs. Once current reaches the threshold, the MAX14588 turns off after 21ms (typ) blanking time, and stays off during the retry period when set to autoretry mode. The device latches off after the blanking time when set to latch-off mode. The device limits the current continuously when set to continuous mode. The MAX14588 also features reverse current and thermal shutdown protection.

The MAX14588 is available in a small, 16-pin (3mm x 3mm) TQFN package. The MAX14588 operates over the -40°C to +125°C extended temperature range.

***Ordering Information* appears at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX14588.related**.*

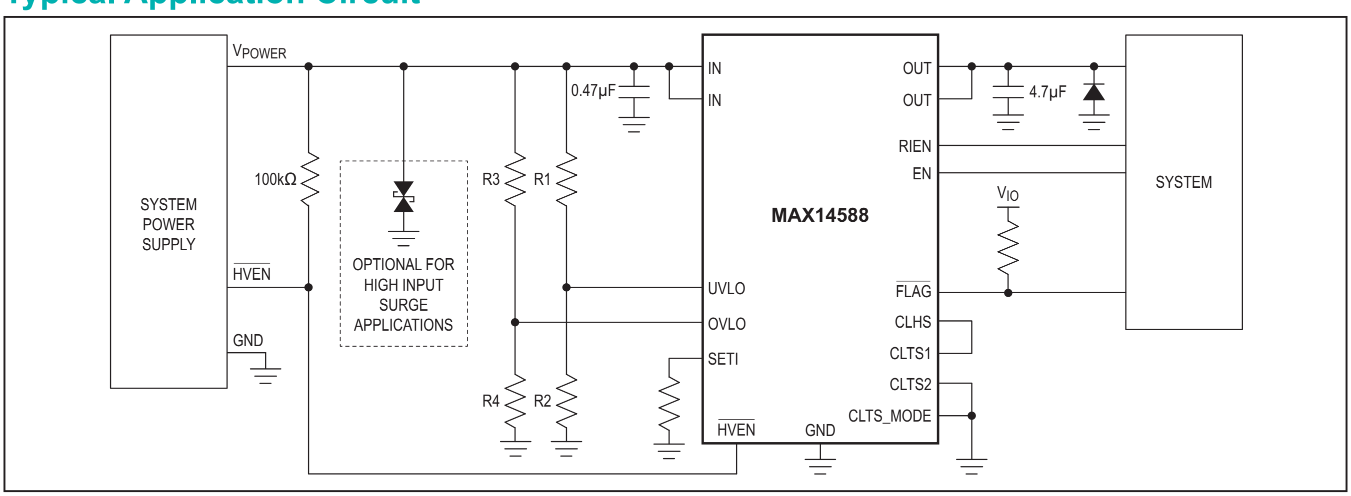
Benefits and Features

- Robust Industrial Power Protection
  - Wide Input Supply Range: +4.5V to +36V
  - Negative Input Tolerance to -36V
  - Low R_{ON} 190mΩ (typ)
  - Reverse Current Flow Control Input
  - Thermal Overload Protection
  - Extended -40ºC to +125ºC Temperature Range
- Flexible Design Options
  - Adjustable OVLO and UVLO Thresholds
  - Programmable Forward-Current Limit: 0.15A to 1A
  - Programmable Overcurrent Fault Response: Autoretry, Latch-Off, and Continuous
  - Dual Enable Inputs: EN and High Voltage $\overline{\text{HVEN}}$
- Saves Space
  - 16-Pin, 3mm x 3mm, TQFN Package

Applications

- Sensor Systems
- Condition Monitoring
- Factory Sensors
- Process Analytics
- Process Instrumentation
- Weighing and Batching Systems

Typical Application Circuit



19-6551; Rev 0; 12/12

Absolute Maximum Ratings

(All voltages referenced to GND.)
IN to GND ....-40V to +40V
IN to OUT ....-40V to +40V
OUT ....-0.3V to +40V
$\overline{\text{HVEN}}$ ....-40V to +40V
OVLO, UVLO, $\overline{\text{FLAG}}$, EN, RIEN,
CLTS1, CLTS2, CLTS_MODE ....-0.3V to +6V
SETI.. -0.3V to min(V_{IN}, 1.22V)+0.3V
CLHS .... -0.3V to min(V_{IN}, 5V)+0.3V

I_{IN} (DC Operating)(Note 1)..1.0A
Continuous Power Dissipation (T_A = +70ºC)
TQFN (derate 20.8mW/ºC above +70ºC) 1667mW
Operating Temperature Range.........................-40ºC to +125ºC
Maximum Junction Temperature ....+150ºC
Storage Temperature Range............................-65ºC to +150ºC
Lead Temperature (soldering, 10s) ....+300ºC
Soldering Temperature (reflow).....................................+260ºC

Note 1: DC current is also limited by the thermal design of the system.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 2)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA})...........48ºC/W
Junction-to-Case Thermal Resistance (θ_{JC})................10ºC/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = 4.5V to 36V, T_A = -40ºC to +125ºC, unless otherwise noted. Typical values are at V_{IN} = 24V, R_{SETI} = 12kΩ, T_A = +25ºC.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Voltage	V_{IN}		4.5		36	V
Shutdown IN Current	I_{SHDN}	V_{EN} = 0V, $V_{\overline{HVEN}}$ = 5V		6.6	16	µA
Shutdown OUT Current	I_{OFF}	V_{EN} = 0V, $V_{\overline{HVEN}}$ = 5V, V_{OUT} = 0V		0.1	2	µA
Reverse IN Current	I_{IN_RVS}	V_{IN} = -40V, V_{OUT} = V_{GND} = 0V	-35	-21		µA
Supply Current	I_{IN}	V_{IN} = 15V, $V_{\overline{HVEN}}$ = 0V		530	800	µA
Internal Overvoltage Trip Level	V_{OVLO}	V_{IN} rising	32	33	34.3	V
		V_{IN} falling	30.3	32	33.7	
Internal Undervoltage Trip Level	V_{UVLO}	V_{IN} falling	17.5	18.5	19.5	V
		V_{IN} rising	18.2	19.2	20.2	
Overvoltage Lockout Hysteresis		% of typical OVLO		3		%
External OVLO Adjustment Range		(Note 4)	6		36	V
External OVLO Select Threshold Voltage	V_{SEL_OVLO}		0.3	0.4	0.5	V
External OVLO Leakage	I_{OVLO_LEAK}	V_{OVLO} < 1.2V	-100		+100	nA
External UVLO Adjustment Range		(Note 4)	4.5		24	V
External UVLO Select Threshold Voltage	V_{SEL_UVLO}		0.3	0.4	0.5	V

Electrical Characteristics (continued)

(V_{IN} = 4.5V to 36V, T_A = -40ºC to +125ºC, unless otherwise noted. Typical values are at V_{IN} = 24V, R_{SETI} = 12kΩ, T_A = +25ºC.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External UVLO Leakage	I_{UVLO_LEAK}	V_{UVLO} < 1.2V	-100		+100	nA
BG Reference Voltage	V_{BG}		1.196	1.220	1.247	V
CLHS Voltage	V_{CLHS}	Source 100µA	23	3.5		V
INTERNAL FETs						
Internal FETs On-Resistance	R_{ON}	I_{LOAD} = 100mA, V_{IN} ≥ 8V		190	370	mΩ
Current-Limit Adjustment Range	I_{LIM}		0.15		1.0	A
Current-Limit Accuracy		0.15A ≤ I_{LIM} < 0.3A	-20		+20	%
		0.3A ≤ I_{LIM} < 1.0A	-10		+10	
$\overline{FLAG}$ Assertion Drop Voltage Threshold	V_{FA}	Increase (V_{IN} - V_{OUT}) drop until $\overline{FLAG}$ asserts, V_{IN} = 24V	400	600	800	mV
$\overline{FLAG}$ Output Logic-Low Voltage		I_{SINK} = 1mA			0.4	V
$\overline{FLAG}$ Output Leakage Current		V_{IN} = V_{FLAG} = 5V, flag deasserted			2	µA
Reverse-Current Blocking Threshold	V_{RIB}	V_{OUT} - V_{IN}	25	100	250	mV
Reverse-Blocking Supply Current	I_{RBL}	V_{OUT} - V_{IN} > 130mV, current into OUT		430	700	µA
LOGIC INPUTS						
$\overline{HVEN}$ Threshold Voltage	V_{HVENTH}		1	2	3.5	V
$\overline{HVEN}$ Threshold Hysteresis				2		%
$\overline{HVEN}$ Input Current	$I_{HVEN\_}$	$V_{\overline{HVEN}}$ = 36V		26	41	µA
$\overline{HVEN}$ Input Reverse Current	I_{HVEN_R}	V_{IN} = $V_{\overline{HVEN}}$ = -36V	-43	-28		µA
EN, RIEN, CLTS1, CLTS2, CLTS_MODE Input Logic-High	V_{IH}		1.4			V
EN, RIEN, CLTS1, CLTS2, CLTS_MODE Input Logic- Low	V_{IL}				0.4	V
EN, RIEN, CLTS1, CLTS2, CLTS_MODE Input Leakage Current	ILEAK	V_{LOGIC} = 5V	-1		+1	µA
DYNAMIC (NOTE 5)						
Switch Turn-On Time	t_{ON}	From OFF to ON (see Table 2), R_{LOAD} = 240Ω, C_{OUT} = 470µF		500		µs
Switch Turn-Off Time	t_{OFF}	From ON to OFF (see Table 2), R_{LOAD} = 47Ω, C_{OUT} = 1µF		3		µs
Overvoltage Switch Turn-Off Time	t_{OFF_OVP}	From (V_{IN} > V_{OVLO}) to (V_{OUT} = 80% of V_{IN_OVLO}), R_{LOAD} = 47Ω		3		µs
Overcurrent Switch Turn-Off Time	t_{OFF_OCP}	After t_{BLANK}		3		µs

Electrical Characteristics (continued)

(V_{IN} = 4.5V to 36V, T_A = -40ºC to +125ºC, unless otherwise noted. Typical values are at V_{IN} = 24V, R_{SETI} = 12kΩ, T_A = +25ºC.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Debounce Time	t_{DEB}	From (V_{IN_UVLO} < V_{IN} < V_{IN_OVLO}) and (EN = high or $\overline{HVEN}$ = low) to V_{OUT} = 10% of V_{IN}	14	16.5	19	ms
Blanking Time	t_{BLANK}		17.8	21	24.1	ms
Autoretry Time	t_{RETRY}	After blanking time from I_{OUT} > I_{LIM} to $\overline{FLAG}$ deasserted	527	620	713	ms
THERMAL PROTECTION						
Thermal Shutdown				150		ºC
Thermal Shutdown Hysteresis				30		ºC

Note 3: All devices are 100% production tested at T_A = + 25ºC. Specifications over the operating temperature range are guaranteed by design.

Note 4: All timing is measured using 20% and 80% levels.

Timing Diagrams

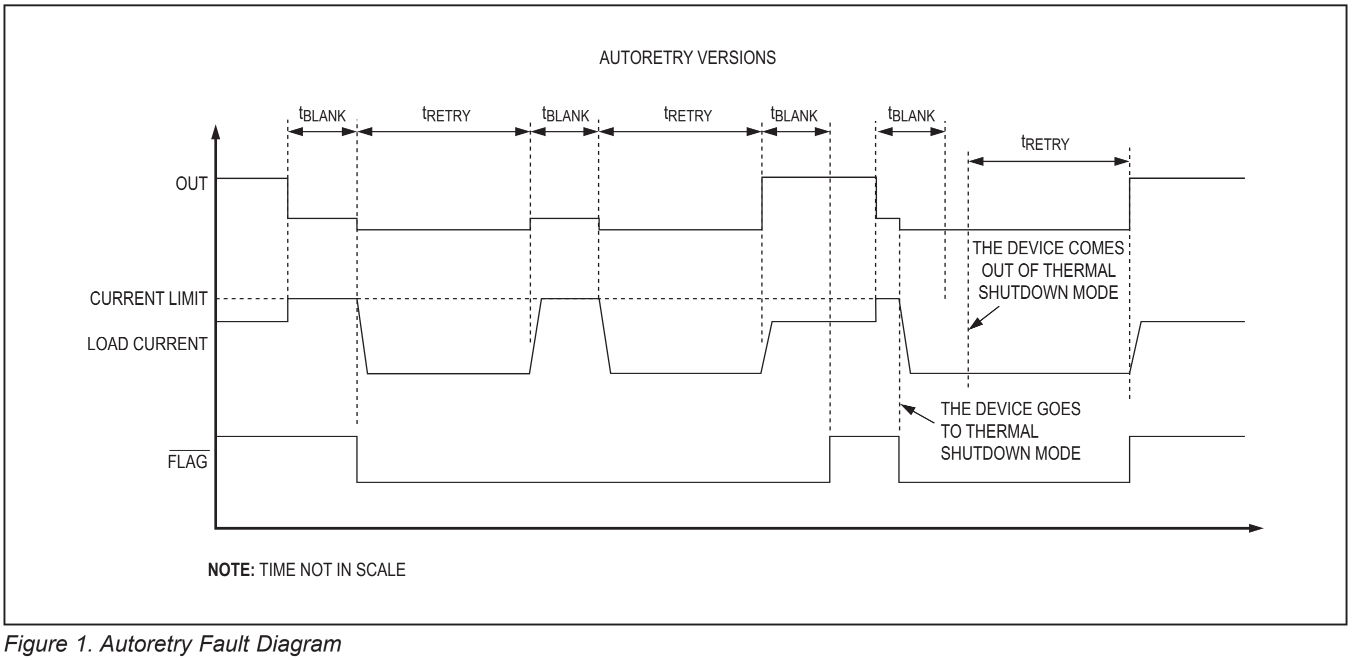


Figure 1. Autoretry Fault Diagram

Timing Diagrams (continued)

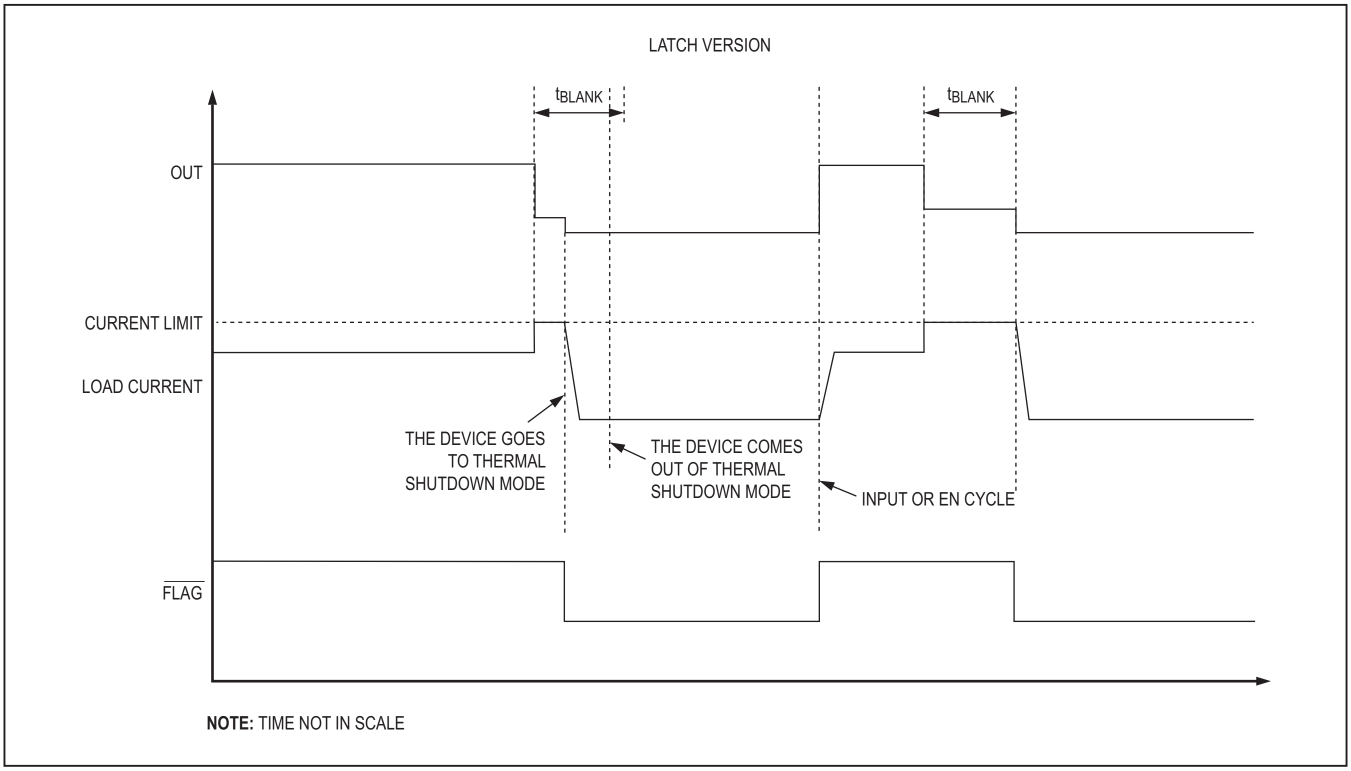


Figure 2. Latchoff Fault Diagram

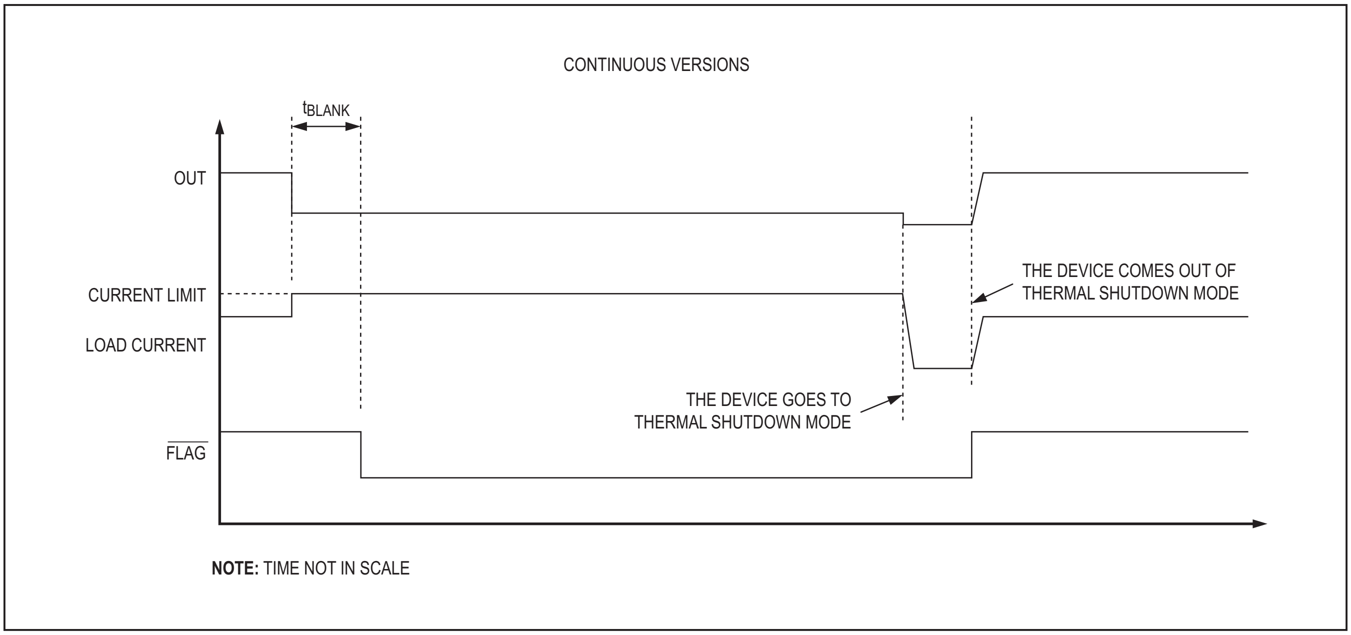


Figure 3. Continuous Fault Diagram

Timing Diagrams (continued)

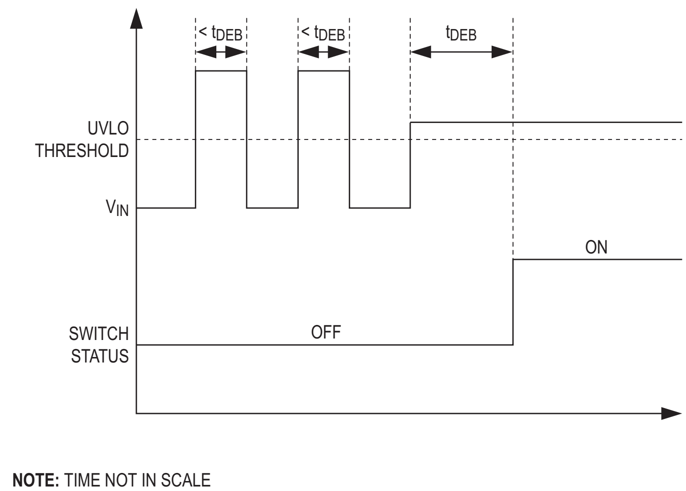
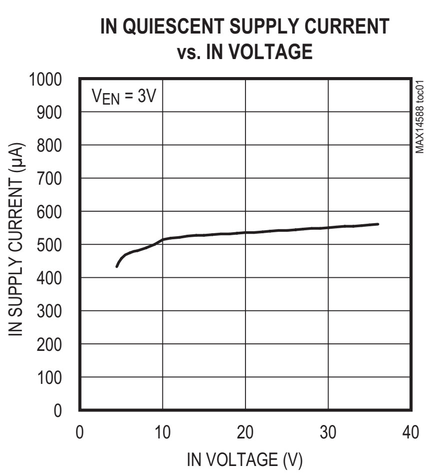
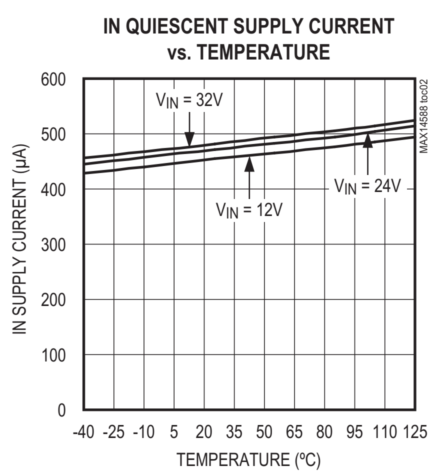


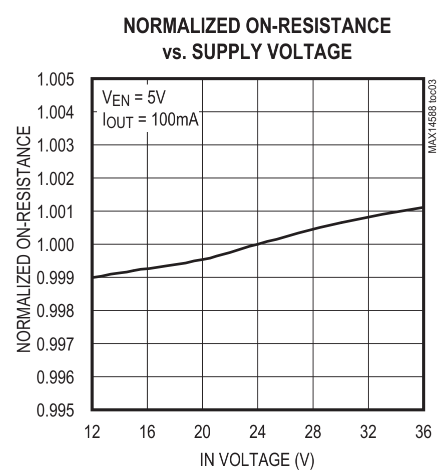
Figure 4. Debounce Timing

Typical Operating Characteristics

(C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)



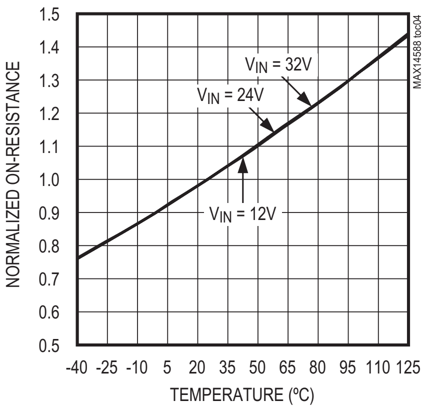




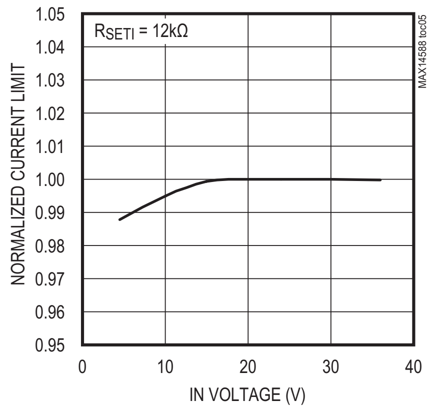
Typical Operating Characteristics (continued)

(C_{IN} = 1µF, C_{OUT} = 1µF, T_A = +25°C, unless otherwise noted.)

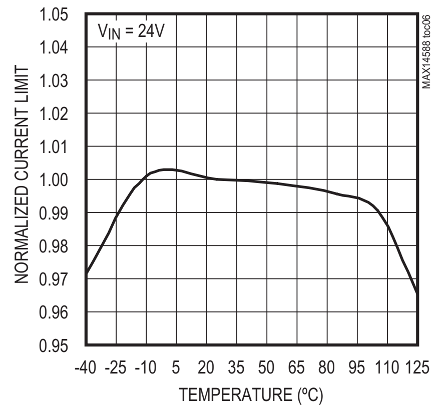
NORMALIZED ON-RESISTANCE vs. TEMPERATURE



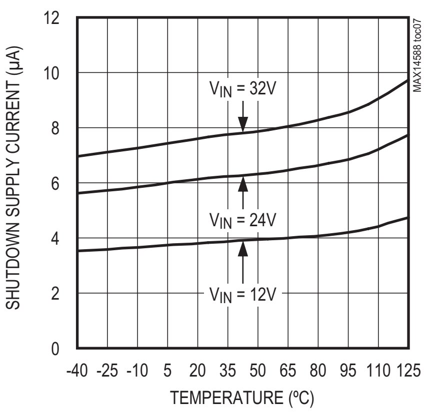
NORMALIZED CURRENT LIMIT vs. SUPPLY VOLTAGE



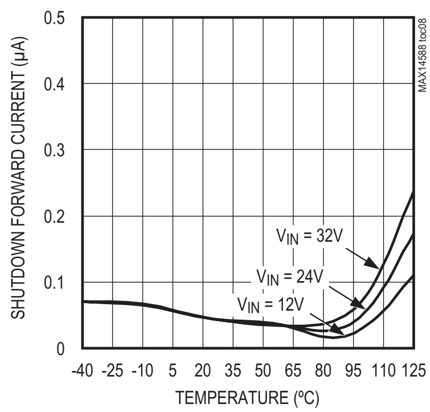
NORMALIZED CURRENT LIMIT vs. TEMPERATURE



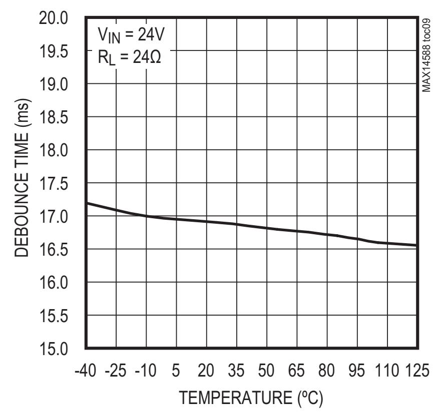
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



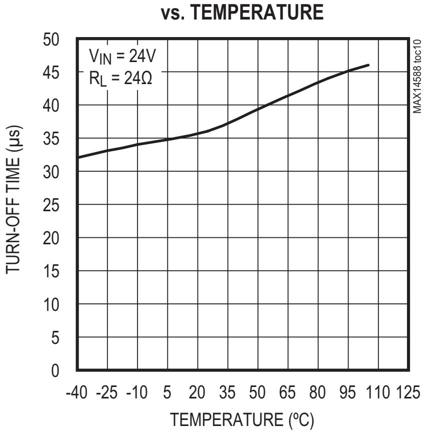
SHUTDOWN FORWARD CURRENT vs. TEMPERATURE



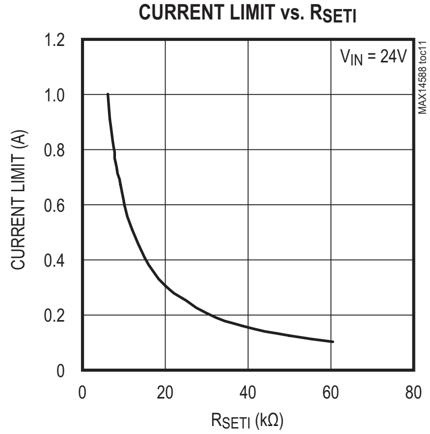
SWITCH DEBOUNCE TIME vs. TEMPERATURE



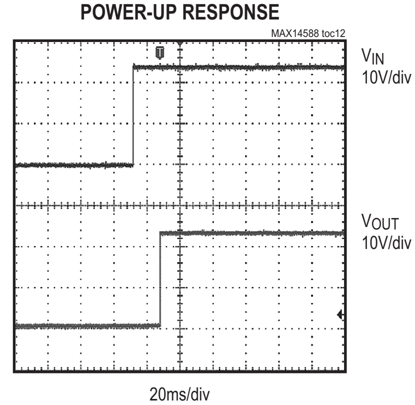
SWITCH TURN-OFF TIME vs. TEMPERATURE



CURRENT LIMIT vs. R_{SETI}

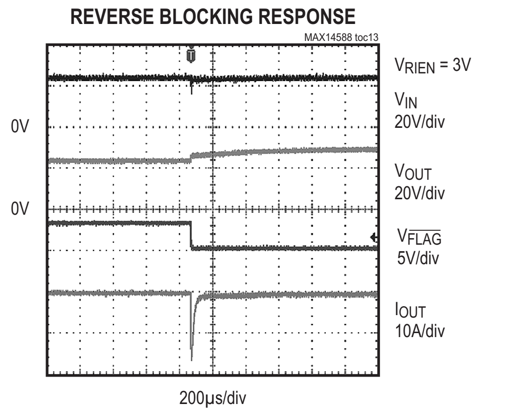


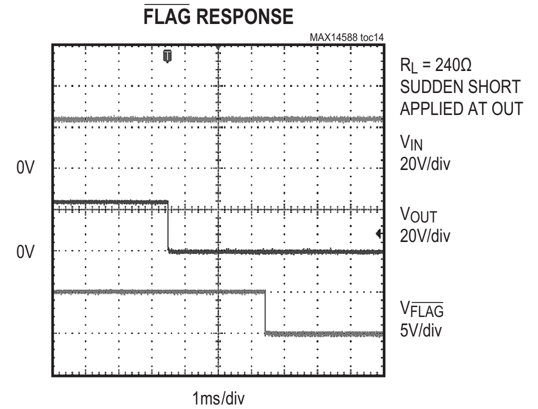
POWER-UP RESPONSE

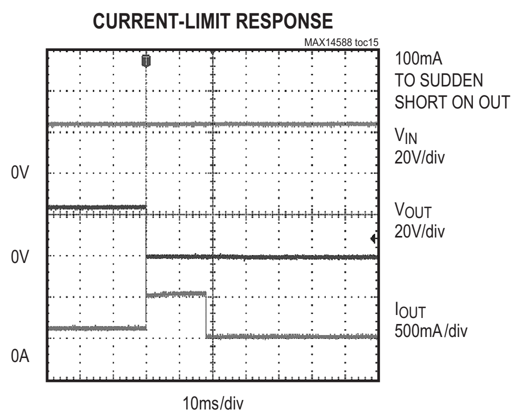


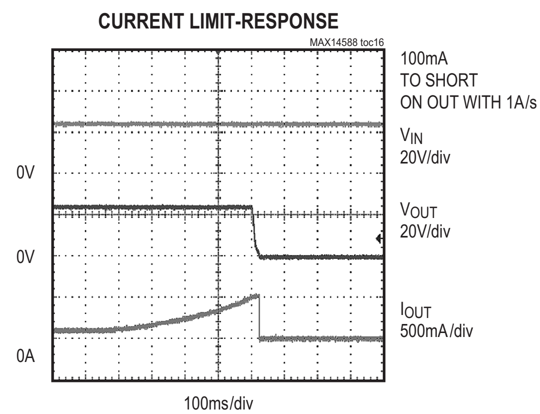
Typical Operating Characteristics (continued)

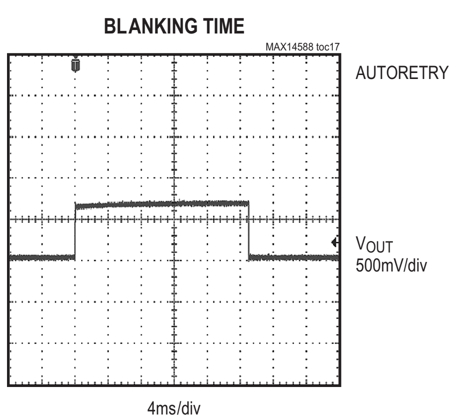
(C_{IN} = 1μF, C_{OUT} = 1μF, T_A = +25°C, unless otherwise noted.)

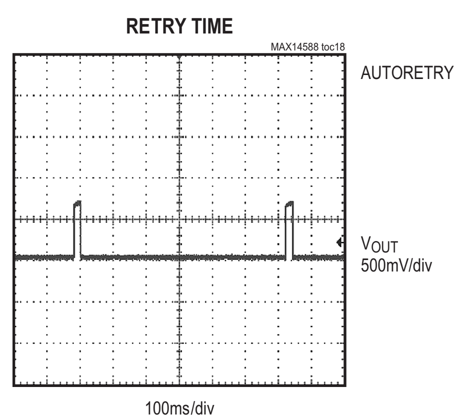




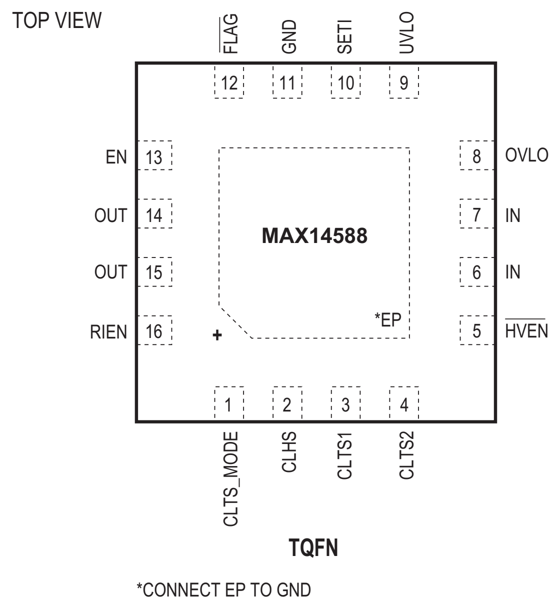








Pin Configuration



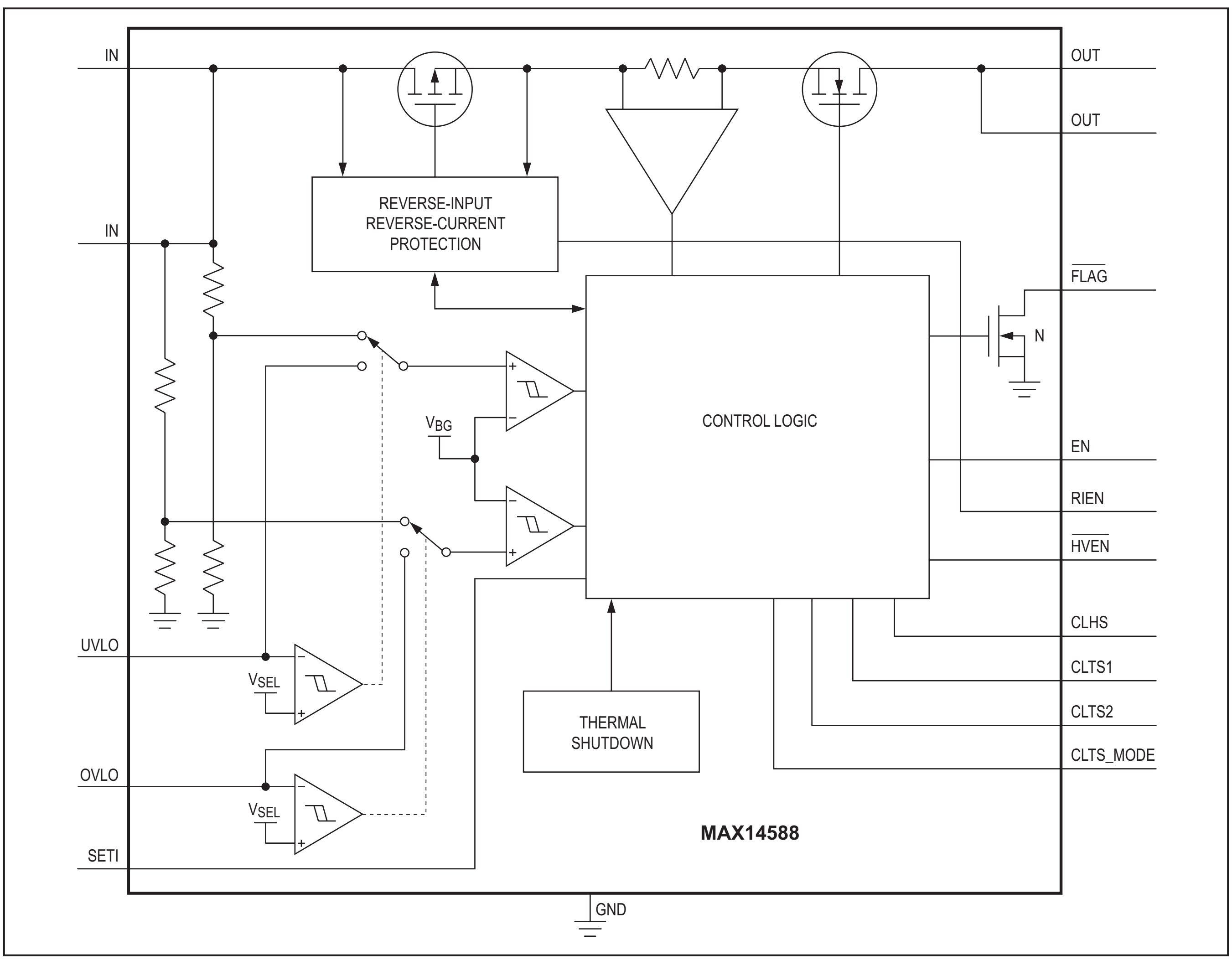
Pin Description

PIN	NAME	FUNCTION
1	CLTS_MODE	Current-Limit-Type Select Mode. CLTS_MODE = 0: CLTS1 and CLTS2 are sampled only when (V_{IN} – V_{OUT}) < 0.6V. CLTS_MODE = 1: CLTS1 and CLTS2 are continuously sampled.
2	CLHS	Current-Limit-Type-Select Logic-High Voltage. Connect CLTS_MODE/CLTS1/CLTS2 to CLHS for logic-high.
3	CLTS1	Current-Limit-Type Select 1. See Table 1.
4	CLTS2	Current-Limit-Type Select 2. See Table 1.
5	$\overline{HVEN}$	36V Capable Active-Low Enable Input. See Table 2.
6, 7	IN	Overvoltage Protection Input. Bypass IN to ground with a 0.47μF ceramic capacitor.
8	OVLO	Externally Programmable Overvoltage Lockout Threshold. Connect OVLO to GND to use the default internal OVLO threshold. Connect OVLO to an external resistor-divider to define a threshold externally and override the preset internal OVLO threshold.
9	UVLO	Externally Programmable Undervoltage Lockout Threshold. Connect UVLO to GND to use the default internal UVLO threshold. Connect UVLO to an external resistor-divider to define a threshold externally and override the preset internal UVLO threshold.
10	SETI	Overload-Current-Limit Adjust. Connect a resistor from SETI to GND to program the overcurrent limit. SETI must be connected to a resistor. If SETI is connected to GND, the FETs turn off and $\overline{FLAG}$ is asserted. Do not connect more than 10pF to SETI.
11	GND	Ground

Pin Description (continued)

PIN	NAME	FUNCTION
12	$\overline{FLAG}$	Open-Drain Fault Indicator Output. $\overline{FLAG}$ goes low when the fault duration exceeds the blanking time, reverse current is detected, thermal shutdown mode is active, OVLO threshold is reached, or SETI is connected to GND.
13	EN	Active-High Enable Input. See Table 2.
14,15	OUT	Output Voltage. Output of internal FETs. Bypass OUT to GND with a 1µF ceramic capacitor placed as close to the device as possible.
16	RIEN	Reverse-Current Enable Input. Connect RIEN to GND to disable the reverse-current flow protection. Connect RIEN to logic-high to activate the reverse-current flow protection.
—	EP	Exposed Pad. Connect EP to ground. Do not use EP as the only ground connection.

Functional Diagram



Detailed Description

The MAX14588 is an adjustable overvoltage and overcurrent protection device designed to protect systems against positive and negative input voltage faults up to ±40V, and features a low 190mΩ (typ) on-resistance FET. If the input voltage exceeds the OVLO threshold or falls below the UVLO, the internal FETs are turned off to prevent damage to the protected components. If the OVLO or the UVLO pin is set below the external OVLO or UVLO select threshold (V_{SEL_OVLO}, V_{SEL_UVLO}), the device automatically selects the internal ±5% accurate trip thresholds. The internal OVLO threshold is preset to 33V (typ), and the internal UVLO threshold is preset to 19V (typ).

Current-Limit Type Select

The MAX14588 power-up current-limit default is continuous mode when CLTS_MODE is low. After power up, the current-limit type can be programmed externally through CLTS1 and CLTS2 (Table 1). When CLTS_MODE is high, CLTS1 and CLTS2 are sampled continuously. When CLTS_MODE is low, CLTS1 and CLTS2 are sampled only when V_{IN}-V_{OUT} < 0.6V. Connect CLTS1, CLTS2, and CLTS_MODE to CLHS for logic-high or to GND for logic-low.

Autoretry

When the current threshold is reached, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ asserts if the overcurrent condition is present for t_{BLANK} .The timer resets if the overcurrent condition disappears before t_{BLANK} has elapsed. A retry time delay, t_{RETRY}, is started immediately after t_{BLANK} has elapsed and during t_{RETRY} time, the FETs are off. At the end of t_{RETRY}, the FETs are turned on again. If the fault still exists, the cycle is repeated and the $\overline{FLAG}$ stays low. When the fault is removed, the FETs stay on. (Figure 1)

Table 1. Current-Limit Type Select

CLTS2	CLTS1	CURRENT-LIMIT TYPE
0	0	LATCH OFF
0	1	AUTORETRY
1	0	CONTINUOUS
1	1	CONTINUOUS

The autoretry feature reduces the system power in case of overcurrent or short-circuit conditions. During t_{BLANK} time, when the switch is on, the supply current is held at the current limit. During t_{RETRY} time, when the switch is off, there is no current through the switch. Thus, the output current is much less than the programmed current limit. Calculate the average output current using the following equation.

$$I_{LOAD} = I_{LIM}\left[\frac{t_{BLANK}}{t_{BLANK} + t_{RETRY}}\right]$$

With a 21ms (typ) t_{BLANK} and 620ms (typ) t_{RETRY}, the duty cycle is 3.3%, resulting in a 96.7% power saving.

Latch-Off

When the current threshold is reached, the t_{BLANK} timer begins counting. The $\overline{FLAG}$ asserts if the overcurrent condition is present for t_{BLANK} .The timer resets when the overcurrent condition disappears before t_{BLANK} has elapsed. The switch turns off and stays off if the overcurrent condition continues beyond the blanking time. To reset the switch, either toggle the control logic EN or $\overline{HVEN}$ or cycle the input voltage. (Figure 2)

Continuous

When the current threshold is reached, the MAX14588 limits the output current to the programmed current limit. The $\overline{FLAG}$ asserts if the overcurrent condition is present for t_{BLANK} and deasserts when the overload condition is removed. (Figure 3)

Reverse-Current Block Enable (RIEN)

This feature disables the reverse-current protection and enables reverse-current flow from OUT to IN. The reverse-current block enable feature is useful in applications with inductive loads.

Fault Flag Output

$\overline{FLAG}$ is an open-drain fault indicator output and requires an external pull-up resistor to a DC supply. $\overline{FLAG}$ goes low when any of the following conditions occur:

- The blanking time has elapsed
- The reverse-current protection has tripped
- The die temperature exceeds +150ºC
- SETI is connected to ground
- OVLO threshold is reached

Thermal Shutdown Protection

The MAX14588 has a thermal-shutdown feature to protect the device from overheating. The device turns off and the $\overline{FLAG}$ asserts when the junction temperature exceeds +150ºC (typ). The devices exit thermal shutdown and resume normal operation after the junction temperature cools by 30ºC (typ), except when in latch off mode, the device remains latched off.

The thermal limit behaves similar to the current limit. For autoretry mode, the thermal limit works with auto retry timer. When the device comes out of the thermal limit, it starts after the retry time. For latch off mode, the device latches off until power or EN cycle. For continuous mode, the device only disables while the temperature is over the limit. There is no blanking time for thermal protection.

Overvoltage Lockout (OVLO)

The MAX14588 has a 33V (typ) preset OVLO threshold when the voltage at OVLO is set below the external OVLO select voltage (V_{SEL}). Connect OVLO to GND to activate the preset OVLO threshold. Connect the external resistors to OVLO pin as shown in the *Typical Operating Circuit* to externally adjust the OVLO threshold. Use the following equation to adjust the OVLO threshold. The recommended value for R3 is 2.2MΩ.

$$V_{OVLO} = V_{BG} \times \left[1 + \frac{R3}{R4}\right]$$

Undervoltage Lockout (UVLO)

The MAX14588 has a 19V (typ) preset UVLO threshold when the voltage at UVLO is set below the external OVLO select voltage (V_{SEL}). Connect UVLO to GND to activate the preset UVLO threshold. Connect the external resistors to UVLO pin as shown in the *Typical Operating Circuit* to externally adjust the UVLO threshold. Use the following equation to adjust the UVLO threshold. The recommended value for R1 is 2.2MΩ.

$$V_{UVLO} = V_{BG} \times \left[1 + \frac{R1}{R2}\right]$$

Switch Control

There are two independent enable inputs ($\overline{HVEN}$ and EN) for MAX14588. $\overline{HVEN}$ is a high-voltage capable input. Toggle $\overline{HVEN}$ or EN to reset the fault condition once short-circuit is detected and the device shuts down (Table 2).

Input Debounce Protection

The MAX14588 features input debounce protection. When the input voltage is higher than the UVLO threshold voltage for a period greater than the debounce time (t_{DEB}), the internal FETs are turned on. This feature is intended for applications where the EN or $\overline{HVEN}$ signal is present when the power supply ramps up (Figure 3).

Applications Information

Setting the Current Limit / Threshold

A resistor from SETI to ground programs the current-limit/threshold value for the MAX14588. Leaving SETI unconnected selects a 0A current limit/threshold. Connecting SETI to ground asserts $\overline{FLAG}$.

Use the following formula to calculate the current limit:

$$R_{SETI}(k\Omega) = \frac{6100}{I_{LIM}(mA)}$$

IN Bypass Capacitor

Connect a minimum of 0.47μF capacitor from IN to GND to limit the input voltage drop during momentary output short-circuit conditions. Larger capacitor values further reduce the voltage undershoot at the input.

Hot Plug IN

In many system powering applications, an input filtering capacitor is required to lower the radiated emission, enhance the ESD capability, etc. In hot plug applications, parasitic cable inductance along with the input capacitor causes overshoot and ringing when the powered cable is connected to the input terminal.

This effect causes the protection device to see almost twice the applied voltage. An input voltage of 24V can easily exceed the absolute maximum rating of 40V, which may permanently damage the device. A transient voltage suppressor (TVS) is often used for industrial applications to protect the system from these conditions. We recommend using a TVS that is capable of limiting the input surge to 40V placed close to the input terminal.

Table 2. Enable Inputs

$\overline{HVEN}$	EN	SWITCH STATUS
0	0	ON
0	1	ON
1	0	OFF
1	1	ON

OUT Bypass Capacitor

For stable operation over the full temperature range and over the entire programmable current-limit range, connect a 4.7μF ceramic capacitor from OUT to ground. Excessive output capacitance can cause a false overcurrent condition due to decreased dv/dt across the capacitor. Calculate the maximum capacitive load (C_{MAX}) value that can be connected to OUT by using the following formula:

$$C_{MAX}(\mu F) = \frac{I_{LIM}\ (mA) \times t_{BLANK(TYP)}\ (ms)}{V_{IN}(V)}$$

For example, for V_{IN} = 24V, $t_{BLANK(TYP)}$ = 20ms, and I_{LIM} = 1A, C_{MAX} equals 833μF.

Output Freewheeling Diode for Inductive Hard Short to Ground

In applications that require protection form a sudden short to ground with an inductive load or a long cable, a schottky diode between the OUT terminal and ground is recommended. This is to prevent a negative spike on the OUT due to the inductive kickback during a short-circuit event.

Layout and Thermal Dissipation

To optimize the switch response time to output short-circuit conditions, it is very important to keep all traces as short as possible to reduce the effect of undesirable parasitic inductance. Place input and output capacitors as close as possible to the device (no more than 5mm). IN and OUT must be connected with wide short traces to the power bus. During normal operation, the power dissipation is small and the package temperature change is minimal. If the output is continuously shorted to ground at the maximum supply voltage, the switches with the autoretry option do not cause thermal shutdown detection to trip:

$$P_{(MAX)} = \frac{V_{IN(MAX)} \times I_{OUT(MAX)} \times t_{BLANK}}{t_{RETRY} + t_{BLANK}}$$

Attention must be given to continuous current-limit mode when the power dissipation during a fault condition can cause the device to reach the thermal shutdown threshold. Thermal vias from the exposed pad to ground plane are highly recommended to increase the system thermal capacitance while reducing the thermal resistance to the ambient.

Ordering Information

PART	TEMP RANGE	TOP MARK	PIN-PACKAGE
MAX14588ETE+T	-40ºC to +125ºC	AJZ	16 TQFN-EP*

+ Denotes a lead(Pb)-free package/RoHS-compliant package.

T = Tape and reel

**EP = Exposed Pad*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN-EP	T1633+5	**21-0136**	**90-0032**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/12	Initial release	—

