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# MAX14616/MAX14616A

# Micro-USB Interface Circuit Plus Intelligent Li+ Battery Chargers

## General Description

The MAX14616/MAX14616A are a complete solution for interfacing to a micro-USB connector and include an advanced charger detection block, a linear battery charger, and a switch block capable of multiplexing USB, UART, audio, and composite video signals. The devices include an LED driver for battery charge status and battery present detection.

The MAX14616/MAX14616A support multiplexing USB 2.0 Hi-Speed, UART, and stereo audio signals with a single micro-USB connector. The USB channel features low 3Ω (typ) on-resistance and 7pF (typ) on capacitance to minimize USB signal degradation. The audio inputs feature negative rail signal operation down to -2V and 0.1Ω on-resistance flatness for low THD.

The MAX14616/MAX14616A charger detection block supports USB Battery Charger Detection Revision 1.1 requirements and also detects many common non-USB-defined power adapters. The SFOUT LDO provides a voltage-limited USB VBUS output for powering devices such as USB transceivers that cannot withstand high voltage. The MAX14616/MAX14616A include a composite video cable unplug detector capable of detecting the removal of a video termination resistor.

The MAX14616/MAX14616A battery charger adds a battery present detector to automatically disable the battery charger in case the battery is removed. They also include an open-drain LED driver to indicate the battery charger operation status.

The MAX14616/MAX14616A are available in a 25-bump (2mm x 2mm, 0.4mm pitch) WLP package and operates over the -40°C to +85°C extended temperature range.

## Applications

- Media Players
- Cell Phones
- Digital Cameras
- eReaders
- Tablets

## Benefits and Features

- High Level of Integration
  - Complete Solution for Micro-USB Connector Multiplexing
    - USB 2.0 Hi-Speed Switch with 3Ω (typ) On-Resistance
    - Negative-Rail Audio Inputs with Low THD
    - Detection Logic for Accessory Identification
    - Composite Video Load Removal Detection
- Internal Li+ Battery Charger with +28V (max) Input
- USB Battery Charger Detection
  - Supports USB BC1.1 with Advanced Features from USB BC1.2
  - Data Contact Detection (DCD) Support
  - USB DCP, SDP, and CDP Detection
  - Non-USB Defined Charger Detection Capability
- High-Voltage Protected LDO for USB Transceiver
- Charger Status LED Output Driver
- Battery Presence Monitor
- High-ESD Protection on COMN1, COMP2, and UID
  - ±15kV for Human Body Model
  - ±10kV for IEC 61000-4-2 Air Gap Discharge
  - ±7kV for IEC 61000-4-2 Contact Discharge
- Saves Power in Portable Application
  - Low Supply Current
- Saves Space
  - 25-Bump, 2mm x 2mm, WLP Package

***Ordering Information* appears at end of data sheet.**

*19-6180; Rev 1; 6/12*

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## Absolute Maximum Ratings

(All voltages referenced to GND.)
BAT, JIG, $V_{IO}$, $\overline{INT}$, THM .....-0.3V to +6V
LED.....-0.3V to +6V
VB (Charger Mode) .....0.3V to +30V
VB (Microphone Mode) (Note 1) .....-0.3V to ($V_{SWPOS}$ + 0.3V)
SFOUT–VB.....+0.3V
CAP .....-0.3V to +4V
SDA, SCL .....-0.3V to ($V_{BAT}$ + 0.3V)
SWITCH ENABLED or CPEn = 1 (Note 1)
SL1, SR2, COMN1, COMP2, UID, MIC,
IDB, DN1, DP2 .....-2.1V to ($V_{SWPOS}$ + 0.3V)
UT1, UR2.....-0.3V to ($V_{SWPOS}$ + 0.3V)
SWITCH DISABLED and CPEn = 0 (Note 2)
SL1, SR2, MIC, IDB, DN1, DP2,
UT1, UR2.....-0.3V to ($V_{CCINT}$ + 0.3V)
COMN1, COMP2, UID .....-0.3V to +6V
Continuous Current into COMN1, COMP2 .....±200mA
Continuous Current into BAT, VB .....±1300mA
Continuous Current into All Other Bumps.....±100mA
Continuous Power Dissipation ($T_A$ = +70°C)
WLP (derate 19.2mW/°C above +70°C).....1536mW
Operating Temperature Range..... -40°C to +85°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow) (Note 3).....+260°C

**Note 1:** $V_{SWPOS}$ = min($V_{CCINT}$, +3.3V)
**Note 2:** $V_{CCINT}$ = max($V_{BAT}$, min($V_{VB}$, +4V))
**Note 3:** The WLP package is constructed using a unique set of package techniques that impose a limit on the thermal profile that the device can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Thermal Characteristics (Note 4)

WLP
Junction-to-Ambient Thermal Resistance ($\theta_{JA}$) .....52°C/W

**Note 4:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{BAT}$ = 2.8V to 5.5V, $V_{VB}$ = 3.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{BAT}$ = 3.6V, $V_{VB}$ = 5.0V, $T_A$ = +25°C.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Voltage | $V_{BAT}$ | | | 2.8 | | 5.5 | V |
| | $V_{VB}$ | | | 3.5 | | 28 | |
| | $V_{IO}$ | | | 1.6 | | 5.5 | |
| Allowed VB Input-Voltage Range | $V_{VB}$ | | | 0 | | 28 | V |
| BAT Undervoltage Lockout Threshold | $V_{UVLO}$ | | | 0.4 | 2.0 | 2.65 | V |
| BAT Supply Current | $I_{BAT}$ | $V_{BAT}$ = 3.6V, $V_{VB}$ = 0V, no accessory attached | Low-power mode, LowPwr = 1, CPEn =0, ADCEn = 0 | | 3 | 6 | µA |
| | | | LowPwr = 0, CPEn = 0 | | 28 | 50 | |
| | | | LowPwr = 0, CPEn = 1 | | 45 | 65 | |

## Electrical Characteristics (continued)

($V_{BAT}$ = 2.8V to 5.5V, $V_{VB}$ = 3.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{BAT}$ = 3.6V, $V_{VB}$ = 5.0V, $T_A$ = +25°C.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| VB Supply Current | $I_{VB}$ | $V_{BAT}$ = 0V, $I_{OUT}$ = 0mA, charger forced off | $V_{VB}$ = 5V, CPEn = 0, MBCHOSTEN = 0, SFOUT is off, UID = open | | 350 | 500 | µA |
| | | | $V_{VB}$ = 5V, CPEn = 0, MBCHOSTEN= 0, SFOUT is on, UID = open | | 470 | 3000 | |
| $V_{IO}$ Supply Current | $I_{IO}$ | LED = unconnected | | | 0.1 | 1 | µA |
| Internal VB Regulator Voltage | $V_{PVB}$ | | | 3.3 | 4 | 5.5 | V |
| Internal Positive Regulator Voltage for Switches | $V_{SWPOS}$ | | | 3.3 | 3.4 | 3.5 | V |
| Internal Negative Regulator Voltage for Switches | $V_{SWNEG}$ | | | -2 | -1.9 | -1.8 | V |
| **CHARGER DETECTION** | | | | | | | |
| VB-Detect-Threshold Voltage Rising | $V_{VBDET}$ | | | 3.2 | 3.4 | 3.6 | V |
| VB-Detect-Threshold Voltage Hysteresis | $V_{VBDET\_HYST}$ | | | | 0.5 | | V |
| DP_SRC and DM_SRC Voltage | $V_{DP\_SRC}$, $V_{DM\_SRC}$ | 0µA ≤ $I_{LOAD}$ ≤ 200µA | | 0.5 | 0.6 | 0.7 | V |
| DAT_REF Voltage | $V_{DAT\_REF}$ | | | 0.25 | 0.3 | 0.35 | V |
| LGC Voltage | $V_{LGC}$ | | | 1.15 | 1.24 | 1.3 | V |
| DP and DM Sink Current | $I_{DP\_SINK}$, $I_{DM\_SINK}$ | 0.15V ≤ $V_{DP}$ = $V_{DM}$ ≤ 3.6V | | 55 | 80 | 105 | µA |
| DP Source Current | $I_{DP\_SRC}$ | 0V ≤ $V_{DP}$ ≤ 2.5V | | 5.5 | 8 | 10 | µA |
| DP and DM Pulldown Resistance | $R_{DP\_DWN}$, $R_{DM\_DWN}$ | | | 17 | 20 | 23.3 | kΩ |
| DP/DM Pulldown Current | $I_{DP\_PD}$, $I_{DM\_PD}$ | $V_{DM}$ = 0.15V or 3.6V | | 0.01 | 0.15 | 0.5 | µA |
| COMN1 to VB Voltage Ratio | $V_{BUS25}$ | $V_{VB}$ = 5V | | 22.5 | 25 | 27.5 | % |
| | $V_{BUS47}$ | | | 42.3 | 47 | 51.7 | |
| | $V_{BUS75}$ | | | 70 | 75 | 80 | |
| $V_{IO}$ Reset Falling Threshold | $V_{IO\_RST\_TH}$ | | | 0.5 | 0.8 | 1.1 | V |
| Battery Present Detect Threshold | $V_{THM}$ | % of $V_{SFOUT}$ | $V_{THM}$ rising | 18.0 | 18.5 | 19.0 | % |
| | | | $V_{THM}$ falling | | 18.3 | | |
| **ACCESSORY DETECTION** | | | | | | | |
| UID Low-Power Pullup Voltage | $V_{UID\_PU}$ | $V_{BAT}$ = 3.6V, $V_{VB}$ = 0V, LowPwr = 1 | | | 1.6 | | V |
| UID Low-Power Threshold Voltage | $V_{UID\_LP}$ | $V_{BAT}$ = 3.6V, $V_{VB}$ = 0V, LowPwr = 1 | | 0.4 | 0.7 | 1 | V |
| UID Low-Power Pullup Resistance | $R_{UID\_LP}$ | | | 2 | 3.4 | | MΩ |
| ADC Low Threshold | $R_{ADCLow}$ | | | 32 | 40 | 49 | Ω |

## Electrical Characteristics (continued)

($V_{BAT}$ = 2.8V to 5.5V, $V_{VB}$ = 3.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{BAT}$ = 3.6V, $V_{VB}$ = 5.0V, $T_A$ = +25°C.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| ADC ID Pullup Current | $I_{PUP}$ | $V_{UID}$ = 2.55V and 0.9V | 2.19 | 2.28 | 2.37 | µA |
| | | $V_{UID}$ = 2.50V and 0.76V | 5.756 | 6 | 6.24 | |
| | | $V_{UID}$ = 2.35V and 0.70V | 16.032 | 16.7 | 17.368 | |
| | | $V_{UID}$ = 2.20V and 0.57V | 45.214 | 47 | 48.786 | |
| | | $V_{UID}$ = 2.12V and 0.05V | 146.88 | 153 | 159.12 | |
| | | $V_{UID}$ = 2.04V and 0.05V | 2.235 | 2.5 | 2.735 | mA |
| ADC Detection Resistors | $R_{ADC}$ | GND | 0 | | 0.032 | kΩ |
| | | $R_{VID}$ | 0.049 | 0.075 | 0.472 | |
| | | 1kΩ resistor | 0.531 | 1 | 1.433 | |
| | | R1 | 1.722 | 2 | 2.112 | |
| | | R2 | 2.465 | 2.604 | 2.684 | |
| | | R3 | 3.091 | 3.208 | 3.35 | |
| | | R4 | 3.826 | 4.014 | 4.11 | |
| | | R5 | 4.67 | 4.82 | 5.05 | |
| | | R6 | 5.73 | 6.03 | 6.54 | |
| | | R7 | 7.39 | 8.03 | 8.43 | |
| | | R8 | 9.5 | 10.03 | 10.31 | |
| | | R9 | 11.6 | 12.03 | 12.69 | |
| | | R10 | 14.03 | 14.46 | 14.77 | |
| | | R11 | 16.76 | 17.26 | 17.61 | |
| | | R12 | 19.92 | 20.5 | 20.79 | |
| | | R13 | 23.49 | 24.07 | 24.63 | |
| | | R14 | 27.8 | 28.7 | 29.3 | |
| | | R15 | 33 | 34 | 34.7 | |
| | | R16 | 39 | 40.2 | 43 | |
| | | R17 | 49.6 | 49.9 | 53.4 | |
| | | R18 | 60.4 | 64.9 | 67.6 | |
| | | R19 | 76.3 | 80.07 | 84.9 | |
| | | R20 | 95.6 | 102 | 104 | |
| | | R21 | 117 | 121 | 129 | |
| | | R22 | 143 | 150 | 153 | |
| | | R23 | 173 | 200 | 212 | |
| | | R24 | 239 | 255 | 260 | |
| | | R25 | 293 | 301 | 312 | |
| | | R26 | 350 | 365 | 384 | |
| | | R27 | 425 | 442 | 450 | |
| | | R28 | 508 | 523 | 533 | |
| | | R29 | 601 | 619 | 655 | |
| | | R30 | 737 | 1000 | 1032 | |
| | | Open | 1158 | | | |

## Electrical Characteristics (continued)

($V_{BAT}$ = 2.8V to 5.5V, $V_{VB}$ = 3.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{BAT}$ = 3.6V, $V_{VB}$ = 5.0V, $T_A$ = +25°C.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **USB ANALOG SWITCH (DN1, DP2)** | | | | | | |
| Analog Signal Range | $V_{DN1}$, $V_{DP2}$ | RUID = open, LowPwr = 1 and CPEn = 0 (Note 2) | 0 | | $V_{CCINT}$ | V |
| | | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1 (Note 1) | 0 | | $V_{SWPOS}$ | |
| On-Resistance | $R_{ONUSB}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{COMN1}$, $I_{COMP2}$ = 10mA, 0V ≤ $V_{COMN1}$, $V_{COMP2}$ ≤ 3.0V | | 3 | 6 | Ω |
| On-Resistance Match Between Channels | $\Delta R_{ONUSB}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{COMN1}$, $I_{COMP2}$ = 10mA, $V_{COMN1}$, $V_{COMP2}$ = 400mV | | | 0.5 | Ω |
| On-Resistance Flatness | $R_{FLATUSB}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{COMN1}$, $I_{COMP2}$ = 10mA, 0V ≤ $V_{COMN1}$, $V_{COMP2}$ ≤ 3.3V | | 0.1 | 0.3 | Ω |
| Off-Leakage Current | $I_{LUSB\ (OFF)}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 4.2V, switch open, $V_{DN1}$, $V_{DP2}$ = 0.3V or 2.5V and $V_{COMN1}$, $V_{COMP2}$ = 2.5V or 0.3V | -360 | | +360 | nA |
| On-Leakage Current | $I_{USB(ON)}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 4.2V, switch closed, $V_{DN1}$, $V_{DP2}$ = 0.3V or 2.5V | -360 | | +360 | nA |
| **UART ANALOG SWITCHES (UT1, UR2)** | | | | | | |
| Analog Signal Range | $V_{UT1}$, $V_{UR2}$ | RUID = open, LowPwr = 1 and CPEn = 0 (Note 2) | 0 | | $V_{CCINT}$ | V |
| | | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1 (Note 1) | 0 | | $V_{SWPOS}$ | |
| On-Resistance | $R_{ONUART}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{COMN1}$, $I_{COMP2}$ = 10mA, 0V ≤ $V_{COMN1}$, $V_{COMP2}$ ≤ 3.0V | | 3 | 6 | Ω |
| On-Resistance Match Between Channels | $\Delta R_{ONUART}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{COMN1}$, $I_{COMP2}$ = 10mA, $V_{COMN1}$, $V_{COMP2}$ = 1.5V | | | 0.5 | Ω |
| On-Resistance Flatness | $R_{FLATUART}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{COMN1}$, $I_{COMP2}$ = 10mA, 0V ≤ $V_{COMN1}$, $V_{COMP2}$ ≤ 3.0V | | 0.1 | 0.3 | Ω |
| Off-Leakage Current | $I_{LUART(OFF)}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 4.2V, switch open, $V_{UT1}$, $V_{UR2}$ = 0.3V or 2.5V and $V_{COMN1}$, $V_{COMP2}$ = 2.5V or 0.3V | -360 | | +360 | nA |

## Electrical Characteristics (continued)

($V_{BAT}$ = 2.8V to 5.5V, $V_{VB}$ = 3.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{BAT}$ = 3.6V, $V_{VB}$ = 5.0V, $T_A$ = +25°C.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| On-Leakage Current | $I_{LUART(ON)}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 4.2V, switch closed, $V_{UT1}$, $V_{UR2}$ = 0.3V or 2.5V | -360 | | +360 | nA |
| **AUDIO ANALOG SWITCHES (SL1, SR2)** | | | | | | |
| Analog Signal Range | $V_{AUDIO}$ | RUID = open, LowPwr = 1 and CPEn = 0 (Note 2) | 0 | | $V_{CCINT}$ | V |
| | | (RUID < 1050kΩ or LowPwr=0) and CPEn = 1 (Note 1) | $V_{SWNEG}$ | | $V_{SWPOS}$ | |
| On-Resistance | $R_{ONA}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{COMN1}$, $I_{COMP2}$ = 10mA, 0V ≤ $V_{COMN1}$, $V_{COMP2}$ ≤ 3.0V | | 3 | 6 | Ω |
| On-Resistance Match Between Channels | $\Delta R_{ONA}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{COMN1}$, $I_{COMP2}$ = 10mA, $V_{COMN1}$, $V_{COMP2}$ = 1.5V | | | 0.5 | Ω |
| On-Resistance Flatness | $R_{FLATA}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{COMN1}$, $I_{COMP2}$ = 10mA, 0V ≤ $V_{COMN1}$, $V_{COMP2}$ ≤ 3.0V | | 0.1 | 0.3 | Ω |
| Audio Off-Leakage Current | $I_{LA(OFF)}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 4.2V, switch open, $V_{SL1}$, $V_{SR2}$ = 0.3V or 2.5V, $V_{COMN1}$, $V_{COMP2}$ = 2.5V or 0.3V | -360 | | +360 | nA |
| Audio On-Leakage Current | $I_{LA(ON)}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 4.2V, switch closed, $V_{SL1}$, $V_{SR2}$ = 0.3V or 2.5V | -360 | | +360 | nA |
| Shunt Resistor | $R_{SHUNT}$ | $I_{SHUNT}$ = 10mA | 30 | 100 | 170 | Ω |
| **MIC ANALOG SWITCHES (MIC)** | | | | | | |
| Analog Signal Range | $V_{MIC}$ | RUID = open, LowPwr = 1 and CPEn = 0 (Note 2) | 0 | | $V_{CCINT}$ | V |
| | | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1 | 0 | | 2.5 | |
| On-Resistance | $R_{ONMIC}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{MIC}$ = 10mA, 0V ≤ $V_{MIC}$ ≤ 3.0V | | 30 | 50 | Ω |
| On-Resistance Flatness | $R_{FLATMIC}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{MIC}$ = 10mA, 0V ≤ $V_{MIC}$ ≤ 3.0V | | 3 | 10 | Ω |
| MIC Off-Leakage Current | $I_{LMIC(OFF)}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 4.2V, switch open, $V_{MIC}$ = 0.3V or 2.5V, $V_{VB}$ = 2.5V or 0.3V | -360 | | +360 | nA |

## Electrical Characteristics (continued)

($V_{BAT}$ = 2.8V to 5.5V, $V_{VB}$ = 3.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{BAT}$ = 3.6V, $V_{VB}$ = 5.0V, $T_A$ = +25°C.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| MIC On-Leakage Current | $I_{LMIC(ON)}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 4.2V, switch closed, $V_{MIC}$ = 0.3V or 2.5V | | 32 | 60 | µA |
| **ID BYPASS ANALOG SWITCH (IDB)** | | | | | | |
| Analog Signal Range | $V_{IDB}$ | RUID = open, LowPwr = 1 and CPEn = 0 (Note 2) | 0 | | $V_{CCINT}$ | V |
| | | (RUID < 1050kΩ or LowPwr = 0) and CPEn =1 | $V_{SWNEG}$ | | $V_{SWPOS}$ | |
| On-Resistance | $R_{ONIDB}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{IDB}$ = 10mA, 0V ≤ $V_{IDB}$ ≤ 2.5V | | 3 | 6 | Ω |
| On-Resistance Flatness | $R_{FLATIDB}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 3.0V, $I_{IDB}$ = 10mA, 0V ≤ $V_{IDB}$ ≤ 2.5V | | 0.1 | 0.3 | Ω |
| IDB Off-Leakage Current | $I_{LIDB(OFF)}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 4.2V, switch open, $V_{IDB}$ = 0.3V or 2.5V and $V_{UID}$ = 2.5V or 0.3V | -360 | | +360 | nA |
| IDB On-Leakage Current | $I_{LIDB(ON)}$ | (RUID < 1050kΩ or LowPwr = 0) and CPEn = 1, $V_{BAT}$ = 4.2V, switch closed, $V_{IDB}$ = 0.3V or 2.5V | -360 | | +360 | nA |
| **DIGITAL SIGNALS ($\overline{INT}$, SCL, SDA, JIG, BOOT, LED)** | | | | | | |
| Input Logic-High | $V_{IH}$ | | 1.4 | | | V |
| Input Logic-Low | $V_{IL}$ | | | | 0.4 | V |
| Input Leakage Current | $I_{INLEAK}$ | | -250 | | +250 | nA |
| Open-Drain Output-Voltage Low | $V_{INTL}$, $V_{JIGL}$, $V_{LEDL}$ | $I_{SINK}$ = 3mA | | | 0.4 | V |
| **DYNAMIC PERFORMANCE** | | | | | | |
| Analog Switch Turn-On Time | $t_{ON}$ | I²C STOP to switch on, $R_L$ = 50Ω | | 0.2 | 0.5 | ms |
| Analog Switch Turn-Off Time | $t_{OFF}$ | I²C STOP to switch off, $R_L$ = 50Ω | | 0.1 | 0.5 | ms |
| Break-Before-Make Delay Time | $t_{BBM}$ | $R_L$ = 50Ω, $T_A$ = +25°C (Note 6) | 0 | | | µs |
| MUIC Clock Period | $t_{CK}$ | | | 14.64 | | µs |
| USB Charger Detect Time | $t_{DPSRC\_ON}$ | | 40 | 46 | 60 | ms |
| JIG Assertion Time | | Resistor attached to ID until JIG assert (Note 7) | | 0.5 | | ms |
| Charger Detect Current Delay | $t_{VDPSRC\_HICRNT}$ | | 46 | | 60 | ms |
| VBUS Debounce Time | $t_{MDEB}$ | | 20 | 30 | 40 | ms |
| DCD Debounce Time | | | 36 | 40 | 44 | ms |

## Electrical Characteristics (continued)

($V_{BAT}$ = 2.8V to 5.5V, $V_{VB}$ = 3.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{BAT}$ = 3.6V, $V_{VB}$ = 5.0V, $T_A$ = +25°C.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| DCD Timeout | | DCDCpl = 0 | | 1.8 | 2 | 2.2 | sec |
| | | DCDCpl = 1 | | | | 900 | ms |
| Charger Detection Delay Timeout | | CDDelay = 1 | | | 500 | | ms |
| COMN1, COMP2 On Capacitance | $C_{ONCOM}$ | Applied voltage is $0.5V_{PP}$, DC bias = 0V, f = 240MHz, COMN1/COMP2 connected to DN1/DP2 | | | 7 | | pF |
| UID On Capacitance | $C_{ONUID}$ | Applied voltage is $0.5V_{PP}$, DC bias = 0V, f = 1MHz, UID connected to MIC | | | 7 | | pF |
| Off Capacitance | $C_{OFF}$ | Applied voltage is $0.5V_{PP}$, DC bias = 0V, f = 1MHz | UT1, UR2 | | 3 | | pF |
| | | | DN1, DP2 | | 3 | | |
| | | | MIC | | 3 | | |
| | | | IDB | | 3 | | |
| Off-Isolation | | $R_L$ = 50Ω, f = 20kHz, $V_{COMN1}$, $V_{COMP2}$ = $0.5V_{PP}$ | UT1, UR2 | | -60 | | dB |
| MIC Isolation | | BAT to MIC, MIC to UID switch enabled, $R_L$ = 600Ω, 100Hz ≤ f ≤ 6kHz, $V_{BAT}$ = 3.6V ± 0.5V | | | 80 | | dB |
| BAT Supply PSRR | | Noise from BAT to COMN1, COMP2 or MIC, $R_L$ = 50Ω, f = 10kHz, $V_{BAT}$ = 3.6V ± 0.2V | | | 90 | | dB |
| Crosstalk | | Any switch to any switch, $R_L$ = 50Ω, f = 20kHz, $V_{COMN1}$, $V_{COMP2}$ = $1V_{RMS}$ | | | 100 | | dB |
| MIC Total Harmonic Distortion | THD | MIC channel, 20Hz ≤ f ≤ 20kHz, $V_{COMN1}$, $V_{COMP2}$ = $0.5V_{PP}$, $R_L$ = 50Ω, DC bias = 0V, $T_A$ = +25°C | | | 0.05 | | % |
| **BATTERY CHARGER ($V_{VB}$ = 5V, $V_{BAT}$ = 4V, $T_A$ = -40°C to +85°C, unless otherwise specified)** | | | | | | | |
| VBUS Charger Operating Range | $V_{BUSOP}$ | | | 4.0 | | $V_{OVLO}$ | V |
| VBUSOK Trip Point | $V_{BTP}$ | $V_{VB}$ – $V_{BAT}$, rising | | 150 | 250 | 350 | mV |
| | | $V_{VB}$ – $V_{BAT}$, falling | | 20 | 45 | 100 | |
| | | $V_{VB}$ – $V_{BAT}$, hysteresis | | | 205 | | |
| Input-Undervoltage Threshold | $V_{BUVLO}$ | VB rising | | 3.8 | 3.9 | 4.0 | V |
| Input-Undervoltage Threshold Hysteresis | | | | | 600 | | mV |
| Input-Overvoltage Protection Threshold | $V_{OVLO}$ | VB rising | OTPCGHCVS = 00 | 7.1 | 7.5 | 7.8 | V |
| | | | OTPCGHCVS = 01 | | 6.0 | | |
| | | | OTPCGHCVS = 10 | | 6.5 | | |
| | | | OTPCGHCVS = 11 | | 7.0 | | |

## Electrical Characteristics (continued)

($V_{BAT}$ = 2.8V to 5.5V, $V_{VB}$ = 3.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{BAT}$ = 3.6V, $V_{VB}$ = 5.0V, $T_A$ = +25°C.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Input-Overvoltage Threshold Hysteresis | $V_{OVLO\_HYS}$ | | | | 200 | | mV |
| SFOUT LDO Voltage | $V_{SFOUT}$ | $V_{VB}$ = 6.0V, $I_{SFOUT}$ = 0mA | | 5.0 | 5.25 | 5.5 | V |
| | | $V_{VB}$ = 5.0V, $I_{SFOUT}$ = 15mA | | | 4.9 | | |
| VB to BAT Input Resistance | | $V_{VB}$ = 4.1V, $V_{BAT}$ = 4.0V | | | 0.5 | | Ω |
| BAT Battery Regulation Voltage | | $I_{BAT}$ = 5mA, MBCCVWRC = 0000 | $T_A$ = +25°C | 4.179 | 4.2 | 4.221 | V |
| | | | $T_A$ = -40°C to +85°C | 4.158 | 4.2 | 4.242 | |
| BAT Regulation Programmable Range | $V_{BATREG}$ | $I_{BAT}$ = 5mA (Note 8) | MBCCVWRC = 0001 | | 4.0 | | V |
| | | | MBCCVWRC = 1111 | | 4.35 | | |
| BAT Restart Fast-Charge Threshold | $V_{BATRS}$ | From BAT regulation voltage, active only when AUTOSTOP is enabled | | | -150 | | mV |
| BAT Restart Fast-Charge Debounce | | | | | 62 | | ms |
| Battery Fast-Charge Current | $I_{BAT}$ | $V_{BAT}$ = 3.5V | MBCICHWRCL = 0 | | 90 | | mA |
| | | $V_{BAT}$ = 3.5V, MBCICHWRCL = 1 | MBCICHWRCH = 0000 | | 200 | | |
| | | | MBCICHWRCH = 0001 | | 250 | | |
| | | | MBCICHWRCH = 0010 | | 300 | | |
| | | | MBCICHWRCH = 0011 | | 350 | | |
| | | | MBCICHWRCH = 0100 | | 400 | | |
| | | | MBCICHWRCH = 0101 | 414 | 450 | 486 | |
| | | | MBCICHWRCH = 0110 | | 500 | | |
| | | | MBCICHWRCH = 0111 | | 550 | | |
| | | | MBCICHWRCH = 1000 | | 600 | | |
| | | | MBCICHWRCH = 1001 | | 650 | | |
| | | | MBCICHWRCH = 1010 | | 700 | | |
| | | | MBCICHWRCH = 1011 | | 750 | | |
| | | | MBCICHWRCH = 1100 | | 800 | | |
| | | | MBCICHWRCH = 1101 | | 850 | | |
| | | | MBCICHWRCH = 1110 | | 900 | | |
| | | | MBCICHWRCH = 1111 | | 950 | | |

## Electrical Characteristics (continued)

($V_{BAT}$ = 2.8V to 5.5V, $V_{VB}$ = 3.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{BAT}$ = 3.6V, $V_{VB}$ = 5.0V, $T_A$ = +25°C.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Battery End-of-Charge Threshold | $I_{BAT\_STOP}$ | $I_{BAT}$ falling, battery is charged | EOCS = 0000 | | 50 | | mA |
| | | | EOCS = 0001 | | 60 | | |
| | | | EOCS = 0010 | | 70 | | |
| | | | EOCS = 0011 | | 80 | | |
| | | | EOCS = 0100 | | 90 | | |
| | | | EOCS = 0101 | | 100 | | |
| | | | EOCS = 0110 | | 110 | | |
| | | | EOCS = 0111 | | 120 | | |
| | | | EOCS = 1000 | | 130 | | |
| | | | EOCS = 1001 | | 140 | | |
| | | | EOCS = 1010 | | 150 | | |
| | | | EOCS = 1011 | | 160 | | |
| | | | EOCS = 1100 | | 170 | | |
| | | | EOCS = 1101 | | 180 | | |
| | | | EOCS = 1110 | | 190 | | |
| | | | EOCS = 1111 | | 200 | | |
| VB Prequalification Charge Current | $I_{PRECHG}$ | $V_{BAT}$ = 2V, $V_{VB}$ = 5V | | | 93 | | mA |
| Battery Charger Soft-Start Time | | Ramp time from 93mA to fast-charge current | | | 1.2 | | ms |
| Precharge Threshold | $V_{PRECHG}$ | | | | 2.5 | | V |
| Precharge Threshold Hysteresis | | | | | 170 | | mV |
| Precharge Watchdog Timeout | | | | | 30 | | min |
| Fast-Charge Timer | | TCHW = 000,001, 010, 101, or 110 | | | 5 | | Hour |
| | | TCHW = 011 | | | 6 | | |
| | | TCHW = 100 | | | 7 | | |
| Top-Off Timer | | | | | 30 | | min |
| Die Temperature Thermal Limit | $T_J$ | Die temperature rising (Note 9) | | | +105 | | °C |

## Electrical Characteristics (continued)

($V_{BAT}$ = 2.8V to 5.5V, $V_{VB}$ = 3.5V to 5.5V, $T_A$ = -40°C to +85°C, unless otherwise noted. Typical values are at $V_{BAT}$ = 3.6V, $V_{VB}$ = 5.0V, $T_A$ = +25°C.) (Note 5)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **I²C TIMING SPECIFICATIONS (Figure 1)** | | | | | | |
| I²C Maximum Clock Frequency | $f_{I2CCLK}$ | | | 400 | | kHz |
| Bus Free Time Between STOP and START Conditions | $t_{BUF}$ | | 1.3 | | | µs |
| Repeated Start (SR) Condition Setup Time | $t_{SU:STA}$ | 90% to 90% | 0.6 | | | µs |
| START Condition Hold Time | $t_{HD:STA}$ | 10% of SDA to 90% of SCL | 0.6 | | | µs |
| STOP Condition Setup Time | $t_{SU:STO}$ | 90% of SCL to 10% of SDA | 0.6 | | | µs |
| Clock Low Period | $t_{LOW}$ | 10% to 10% | 1.3 | | | µs |
| Clock High Period | $t_{HIGH}$ | 90% to 90% | 0.6 | | | µs |
| Data Valid to SCL Rise Time | $t_{SU:DAT}$ | Data setup time | 100 | | | ns |
| Data Setup Time to SCL Fall | $t_{HD:DAT}$ | Data hold time | 0 | | | ns |
| **ESD PROTECTION** | | | | | | |
| COMN1, COMP2, UID, BC | | Human Body Model | | ±15 | | kV |
| | | IEC61000-4-2 Air Gap | | ±10 | | |
| | | IEC61000-4-2 Contact | | ±7 | | |
| All Other Pins | | Human Body Model | | ±2 | | kV |

**Note 5:** All devices are 100% production tested at $T_A$ = +25°C. Limits over the operating temperature range are guaranteed by design.

**Note 6:** Not production tested. Guaranteed by design.

**Note 7:** The JIG assertion time is a function of the ADC debounce time. Set the ADCDbSet bits in the CONTROL3 register to adjust this delay.

**Note 8:** Set the MBCCVWRC bits in the CHGCTRL3 register to adjust the battery regulation voltage, $V_{BATREG}$.

**Note 9:** The battery charge current is reduced when the die temperature reaches this limit.

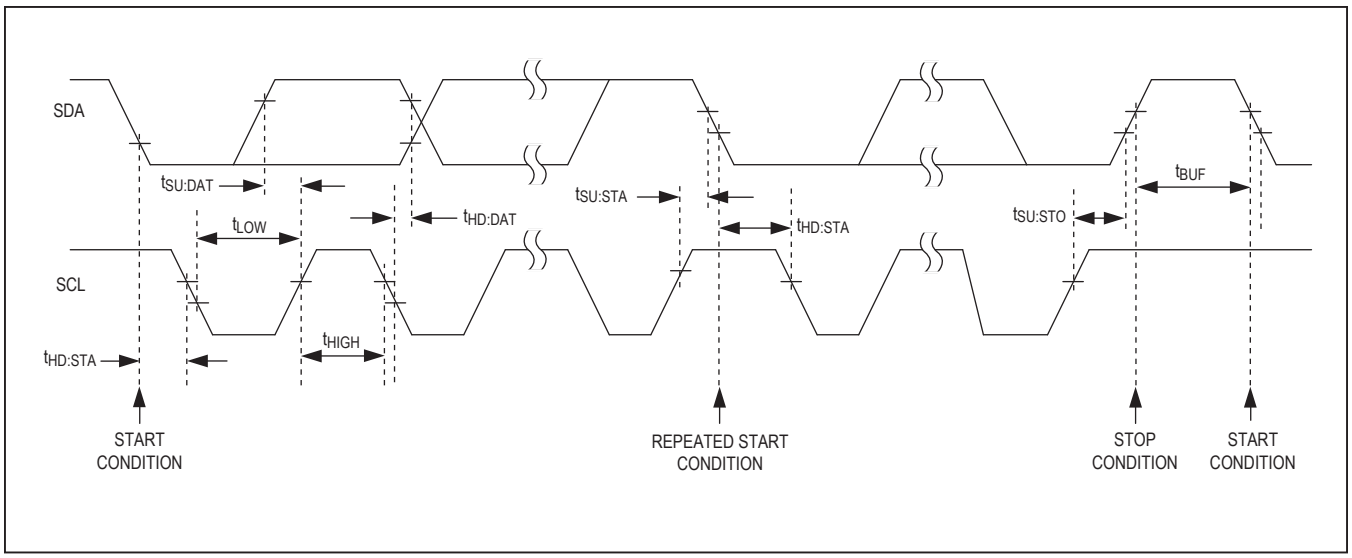
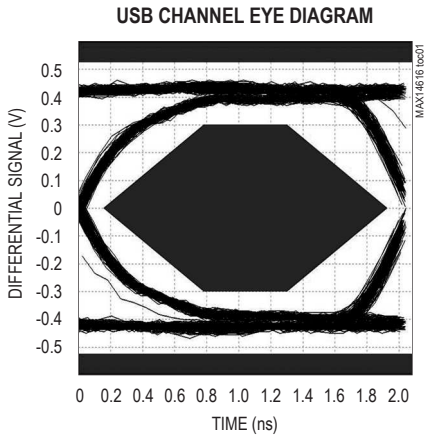
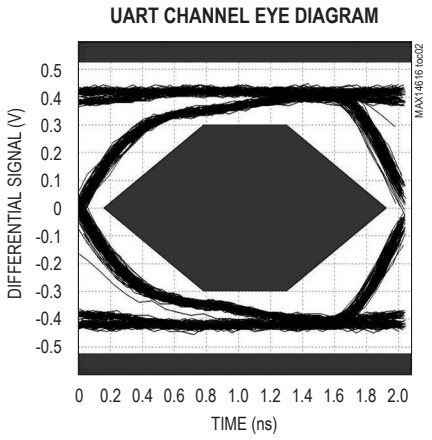


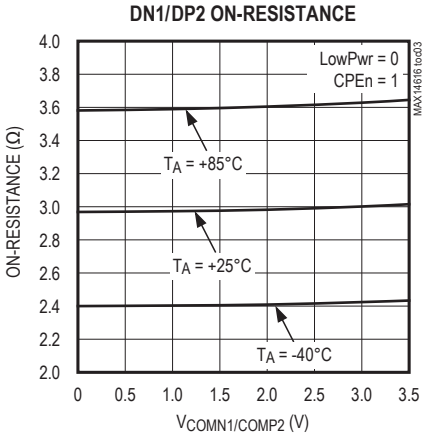

*Figure 1. I²C Timing Diagram*

## Typical Operating Characteristics

($V_{BAT}$ = 4.0V, $V_{VB}$ = 0V, $T_A$ = +25°C, unless otherwise noted.)



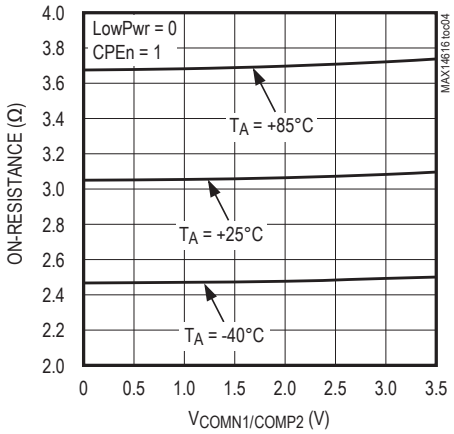



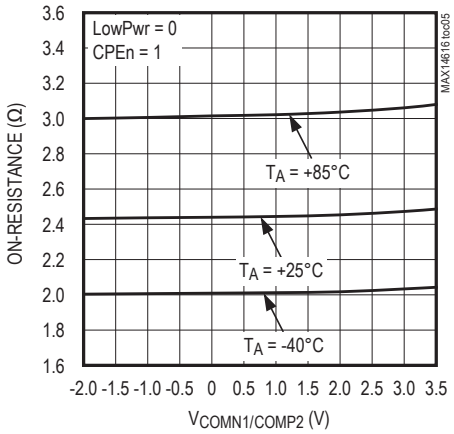
## Typical Operating Characteristics (continued)

($V_{BAT}$ = 4.0V, $V_{VB}$ = 0V, $T_A$ = +25°C, unless otherwise noted.)

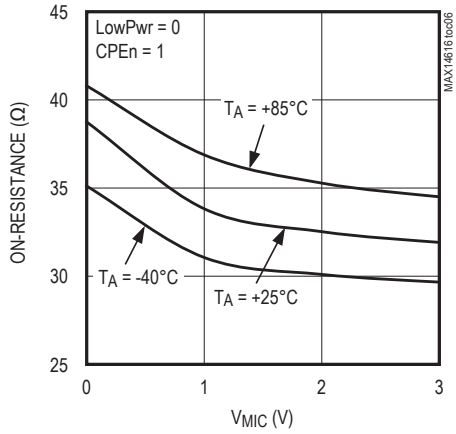
**UT1/UR2 ON-RESISTANCE**



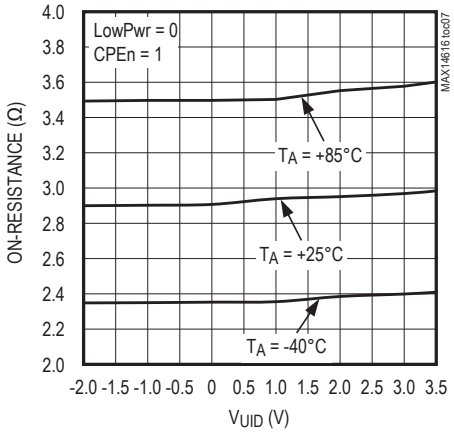

**SL1/SR2 ON-RESISTANCE**



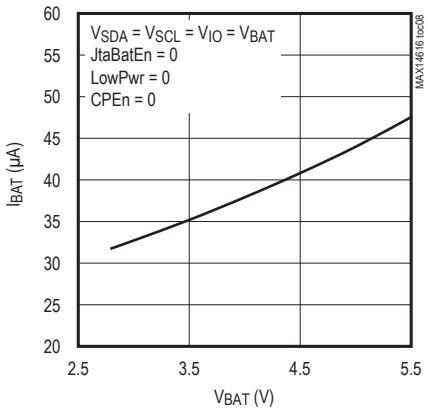

**MIC ON-RESISTANCE**



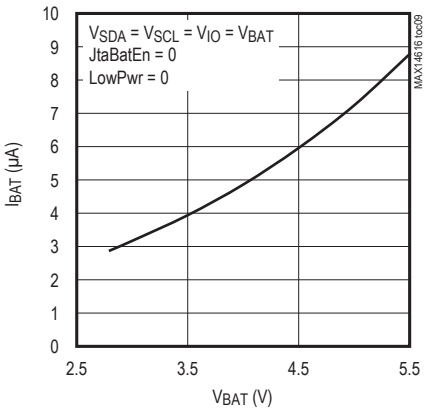

**IDB ON-RESISTANCE**



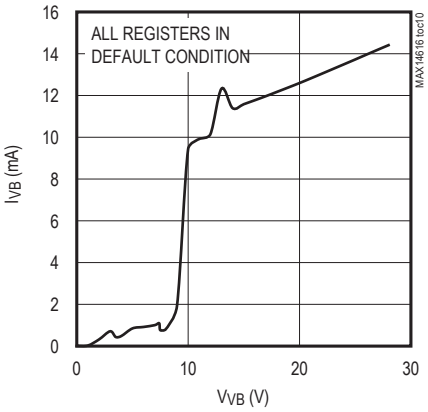

**SUPPLY CURRENT vs. $V_{BAT}$**




**SUPPLY CURRENT vs. $V_{BAT}$**



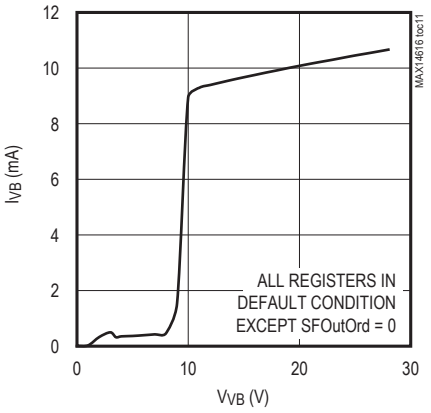

**SUPPLY CURRENT vs. $V_{VB}$ (SFOUT ON)**



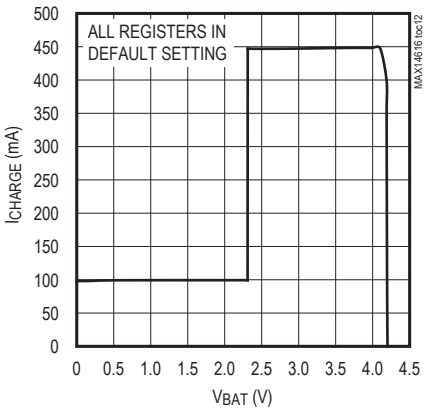
## Typical Operating Characteristics (continued)

($V_{BAT}$ = 4.0V, $V_{VB}$ = 0V, $T_A$ = +25°C, unless otherwise noted.)

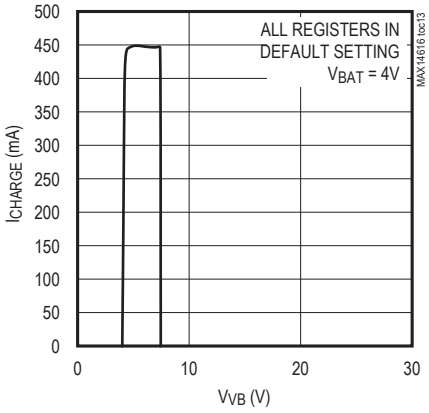
**SUPPLY CURRENT vs. $V_{VB}$ (SFOUT OFF)**



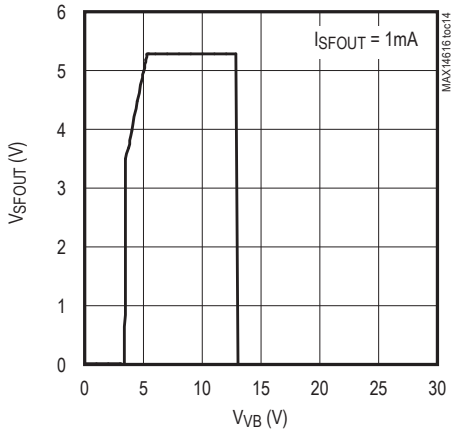

**CHARGE CURRENT vs. $V_{BAT}$ ($V_{VB}$ = 5V)**



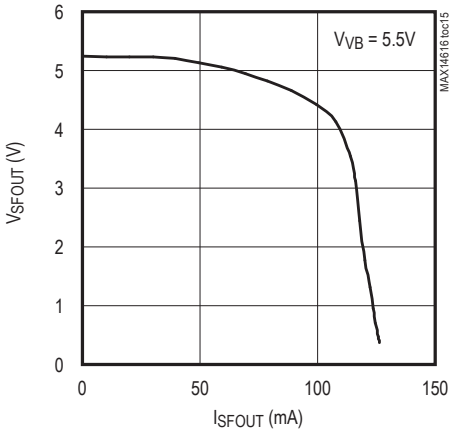

**CHARGE CURRENT vs. $V_{VB}$**



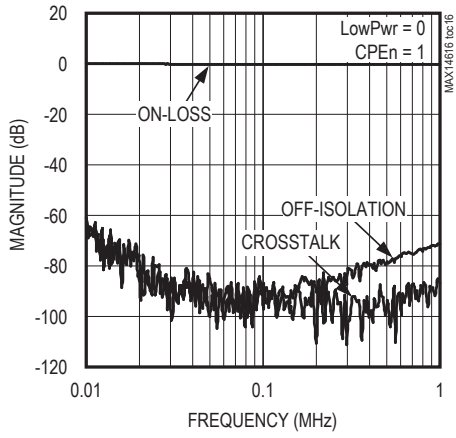

**SFOUT VOLTAGE vs. VB VOLTAGE**



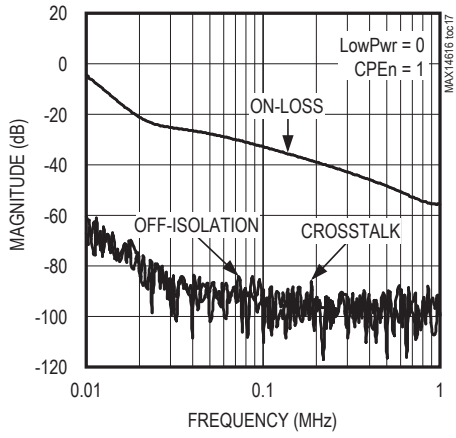

**$V_{SFOUT}$ vs. $I_{SFOUT}$**




**SL1/SR2 FREQUENCY RESPONSE**



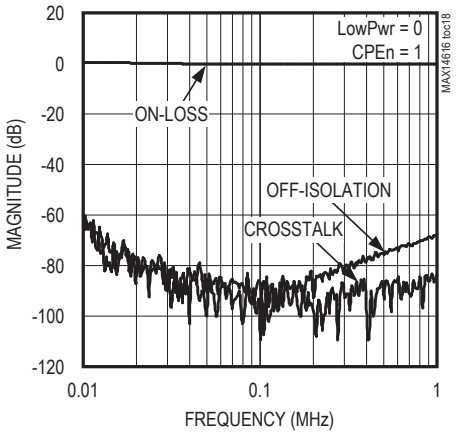

**MIC FREQUENCY RESPONSE**



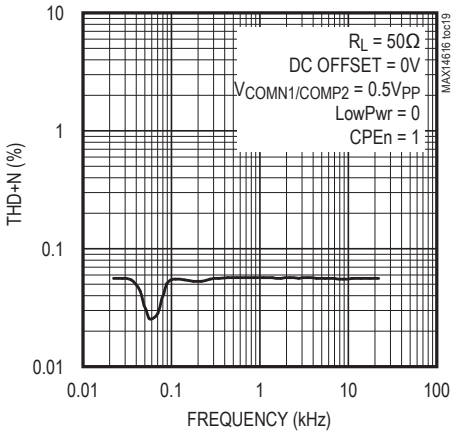
## Typical Operating Characteristics (continued)

($V_{BAT}$ = 4.0V, $V_{VB}$ = 0V, $T_A$ = +25°C, unless otherwise noted.)

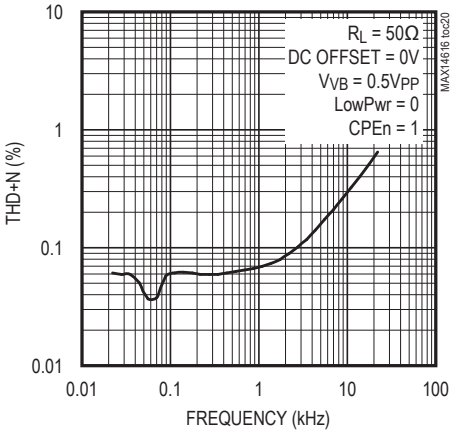
**IDB FREQUENCY RESPONSE**



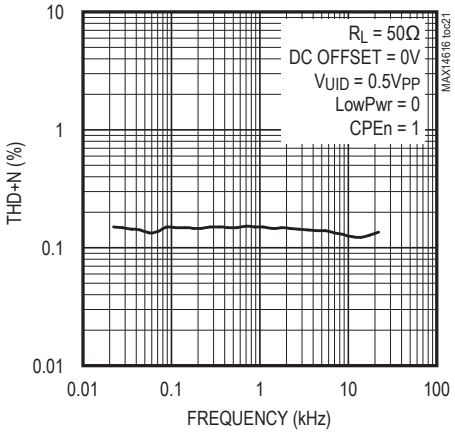

**SL1/SR2 THD+N**




**MIC THD+N**



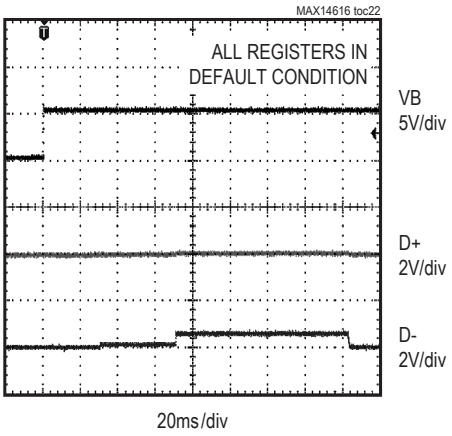

**IDB THD+N**



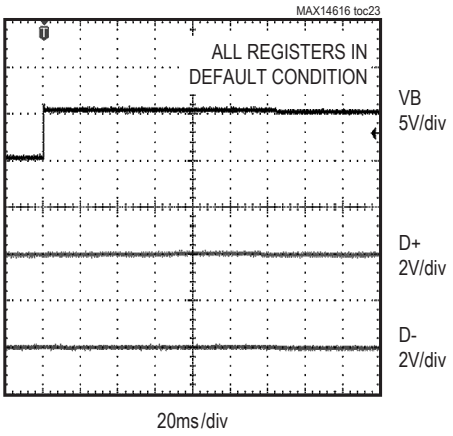
## Typical Operating Characteristics (continued)

($V_{BAT}$ = 4.0V, $V_{VB}$ = 0V, $T_A$ = +25°C, unless otherwise noted.)

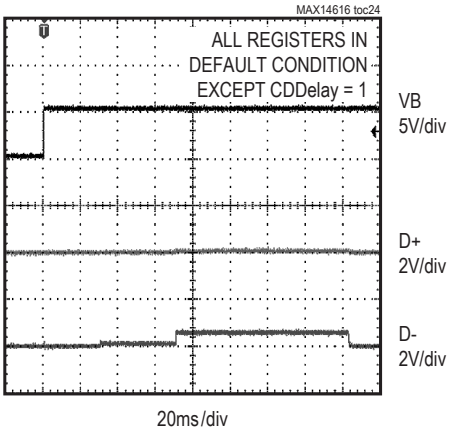
**DCP INSERT**



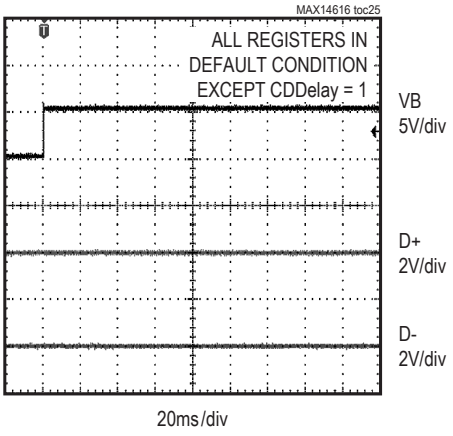

**SDP INSERT**



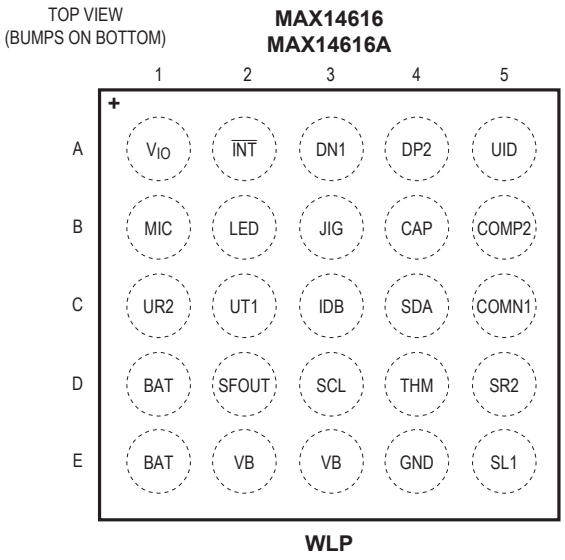

**DCP INSERT (CDDelay = 1)**




**SDP INSERT (CDDelay = 1)**



## Bump Configuration




**WLP**

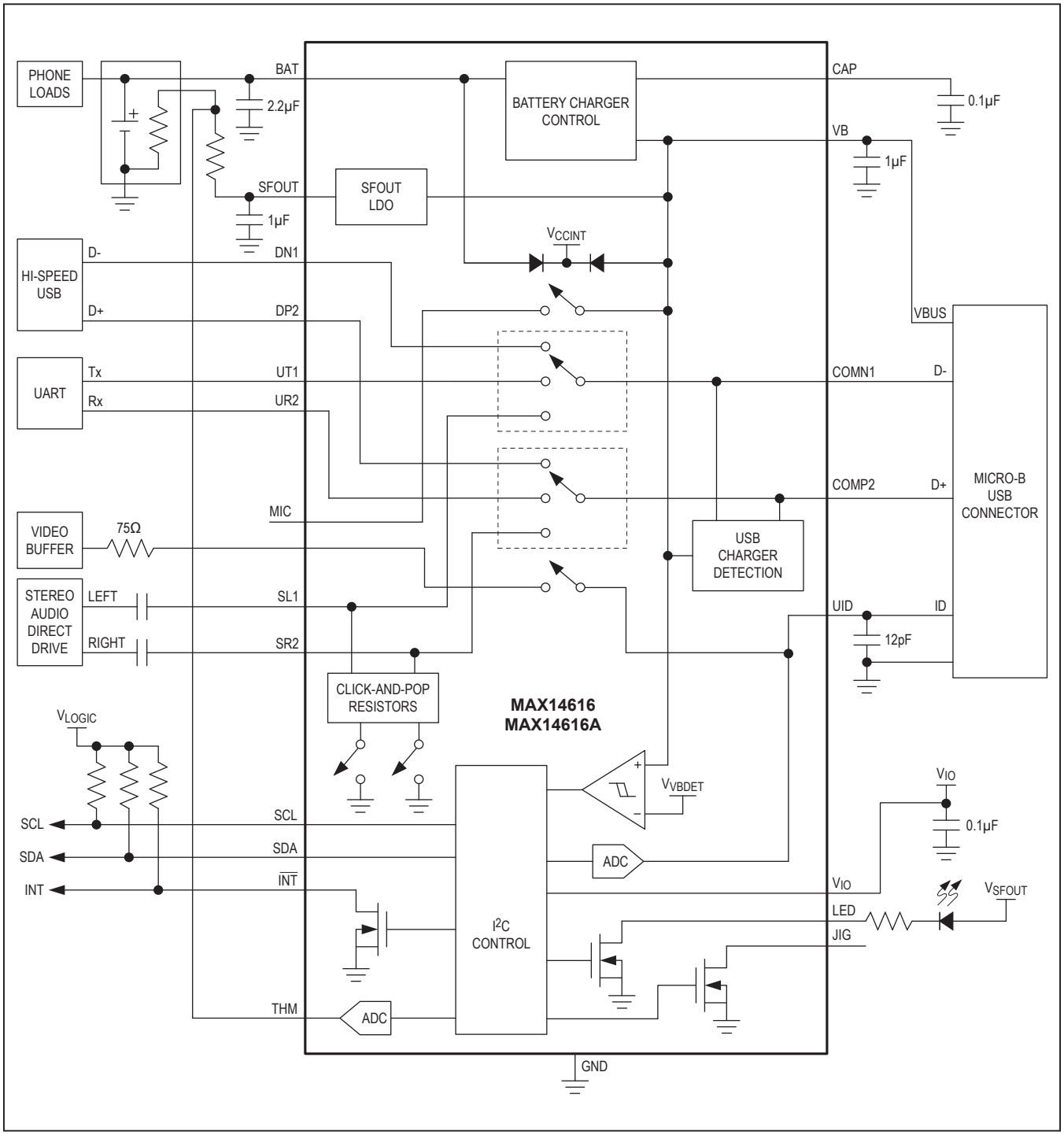
## Bump Description

| BUMP | NAME | FUNCTION |
|---|---|---|
| A1 | $V_{IO}$ | I²C Reset Input. A falling edge on $V_{IO}$ causes the I²C registers to reset. |
| A2 | $\overline{INT}$ | Active-Low Open-Drain Interrupt Output. Connect $\overline{INT}$ to an external pullup resistor. |
| A3 | DN1 | USB D- Input/Output |
| A4 | DP2 | USB D+ Input/Output |
| A5 | UID | USB ID Input. Connect UID to ID on micro-USB connector. Maximum capacitance allowed from UID to ground is 1nF. |
| B1 | MIC | Microphone Output |
| B2 | LED | Open-Drain LED Driver. LED is controlled by the battery charger status (Table 4) or the BTLDSet bits in the CONTROL3 register. |
| B3 | JIG | Factory-Mode Open-Drain Output. JIG is controlled by the internal state machine or manually controlled by the JIGSet register bits. |
| B4 | CAP | Internal LDO Bypass Output. Bypass CAP to GND with a 0.1µF (typ) ceramic capacitor for proper operation. Do not use CAP to drive an external load. |
| B5 | COMP2 | Common Input/Output 2. Connect COMP2 to D+ on the micro-USB connector. |

## Bump Description (continued)

| BUMP | NAME | FUNCTION |
|---|---|---|
| C1 | UR2 | UART Receiver Input/Output |
| C2 | UT1 | UART Transmitter Input/Output |
| C3 | IDB | USB ID Bypass. IDB is used to sense ID of the micro-USB connector for USB OTG transceivers and the pass composite video. |
| C4 | SDA | $I^2C$ Serial Data Input/Output. Connect SDA to external pullup resistor. |
| C5 | COMN1 | Common Input/Output 1. Connect COMN1 to D- on the micro-USB connector. |
| D1, E1 | BAT | Battery Charger Output and Chip-Power Input. Bypass BAT to GND with a 2.2µF (min) ceramic capacitor. |
| D2 | SFOUT | Overvoltage-Protected LDO Output. Internal LDO is powered from VB. Bypass SFOUT to GND with a 1µF (min) ceramic capacitor. |
| D3 | SCL | $I^2C$ Serial Clock Input. Connect SCL to an external pullup resistor. |
| D4 | THM | Battery Presence Detection |
| D5 | SR2 | Stereo Audio Input/Output 2 |
| E2, E3 | VB | USB VBUS Input. VB provides power for internal circuitry when $V_{BAT}$ is less than $V_{VB}$. VB is also the input source for the battery charger. Bypass VB to GND with a 1µF (min) ceramic capacitor. |
| E4 | GND | Ground |
| E5 | SL1 | Stereo Audio Input/Output 1 |

## Functional Diagram/Typical Application Circuit



## Register Map

| ADDRESS | NAME | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x00 | **DEVICEID** | ChipID | | | | | DeviceID | | |
| 0x01 | **INT1** | 0 | 0 | 0 | 0 | ADC1KI | ADCErrorI | ADCLowI | ADCI |
| 0x02 | **INT2** | 0 | 0 | VidRmI | VBVoltI | DXOVPI | DCDTmrI | ChgDetRunI | ChgTypI |
| 0x03 | **INT3** | 0 | 0 | BatDetI | ChgEnbldI | MBCCHGERRI | OVPI | CGMBCI | EOCI |
| 0x04 | **STATUS1** | ADC1K | ADCError | ADCLow | ADC | | | | |
| 0x05 | **STATUS2** | VidRm | VBVolt | DXOVP | DCDTmr | ChgDetRun | ChgTyp | | |
| 0x06 | **STATUS3** | 0 | BatDet | | ChgEnbld | MBCCHGERR | OVP | CGMBC | EOC |
| 0x07 | **INTMASK1** | 0 | 0 | 0 | 0 | ADC1KM | ADCErrorM | ADCLowM | ADCM |
| 0x08 | **INTMASK2** | 0 | 0 | VidRmM | VBVoltM | DXOVPM | DCDTmrM | ChgDetRunM | ChgTypM |
| 0x09 | **INTMASK3** | 0 | 0 | BatDetM | ChgEnbldM | MBCCHGERRM | OVPM | CGMBCM | EOCM |
| 0x0A | **CDETCTRL1** | CDPDet | 0 | DCDCpl | CDDelay | DCD2sCt | DCDEn | ChgTypMan | ChgDetEn |
| 0x0B | **CDETCTRL2** | 0 | 0 | 0 | 0 | DxOVPEn | JtaBatEn | VidRmEn | FrcChg |
| 0x0C | **CONTROL1** | IDBEn | MicEn | COMP2Sw | | | COMN1Sw | | |
| 0x0D | **CONTROL2** | RCPS | USBCpInt | AccDet | SFOutOrd | SFOutAsrt | CPEn | ADCEn | LowPwr |
| 0x0E | **CONTROL3** | 0 | 0 | ADCDbSet | | BTLDSet | | JIGSet | |
| 0x0F | **CHGCTRL1** | 0 | TCHW | | | 0 | 1 | 0 | 0 |
| 0x10 | **CHGCTRL2** | VCHGR_RC | MBCHOSTEN | 0 | 1 | 0 | 1 | 0 | 0 |
| 0x11 | **CHGCTRL3** | 1 | 0 | 1 | 0 | MBCCVWRC | | | |
| 0x12 | **CHGCTRL4** | 0 | 0 | 0 | MBCICHWRCL | MBCICHWRCH | | | |
| 0x13 | **CHGCTRL5** | 0 | 0 | 1 | 0 | EOCS | | | |
| 0x14 | **CHGCTRL6** | 0 | 1 | AUTOSTOP | 1 | 0 | 0 | 0 | 1 |
| 0x15 | **CHGCTRL7** | 0 | 0 | 0 | 0 | 0 | 0 | OTPCGHCVS | |

## Detailed Register Map

| FIELD NAME | READ/WRITE | BITS | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| **DEVICEID (0x00)** | | | | |
| ChipID (MAX14616) | Read Only | [7:3] | 01110 | **Chip Version** |
| ChipID (MAX14616A) | Read Only | [7:3] | 10010 | **Chip Version** |
| DeviceID | Read Only | [2:0] | 101 | **Device Identification** |
| **INT1 (0x01) (All bits are cleared after a read)**<br>Bits in this register are set when associated bits in the STATUS1 register change. $\overline{INT}$ is asserted when any bit in the INT1 register is set, unless masked in the INTMASK1 register. | | | | |

## Detailed Register Map (continued)

| FIELD NAME | READ/WRITE | BITS | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| RFU | Read Only | [7:4] | 0000 | Reserved |
| ADC1KI | Read Only | [3] | (Note 10) | **ADC 1K Detected or Removed Interrupt**<br>0 = No change<br>1 = ADC1K bit has changed |
| ADCErrorI | Read Only | [2] | (Note 10) | **ADC Error Interrupt**<br>0 = No change<br>1 = ADCError bit has changed |
| ADCLowI | Read Only | [1] | (Note 10) | **ADC Low-Bit Change Interrupt**<br>0 = No change<br>1 = ADCLow bit has changed |
| ADCI | Read Only | [0] | (Note 10) | **ADC Change Interrupt**<br>0 = No change<br>1 = ADC bits have changed |
| **INT2 (0x02) (All bits are cleared after a read)**<br>Bits in this register are set when associated bits in the STATUS2 register change. $\overline{INT}$ is asserted when any bit in the INT2 register is set, unless masked in the INTMASK2 register. | | | | |
| RFU | Read Only | [7:6] | 00 | Reserved |
| VidRmI | Read Only | [5] | (Note 10) | **Video Cable Removal Interrupt**<br>0 = No change<br>1 = VidRm bit has changed |
| VBVoltI | Read Only | [4] | (Note 10) | **VB Voltage Interrupt**<br>0 = No change<br>1 = VBVolt bit has changed |
| DXOVPI | Read Only | [3] | (Note 10) | **D+/D- OVP Interrupt**<br>0 = No change<br>1 = DXOVP bit has changed |
| DCDTmrI | Read Only | [2] | (Note 10) | **DCD Timer Interrupt**<br>0 = No change<br>1 = DCDTmr bit has changed |
| ChgDetRunI | Read Only | [1] | (Note 10) | **Charger Detection Running Status Interrupt**<br>0 = No change<br>1 = ChgDetRun bit has changed |
| ChgTypI | Read Only | [0] | (Note 10) | **Charger Type Interrupt**<br>0 = No change<br>1 = ChgTyp bits have changed |
| **INT3 (0x03) (All bits are cleared after a read)**<br>Bits in this register are set when associated bits in the STATUS3 register change. $\overline{INT}$ is asserted when any bit in the INT3 register is set, unless masked in the INTMASK3 register. | | | | |

## Detailed Register Map (continued)

| FIELD NAME | READ/WRITE | BITS | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| RFU | Read Only | [7:6] | 00 | Reserved |
| BatDetI | Read Only | [5] | (Note 10) | **Battery Presence Detect**<br>0 = No change<br>1 = BatDet bits have changed |
| ChgEnbldI | Read Only | [4] | (Note 10) | **Battery Charger Enable Interrupt**<br>0 = No change<br>1 = ChgEnbld bit has changed |
| MBCCHGERRI | Read Only | [3] | (Note 10) | **Battery Fast-Charge Timer Expire Interrupt**<br>0 = No change<br>1 = MBCCHGERR has changed |
| OVPI | Read Only | [2] | (Note 10) | **VB Overvoltage Protection Interrupt**<br>0 = No change<br>1 = OVP bit has changed |
| CGMBCI | Read Only | [1] | (Note 10) | **Charger Voltage OK Interrupt**<br>0 = No change<br>1 = CGMBC bit has changed |
| EOCI | Read Only | [0] | (Note 10) | **End-of-Charge Interrupt**<br>0 = No change<br>1 = EOC bit has changed |
| **STATUS1 (0x04)**<br>Changes in bits in this register generate an interrupt in the INT1 register. | | | | |
| ADC1K | Read Only | [7] | (Note 10) | **ADC 1KΩ Resistor Detection**. This bit is set when a 1kΩ or larger resistor to ground is detected on UID.<br>0 = No 1kΩ on UID<br>1 = 1kΩ detected on UID |
| ADCError | Read Only | [6] | (Note 10) | **ADC Error Detection**. This bit is set when the ADC cannot converge on a value due to noise or other interference.<br>0 = ADC Detection Error has not occurred<br>1 = ADC Detection Error has occurred |
| ADCLow | Read Only | [5] | (Note 10) | **ADCLow Bit**. This bit is cleared when UID is connected to GND. ADCLow is used to detect a 75Ω video cable; a video cable is present when ADCLow = 1 and ADC = 00000. See the *Accessory Detection* section for more information.<br>0 = UID resistance < 30Ω<br>1 = UID resistance ≥ 30Ω |
| ADC | Read Only | [4:0] | (Note 10) | **ADC Output**. Any change in the ADC bits triggers an interrupt in the INT1 register. See Table 4 in the *Accessory Detection* section. |
| **STATUS2 (0x05)**<br>Changes in bits in this register generate an interrupt in the INT2 register. | | | | |

## Detailed Register Map (continued)

| FIELD NAME | READ/WRITE | BITS | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| VidRm | Read Only | [7] | (Note 10) | **Video Cable Removal Detection Output**. VidRmEn must to be set to 1 and video amplifier is enabled and outputting a video signal for correct operation of VidRm function. The load removal can only be detected if the video amp is enabled and outputting a video signal. The video cable removal senses the change in the voltage drop across IDB and UID due to the presence of a video signal if a 75Ω monitor load is connected.<br>0 = Video load present<br>1 = Video cable load not present |
| VBVolt | Read Only | [6] | (Note 10) | **VB Detection Comparator Output**. This bit is set when the VBUS voltage rises above the VB detect threshold, $V_{VBDET}$.<br>0 = $V_{VB} < V_{VBDET}$<br>1 = $V_{VB} \geq V_{VBDET}$ |
| DXOVP | Read Only | [5] | (Note 10) | **D+/D- OVP Flag**. When DXOVP = 1, the charger detection state machine is forced off and CHGTYP = 000 to avoid reverse biasing from D+/D-. This flag can be asserted only when $V_{VB} \geq V_{VBDET}$.<br>0 = $V_{COMN1}$ and $V_{COMP2} \leq V_{CCINT}$<br>1 = $V_{COMN1}$ or $V_{COMP2} > V_{CCINT}$ |
| DCDTmr | Read Only | [4] | (Note 10) | **Data Contact Detection (DCD) Timer**.<br>0 = DCD timer is not running or is not expired<br>1 = DCD timer has been running for longer that 2 sec (min) |
| ChgDetRun | Read Only | [3] | (Note 10) | **Charger Detection State Machine Status**.<br>0 = Charger detection state machine is not running<br>1 = Charger detection state machine is running |
| ChgTyp | Read Only | [2:0] | (Note 10) | **USB Charger Detection Output**.<br>000 = Nothing attached<br>001 = USB cable attached<br>010 = Charging downstream port. Charger current depends on USB operating speed.<br>011 = Dedicated charger. The maximum charge current for the port is 1.5A.<br>100 = Apple 500mA charger. The maximum charge current for the port is 500mA.<br>101 = Apple 1A or 2A charger<br>110 = Special charger (bias on D+/D-)<br>111 = Reserved |
| **STATUS3 (0x06)** Changes in bits in this register generate an interrupt in the INT3 register. | | | | |

## Detailed Register Map (continued)

| FIELD NAME | READ/WRITE | BITS | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| RFU | Read Only | [7] | 0 | Reserved |
| BatDet | Read Only | [6:5] | (Note 10) | **Battery Presence Monitor**<br>00 = Battery not present<br>01 = Reserved<br>10 = Battery present<br>11 = Reserved |
| ChgEnbld | Read Only | [4] | 0 | **Battery Charger Enable Status**. This bit only indicates the charger logic is enabled and does not indicate if the charger is passing current. See Tables 1 and 2.<br>0 = Charger is not enabled<br>1 = Charger is enabled |
| MBCCHGERR | Read Only | [3] | (Note 10) | **Battery Charger Error and Fast-Charging Timer Status**. Set the battery fast-charge timer in the CHGCTRL1 register (0x0F).<br>0 = Timer not expired<br>1 = Timer expired |
| OVP | Read Only | [2] | (Note 10) | **VB Overvoltage Protection Trip Level Status**. Set the VB overvoltage protection threshold in the CHGCTRL7 register (0x15).<br>0 = $V_{VB} \le V_{OVLO}$<br>1 = $V_{VB} > V_{OVLO}$ |
| CGMBC | Read Only | [1] | (Note 10) | **Charger Power-OK Monitor**. This bit is set when the VB voltage is greater than the VBUSOK trip point voltage.<br>0 = $V_{VB} < V_{BTP}$<br>1 = $V_{VB} \ge V_{BTP}$ |
| EOC | Read Only | [0] | (Note 10) | **End-of-Charge Status**. This bit is set while charging a battery.<br>0 = Charger is in prequalification mode, fast-charge mode, disabled, or 30-minute top-off timer has expired (AUTOSTOP = 1)<br>1 = Charger is in top-off mode (AUTOSTOP = 1) or $I_{BAT} < I_{EOCS}$ (AUTOSTOP = 0). |
| **INTMASK1 (0x07)** Set the bits in the INTMASK1 register to mask interrupts at the $\overline{INT}$ output that are generated in the STATUS1 and INT1 registers. | | | | |
| RFU | Read Only | [7:4] | 0000 | Reserved |
| ADC1KM | Read/Write | [3] | 0 | **ADC 1K Detection Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| ADCErrorM | Read/Write | [2] | 0 | **ADC Error Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| ADCLowM | Read/Write | [1] | 0 | **ADC Low-Bit Change Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| ADCM | Read/Write | [0] | 0 | **ADC Change Interrupt Mask**<br>0 = Mask<br>1 = Not masked |

## Detailed Register Map (continued)

| FIELD NAME | READ/WRITE | BITS | DEFAULT | DESCRIPTION |
|---|---|---|---|---|
| **INTMASK2 (0x08)**<br>Set the bits in the INTMASK2 register to mask interrupts at the $\overline{INT}$ output that are generated in the STATUS2 and INT2 registers. | | | | |
| RFU | Read Only | [7:6] | 00 | Reserved |
| VidRmM | Read/Write | [5] | 0 | **Video Cable Removal Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| VBVoltM | Read/Write | [4] | 0 | **VB Voltage Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| DXOVPM | Read/Write | [3] | 0 | **D+/D- OVPInterrupt Mask**<br>0 = Mask<br>1 = Not masked |
| DCDTmrM | Read/Write | [2] | 0 | **DCD Timer Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| ChgDetRunM | Read/Write | [1] | 0 | **Charger Detection Running Status Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| ChgTypM | Read/Write | [0] | 0 | **Charger Type Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| **INTMASK3 (0x09)**<br>Set the bits in the INTMASK3 register to mask interrupts at the $\overline{INT}$ output that are generated in the STATUS3 and INT3 registers. | | | | |
| RFU | Read Only | [7:6] | 00 | Reserved |
| BatDetM | Read/Write | [5] | 0 | **Battery Detection Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| ChgEnbldM | Read/Write | [4] | 0 | **Battery Charger Enable Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| MBCCHGERRM | Read/Write | [3] | 0 | **Battery Fast-Charge Timer Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| OVPM | Read/Write | [2] | 0 | **VB Overvoltage Protection Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| CGMBCM | Read/Write | [1] | 0 | **Charger Voltage Power-OK Interrupt Mask**<br>0 = Mask<br>1 = Not masked |
| EOCM | Read/Write | [0] | 0 | **End-of-Charge Interrupt Mask**<br>0 = Mask<br>1 = Not masked |