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General Description

The MAX14690 is a battery-charge-management solution ideal for low-power wearable applications. The device includes a linear battery charger with a smart power selector and several power-optimized peripherals. The MAX14690 features two ultra-low-power buck regulators with a typical quiescent current of 900nA. In addition, three ultra-low power low-dropout (LDO) linear regulators, with a typical quiescent current of 600nA are included. In total, the MAX14690 can provide up to five regulated voltages, each with an ultra-low quiescent current, critical to battery life for the unique power profile in 24/7 operation devices, such as those in the wearable market.

The battery charger features a smart power selector that allows operation on a dead battery when connected to a power source. To avoid overloading a power adapter, the input current to the smart power selector is limited based on an I^2C register setting. If the charger power source is unable to supply the entire system load, the smart power control circuit supplements the system load with current from the battery.

The two synchronous, high-efficiency step-down buck regulators feature a fixed-frequency PWM mode for tighter regulation and a burst mode for increased efficiency during light-load operation. The output voltage of these regulators can be programmed through I^2C with the default preconfigured.

The three configurable LDOs each have a dedicated input pin. Each LDO regulator output voltage can be programmed through I^2C with the default preconfigured. The linear regulators can also be configured to operate as power switches that may be used to disconnect the quiescent load of the system peripherals.

The MAX14690 features a programmable power controller that allows the device to be configured for applications that require the device be in a true-off, or always-on, state. The controller also provides a delayed reset signal and voltage sequencing.

The MAX14690 is available in a 36-bump, 0.4mm pitch, 2.72mm x 2.47mm wafer-level package (WLP).

Ordering Information ***appears at end of data sheet.***

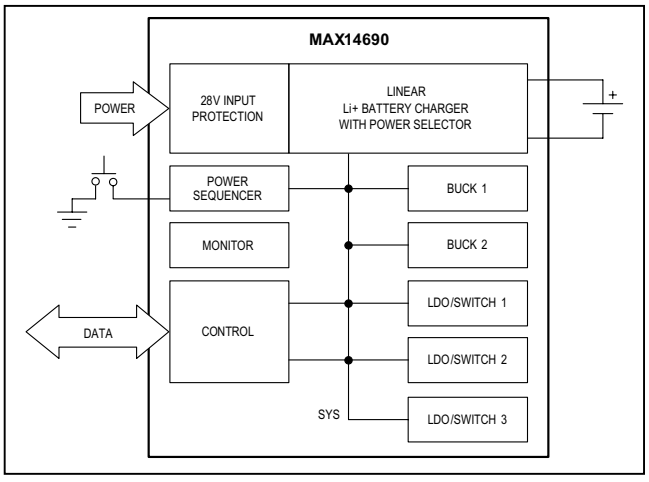
Benefits and Features

- Extend System Use Time Between Battery Charging
  - Dual Ultra-Low-I_Q 200mA Buck Regulators
    - Output Programmable from 0.8V to 1.8V and 1.5V to 3.3V
    - 0.9µA (typ) Quiescent Current
    - Automatic Burst or Forced-PWM Modes
  - Three Ultra-Low-I_Q 100mA LDOs
    - Output Programmable from 0.8V to 3.6V
    - 0.6µA (typ) Quiescent Current
    - 2.7V to 5.5V Input with Dedicated Pin
- Easy-to-Implement Li+ Battery Charging
  - Smart Power Selector
  - 28V/-5.5V Tolerant Input
  - Thermistor Monitor
- Minimize Solution Footprint Through High Integration
  - Provides Five Regulated Voltage Rails
  - Switch Mode Option on Each LDO
- Optimize System Control
  - Monitors Pushbutton for Ultra-Low Power Mode
  - Power-On Reset Delay and Voltage Sequencing
  - On-Chip Voltage Monitor Multiplexer

Applications

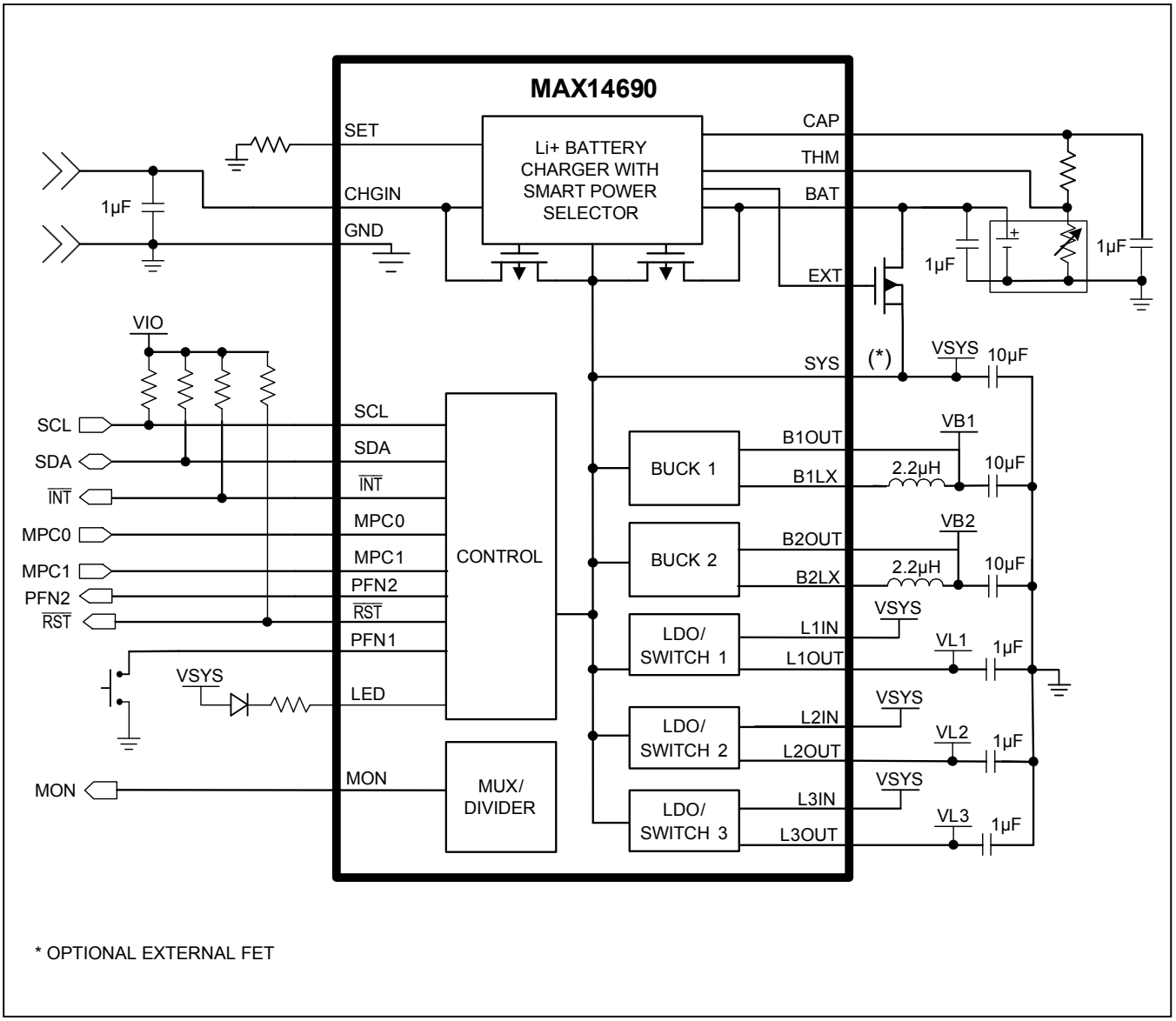
- Wearable Electronics
- Fitness Monitors
- Portable Medical Devices

Block Diagram



maxim integrated™

Typical Application Circuit



Absolute Maximum Ratings

(Voltages referenced to GND.)
SDA, SCL, THM, $\overline{RST}$, SYS, PFN1, PFN2, MPC0, MPC1, $\overline{INT}$, MON, BAT LED, L1IN, L2IN, L3IN..... -0.3V to +6.0V
B1LX, B2LX, B1OUT, B2OUT, EXT ..... -0.3V to (V_{SYS} + 0.3V)
L1OUT..... -0.3V to (V_{L1IN} + 0.3V)
L2OUT..... -0.3V to (V_{L2IN} + 0.3V)
L3OUT..... -0.3V to (V_{L3IN} + 0.3V)
CHGIN ..... -6V to +30V
CAP ..... -0.3V to min (V_{CHGIN} + 0.3V, +6V)
SET ..... -0.3V to V_{BAT} + 0.3V
Continuous Current into CHGIN, BAT, SYS .....±1000mA
Continuous Current into any other terminal .....±100mA
Continuous Power Dissipation (multilayer board at +70°C):
6 x 6 Array 36-Bump 2.72mm x 2.47mm
0.4mm Pitch WLP (derate 21.70mW/°C).....1.74W
Operating Temperature Range..... -40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature Soldering (10s).....+300°C
Soldering Temperature (reflow).....+260°C

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....46°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL SUPPLY CURRENT (L_IN Connected to SYS)						
Charger Input Current	I_{CHG}	All functions disabled		0.26		mA
		Power on, V_{CHGIN} = 5V SYS switch closed, buck regulators in burst mode, LDO1 enabled, I_{SYS} = 0A, I_{B_OUT} = 0A, I_{L_OUT} = 0A			2	
BAT Input Current	I_{BAT}	Power off, V_{CHGIN} = 0V, SYS switch open		0.95		µA
		Power on, V_{CHGIN} = 0V SYS switch closed, 2x buck regulators in Burst mode, LDOs disabled. I_{SYS} = 0A, I_{B_OUT} = 0A		3		
		Power on, V_{CHGIN} = 0V SYS switch closed, 2x buck regulators in Burst mode, LDO1 enabled, I_{SYS} = 0A, I_{B_OUT} = 0A, I_{L_OUT} = 0A		3.5		
		Power on, V_{CHGIN} = 0V SYS switch closed, 2x buck regulators in burst mode, 3x LDOs enabled, I_{SYS} = 0A, I_{B_OUT} = 0A, I_{L_OUT} =0A		4.6		

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BUCK REGULATOR 1 (V_{SYS} = +3.7V, Burst mode operation, L = 2.2µH, C = 10µF, V_{B1OUT} = 1.2V)						
Input Voltage	V_{IN_BUCK1}	Input voltage = V_{SYS}	2.7		5.5	V
Output Voltage	V_{OUT_BUCK1}	25mV step resolution (Note 3)	0.8		1.8	V
Quiescent Supply Current	I_{Q_BUCK1}	Burst mode, I_{OUT} = 0mA (Note 4)		0.915	2	µA
	I_{PWM1_BUCK1}	FPWM mode, L = 4.7µH (ESR = 0.6Ω, 2MHz RAC = 2.13Ω), I_{OUT} = 0mA		2.5	3.5	mA
Output Accuracy	ACC_{BUCK1}	I_{OUT} = 1mA (V_{OUT_BUCK1} > 1V, C > 50µF)	-2.6		+2.9	%
Load Regulation	V_{ERR_BUCK1}	From I_{OUT} = 0 to 200mA (V_{B1OUT} = 1.2V average voltage)	-3	-1		%
Peak-to-Peak Ripple in Burst Mode	$V_{PPRIPPLE1}$	I_{OUT} = 10mA, C = 20µF		25		mV
		I_{OUT} = 10mA, C = 10µF		43		
Maximum Operative Output Current	I_{OUT_BUCK1}		200			mA
B1OUT Pulldown Current	I_{LEAK_B1OUT}	V_{OUT} = V_{SYS}		200	350	µA
		V_{REG} < V_{OUT} < V_{REG} + 0.1V		10	100	nA
pMOS On-Resistance	R_{ONP_BUCK1}			0.22	0.4	□
nMOS On-Resistance	R_{ONN_BUCK1}			0.18	0.3	□
Oscillator Frequency	f_{BUCK1}	FPWM mode	1.78	2	2.24	MHz
Maximum Duty Cycle	D_{MAX_BUCK1}			100		%
Short-Circuit Current Limit	I_{SHRT_BUCK1}		1.1	1.3	1.62	A
BLX Leakage Current	I_{BLX_BUCK1}				1	µA
Active Discharge Current	I_{D_BUCK1}	V_{B1OUT} = 1.2V	8	18	36	mA
Full Turn-On Time	T_{ON_BUCK1}	Time from enable to full current capability		58		ms
Thermal-Shutdown Temperature	T_{SHDN_BUCK1}			150		°C
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_HYST\_BUCK1}$			20		°C

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BUCK REGULATOR 2 (V_{SYS} = +3.7V, Burst mode operation, L = 2.2µH, C = 10µF, V_{B2OUT} = 1.8V.)						
Input Voltage	V_{IN_BUCK2}	Input voltage = V_{SYS}	2.7		5.5	V
Output Voltage	V_{OUT_BUCK2}	50mV step resolution	1.5		3.3	V
Quiescent Supply Current (Note 4)	I_{Q_BUCK2}	Burst mode, I_{OUT} = 0mA (Note 4)		1	2	µA
	I_{PWM1_BUCK2}	FPWM mode, L = 4.7µH (ESR = 0.6Ω, 2MHz RAC = 2.13Ω) I_{OUT} = 0mA		2.4	3.5	mA
Output Accuracy	ACC_{BUCK2}	I_{OUT} = 1mA, V_{OUT_BUCK2} > 1.5V, C > 50µF, V_{SYS} > V_{B2OUT} + 150mV	-2		+2.93	%
Load Regulation	V_{ERR_BUCK2}	From I_{OUT} = 0 to 200mA, V_{B2OUT} = 1.8V average voltage	-3.1	-1		%
Peak-to-Peak Ripple In Burst Mode	$V_{PPRIPPLE2}$	I_{OUT} = 10mA, C = 20µF		38		mV
		I_{OUT} = 10mA, C = 10µF		54		
Maximum Operative Output Current	I_{OUT_BUCK2}		200			mA
B2OUT Pulldown Current	I_{LEAK_B2OUT}	V_{OUT} = V_{SYS}		5	10	µA
		V_{REG} < V_{OUT} < V_{REG} + 0.1V		10		nA
pMOS On-Resistance	R_{ONP_BUCK2}			0.22	0.4	Ω
nMOS On-Resistance	R_{ONN_BUCK2}			0.18	0.3	Ω
Oscillator Frequency	f_{BUCK2}	FPWM mode	1.78	2.00	2.24	MHz
Maximum Duty Cycle	D_{MAX_BUCK2}			100		%
Short-Circuit Current Limit	I_{SHRT_BUCK2}		1.4	1.8	2.2	A
BLX Leakage Current	I_{BLX_BUCK2}				1	µA
Active Discharge Current	I_{D_BUCK2}	V_{B2OUT} = 1.8V	8	18	36	mA
Full Turn-On Time	t_{ON_BUCK2}	Time from enable to full current capability		58		ms
Thermal-Shutdown Temperature	T_{SHDN_BUCK2}			150		°C
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_HYST\_BUCK2}$			20		°C

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDOs (C = 1µF, unless otherwise noted. Typical values are at V_{L_IN} = 3.7V, with I_{L_OUT} = 10mA, V_{L_OUT} = 3V.)						
Input Voltage	V_{IN_LDO}	LDO_Mode = 0	2.7		5.5	V
		LDO_Mode = 1	1.8		5.5	V
Quiescent Supply Current	I_{Q_LDO}	I_{L_OUT} = 0mA		0.56	1.2	µA
	$I_{Q\_LDO\_AD}$	I_{L_OUT} = 0mA, VL_IN = 1.8V, LDO_ActDSC = 1, LDO_En = 00		40		µA
Maximum Output Current	$I_{L\_OUT\_MAX}$		100			mA
Output Voltage	V_{L_OUT}		0.8		3.6	V
Output Accuracy	ACC_{LDO}	V_{L_IN} = (V_{L_OUT} + 0.5V) or higher, I_{L_OUT} = 100µA			3	%
Dropout Voltage	V_{DROP_LDO}	V_{L_IN} = 3.3V, $I_{L\_OUT\_}$ = 100mA, V_{L_OUT} = 3.3V			100	mV
Line Regulation Error	$V_{LINEREG\_LDO}$	V_{L_IN} = (V_{L_OUT} + 0.5V) to 5.5V	-0.09		0.09	%/V
Load Regulation Error	$V_{LOADREG\_LDO}$	I_{L_OUT} = 100µA to 100mA	0.003		0.008	%/mA
Line Transient	$V_{LINETRAN\_LDO}$	V_{L_IN} = 4V to 5V, 200ns rise time		±36		mV
		V_{L_IN} = 4V to 5V, 1µs rise time		±28		mV
Load Transient	$V_{LOADTRAN\_LDO}$	I_{L_OUT} = 0mA to 10mA, 200ns rise time		145		mV
		I_{L_OUT} = 0mA to 100mA, 200ns rise time		290		mV
Active Discharge Current	I_{PDL}	V_{L_IN} = 3.7V	9	21	37	mA
Turn-On Time	t_{ON_LDO}	I_{L_OUT} = 0mA, time to 90% of final value		2.3		ms
		V_{L_IN} = 3V, switch mode, I_{L_OUT} = 0mA, time to 90% of final value		0.45		ms
Short-Circuit Current Limit	I_{SHRT_LDO}	V_{L_OUT} = GND		385		mA
		V_{L_OUT} = GND, switch mode		375		mA
Switch Mode Resistance	R_{ON_LDO}	V_{L_IN} = 2.7V, switch mode		0.58	0.9	Ω
		V_{L_IN} = 1.8V, switch mode		0.89	1.35	Ω
Thermal-Shutdown Temperature	T_{SHDN_LDO}			150		°C
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_HYST\_LDO}$			16		°C
Output Noise	OUT_{NOISE}	10Hz to 100kHz, V_{L_IN} = 5V, V_{L_OUT} = 3.3V		110		µVRMS
		10Hz to 100kHz, V_{L_IN} = 5V, V_{L_OUT} = 2.5V		95		
		10Hz to 100kHz, V_{L_IN} = 5V, V_{L_OUT} = 1.2V		60		
		10Hz to 100kHz, V_{L_IN} = 5V, V_{L_OUT} = 0.8V		60		

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN TO SYS PATH (V_{CHGIN} = 5.0V, V_{SYS} = V_{SYS_REG}.) (Note 2)						
Allowed CHGIN Input Voltage Range	V_{CHGIN_RNG}		-5.5		28	V
Allowed BAT Voltage Range	V_{BAT_RNG}		0		5.5	V
V_{CHGIN} Detect Threshold	V_{CHGIN_DET}	Rising	3.8	3.9	4.1	V
		Falling	3.0	3.1	3.2	
V_{CHGIN} Overvoltage Threshold	V_{CHGIN_OV}	Rising	7.2	7.5	7.8	V
V_{CHGIN} Overvoltage Threshold Hysteresis	$V_{CHGIN\_OV\_HYS}$			200		mV
V_{CHGIN} Valid Trip Point	$V_{CHGIN-SYS\_TP}$	V_{CHGIN} - V_{SYS}, rising, V_{BAT} = 4V	45	145	280	mV
V_{CHGIN} Valid Trip-Point Hysteresis	$V_{CHGIN-SYS\_TP\_HYS}$			200		mV
Input Limiter Current	I_{LIM}	ILimCntl[1:0] = 00		0		mA
		ILimCntl[1:0] = 01		90		
		ILimCntl[1:0] = 10		450		
		ILimCntl[1:0] = 11		1000		
Internal CAP Regulator	V_{CAP}	V_{CHGIN} = 5V	3.9	4.2	4.7	V
SYS Regulation Voltage	V_{SYS_REG}	V_{CHGIN} = 5V, I_{SYS} = 1mA	4.55	4.65	4.75	V
SYS Regulation Voltage Dropout	$V_{CHGIN-SYS}$	V_{CHGIN} = 4V, I_{SYS} = 1mA		40		mV
CHGIN-to-SYS On-Resistance	$R_{CHGIN-SYS}$	V_{CHGIN} = 4.4V, I_{SYS} = 400mA		0.370	0.66	□
Thermal-Shutdown Temperature	T_{CHGIN_SHDN}	(Note 5)		+150		°C
Thermal-Shutdown Temperature Hysteresis	$T_{CHGIN\_SHDN\_HYS}$			20		°C
Input Current Soft-Start Time	t_{SFST_LIM}			1		ms
Internal Supply Switchover Threshold	V_{CCINT_TH}	V_{CHGIN} = V_{CAP} rising, V_{BAT} = 4.2V	2.5	2.8	3.0	V

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS, BATTERY, AND V_{CCINT} UVLOs						
SYS UVLO Threshold	$V_{SYSUVLO\_R}$	Rising		2.644	2.69	V
	$V_{SYSUVLO\_F}$	Falling	2.57	2.618	2.67	V
SYS UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$	Hysteresis		26		mV
SYS UVLO Falling Debounce Time	$t_{SYSUVLO\_FDEB}$	SYS falling		20		µs
V_{CCINT} UVLO Threshold (POR)	V_{UVLO}	V_{CCINT} rising	0.8	1.82	2.6	V
V_{CCINT} UVLO Threshold Hysteresis	V_{UVLO_HYS}			140		mV
BAT UVLO Threshold	V_{BAT_UVLO}	Rising (valid only when CHGIN is present, when $V_{BAT} < V_{BAT\_UVLO}$, the BAT-SYS switch opens and BAT is connected to SYS through a diode.)	1.9	2.05	2.2	V
BAT UVLO Threshold Hysteresis	$V_{BAT\_UVLO\_HYS}$	Hysteresis		50		mV
BATTERY CHARGER (V_{BAT} = 4.2V. Typical values are at V_{CHRGIN} = 5.0V, V_{SYS} = V_{SYS_REG}.)						
BAT-to-SYS On-Resistance	$R_{BAT-SYS}$	V_{BAT} = 4.2V, I_{BAT} = 300mA		80	140	m□
Current Reduce Thermal Threshold Temperature	T_{CHG_LIM}	(Note 6)		120		°C
BAT-to-SYS Switch On Threshold	$V_{BAT-SYS-ON}$	SYS falling	10	22	35	mV
BAT-to-SYS Switch Off Threshold	$V_{BAT-SYS-OFF}$	SYS rising	-3	-1.5	0	mV
SYS Threshold Voltage Charger Limiting Current	V_{SYS_LIM}	Threshold at which the charger starts to limit the current due to SYS falling		4.36		V
FChg-MtChg Threshold	$V_{FCHG-MTCHG}$	If V_{SYS} drops below this value the charger will not move to maintain charge		4.49		V
FChg-MtChg Threshold Hysteresis	$V_{FCHG-MTCHG\_HYS}$			50		mV
Charger Current Soft-Start Time	t_{CHG_SOFT}			1		ms
PRECHARGE						
Precharge Current	I_{PCHG}	IPChg = 00		5		%IFChg
		IPChg = 01	9	10	11	
		IPChg = 10		20		
		IPChg = 11		30		

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Prequalification Threshold	V_{BAT_PChg}	VPChg = 000, V_{BAT} rising			2.1		V
		VPChg = 001, V_{BAT} rising		2.15	2.25	2.35	
		VPChg = 010, V_{BAT} rising			2.40		
		VPChg = 011, V_{BAT} rising			2.55		
		VPChg = 100, V_{BAT} rising			2.7		
		VPChg = 101, V_{BAT} rising			2.85		
		VPChg = 110, V_{BAT} rising			3.0		
		VPChg = 111, V_{BAT} rising			3.15		
Prequalification Threshold Hysteresis	$V_{BAT\_PChg\_HYS}$				90		mV
FAST CHARGE							
SET Current Gain Factor	K_{SET}				2000		A/A
SET Regulation Voltage	V_{SET}				1		V
Fast-Charge Current	I_{FChg}	R_{SET} = 400kΩ			5		mA
		R_{SET} = 40kΩ		45	50	55	
		R_{SET} = 4kΩ			500		
1/2 Fast-Charge Current Comparator Threshold	I_{FC_HALF}				50		%IFChg
1/5 Fast-Charge Current Comparator Threshold	I_{FC_FIFTH}				20		%IFChg
MAINTAIN CHARGE							
Charge Done Qualification	I_{Chg_DONE}	ChgDone = 00			5		%IFChg
		ChgDone = 01		8.5	10	11.5	
		ChgDone = 10			20		
		ChgDone = 11			30		
BAT Regulation Voltage	V_{BatReg}	BatReg = 000			4.05		V
		BatReg = 001			4.10		
		BatReg = 010			4.15		
		BatReg = 011	T_A = +25°C	4.179	4.2	4.221	
			T_A = -40°C to +85°C	4.158	4.2	4.242	
		BatReg = 100			4.25		
		BatReg = 101			4.3		
		BatReg = 110	T_A = +25°C	4.32	4.35	4.38	
			T_A = -40°C to +85°C	4.30	4.35	4.40	
BAT Recharge Threshold	$V_{BatReChg}$	BatReChg = 00			70		mV
		BatReChg = 01			120		
		BatReChg = 10			170		
		BatReChg = 11			220		

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGER TIMER						
Maximum Prequalification Time	t_{PChg}	PChgTmr = 00		30		min
		PChgTmr = 01		60		
		PChgTmr = 10		120		
		PChgTmr = 11		240		
Maximum Fast-Charge Time	t_{FChg}	FChgTmr = 00		75		min
		FChgTmr = 01		150		
		FChgTmr = 10		300		
		FChgTmr = 11		600		
Maintain-Charge Time	t_{MTChg}	TOChgTmr = 00		0		min
		TOChgTmr = 01		15		
		TOChgTmr = 10		30		
		TOChgTmr = 11		60		
Timer Accuracy	t_{CHG_ACC}		-10		+10	%
Timer Extend Threshold	TIM_{EXD_THRES}	If charge current is reduced due to I_{LIM} or TDIE, this is the percentage of charge current below which timer clock operates at half speed		50		%
Timer Suspend Threshold	TIM_{SUS_THRES}	If charge current is reduced due to I_{LIM} or TDIE, this is the percentage of charge current below which timer clock pauses		20		%
THERMISTOR MONITOR AND NTC DETECTION (RPU = 10k, RTHM = 10k, 3380ß)						
THM Hot Threshold	T_4	V_{THM} falling	21.3	23.3	25.3	%CAP
THM Warm Threshold	T_3	V_{THM} falling	30.9	32.9	34.9	
THM Cool Threshold	T_2	V_{THM} rising	62.5	64.5	66.5	
THM Cold Threshold	T_1	V_{THM} rising	71.9	73.9	75.9	
THM Disable Threshold	THM_{DIS}	V_{THM} rising	91	93	95	
THM Threshold Hysteresis	THM_{HYS}			60		mV
THM Input Leakage	I_{LKG_THM}		-1		+1	µA

Electrical Characteristics (continued)

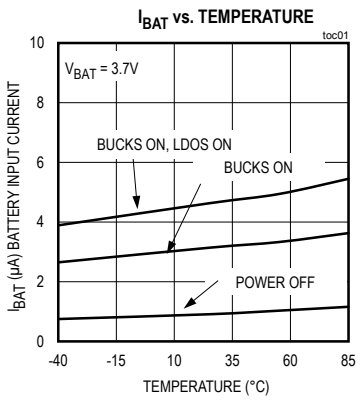
(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

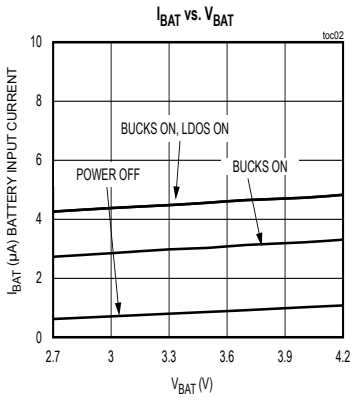
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL SIGNALS						
PFN1 PFN2 Button Timer Accuracy			-10		+10	%
Input Logic-High (SDA, SCL, MPC0, MPC1, PFN1, PFN2)	V_{IH}		1.4			V
Input Logic-Low (SDA, SCL, MPC0, MPC1, PFN1, PFN2)	V_{IL}				0.5	V
Output Logic-Low (SDA, $\overline{RST}$, $\overline{INT}$, LED, PFN2)	V_{OL}	I_{OL} = 4mA			0.4	V
High Level Leakage Current (SDA, $\overline{RST}$, $\overline{INT}$, LED, PFN2)	I_{LK}		-1		+1	µA
SCL Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
START Condition (Repeated) Hold-Time	$t_{HD:STA}$	(Note 7)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 8)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 8)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 9)		50		ns

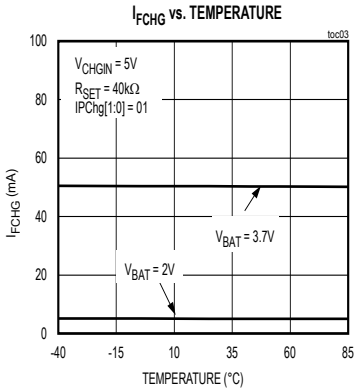
Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 3: For input voltages larger than 4.4V, output regulated voltage below 1V are available ONLY in burst mode.
Note 4: This value is included in the I_{BAT} quiescent current values for the on states.
Note 5: When the die temperature exceeds T_{CHGIN_SHDN}, the CHGIN-to-SYS path, and the charger is turned off.
Note 6: When the die temperature exceeds T_{CHG_LIM}, the charger current starts to decrease.
Note 7: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 8: The maximum $t_{HD:DAT}$ has to be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 9: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

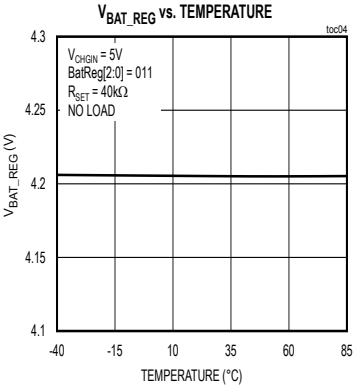
Typical Operating Characteristics

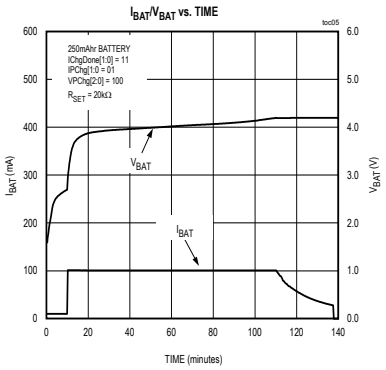
(V_{BAT} = 3.7V, V_{CHGIN} = 0V, registers in their default state, T_A = +25°C, unless otherwise noted.)

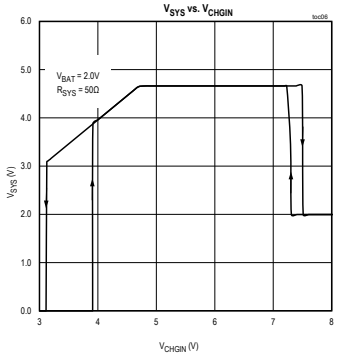


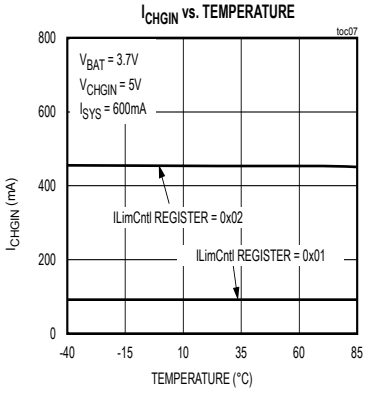


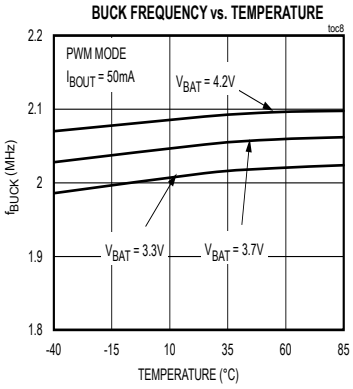






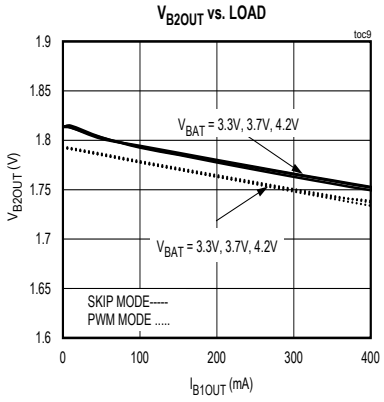


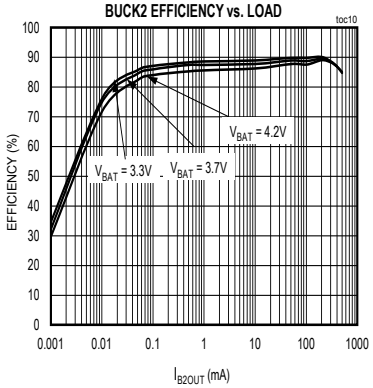


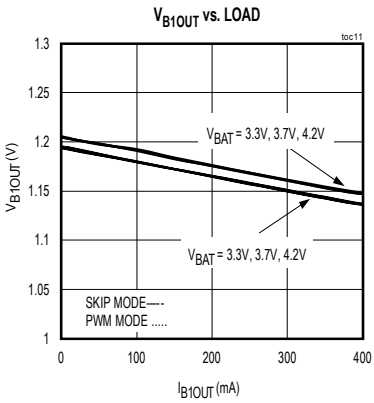


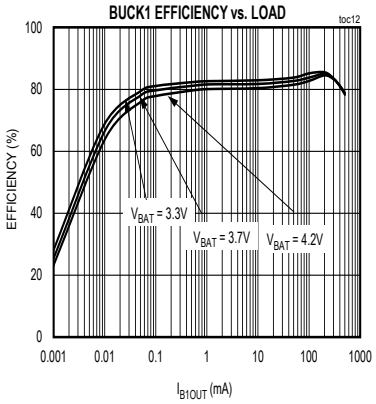
Typical Operating Characteristics (continued)

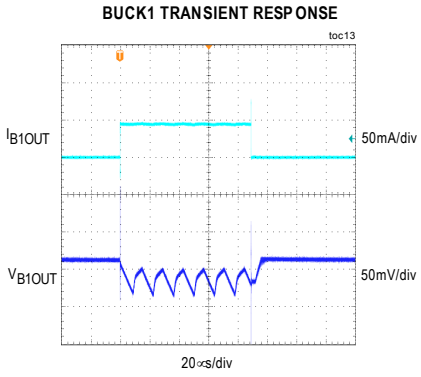
(V_{BAT} = 3.7V, V_{CHGIN} = 0V, registers in their default state, T_A = +25°C, unless otherwise noted.)

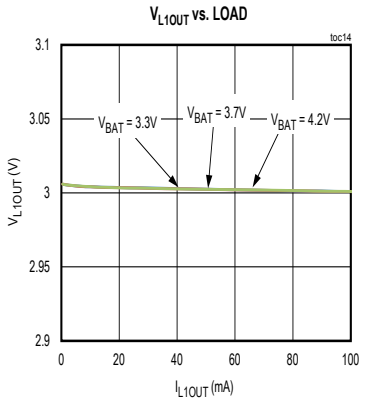


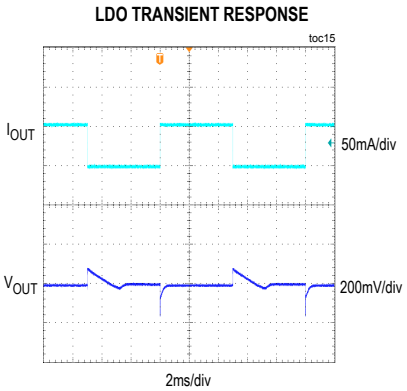


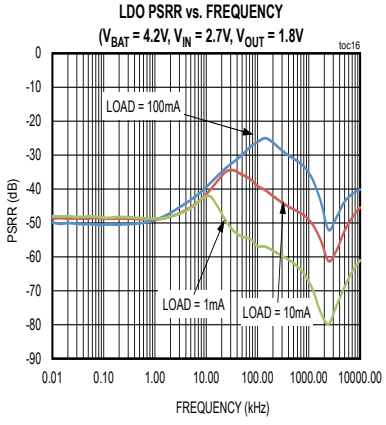


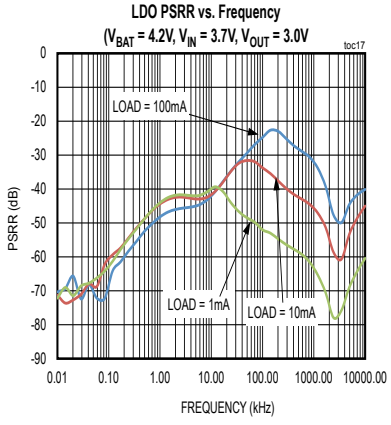




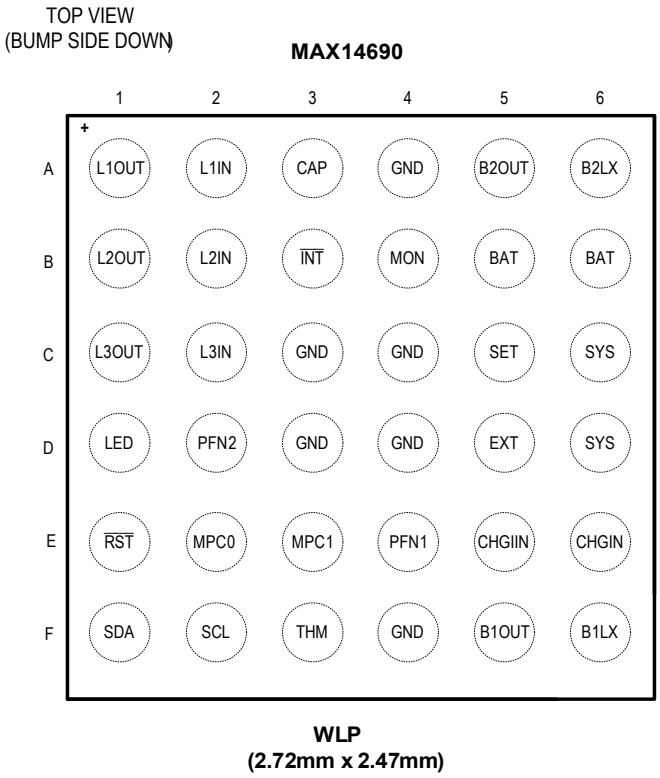








Pin Configuration



WLP
(2.72mm x 2.47mm)

Bump Description

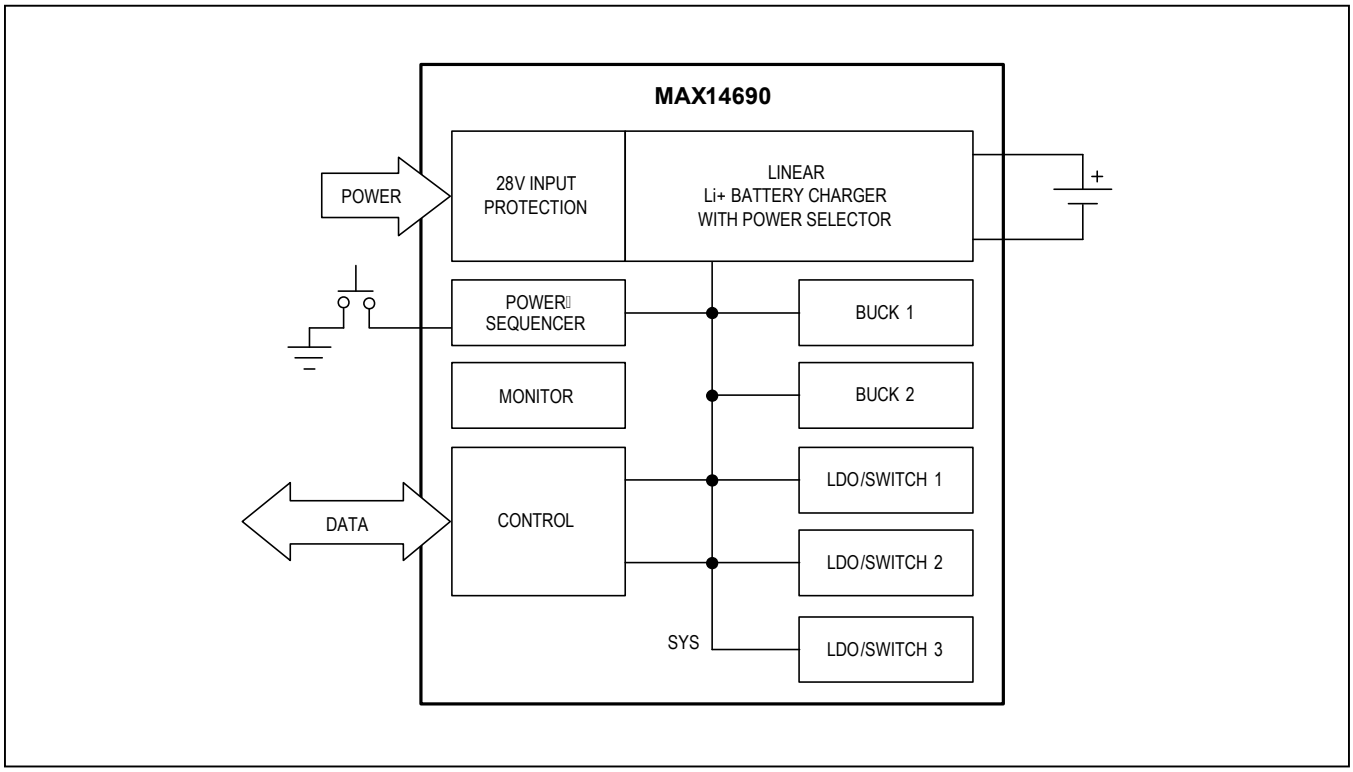
BUMP	NAME	FUNCTION
A1	L1OUT	LDO1 Output. Bypass with a minimum 1µF capacitor to GND.
A2	L1IN	LDO1 Input
A3	CAP	Bypass for Internal LDO. Bypass with a 1µF capacitor to GND.
A4, C3, C4 D3, D4, F4	GND	Ground
A5	B2OUT	1.5V – 3.3V Buck Regulator Output Feedback. Bypass with a minimum 10µF capacitor to GND.
A6	B2LX	1.5V – 3.3V Buck Regulator Switch. Connect 2.2µH inductor to B2OUT.
B1	L2OUT	LDO2 Output. Bypass with a minimum 1µF capacitor to GND.
B2	L2IN	LDO2 Input
B3	$\overline{INT}$	Open-Drain, Active-Low Interrupt Output.
B4	MON	Voltage Monitor Pin
B5,B6	BAT	Battery Connection. Connect BAT to a positive battery terminal, bypass BAT with a minimum 1µF capacitor to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
C1	L3OUT	LDO3 Output. Bypass with a minimum 1µF capacitor to GND.
C2	L3IN	LDO3 Input
C5	SET	External Resistor For Battery Charge Current Level Setting. Do not connect any external capacitance on this pin; maximum allowed capacitance (C_{SET} < 5µs/R_{SET}) pF.
C6, D6	SYS	System Load Connection. Connect SYS to the system load. Bypass SYS with a minimum 10µF low-ESR ceramic capacitor to GND.
D1	LED	LED Open-Drain Pulldown Current. Add an external current limiting pullup resistor.
D2	PFN2	Power Function Control Input/Output. Programmable functionality via PwrFnMode. See Table 1.
D5	EXT	Push-Pull Gate Drive for Optional External pFET from BAT-to-SYS. Output is pulled to GND when charger is disconnected and internal BAT-SYS FET is switched on. Otherwise, this output is pulled high to the SYS voltage.
E1	$\overline{RST}$	Power-On Reset Output. Active-low, open-drain.
E2	MPC0	Multipurpose Configuration Input 0
E3	MPC1	Multipurpose Configuration Input 1
E4	PFN1	Power Function Control Input. Programmable functionality via PwrFnMode. See Table 1.
E5, E6	CHGIN	+28V Protected Charger Input. Bypass CHGIN with 1µF capacitor to GND.
F1	SDA	Open-Drain, I^2C Serial Data Input/Output.
F2	SCL	I^2C Serial Clock Input
F3	THM	Battery Temperature Thermistor Measurement Connection. Connect a 10kΩ resistor from THM to CAP and a 10kΩ, 3380A NTC thermistor from THM to GND.
F5	B1OUT	0.8V – 1.8V Buck Regulator Output Feedback. Bypass B1OUT with a minimum 10µF capacitor to GND.
F6	B1LX	0.8V – 1.8V Buck Regulator Switch Terminal. Connect B1LX to B1OUT with a 2.2µH inductor.

Note: *All capacitance values listed in this document refer to effective capacitance. Be sure to specify capacitors that will meet these requirements under typical system operating conditions taking into consideration the effects of voltage and temperature.*

Block Diagram



Detailed Description

Power Regulation

The MAX14690 family includes two high-efficiency, low quiescent current buck regulators, and three low quiescent current linear regulators that are also configurable as power switches. Excellent light-load efficiency allows the switching regulators to run continuously without significant energy cost. The standard operating mode for the buck regulators is burst mode, but they can be forced to operate in PWM mode through an I^2C register.

Power On/Off and Reset Control

The behavior of power function control pins (PFN1 and PFN2) is preconfigured to support one of the multiple types of wearable application cases. Table 1 describes the behavior of the PFN1 and PFN2 pins based on the PwrRstCfg[3:0] bits and Figure 1 shows basic flow diagrams associated with each mode.

A soft reset will reset all register values and pulls the $\overline{RST}$ line low. Hard reset initiates a complete Power-On Reset sequence.

Table 1. Power Function Input Control Modes

PwrRstCfg [3:0]	PFN1	PFN1 PU/PD PFNxResEna = 1 (0x1D[7])	PFN2	PFN2 PU/PD PFNxResEna = 1 (0x1D[7])	NOTES
0000	Enable	Pulldown	Active-Low Manual Reset	Pullup*	On/off Mode with 10ms debounce. Active-high on/off control on PFN1. Logic-low on PFN2 generates 10ms pulse on $\overline{RST}$. Note that, in this mode, the PWR_OFF_CMD in I^2C has no effect.
0001	Disable	Pullup*	Active-Low Manual Reset	Pullup*	On/off Mode with 10ms debounce. Active-low on/off control on PFN1. Logic-low on PFN2 generates 10ms pulse on $\overline{RST}$. Note that, in this mode, the PWR_OFF_CMD in I^2C has no effect.
0010	Hard-Reset on Rising Edge	Pulldown	Soft-Reset on Rising-Edge	Pulldown	Always-On Mode (i.e., device can only be put in off state through PWR_OFF_CMD). 50ms hard-reset off time. 10ms soft-reset pulse time. 200ms delay prior to both reset behaviors.
0011	Hard-Reset on Falling Edge	Pullup*	Soft-Reset Falling-Edge	Pullup*	Always-On Mode (i.e., device can only be put in off state via PWR_OFF_CMD). 50ms hard-reset off time. 10ms soft-reset pulse time. 200ms delay prior to both reset behaviors.
0100	Hard-Reset After CHGIN Attach When High	Pulldown	Soft-Reset After CHGIN Attach When High	Pulldown	Charger Reset High Mode (i.e., device can only be put in off state through PWR_OFF_CMD). 50ms hard-reset off time. 10ms soft-reset pulse time. 200ms delay prior to both reset behaviors.
0101	Hard-Reset After CHGIN Attach When Low	Pullup*	Soft-Reset After CHGIN Attach When Low	Pullup*	Charger Reset Low Mode (i.e., device can only be put in off state through PWR_OFF_CMD). 50ms hard-reset off time. 10ms soft-reset pulse time. 200ms delay prior to both reset behaviors.
0110	$\overline{KIN}$	Pullup*	$\overline{KOUT}$	None	On/Off mode through specific long-press button timing or PWR_OFF_CMD.
0111	$\overline{KIN}$	Pullup*	$\overline{KOUT}$	None	Custom Soft-Reset. Off mode through PWR_OFF_CMD (30ms delay). On mode through specific long-press (3s) or CHGIN insertion. Soft-reset through specific long press (12s).
1000-1111	—	—	—	—	Reserved

* *Pullup is connected to* V_{CCINT}.

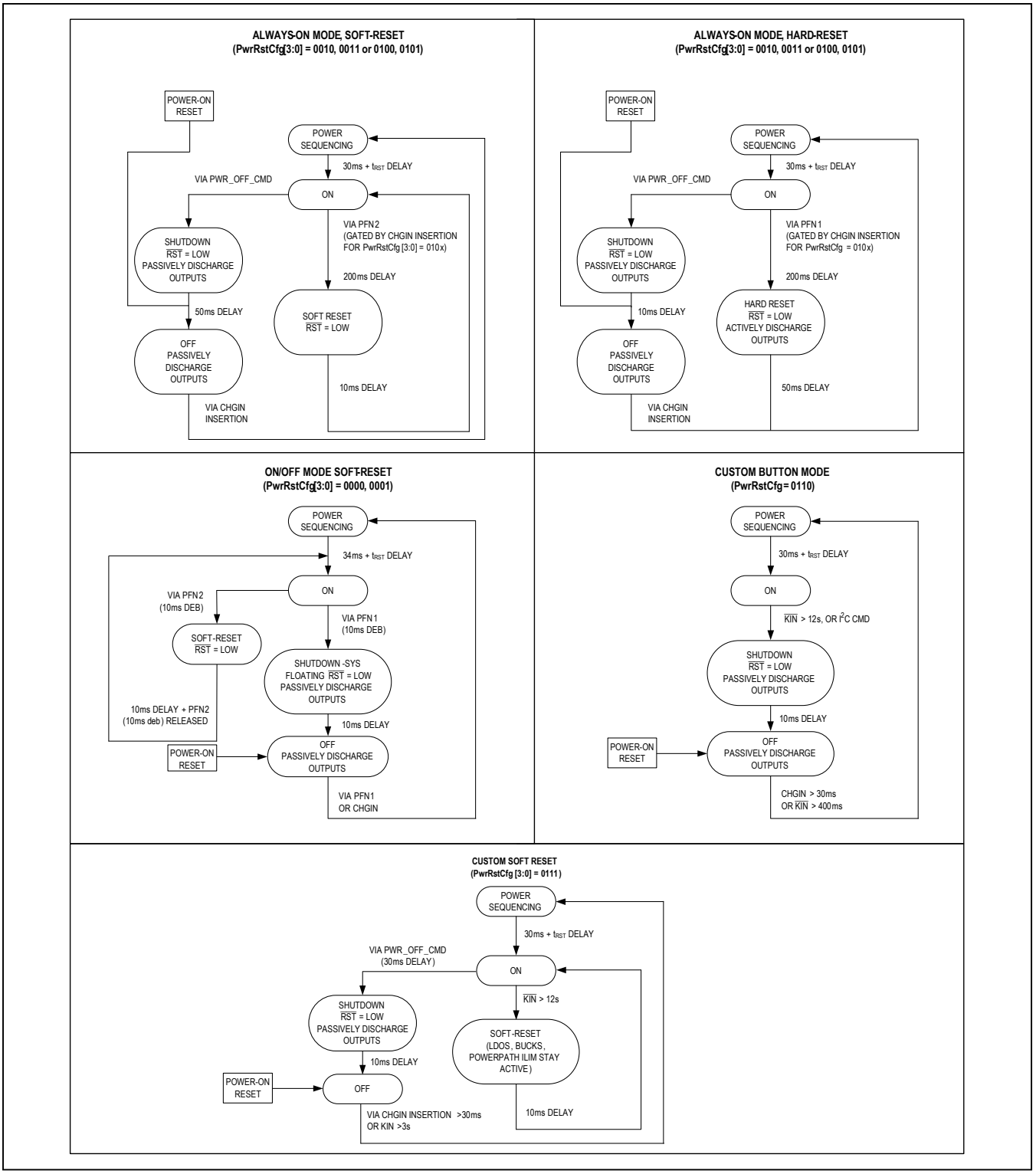


Figure 1. Power Function Input Control Modes Flow Diagrams

Power Sequencing

The sequencing of the buck regulators and LDOs during power-on is configurable. See Table 1 for details. Regulators can be configured to turn on at one of three points during the power-on process: 34ms after the power-on event, after the $\overline{RST}$ signal is released, or at two points in between. The two points between SYS and $\overline{RST}$ are fixed proportionally to the duration of the Power-On Reset (POR) process, but the overall time of the reset delay is configurable (80ms, 120ms, 220ms, 420ms). The timing relationship is presented graphically in Figure 2.

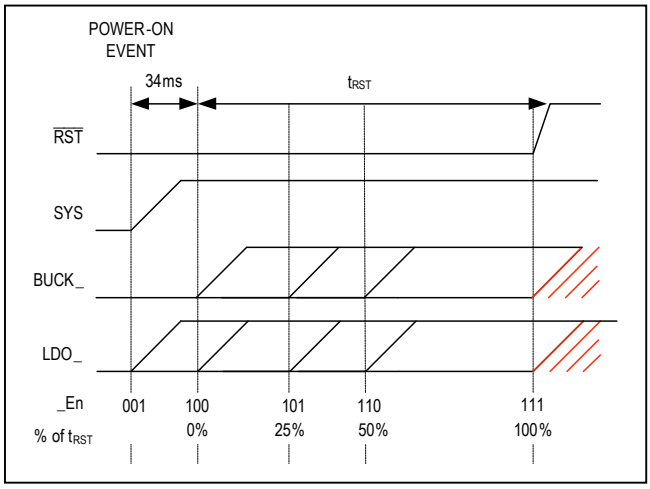


Figure 2. Reset Sequence Programming

Additionally, the regulators can be selected to default off and can be turned on with an I²C command after $\overline{RST}$ is released. Each LDO regulator can be configured to be always-on as long as SYS or BAT is present.

The SYS voltage is monitored during the power-on sequence. If an undervoltage condition is detected on SYS during the sequencing process with a valid voltage at CHGIN, the process repeats from the point where SYS was enabled to allow more time for the voltage to stabilize. If there is not a valid voltage at CHGIN, the device returns to the off state to avoid draining the battery. Power is also turned off if an undervoltage condition is detected on SYS.

Smart Power Selector

The smart power selector seamlessly distributes power from the external CHGIN input to the battery (BAT) and the system (SYS). With both an external adapter and battery connected, the smart power selector basic functions are:

- When the system load requirements are less than the input current limit, the battery is charged with residual power from the input.
- When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load.
- When the battery is connected and there is no external power input, the system is powered from the battery.

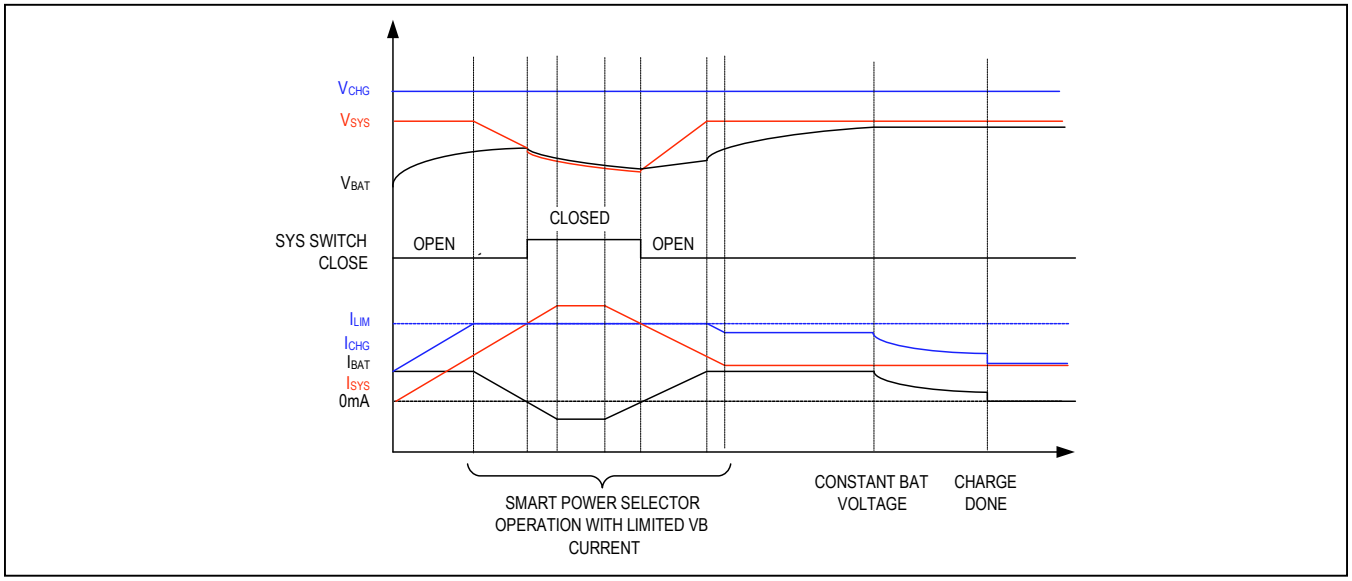


Figure 3. Smart Power Selector Current/Voltage Behavior

Thermal Current Regulation

In case the die temperature exceeds the normal limit, the MAX14690 will attempt to limit the temperature increase by reducing the input current from CHGIN. In this condition, the system load has priority over charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit, no input current is drawn from CHGIN and the battery powers the entire system load.

System Load Switch

An internal 80mΩ (typ) MOSFET connects SYS to BAT when no voltage source is available on CHGIN. When an external source is detected at CHGIN, this switch opens and SYS is powered from the input source through the input current limiter. The SYS-to-BAT switch also prevents V_{SYS} from falling below V_{BAT} when the system load exceeds the input current limit. If V_{SYS} drops to V_{BAT} due to the current limit, the load switch turns on so the load is supported by the battery. If the system load continuously exceeds the input current limit the battery is not charged. This is useful for handling loads that are nominally below the input current limit but have high current peaks exceeding the input current limit. During these peaks, battery energy is used, but at all other times the battery charges. See Figure 3.

The pin EXT can drive the gate of an external pMOS connected between SYS (source, bulk) and BAT (drain) in parallel to the internal one.

EXT voltage is the buffered version of the internal gate command that controls the internal 80mΩ (typ) MOSFET.

Note: The body diode of an external pMOS connected between BAT and SYS remains present when the device is in off mode.

Input Limiter

The input limiter distributes power from the external adapter to the system load and battery charger. In addition to the input limiter's primary function of passing power to the system load and charger, it performs several additional functions to optimize use of available power:

Invalid CHGIN Voltage Protection: If CHGIN is above the overvoltage threshold, the MAX14690 enters overvoltage lockout (OVL). OVL protects the MAX14690 and downstream circuitry from high-voltage stress up to 28V and down to -5.5V. During OVL, the internal circuit remains powered and an interrupt is sent to the host. During OVL, the charger turns off and the system load switch closes, allowing the battery to power SYS. CHGIN is also invalid if it is less than V_{BAT}, or less than the USB undervoltage threshold. With an invalid input voltage, the SYS-to-BAT load switch closes and allows the battery to power SYS.

CHGIN Input Current Limit: The CHGIN input current is limited to prevent input overload. The input current limit is controlled by I^2C.

Thermal Limiting: In case the die temperature exceeds the normal limit (T_{CHG_LIM}), the MAX14690 attempts to limit temperature increase by reducing the input current from CHGIN. In this condition, the system load has priority over the charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit (T_{CHGIN_SHDN}), no input current is drawn from CHGIN and the battery powers the entire system load.

Adaptive Battery Charging: While the system is powered from CHGIN, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, an adaptive charger control loop reduces charge current to prevent V_{SYS} from collapsing.

When the charge current is reduced below 50% due to I_{LIM} or T_{DIE}, the timer clock operates at half speed. When the charge current is reduced below 20% due to I_{LIM} or T_{DIE}, the timer clock is paused.

Fast-Charge Current Setting

The MAX14690 uses an external resistor connected from SET to GND to set the fast-charge current. The pre-charge and charge-termination currents are programmed as a percentage of this value via I^2C registers. The fast-charge current resistor can be calculated as:

$$R_{SET} = K_{SET} \times V_{SET}/I_{FChg}$$

where K_{SET} has a typical value of 2000A/A and V_{SET} has a typical value of 1V. The range of acceptable resistors for R_{SET} is 4kΩ to 400kΩ.

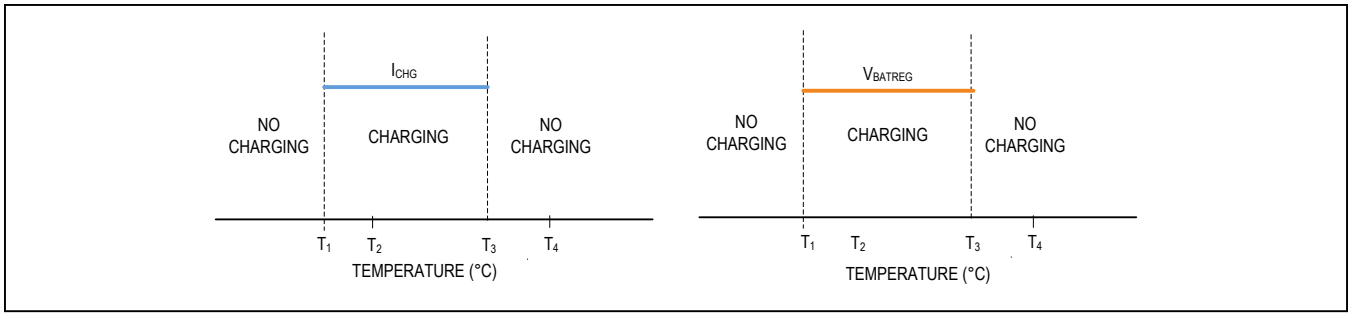


Figure 4a. Charging Behavior Using Thermistor Monitor

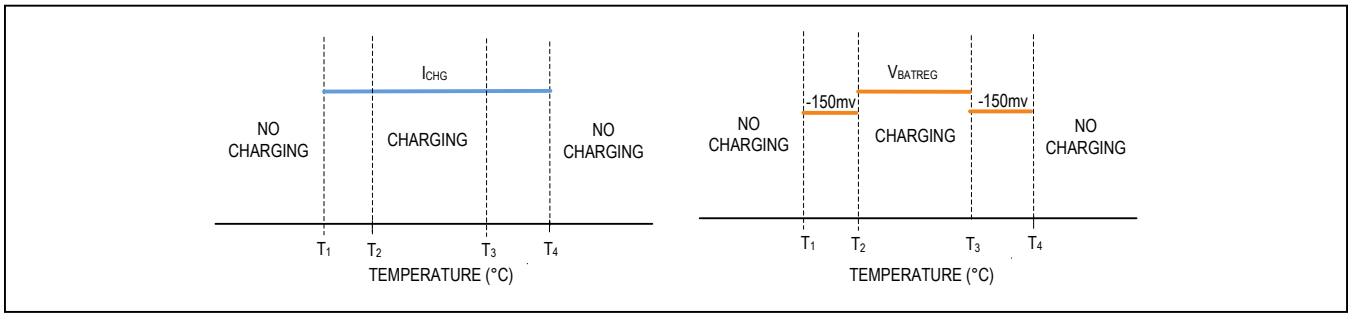


Figure 4b. Charging Behavior Using JEITA Monitor

Table 2. Thermistor Monitoring/JEITA Monitoring Enable Control

ThermEn	JEITAEn	FUNCTION
0	—	Thermistor/JEITA Monitoring Off
1	0	Thermistor Monitoring On
1	1	JEITA Monitoring On

Thermistor/JEITA Monitoring with Charger Shutdown

The MAX14690 includes thermistor and JEITA monitoring to enhance safety when charging Li+ batteries. The battery pack temperature is measured from a divider formed by a pullup resistor connected to CAP and the battery-pack thermistor. The THM pin measures the voltage across the resistor divider and converts it to temperature. There are five temperature zones that can be read from the ThermStat bits in I2C. When thermistor monitoring is enabled, the charger is disabled for temperatures below T1 or above T3, as shown in Figure 4a. When JEITA monitoring is enabled, the charger will be disabled for temperatures below T1 or above T4, as shown in Figure 4b. See Table 2 and Table 3 on configuring the thermistor/JEITA monitoring.

Table 3. Voltage and Example Temperature Thresholds

	%CAP Thresholds on THM	Temperature Thresholds R_{PU} = 10k, R_{THM} = 10k (β = 3380)
T1	73.9	0°C
T2	64.5	10°C
T3	32.9	45°C
T4	23.3	60°C

I2C Interface

The MAX14690 uses the two-wire I2C interface to communicate with the host microcontroller. The configuration settings and status information provided through this interface are detailed in the register descriptions.

I2C Addresses

The registers of the MAX14690 are accessed through the slave address of 0101000 (0x50 for writes/0x51 for reads).

Thermistor Monitoring with Charger Shutdown

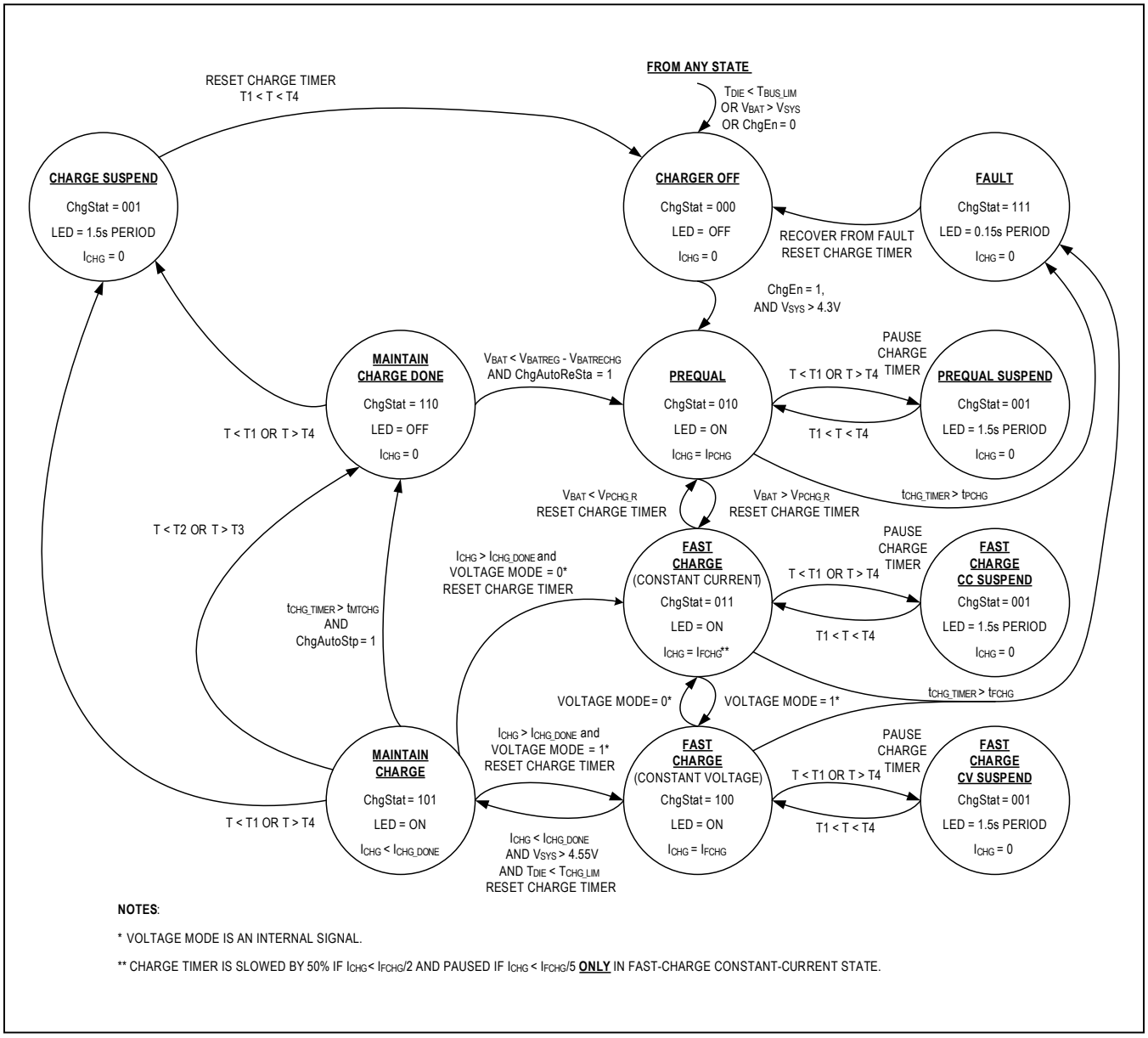


Figure 5. Battery Charger State Diagram

Applications Information

I²C Interface

The MAX14690_ contain an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

Start, Stop, And Repeated Start Conditions

When writing to the MAX14690_ using I²C, the master sends a START condition (S) followed by the MAX14690_ I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See Figure 6.

Table 4. I²C Slave Addresses

ADDRESS FORMAT	HEX	BINARY
7-Bit Slave ID	0x28	0101000
Write Address	0x50	01010000
Read Address	0x51	01010001

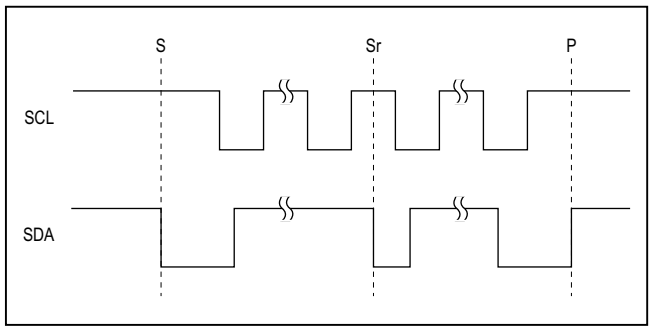


Figure 6. I²C START, STOP and REPEATED START Conditions

Slave Address

Set the Read/Write bit high to configure the MAX14690_ to read mode (Table 4). Set the Read/Write bit low to configure the MAX14690_ to write mode. The address is the first byte of information sent to the MAX14690_ after the START condition.

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *Start, Stop, And Repeated Start Conditions* section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 7). The following procedure describes the single byte write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends 8 data bits
- 7) The slave asserts an ACK on the data line
- 8) The master generates a STOP condition

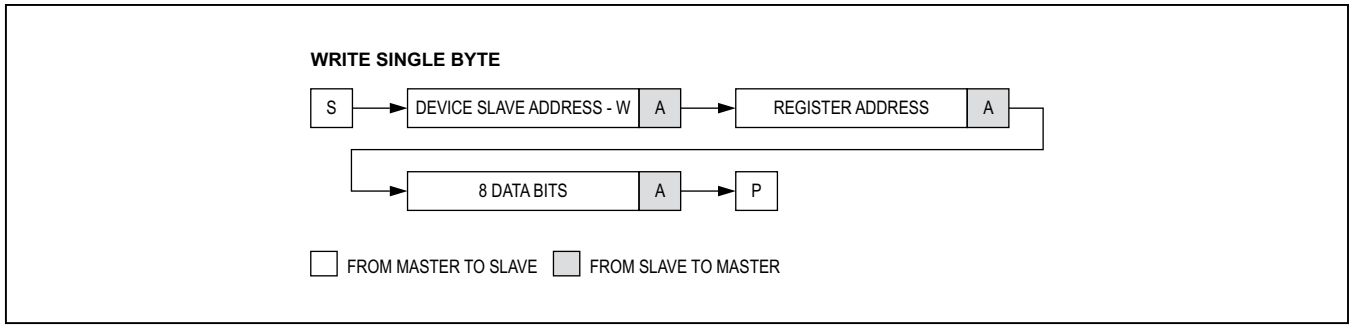


Figure 7. Write Byte Sequence

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 8). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends eight data bits
- 7) The slave asserts an ACK on the data line
- 8) Repeat 6 and 7 N-1 times
- 9) The master generates a STOP condition

Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 9). The following procedure describes the single byte read operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends a REPEATED START condition
- 7) The master sends the 7-bit slave address plus a read bit (high)
- 8) The addressed slave asserts an ACK on the data line
- 9) The slave sends eight data bits
- 10) The master asserts a NACK on the data line
- 11) The master generates a STOP condition

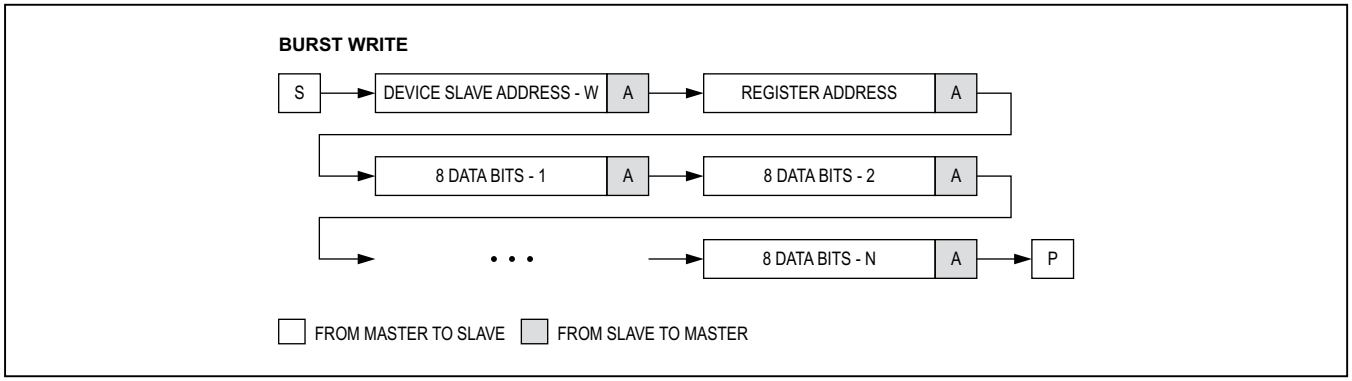


Figure 8. Burst Write Sequence

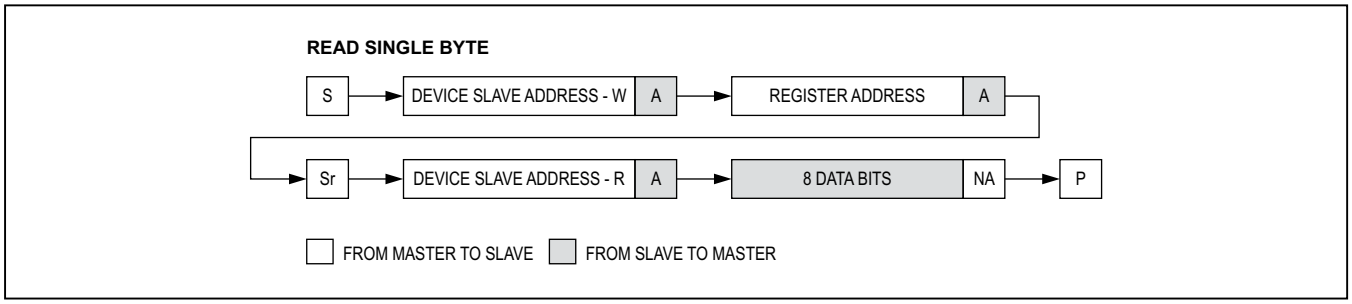


Figure 9. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 210). The following procedure describes the burst byte read operation:

- 1)The master sends a START condition
- 2)The master sends the 7-bit slave address plus a write bit (low)
- 3)The addressed slave asserts an ACK on the data line
- 4)The master sends the 8-bit register address
- 5)The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6)The master sends a REPEATED START condition
- 7)The master sends the 7-bit slave address plus a read bit (high)
- 8)The slave asserts an ACK on the data line
- 9)The slave sends eight data bits
- 10) The master asserts an ACK on the data line
- 11) Repeat 9 and 10 N-2 times
- 12) The slave sends the last eight data bits
- 13) The master asserts a NACK on the data line
- 14) The master generates a STOP condition

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX14690_ generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see Figure 3a11). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

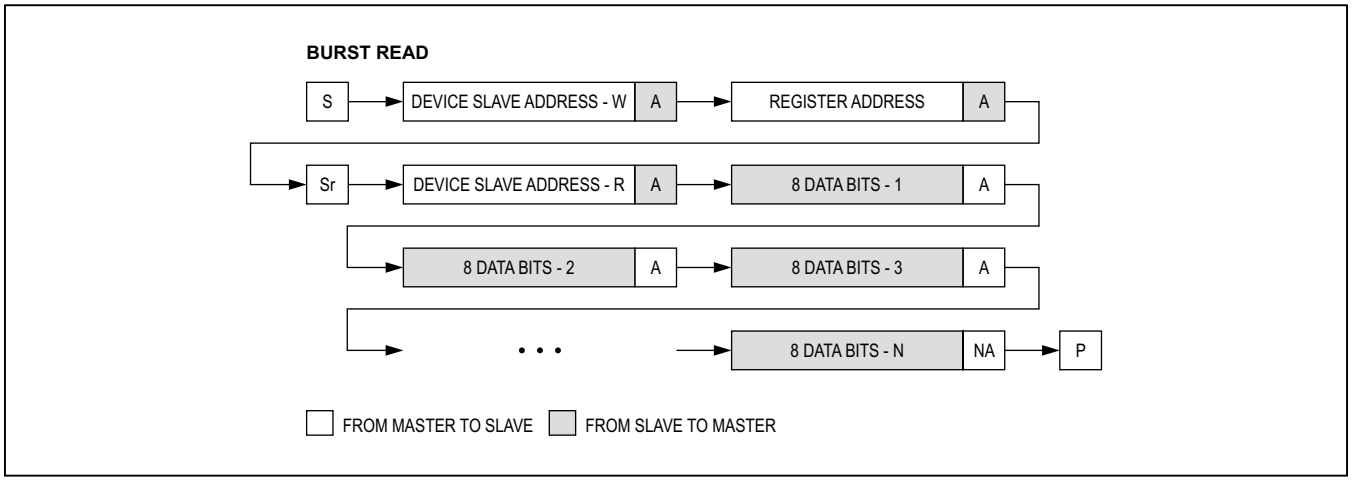


Figure 10. Burst Read Sequence

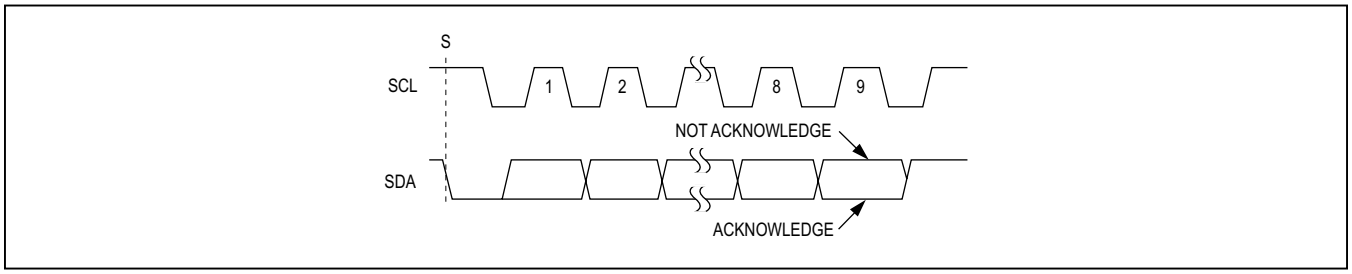


Figure 11. Acknowledge