Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MAX14748

USB Type-C Charger

General Description

The MAX14748 USB battery charger integrates a charger detector, boost/buck converter, and Li+ battery charger with smart power selector to provide fast and safe charging of 2s Li+ battery packs.

The MAX14748 provides support for devices functioning as a UFP/DRP per the USB Type-C 1.1 standard, while also providing detection of legacy USB Battery Charging Specification, Revision 1.2 (BC1.2) compliant chargers in addition to other nonstandard chargers. The programmable Automatic Input Current Limiting (AICL) feature ensures that maximum safe current is drawn from the charging adapter.

The Li+ charger includes an automatic Smart Power Selector™ to simultaneously charge the battery and provide power to the system load. The Smart Power Selector function will supplement the system power with the battery if power from the charging adapter is insufficient. The Li+ charger features JEITA thermal monitoring and charger voltage/current reduction or charger disable.

The MAX14748 is available in a 54-bump, 0.4mm pitch, 3.97mm x 2.77mm x 0.64mm wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

Applications

- Digital Imaging (DSC, DVC)
- Wireless Speakers
- Handheld Barcode Readers

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Minimize Power Management Footprint Through High Integration
  - 13mΩ (typ) Integrated Battery To System Switch
  - Thermal Current Limiting
  - DC-DC Converter with Boost and Reverse Buck
  - High Efficiency
    - 92% in Boost Mode at 1A Output Current and 7.4V Battery Voltage
    - 94% in Reverse Buck Mode at 500mA Output
  - Internal USB Switch for USB D+/D- Data Lines
- Easy-to-Implement Li+ Battery Charging
  - Charges 2s Li-Ion Batteries from Legacy 5V USB Adapters
    - 15W Input Power with 3A Type-C Adapter
    - 7.5W Input Power with DCP Adapter
    - 1A System/Charge Current From DCP Adapter
    - 2A System/Charge Current From 3A Type-C Adapter
  - DRP Mode USB Type-C Specification, Rev 1.1 Compliant
  - UFP Mode USB Type-C Specification, Rev 1.1 Support
  - V_{CONN} and Super-Speed Multiplexer Logic Controls
  - Non-Standard DCP Detection
  - USB Battery Charging Specification, Rev 1.2 Compliant
- Automatic Input Current Limit (AICL) Power Management
- Support Weak/Dead Batteries Detection
  - Smart Power Selector
  - Thermistor Monitor
- Various Protection Features
  - 28V Integrated Overvoltage Protection
  - JEITA Charge Protection
  - ±15kV ESD Protection on USB Adapter Pins

19-100081; Rev 3; 4/18

maxim integrated™

Absolute Maximum Ratings

Voltages Referenced to GND
CHGIN .....-0.3V to +30V
BST .....-0.3V to +16V
SYS to BAT .....-0.3V to +12V
BAT, SYS .....-0.3V to +12V
BYP to CHGIN .....-30V to +0.3V
BYP, THM, $\overline{INT}$, SYSOK, $\overline{FLTIN}$, FSUS, LED, SDA, SCL .....-0.3V to 6V
COMP, SET ..... -0.3V to V_{CCINT} + 0.3V
CC1, CC2, TDN, TDP, CDN, CDP, V_{CONN} .....-0.3V to +6V
CC1, CC2, in fault mode through a 10k resistor ..-0.3V to +20V
CDIR .....-0.3V to +6V
VTPU (VTPU-TPU switch open) ..... -0.3V to V_{CCINT} + 0.3V
TPU (VTPU-TPU switch open) .....-0.3V to 6 or VTPU + 0.3V
VTPU, TPU Maximum Current (VTPU-TPU switch closed) .....-100mA to +100mA
BVCEN .....-0.3V to V_{CCINT} + 0.3V
SFOUT, V_{CCINT}, BREG .....-0.3V to min ((V_{CHGIN} + 0.3), 6)V
LX .....-0.3V to V_{SYS} + 0.3V
NVP .....-0.3V to +30V
AGND, DGND, PGND, GND .....-0.3V to +0.3V
Continuous Current into
CHGIN, SYS.....+6.4A
BAT.....+4.8A
Any Other Terminal.....+100mA
Continuous Power Dissipation (multilayer board at +70°C): 9 x 6 Array 54-Bump, 3.97mm x 2.77mm 0.4mm Pitch WLP (derate 24.46mW/°C) 1.957W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....40.88°C/W

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{BAT} = 8.3V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
BAT Supply Current	I_{BAT}	V_{CHGIN} = 0V or Floating, Type-C detection active		140		µA
		Low Power mode		25		µA
CHGIN Supply Current	I_{CHG}	V_{CHGIN} = +5V, T_A +25°C, ChgEn = 0		5.3		mA
		V_{CHGIN} = +5V, T_A +25°C, Suspend Mode (FSUS = High)		0.98		mA
CHGIN TO BYP PATH						
Allowed CHGIN Input Voltage Range	V_{CHGIN_RNG}		0		28	V
CHGIN Detect Threshold	V_{BDET}	Rising	3.8	3.9	4.0	V
	V_{BDET_F}	Falling	3.6	3.7	3.8	
CHGIN Overvoltage Threshold	V_{OVP}	Rising	5.59	5.66	5.72	V
	V_{OVP_F}	Falling	5.56			V
	V_{OVP_H}	Hysteresis		28		mV

Electrical Characteristics (continued)

(V_{BAT} = 8.3V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN-BYP Resistance	R_{CHGIN_BYP}	V_{CHGIN} = 5V		45		mΩ
CHGIN-BYP Soft-Start Timeout	t_{BYP_SFTTO}	If V_{BYP} has not reached within 50mV of V_{CHGIN} at timeout, a fault is flagged by SysFlt of register 0x02.		100		ms
CHGIN-BYP Soft-Start Current	I_{BYP_SFT}			60		mA
CHGIN-BYP Soft-Start End Comparator	V_{BYP_SFTEND}		15	50	80	mV
CHGIN-BYP Overload Comparator	V_{BYP_OVL}		290	360	420	mV
Input Current Limit	I_{LIM}	SpvChgILim[4:0] = 00100		0.4		A
		SpvChgILim[4:0] = 01110		1.5		
		SpvChgILim[4:0] = 11101		3		
Input Current Limit Programming Range	I_{LIM_RNG}		0.1		3	A
Input Current Limit Programming Step	I_{LIM_STEP}			100		mA
INTERNAL SUPPLIES						
Internal V_{CCINT} Regulator	V_{CCINT}	V_{CHGIN} = 5V, boost off	4.0	4.3	4.6	V
Boost Regulator BREG	V_{BREG}			4.3		V
V_{CCINT} UVLO Threshold	V_{UVLO}	V_{CCINT} rising	3.1	3.4	3.7	V
		V_{CCINT} falling	3.0	3.3	3.6	
V_{CCINT} UVLO Threshold Hysteresis	V_{UVLO_HYS}	Hysteresis		100		mV
SFOUT LDO Voltage	V_{SFOUT}	SfOutLvl = 1, V_{CHGIN} = 6V, I_{SFOUT} = 0	3.15	3.3	3.45	V
		SfOutLvl = 1, V_{CHGIN} = 6V, I_{SFOUT} = 15mA		2.95		
		SfOutLvl = 0, V_{CHGIN} = 6V, I_{SFOUT} = 0	5.0	5.25	5.5	
		SfOutLvl = 0, VCHGIN = 6V, I_{SFOUT} = 15mA		4.9		
SFOUT Maximum Current	I_{SFOUT_MAX}		15			mA

Electrical Characteristics (continued)

(V_{BAT} = 8.3V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Reduce Temperature	T_{CHG_LIM}			120		°C
Thermal Shutdown Temperature	$T_{SHUTDOWN}$			150		°C
Thermal Shutdown Hysteresis	$T_{SHUTDOWN\_H}$			20		°C
BYP UVLO Threshold	$V_{BYPUVLO}$	BYPUVLO[2:0] = 000, V_{BYP} falling		3.8		V
		BYPUVLO[2:0] = 001, V_{BYP} falling		3.9		
		BYPUVLO[2:0] = 010, V_{BYP} falling		4.0		
		BYPUVLO[2:0] = 011, V_{BYP} falling		4.1		
		BYPUVLO[2:0] = 100, V_{BYP} falling		4.2		
		BYPUVLO[2:0] = 101, V_{BYP} falling		4.3		
		BYPUVLO[2:0] = 110, V_{BYP} falling		4.4		
		BYPUVLO[2:0] = 111, V_{BYP} falling		4.5		
BYP UVLO Threshold Hysteresis	$V_{BYPUVLO\_H}$			25		mV
SYS UVLO (SYSOK) Threshold	$V_{SYSUVLO}$	VPChg[2:0] = 000, V_{SYS} rising		5.9		V
		VPChg[2:0] = 001, V_{SYS} rising		6.0		
		VPChg[2:0] = 010, V_{SYS} rising		6.1		
		VPChg[2:0] = 011, V_{SYS} rising		6.2		
		VPChg[2:0] = 100, V_{SYS} rising		6.3		
		VPChg[2:0] = 101, V_{SYS} rising		6.4		
		VPChg[2:0] = 110, V_{SYS} rising		6.5		
		VPChg[2:0] = 111, V_{SYS} rising		6.6		
SYS UVLO Threshold Hysteresis	$V_{SYSUVLO\_H}$			500		mV
BYP-SYS BOOST PATH						
Switching Frequency	f_{BST_SW}			0.8		MHz
Maximum Input Current	I_{BST_MAX}	L = 2.2µH	3			A
Input Peak Current Limit	$I_{BST\_LIM\_PK}$			4.5		A

Electrical Characteristics (continued)

(V_{BAT} = 8.3V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Forced Input Current Limit	IILIM_F	CurLim1Frc = 1 , CurLim1Set[4:0] =	00000		100		mA
			00001		200		
			00010		300		
			00011		400		
			00100	405	450	495	
			00101		600		
			00110		700		
			00111		800		
			01000		900		
			01001		1000		
			01010		1100		
			01011		1200		
			01100		1300		
			01101		1400		
			01110		1500		
			01111		1600		
			10000		1700		
			10001		1800		
			10010		1900		
			10011		2000		
			10100		2100		
			10101		2200		
			10110		2300		
			10111		2400		
			11000		2500		
			11001		2600		
			11010		2700		
			11011		2800		
			11100		2900		
			11101		3000		
			11110		3100		
			11111		3200		
Efficiency	EFF_{BST}	I_{SYS} = 1000mA, V_{BAT} = 7.4V, L1 = Bourns SRP4012TA-2R2M			91.6		%
SYS Regulation Voltage	V_{SYS_REG}	Charger disabled			V_{BAT} + 0.4		V
		Charger in precharge, V_{BAT} = 5V			V_{PCHG} + 0.4		V
SYS Regulation Voltage Limit	V_{SYS_LIM}	See Battery Charger State Diagram			V_{SYS_REG} - 0.2		V

Electrical Characteristics (continued)

(V_{BAT} = 8.3V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BYP-SYS BUCK PATH						
Switching Frequency	f_{BK_SW}			0.8		MHz
Maximum Output Current	I_{BK_MAX}	L = 2.2µH	500			mA
Short-Circuit Peak Current Limit	I_{BK_LIM}			1.3		A
Efficiency	EFF_{BK}	I_{CHGIN} = 500mA , V_{BAT} = 7.4V, L1 = Bourns SRP4012TA-2R2M		94		%
Output Voltage Range	$V_{BK\_OUT\_RNG}$		4		5.5	V
Output Accuracy	$V_{BK\_OUT\_ACC}$		-1.5		+1.5	%
SYS-BAT CHARGER/SWITCH CONTROLLER						
BAT-to-SYS Regulation Voltage	$V_{BAT-SYS\_ON}$			-20		mV
BAT-to-SYS Switch Fast Turn-On Threshold	$V_{BAT-SYS\_OFF}$	V_{SYS} falling		-100		mV
BAT-to-SYS Switch On-Resistance	R_{BAT_SYS}	I_{BAT} = 1A		13		mΩ
Charger Current Soft-Start Time	t_{CHG_SOFT}			1		ms
PRECHARGE						
Precharge Current	I_{PCHG}	IPChg[1:0] = 00		5		$\%I_{FCHG}$
		IPChg[1:0] = 01		10		
		IPChg[1:0] = 10		20		
		IPChg[1:0] = 11, R_{SET} = 20kΩ	27	30	33	
Prequalification Threshold	V_{PCHG}	VPChg[2:0] = 000		5.7		V
		VPChg[2:0] = 001		5.8		
		VPChg[2:0] = 010		5.9		
		VPChg[2:0] = 011		6.0		
		VPChg[2:0] = 100		6.1		
		VPChg[2:0] = 101		6.2		
		VPChg[2:0] = 110		6.3		
		VPChg[2:0] = 111		6.4		
Prequalification Threshold Hysteresis	V_{PCHG_H}			100		mV

Electrical Characteristics (continued)

(V_{BAT} = 8.3V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FAST CHARGE						
SET Current Gain Factor	K_{SET}			10000		A/A
SET Regulation Voltage	V_{SET}			1		V
Fast-Charge Current	I_{FCHG}	R_{SET} = 20kΩ	0.43	0.5	0.57	A
		R_{SET} = 20kΩ, T = 25°C	0.475	0.5	0.525	
		R_{SET} = 10kΩ		1		
		R_{SET} = 4kΩ		2.5		
Fast-Charge Current Scaling	I_{FCHG_T}	T_T_IFChg[2:0] = 000		20		$\%I_{FCHG}$
		T_T_IFChg[2:0] = 001		30		
		T_T_IFChg[2:0] = 002		40		
		T_T_IFChg[2:0] = 003		50		
		T_T_IFChg[2:0] = 004		60		
		T_T_IFChg[2:0] = 005		70		
		T_T_IFChg[2:0] = 006		80		
		T_T_IFChg[2:0] = 007		100		
1/2 Fast-Charge Current Comparator Threshold	I_{FC_HALF}			50		$\%I_{FCHG}$
1/5 Fast-Charge Current Comparator Threshold	I_{FC_FIFTH}			20		$\%I_{FCHG}$
MAINTAIN CHARGE						
Charge Done Qualification	I_{CHG_DONE}	ChgDone[1:0] = 00		5		$\%I_{FCHG}$
		ChgDone[1:0] = 01		10		
		ChgDone[1:0] = 10, R_{SET} = 20kΩ	18	20	22	
BAT Regulation Voltage	V_{BATREG}	BatReg[1:0] = 00, T_A = +25°C	8.258	8.3	8.342	V
		BatReg[1:0] = 00, T_A = -40°C to +85°C	8.217	8.3	8.383	
		BatReg[1:0] = 01		8.4		
		BatReg[1:0] = 10		8.5		
		BatReg[1:0] = 11		8.6		
BAT Recharge Threshold	$V_{BATRECHG}$	BatReChg[1:0] = 00		200		mV
		BatReChg[1:0] = 01		300		
		BatReChg[1:0] = 10		400		
		BatReChg[1:0] = 11		500		
CHARGE TIMER						
Maximum Prequalification Time	t_{PCHG}	PChgTmr[1:0] =00		30		min
		PChgTmr[1:0] = 01		60		
		PChgTmr[1:0] = 10		120		
		PChgTmr[1:0] = 11		240		

Electrical Characteristics (continued)

(V_{BAT} = 8.3V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Fast-Charge Time	t_{FCHG}	FChgTmr[1:0] = 00		75		Min
		FChgTmr[1:0] = 01		150		
		FChgTmr[1:0] = 10		300		
		FChgTmr[1:0] = 11		600		
Maintain Charge Time	t_{TOCHG}	MtChgTmr[1:0] = 00		0		Min
		MtChgTmr[1:0] = 01		15		
		MtChgTmr[1:0] = 10		30		
		MtChgTmr[1:0] = 11		60		
Timer Accuracy	t_{ACC}		-10		+10	%
Timer Extend Threshold	P_{TIMERX}	If charge current is reduced due to I_{LIM} or T_{DIE}, this is the percentage of charge current below which timer clock operates at half speed		50		%
Timer Suspend Threshold	$P_{TIMERSUS}$	If charge current is reduced due to I_{LIM} or T_{DIE}, this is the percentage of charge current below which timer clock pauses		20		%
THERMISTOR MONITOR AND NTC DETECTION						
THM Hot Threshold	T4	V_{THM} falling, WarmCoolSel = 0	21.3	23.3	25.3	$\%V_{TPU}$
		V_{THM} falling, WarmCoolSel = 1	30.9	32.9	34.9	
THM Warm Threshold	T3	V_{THM} falling, WarmCoolSel = 0	30.9	32.9	34.9	$\%V_{TPU}$
		V_{THM} falling, WarmCoolSel = 1	46.5	50	53.5	
THM Cool Threshold	T2	V_{THM} rising, WarmCoolSel = 0 or 1	62.5	64.5	66.5	$\%V_{TPU}$
THM Cold Threshold	T1	V_{THM} rising, WarmCoolSel = 0 or 1	71.9	73.9	75.9	$\%V_{TPU}$
THM Disable Threshold	V_{THM_DIS}	V_{THM} rising	91.0	93.0	95.0	$\%V_{TPU}$
THM Threshold Hysteresis	$V_{THM\_DIS\_H}$			60		mV
JEITA BAT Voltage Reduction	V_{BAT_JEITA}			300		mV
THM Input Leakage	I_{THM_LK}		-1		+1	µA
THM Detection Time	t_{THM_DET}			0.35		ms
DIGITAL I/O (SDA, SCL, $\overline{\text{FLTIN}}$, $\overline{\text{INT}}$, SYSOK, FSUS, LED, CDIR)						
Leakage Current	I_{IO_LK}		-1		+1	µA
Logic Input High-Voltage	V_{IO_IH}		1.4			V
Logic Input Low-Voltage	V_{IO_IL}				0.5	V
Logic Output Low-Voltage	V_{IO_OL}	I_{OL} = 4mA			0.4	V
FSUS Input Pulldown Resistance	R_{FSUS_PD}			470		kΩ
SDA, SCL Bus Low-Detection Current	I_{PD}	V_{SDA} = V_{SCL} = 0.4V		0.2	0.4	µA
SCL Clock Frequency	f_{SCL}	Note 3	0		400	kHz

Electrical Characteristics (continued)

(V_{BAT} = 8.3V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
START Condition (Repeated) Hold Time	t_{HD_SDA}	Note 3	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	t_{SU_STA}		0.6			µs
Data Hold Time	t_{HD_DAT}	Note 4	0		0.9	µs
Data Setup Time	t_{SU_DAT}	Note 4	100			ns
Setup Time for STOP Condition	t_{SU_STO}		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	Note 5		50		ns
BC1.2 DETECTION						
V_{DP_SRC} Voltage	V_{DP_SRC}/V_{SRC06}	I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
V_{DM_SRC} Voltage	V_{DM_SRC}/V_{SRC06}	I_{LOAD} = 0 to 200µA	0.5	0.6	0.7	V
V_{D33} Voltage	V_{SRC33}	I_{LOAD} = 0 to 365µA	2.6		3.4	V
V_{DAT_REF} Voltage	V_{DAT_REF}		0.25	0.32	0.4	V
V_{LGC} Voltage	V_{LGC}		1.5	1.7	1.9	V
I_{DM_SINK} Current	$I_{DM\_SINK}/I_{DATSINK}$	0.15V to 3.6V	55	80	105	µA
I_{DP_SRC} Current	I_{DP_SRC}/I_{DCD}	0V to 2.5V	7	10	13	µA
R_{DM_DWN} Resistor	R_{DM_DWN}/R_{DWN15}		12	20	24	kΩ
I_{WEAK} Current	I_{WEAK}		0.01	0.1	0.5	µA
V_{BUS31} Threshold	V_{BUS31}	DP and DN pins. Threshold in percent of V_{BUS} voltage 4V < V_{BUS} < 5.5V	26	31	36	%
V_{BUS47} Threshold	V_{BUS47}	DP and DN pins. Threshold in percent of V_{BUS} voltage 4V < V_{BUS} < 5.5V	43.3	47	51.7	%
V_{BUS64} Threshold	V_{BUS64}	DP and DN pins. Threshold in percent of V_{BUS} voltage 4V < V_{BUS} < 5.5V	57	64	71	%

Electrical Characteristics (continued)

(V_{BAT} = 8.3V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charger Detection Debounce	t_{CDDEB}		45	50	55	ms
Primary-to-Secondary Timer	$t_{PDSDWAIT}$		27	35	39	ms
Proprietary Charger Debounce	t_{PRDEB}		5	7.5	10	ms
Data Contact Detect Timeout	t_{DCDTMO}	DCD2s = 0	700	800	900	ms
		DCD2s = 1	1.8	2.0	2.2	
DP/DN Overvoltage Debounce	$t_{OVDXDEB}$		90	100	110	µs
OVDX Comparator	$OVDX_{THRESHOLD}$	Rising	0		0.15	V
		Falling	-0.04		+0.08	
CDP/CDN Pulldown Resistor	R_{CDP/CDN_PD}		3	6	12	mΩ
TYPE-C DETECTION						
V_{CONN} Switch Voltage Drop	V_{CONN_REQ}	V_{CONN} = 5.5V, I_{CC_LOAD} = 20mA	5.5		5.6	V
V_{CONN} Bulk Capacitance	C_{VCONN}		10		220	µF
CC Pin Operational Voltage Range	V_{CONN_RNG}				5.5	V
CC Pin Voltage in DFP 3.0A Mode	V_{CC_PIN30}		3.1			V
CC Pin Voltage in DFP 1.5A Mode	V_{CC_PIN15}		1.85			V
CC Pin Low-Power Mode Pulldown Resistance	$R_{LPPD\_CC\_}$			170		kΩ
CC Pin Low-Power Mode Voltage Threshold	$V_{LP\_CC\_}$	Rising		0.7		V
CC Pin Clamp Requirements	$V_{CC\_PIN\_CLAMP}$	60µA ≤ $I_{CC\_}$ ≤ 600µA		1.1	1.32	V
CC UFP Pulldown Resistance	$R_{DUFP\_CC\_}$		4.59	5.1	5.61	kΩ
CC DFP 0.5A Current Source	$I_{DFP0.5\_CC\_}$		72	80	88	µA
CC DFP 1.5A Current Source	$I_{DFP1.5\_CC\_}$		165.6	180	194.4	µA
CC DFP 3.0A Current Source	$I_{DFP3.0\_CC\_}$		303.6	330	356.4	µA
CC R_A and R_D Threshold	$V_{RA\_RD0.5}$	Rising	0.16	0.2	0.25	V
		Falling	0.15			
CC UFP 0.5A R_D Threshold	$V_{UFP\_RD0.5}$	Rising	0.62	0.66	0.7	V
		Falling	0.61			
CC UFP 1.5A R_D Threshold	$V_{UFP\_RD1.5}$	Rising	1.17	1.23	1.31	V
		Falling	1.16			
CC V_{CONN} Detect Threshold	V_{VCONN_DET}	Rising	2.11	2.25	2.4	V
		Falling	2.1			

Electrical Characteristics (continued)

(V_{BAT} = 8.3V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CC DFP V_{OPEN} Detect Threshold	V_{DFP_VOPEN}	Rising	1.51	1.575	1.65	V
		Falling	1.5			
CC DFP V_{OPEN} with 3.0A Detect Threshold	$V_{DFP\_VOPEN3A}$	Rising	2.46	2.6	2.75	V
		Falling	2.45			V
V_{BUS} Valid	V_{BDET}	Rising	3.8	4.12	4.4	V
V_{BUS} Valid Hysteresis	V_{BDET_H}	Falling hysteresis		0.7		V
V_{BUS} Discharge Value	V_{SAFE0V}	Falling. Voltage level where a connected UFP will find V_{BUS} removed.	0.6	0.7	0.84	V
		Rising hysteresis		100		mV
CC Pin Power-Up Time	$t_{CLAMPSWAP}$	The maximum time allowed from removal of voltage clamp to attachment of the 5.1k resistor			15	ms
Type-C CC Pin Detection Debounce	t_{CCDEB}		100		200	ms
Type-C Debounce	t_{PDDEB}		10		20	ms
Type-C Quick Debounce	t_{QDEB}		0.9	1	1.9	ms
V_{BUS} Debounce	t_{VBDEB}		9	10	11	ms
V_{SAFE0V} Debounce	$t_{VSAFE0VDEB}$		9	10	11	ms
Type-C Error Recovery Delay	$t_{ERRORRECOVERY}$		25			ms
Type-C DRP Toggle Time	t_{DRP}		50		100	ms
Duty Cycle of DRP Swap	D_{DRP}	Duty cycle of UFP to DFP role swap	30		70	%
DRP Transition Time	$t_{DRPTRAN}$	Time a role swap from DFP to UFP or reverse is completed			1	ms
DRP Lock Time	$t_{DRPLOCK}$	DRP Lock wait time before transition to unattached state	100		150	ms
V_{CONN} Enable Time	$t_{VCONNON}$	Time from when V_{BUS} is supplied in DFP mode in state Attach.DFP. DRPWait			10	ms
V_{CONN} Disable Time	$t_{VCONNOFF}$	Time from UFP detached or as directed by I^2C command until V_{CONN} is removed			35	ms

Electrical Characteristics (continued)

(V_{BAT} = 8.3V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

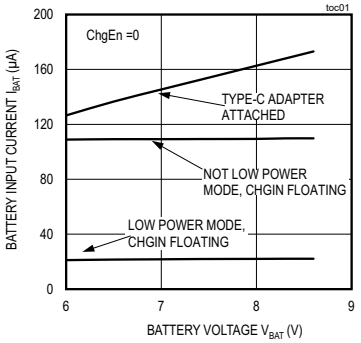
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CC Pin Current Change Time	$t_{SINKADJ}$	Time from CC pin changes state in UFP mode until current drawn from DFP reaches new value			60	ms
V_{BUS} On-Time	t_{VBUSON}	Time from UFP is attached until V_{BUS} On			275	ms
V_{BUS} Off-Time	$t_{VBUSOFF}$	Time from UFP is detached until V_{BUS} reaches V_{SAFE0V}			650	ms
BVCEN Output Low-Voltage	V_{BVCEN_OL}	I_{SINK} = 1mA			0.4	V
BVCEN Output High-Voltage	V_{BVCEN_OH}	I_{SOURCE} = 1mA	V_{CCINT} - 0.4			V

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design and characterization.
Note 3: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 4: The maximum $t_{HD:DAT}$ has to be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 5: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

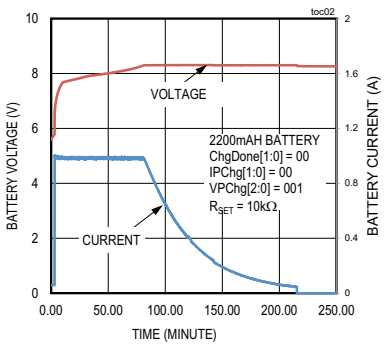
Typical Operating Characteristics

(V_{BAT} = 8.5V, T_A = -20°C to +70°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

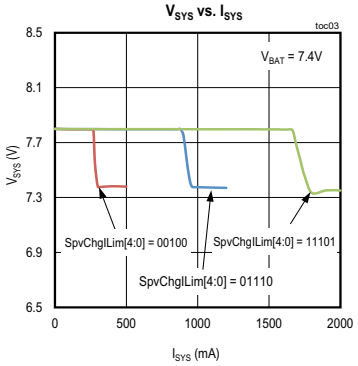
I_{BAT} vs. V_{BAT}



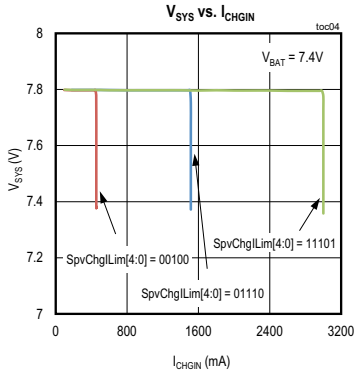
I_{BAT} and V_{BAT} vs. TIME



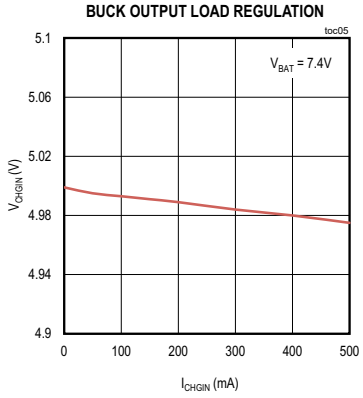
V_{SYS} vs. I_{SYS}



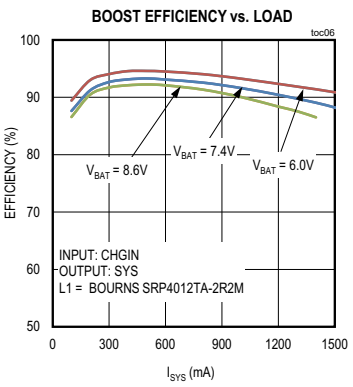
V_{SYS} vs. I_{CHGIN}



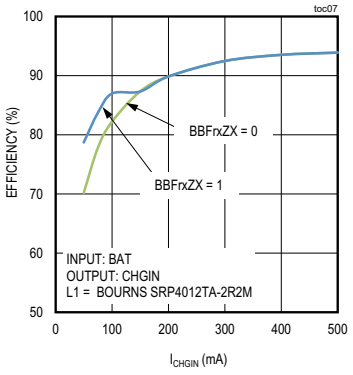
BUCK OUTPUT LOAD REGULATION



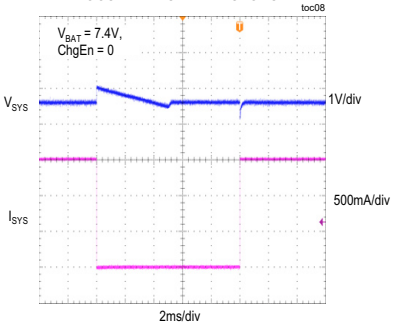
BOOST EFFICIENCY vs. LOAD



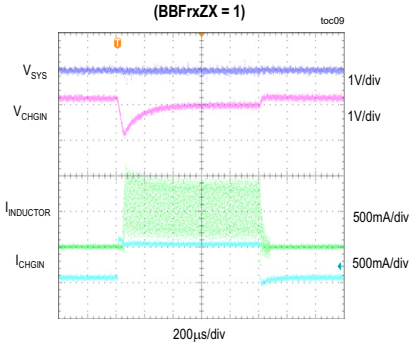
REVERSE BUCK EFFICIENCY vs. LOAD



BOOST TRANSIENT RESPONSE



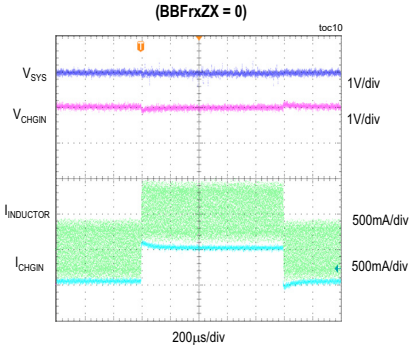
BUCK TRANSIENT RESPONSE (BBFrxZX = 1)



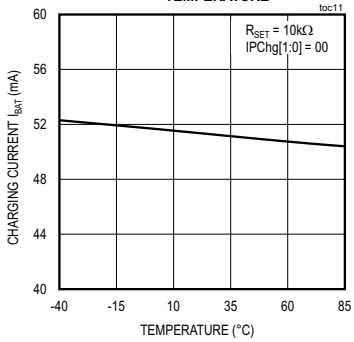
Typical Operating Characteristics (continued)

(V_{BAT} = 8.5V, T_A = -20°C to +70°C, all registers in their default state, unless otherwise noted. Typical values are at V_{CHGIN} = 5.0V, V_{BAT} =7.4V, V_{SYS} = V_{BATREG}, T_A = +25°C.)

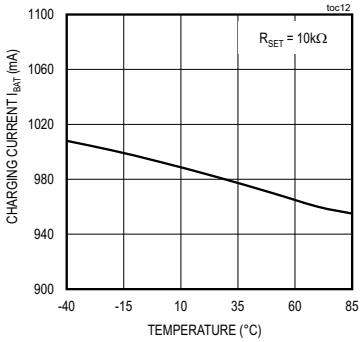
BUCK TRANSIENT RESPONSE
(BBFrxZX = 0)



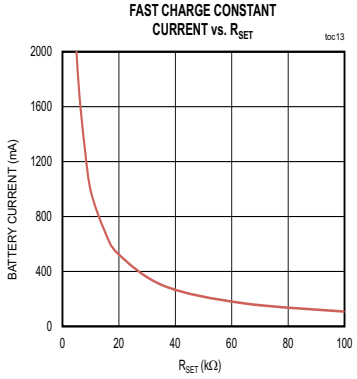
PRECHARGE CURRENT vs. TEMPERATURE



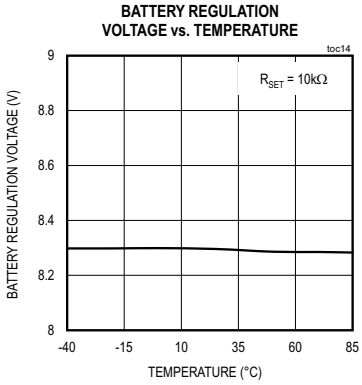
FAST CHARGE CONSTANT CURRENT vs. TEMPERATURE



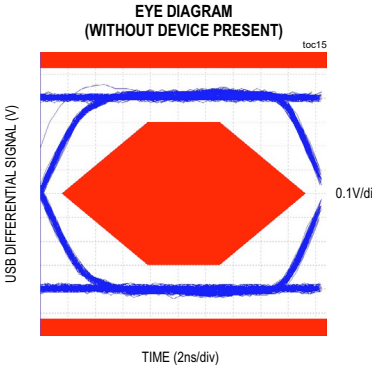
FAST CHARGE CONSTANT CURRENT vs. R_{SET}



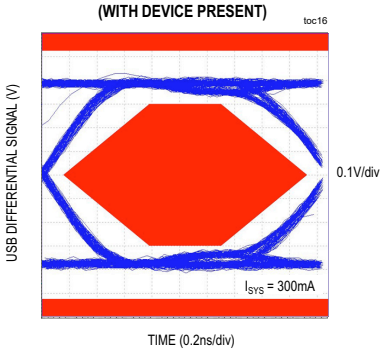
BATTERY REGULATION VOLTAGE vs. TEMPERATURE



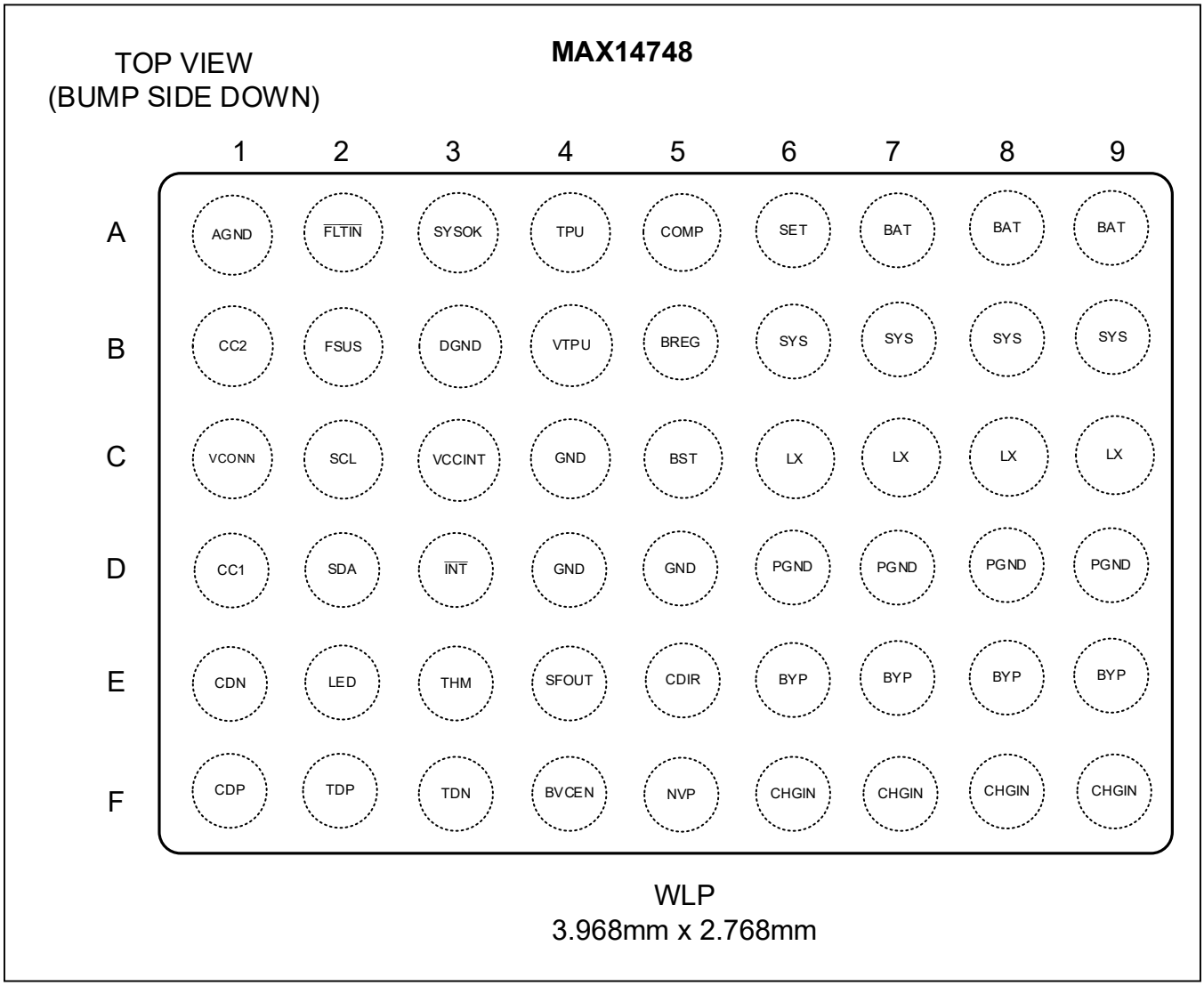
EYE DIAGRAM
(WITHOUT DEVICE PRESENT)



EYE DIAGRAM
(WITH DEVICE PRESENT)



Bump Configuration



Bump Descriptions

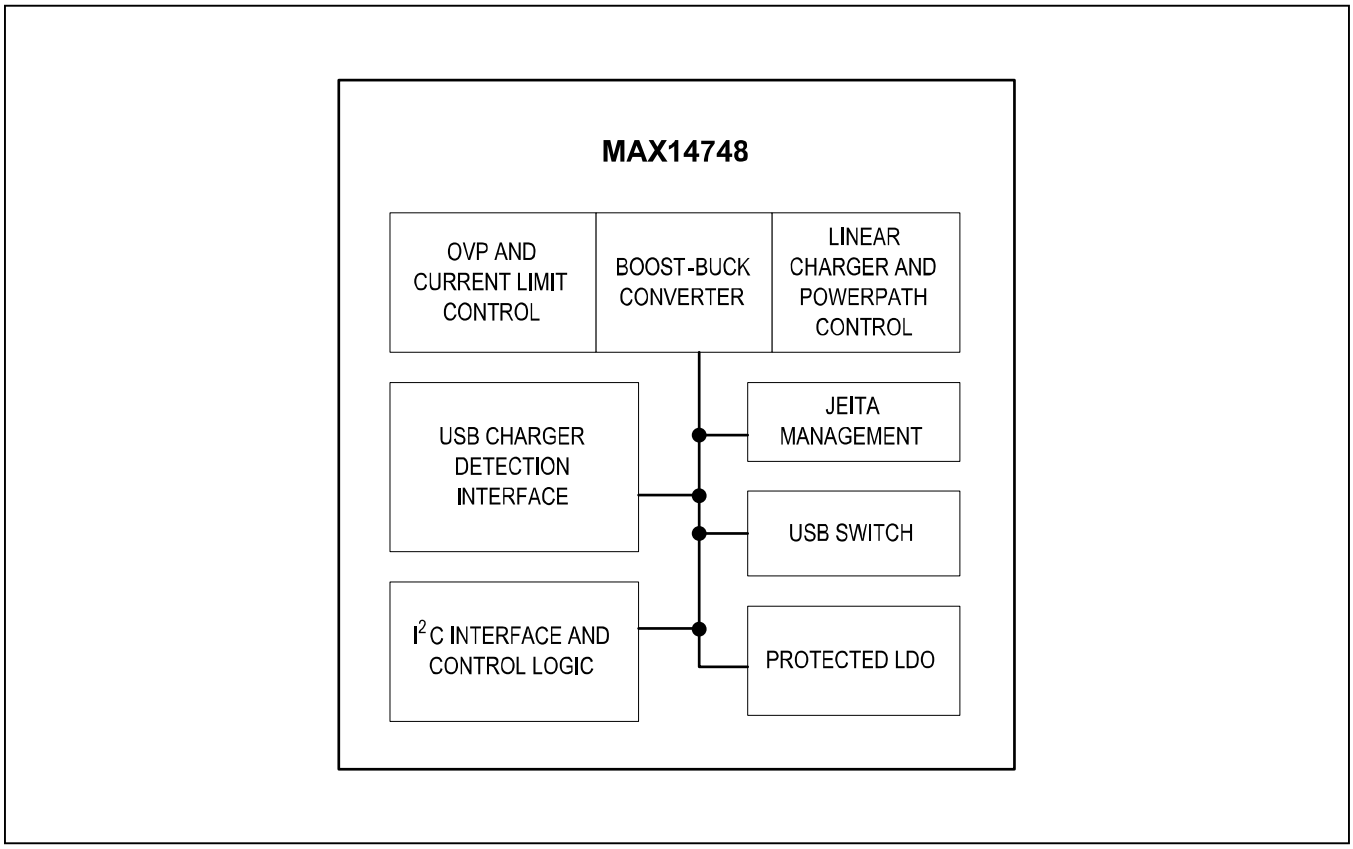
BUMP	NAME	FUNCTION
A1	AGND	Analog Ground.
A2	$\overline{\text{FLTIN}}$	Charger Fault Input. Logic-low on this pin forces the charger into a fault state and generates an interrupt. See Register 0x35 description for more information. Connect to digital I/O supply if not used.
A3	SYSOK	Open-Drain Status Output of SYS Regulation. When V_{SYS} is above the SYS UVLO threshold and Boost is active, this output is high-impedance. When V_{SYS} is below the SYS UVLO threshold, this output is low. Leave unconnected if not used.
A4	TPU	High-Side of Internal Resistor for THM Detection. Connect a 10k resistor between this pin and THM.
A5	COMP	Buck/Boost Converter Compensation Connection. Connect a 3.9nF capacitor for internal Buck/Boost compensation
A6	SET	External Resistor Connection for Fast Charge Current Setting. Connect a resistor to this pin to set the fast charge current. Other charge currents are set as a proportion of fast charge current based on I^2C register settings.
A7–A9	BAT	Battery Connection. Connect a 2s Li-ion+ battery from BAT to GND. Bypass to PGND with a parallel combination of a 0.1µF capacitor and an effective 10µF - 30µF capacitor. Keep the capacitors as close to BAT as possible and keep the stray inductance and resistance of the trace from BAT to the battery terminal as low as possible.
B1	CC2	USB Type-C CC2. Connect to CC2 on USB Type-C connector.
B2	FSUS	Force Suspend Input. Logic-high on this pin causes the input limiter to open and input current from CHGIN is reduced to zero. This pin is internally pulled to GND through a 470kΩ (typ) resistor and has no effect if FSUSMsk = 1.
B3	DGND	Digital Ground.
B4	V_{TPU}	External Voltage Input for TPU connection. Connect to external supply or V_{CCINT}.
B5	BREG	Bypass for Internal Switching Converter Supply. Bypass with 1µF capacitor to AGND.
B6–B9	SYS	System Load Connection. Connect SYS to the system load. Bypass to PGND with a parallel combination of a 0.1µF capacitor and an effective 22µF capacitor. (Note: there is a diode between SYS and BAT)
C1	V_{CONN}	External V_{CONN} Supply Input. Leave unconnected if not used.
C2	SCL	I^2C Serial Clock Input. Connect an external pull-up resistor.
C3	V_{CCINT}	Bypass For Internal Analog Supply. Bypass with 1µF capacitor to GND.
C4, D4, D5	GND	Ground.
C5	BST	Charge Pump Connection. Connect a 0.1µF capacitor between BST and LX.
C6, C7, C8, C9	LX	Switching Node of Boost Converter. Connect a 1.5µH or 2.2µH inductor between LX and BYP. See *Applications Information* section for more details.
D1	CC1	USB Type-C CC1. Connect to CC1 on USB Type-C connector.
D2	SDA	I^2C Serial Data Input/Output. Connect an external pullup resistor.
D3	$\overline{\text{INT}}$	Active-Low, Open-Drain Interrupt Output. Connect an external pullup resistor.
D6, D7, D8, D9	PGND	Power Ground.

Bump Descriptions (continued)

BUMP	NAME	FUNCTION
E1	CDN	USB Connector D-Input. Leave unconnected if not used.
E2	LED	LED Charging Status Indicator. Open-drain output indicating battery charging status. When LEDAuto = 1 and a temperature fault is detected, the output is pulsed at 50% duty cycle for a period of 1.5s. When a charge timer expires or SysFlt fault occurs, LED is pulsed at 50% for a period of 0.15s. When LEDAuto = 0, the open-drain output is controlled by the LEDCtrl bit. Connect this pin to GND if unused.
E3	THM	Battery Temperature Thermistor Measurement Connection. This pin is used for NTC thermistor presence detection and JEITA compliant temperature control.
E4	SFOUT	Output of overvoltage protected LDO powered from CHGIN. Bypass SFOUT with a 1µF ceramic capacitor to GND.
E5	CDIR	USB Cable Orientation Open-drain Output. When CC1 is active, this output is pulled low. Otherwise, this output is high-impedance. Leave unconnected if not used.
E6–E9	BYP	Bypass Connection. Bypass to PGND with a parallel combination of a 0.1µF capacitor and an effective 10µF capacitor.
F1	CDP	USB Connector D+ Input. Leave unconnected if not used.
F2	TDP	USB Transceiver D+ Connection. Connect TDP to device microprocessor USB transceiver D+ line. Leave unconnected if not used.
F3	TDN	USB Transceiver D- Connection. Connect TDN to device microprocessor USB transceiver D- line. Leave unconnected if not used.
F4	BVCEN	External V_{CONN} Supply Enable Output. Push-pull output between V_{CCINT} and GND. Leave unconnected if not used.
F5	NVP	Negative Voltage PFET Gate Control. Leave unconnected if not used.
F6–F9	CHGIN	USB Charger Input. Bypass this pin with a 1µF capacitor to PGND.

Note: *All capacitance values listed in this document refer to effective capacitance. Be sure to specify capacitors that will meet these requirements under typical system operating conditions taking into consideration the effects of voltage and temperature.*

Block Diagram



Detailed Description

The MAX14748 is a battery charger with a Smart Power Selector that safely charges two Li+ cell in accordance with JEITA specifications*.

Input OVP

The MAX14748 CHGIN input is protected by an internal N-channel FET. The device monitors the voltage at CHGIN and, if CHGIN is greater than V_{OVP}, switches off the internal FET to prevent damage to the device. If V_{CHGIN} is above the overvoltage threshold or below the USB valid voltage threshold, the MAX14748 enters overvoltage lockout (OVLO). During OVLO, the internal circuits remain powered, the SYSOK pin is high-impedance, and an interrupt is asserted. During OVLO, the charger turns off and the system load switch closes, allowing the battery to power SYS.

Negative Voltage Protection (NVP)

The MAX14748 provides a gate protection circuit for an external PFET that protects against negative voltages on V_{BUS}. NVP pin drives the gate of the external PFET. If a negative voltage is present on V_{BUS}, e.g., by a backwards connector, the NVP turns off the external PFET, therefore providing negative voltage protection.

Low Power Mode

The MAX14748 features a Low Power mode, which reduces the battery current consumption from 25µA to 140µA. To enter Low Power mode, write 1 to LowPowEn (Register 0x33[7]). To manually exit Low Power mode, set LowPowAbort (Register 0x33[1]) to 1. If a DFP pullup connect to CC1/CC2 is detected, the device automatically exits Low Power mode and resumes normal operations.

Input Current Limiter

The primary function of the input limiter is supplying power from the external adapter at CHGIN to the system load and battery charger. In addition, it performs several other functions to optimize use of the available power efficiently and safely, including:

1) CHGIN Input Current Limiting: The CHGIN input current is limited to prevent input overload. The current limit can be automatically selected through charger detection to match the capabilities of the source. The result is indicated by SpvChgIlim[4:0] in register 0x22. See **Table 1a** for more details. It can also be manually set through CurLim1Frc and CurLim1Set[4:0] in register 0x21. Figure 1 illustrates how the current limit setting is selected.
2) Thermal Limiting: In case the die temperature exceeds the normal limit (T_{CHG_LIM}), the MAX14748 will attempt to limit temperature increase by reducing the input current at CHGIN. In this condition, the system load has priority over charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit (T_{BUS_LIM}), no input current is drawn from CHGIN and the battery powers the entire system load.
3) Adaptive Battery Charging: While the system is powered from CHGIN, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, the battery supplies supplmental current to the load.
4) Adaptive Input Current Limiting: If the MAX14748 input current limit is programmed in such a way that the adapter voltage collapses due to resistive drop, current limiting, or poor load transient response, the AICL loop allows the MAX14748 to regulate the input voltage above a value needed to ensure proper operation. Figure 2 illustrates high-level operation of the AICL block and associated parameters are found in the registers 0x2C to 0x2E.

**JEITA (Japan Electronics and Information Technology Industries Association) Standard, A Guide to the Safe Use of Secondary Lithium Ion Batteries on Notebook–Type Personal Computers, April 20, 2007.*

Table 1a. Automatic Input Current Limit Control

ChgTyp[1:0]	PrChgTyp[2:0]	CCIStat[1:0]	SDPMaxCur[1:0]	CDPMaxCur[1:0]	I_{LIM}	SpvChgIlim[4:0]
“xx”	“xxx”	“11 = 3A”	“00”	“0”	3A	0x1D
“11 = 1.5A”	“xxx”	“11 = 3A”	“xx”	“x”	3A	0x1D
“xx”	“110 = 3A”	“xx”	“xx”	“x”	3A	0x1D
“xx”	“101 = 2.4A”	“00” or “01 = 500mA” or “10 = 1.5A”	“xx”	“x”	2.4A	0x17
“xx”	“100 = 2A” or “001 = 2A”	“00” or “01 = 500mA” or “10 = 1.5A”	“xx”	“x”	2A	0x13
“1x = 1.5A”	“000” or “010 = 500mA”	“00” or “01 = 500mA” or “10 = 1.5A”	“xx”	“x”	1.5A	0x0E
“1x = 1.5A”	“000” or “010 = 500mA” or “011 = 1A”	“10 = 1.5A”	“xx”	“x”	1.5A	0x0E
“xx”	“011 = 1A”	“00” or “01 = 500mA”	“xx”	“x”	1A	0x09
“01 = 500mA”	“000” or “010 = 500mA”	“00” or “01 = 500mA”	“xx”	“x”	0.5A	0x04
“01 = 500mA”	“000”	“10 = 1.5A” or “11 = 3A”	01	“x”	0.5A	0x04
“01 = 500mA”	“000”	“10 = 1.5A” or “11 = 3A”	10	“X”	1.0A	0x09
“01 = 500mA”	“000”	“10 = 1.5A” or “11 = 3A”	11	“x”	1.5A	0x0E
“10 = 1.5A”	“000”	“11 = 3A”	xx	“1”	1.5A	0x0E
“00”	“xxx”	“xx”	“xx”	“x”	NA	NA

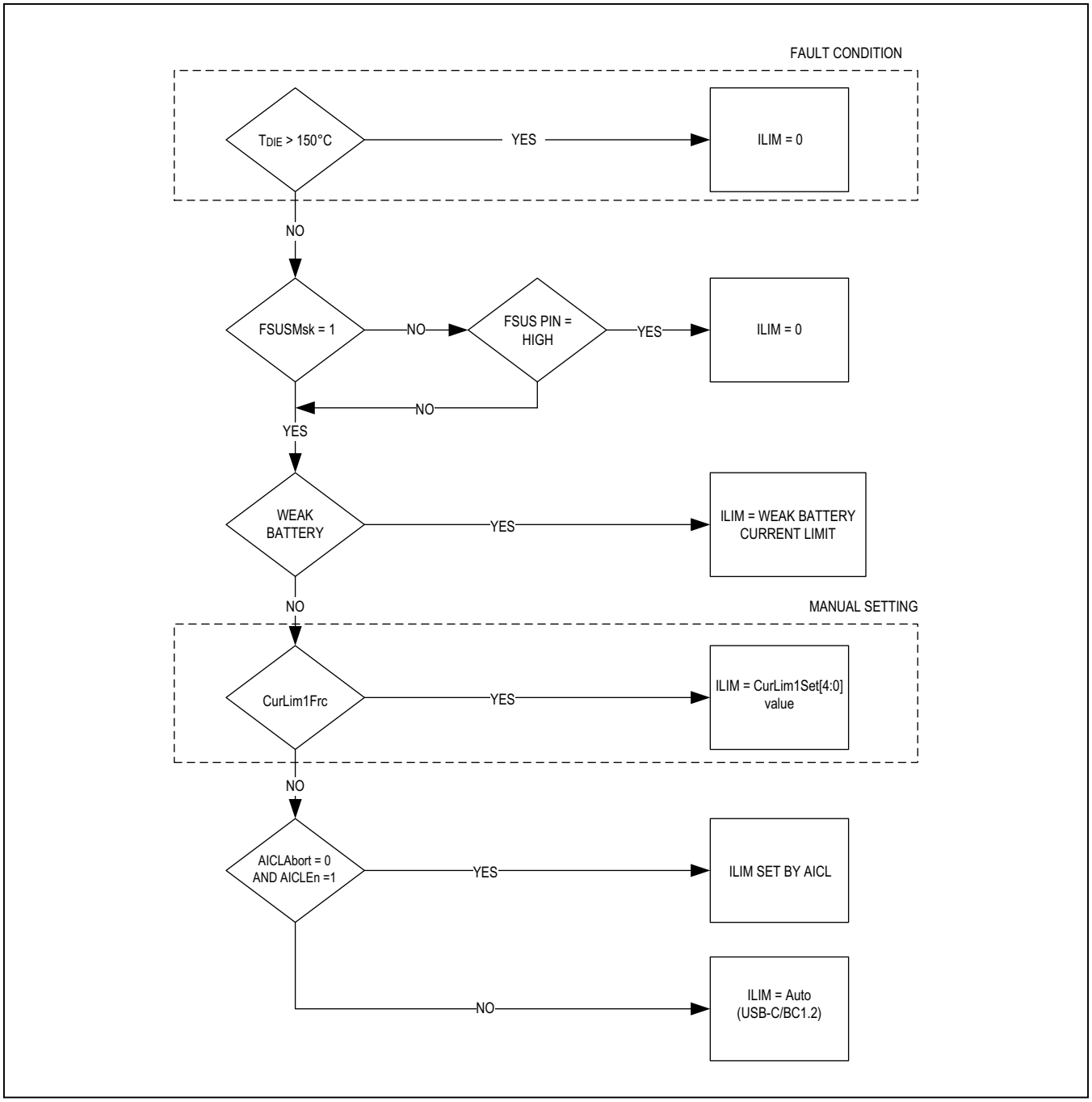


Figure 1. Input Current Limit Settings Flow Diagram

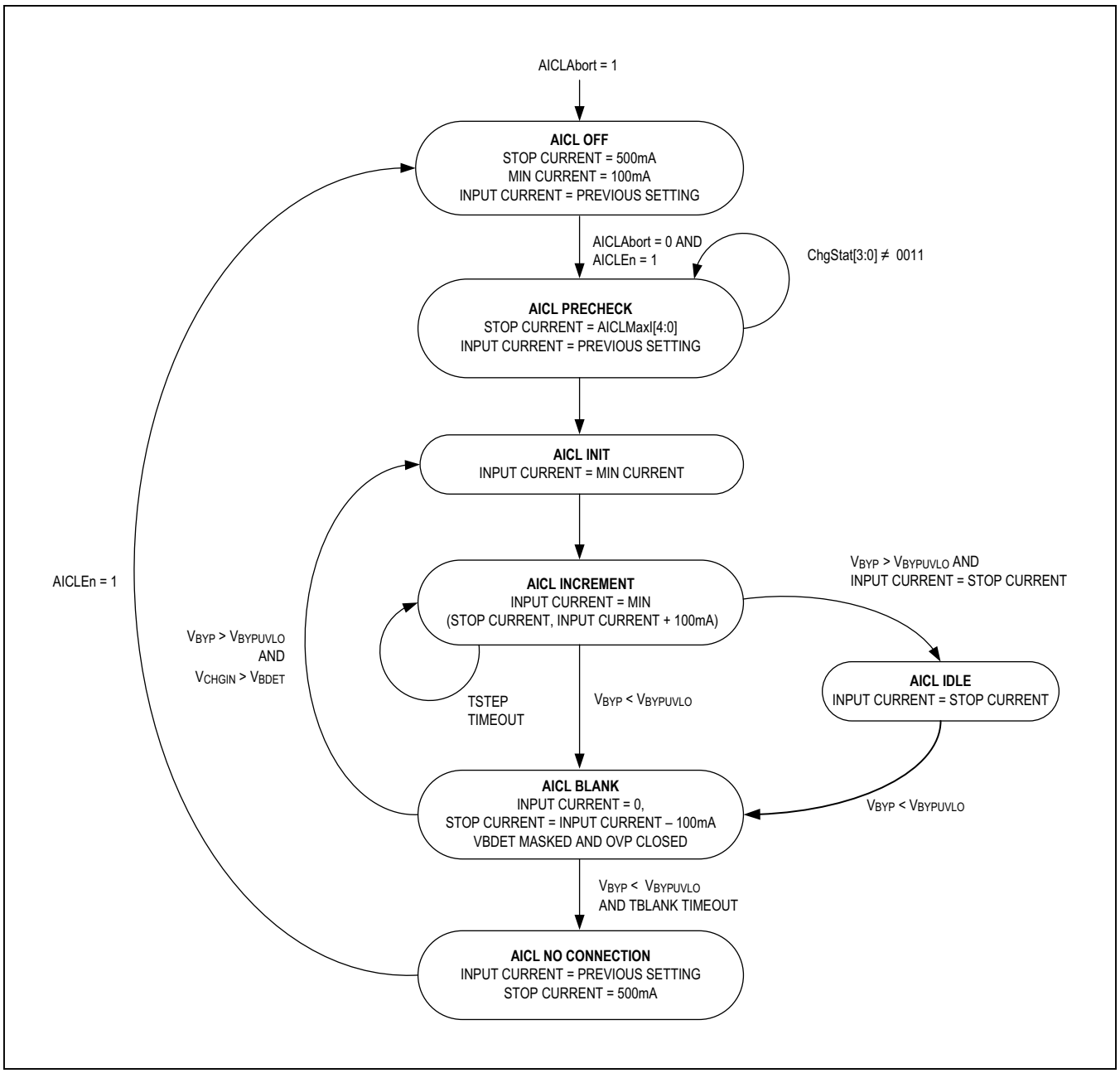


Figure 2. AICL Operation Flow Diagram

Boost Converter with Reverse Buck

Boost Mode

The MAX14748 boost converter operates as either a current-limited voltage source, or current source, depending on the charger operational state. When a valid USB voltage is present at CHGIN, and the charger is disabled, V_{SYS} is regulated to V_{BAT} + 400mV. If the charger is in precharge mode, V_{SYS} is regulated to V_{PCHG} + 400mV. When the system is in fast-charge mode, the boost converter operates as a current source, delivering current into the SYS node that is shared by the battery and system loads.

The boost converter current limit may be acted upon by multiple system blocks, including the programmed input current limit, thermal status, charging current, SYS regulation voltage block, and battery termination voltage block. The minimum requested current from these blocks at any given time determines the active current limit in the boost.

Reverse Buck Mode

The CHGIN-SYS switching converter may operate as a buck converter when needed to supply a load attached to CHGIN. The load may be a Type-C sink or some other proprietary device.

If Type-C DRP operation is enabled, the buck converter can be enabled by the Type-C state machine. The output voltage of the buck can be programmed from 4V to 5.5V in 0.1V steps by writing to BuckVSet[3:0], however, it is not recommended to change the output voltage when the buck is active.

The output of the buck converter turns off when a fault occurs. The specific fault occurred is indicated by DCDCILim, DCDCRunAway, DCDCPGood status bits (register 0x04). See Register Descriptions for more details. When the buck is disabled due to a fault, both VBUSDet (register 0x07) and VSAFE0V (register 0x0A) change to 0. After the fault condition is removed, the buck converter can be restarted by writing 1 to CCSnkRst, CCSrcRst, CCForceError, or USBCRset auto-reset bits.

Smart Power Selector

The Smart Power Selector seamlessly distributes power between CHGIN, battery (BAT) and the system (SYS). The basic modes of operation of the smart power selector are:

1. With a valid external power source:
   a. The external power source at CHGIN is the primary source of energy.
   b. The battery is the secondary source of energy.
   c. Energy delivery to SYS is the highest priority.
   d. Any energy that is not required by SYS is available to the battery.
2. With no power source available at CHGIN:
   a. The battery is the primary source of energy.
   b. Energy delivery to SYS has the highest priority.
3. With a Type-C Sink or other load present at CHGIN:
   a. The battery is the primary source of energy.
   b. Energy delivery to SYS is the highest priority.
   c. Energy delivery to BYP is the second highest priority.

4. SYS Regulation Voltage:
   a. When the charger path is enabled and the charger is disabled, V_{SYS} is regulated to V_{BAT} + 400mV and BAT switch is off.
   b. When the charger is enabled but in a non-charging state such as maitain charge done, thermistor suspend, or timer fault, V_{SYS} is regulated to V_{BAT} + 400mV and BAT switch is off.
   c. When the input charger path is enabled and the battery is charging in prequalification, V_{SYS} is regulated to V_{PCHG} + 400mV. Charge current is reduced when V_{SYS} approaches V_{PCHG} + 200mV.
   d. When the input charger path is enabled and the battery is charging in fast-charge or maintain charge done, the BAT switch is closed and $V_{SYS} = V_{BAT}$. In maintain charge done state, the connection between SYS and BAT acts as an ideal diode. Therefore, when V_{SYS} drops below V_{BAT}, the BAT switch is turned fully on and the battery supplements the SYS load along with the current from CHGIN.
   e. When the switching converter is enabled as a reverse buck, the BAT switch is closed and $V_{SYS} = V_{BAT}$.

Short-Circuit Protection

The MAX14748 provides short-circuit protection to the power nodes. When SYS is shorted to ground, input current from CHGIN is limited by boost converter current limit. Note in this case, FET diode from BAT-SYS prevents control of FET BAT-SYS current. Battery current is not limited by the MAX14748 and a pack protector is needed to limit the battery current.

When either BYP or CHGIN is shorted to ground, the current from BAT is limited by the reverse buck converter.

USB Type-C 1.1

USB Type-C 1.1 UFP and DRP Support

The MAX14748 provides support for devices functioning as a Upstream Facing Port (UFP) or Dual Role Port (DRP) per the current USB Type-C 1.1 specification. When acting as a power source in DRP mode, the MAX14748 can provide a 5V V_{BUS} on the CHGIN pin through operation of the reverse buck converter. The USB Type-C V_{CONN} supply is provided externally via the V_{CONN} pin, and switched internally onto one of the CC pins. An open-drain output pin, BVCEN, is provided to enable the external V_{CONN} supply based on the Type-C state machine output. BVCEN is a push-pull output between GND and V_{CCINT}.

USB BC1.2 Compliant and Nonstandard Charger Support

The BC1.2 charger detection and special charger detection routine is embedded within the Type-C state machine. The BC1.2 and Special Charger detection routine runs always when the state machine enters the ‘AttachWait. SNK’ state of the USB Type-C 1.1 state-machine.

USB Type-C Adapter Insertion

Figure 3a and Figure 3b depict the general timings when a USB Type-C adapter is attached. For more information on the behavior and timings of the USB Type-C 1.1 state-machine, please refer to the USB Type-C specification.

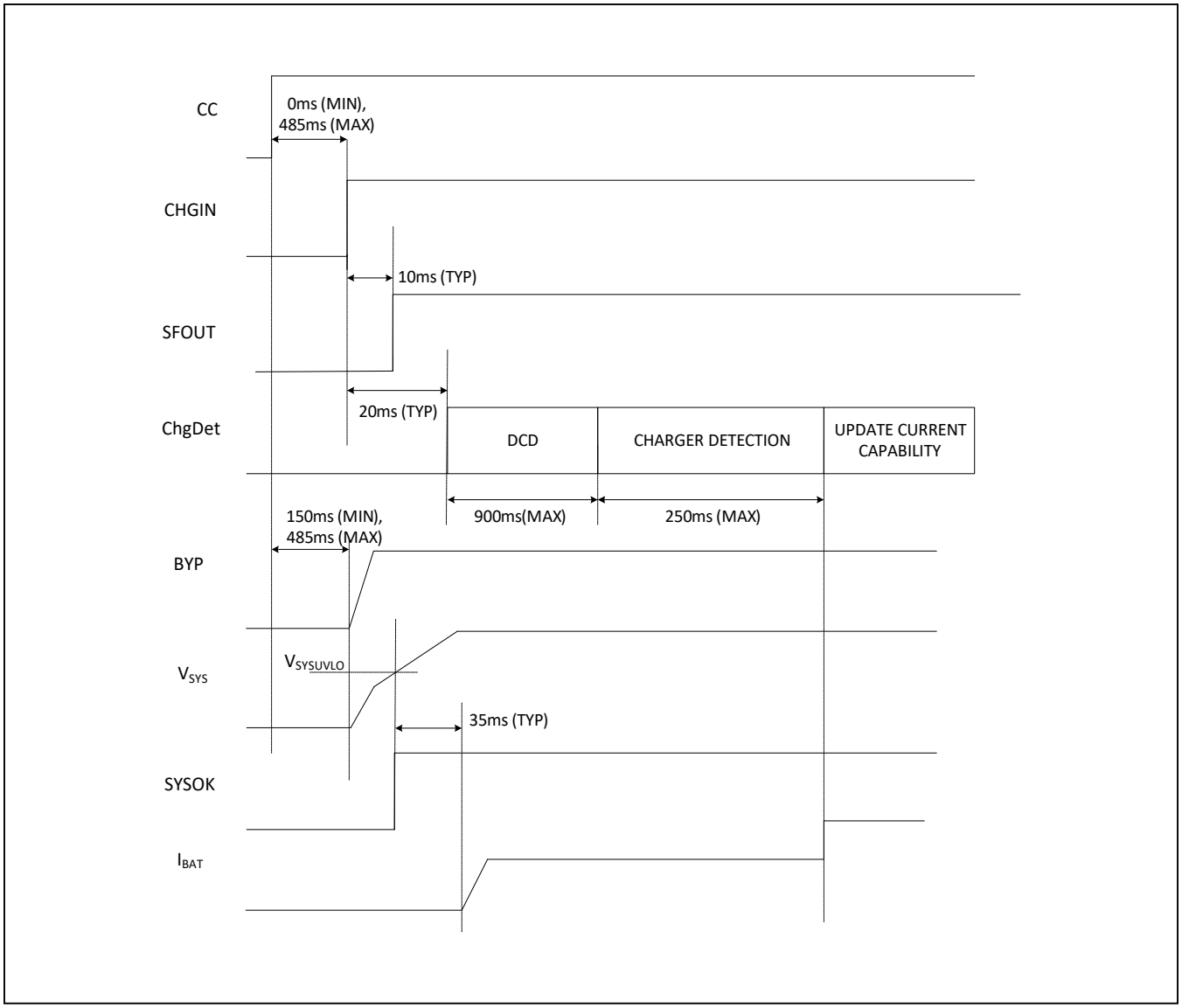


Figure 3a. Type-C Adapter Insertion (CHGINILimGate = 0)