Chipsmall

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MAXIM

Quad SPST +70V Analog Switches

General Description

The MAX14756/MAX14757/MAX14758 are analog switches with a low on-resistance of 10Ω (max) that conduct equally well in both directions. All devices have a rail-to-rail analog-signal range. They operate with a single +10V to +70V supply in unipolar applications or ±35V dual supplies in bipolar applications. The bipolar supplies can be offset and do not have to be symmetrical.

The MAX14756 is a quad normally closed (NC) single-pole/single-throw (SPST) switch, the MAX14757 is a quad normally open (NO) SPST switch, and the MAX14758 has two NO and two NC SPST switches. These switches have 5Ω (typ) on-resistances and low on-leakage currents of 0.01nA (typ). The on-resistance flatness is 0.004Ω (typ).

The devices are suitable for a multitude of analog signal routing and switching applications. They are specified over an extended temperature range of -40°C to +85°C, but can be operated up to +125°C with elevated leakage currents.

Applications

Industrial Control Systems

Instrumentation

Battery Management

Environmental Control Systems

Medical Systems

ATE System

Audio Signal Routing/Switching

Automotive

Features

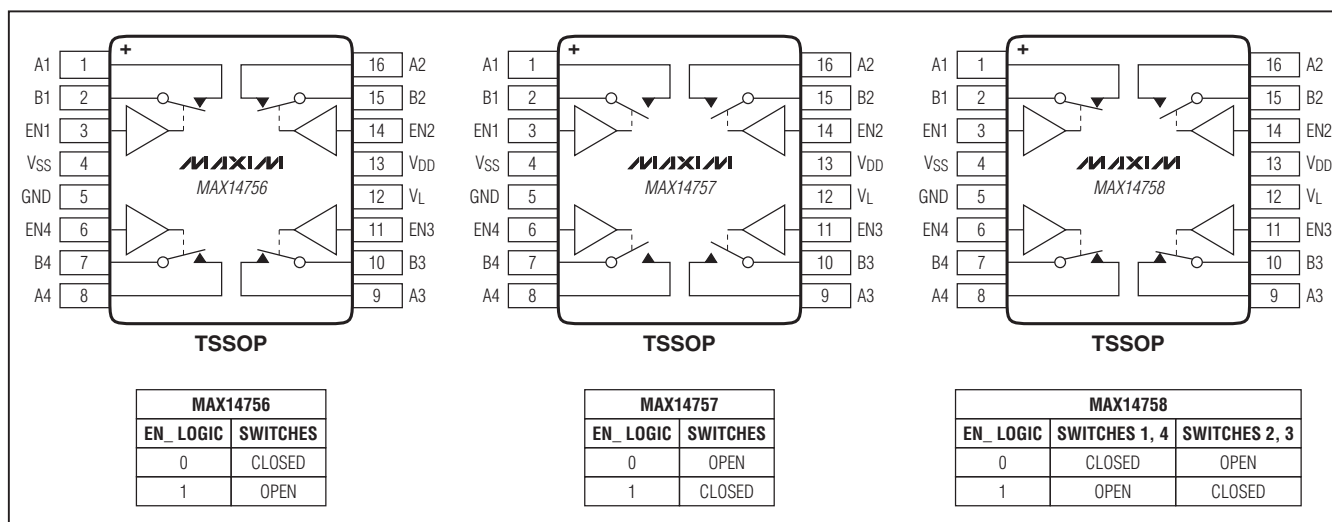♦ **Single-Supply Operation from +10V to +70V**

♦ **Bipolar-Supply Operation Up to ±35V**

♦ **On-Resistance of 10Ω (max)**

♦ **R_{ON} Flatness of 0.004Ω (typ)**

♦ **2.5nA (max) Off-Leakage Currents at +85°C**

♦ **Overvoltage/Undervoltage Clamping Through Protection Diodes**

♦ **500µA (typ) Supply Current**

♦ **TSSOP 16-Pin Package**

♦ **-40°C to +85°C Ambient Temperature Range**

♦ **Functionally Compatible to DG411, DG412, and DG413**

♦ **Functionally Operational Up to +125°C**

Ordering Information

PART	FUNCTION	TEMP RANGE	PIN-PACKAGE
MAX14756EUE+	Quad NC SPST	-40°C to +85°C	16 TSSOP
MAX14757EUE+	Quad NO SPST	-40°C to +85°C	16 TSSOP
MAX14758EUE+	Dual NO + NC SPST	-40°C to +85°C	16 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Functional Diagrams

MAX14756	
EN_ LOGIC	SWITCHES
0	CLOSED
1	OPEN

MAX14757	
EN_ LOGIC	SWITCHES
0	OPEN
1	CLOSED

MAX14758		
EN_ LOGIC	SWITCHES 1, 4	SWITCHES 2, 3
0	CLOSED	OPEN
1	OPEN	CLOSED

MAXIM

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642,
or visit Maxim's website at www.maxim-ic.com.

Quad SPST +70V Analog Switches

ABSOLUTE MAXIMUM RATINGS

V_{DD} to V_{SS} ....-0.3V to +72V
V_{SS} to GND ....-36V to +0.3V
V_L, EN_ to GND ....-0.3V to the lesser of (+12V, V_{DD} + 0.3V)
A_, B_ to V_{SS} ....-0.3V to (V_{DD} + 2V) or 100mA
(whichever occurs first)
Continuous Current into A_, B_ .... ±100mA

Continuous Power Dissipation (T_A = +70°C)
    TSSOP (derate 11.1mW/°C above +70°C) 889mW
Operating Temperature Range .... -40°C to +85°C
Storage Temperature Range........................... -65°C to +150°C
Junction Temperature .... +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TSSOP
    Junction-to-Ambient Thermal Resistance (θ_{JA})...........90°C/W
    Junction-to-Case Thermal Resistance (θ_{JC})................27°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—DUAL SUPPLIES

(V_{DD} = +35V, V_{SS} = -35V, V_{GND} = 0V, V_L = +3.3V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
V_{DD} Supply-Voltage Range	V_{DD}		+10		+35	V
V_{SS} Supply-Voltage Range	V_{SS}		-10		-35	V
V_L Logic Supply-Voltage Range	V_L		+1.6		+11	V
V_{DD} Supply Current	$I_{DD(OFF)}$	$V_{EN\_}$ to switch off state, $V_{A\_}$, $V_{B\_}$ = +20V		200	450	μA
	$I_{DD(ON)}$	$V_{EN\_}$ to switch on state, $V_{A\_}$, $V_{B\_}$ = +20V		500	800	
V_{SS} Supply Current	$I_{SS(OFF)}$	$V_{EN\_}$ to switch off state, $V_{A\_}$, $V_{B\_}$ = +20V		200	450	μA
	$I_{SS(ON)}$	$V_{EN\_}$ to switch on state, $V_{A\_}$, $V_{B\_}$ = +20V		500	800	
V_L Current	I_L	V_L = +11V, V_{EN1} = V_{EN2} = V_{EN3} = V_{EN4} = (0.25 x V_L) or (0.75 x V_L)			0.4	mA
SWITCH						
Analog-Signal Range	$V_{A\_}$, $V_{B\_}$	Figure 1	V_{SS}		V_{DD}	V
Current Through Switch	$I_{A\_}$, $I_{B\_}$	$V_{A\_}$, $V_{B\_}$ = +20V	-50		+50	mA
On-Resistance	R_{ON}	$I_{A\_}$, $I_{B\_}$ = 10mA, $V_{A\_}$, $V_{B\_}$ = ±20V, Figure 1		5	10	Ω
On-Resistance Matching Between Channels	ΔR_{ON}	$I_{A\_}$, $I_{B\_}$ = 10mA, $V_{A\_}$, $V_{B\_}$ = ±20V, 0V (Note 2)		0.3	0.5	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	$I_{A\_}$, $I_{B\_}$ = 10mA, $V_{A\_}$, $V_{B\_}$ = ±20V		0.004		Ω
On-Leakage Current	$I_{A/B\_(ON)}$	$V_{B\_}$ = ±20V, $V_{A\_}$ = unconnected, Figure 2	-5		+5	nA
		$V_{B\_}$ = ±20V, $V_{A\_}$ = unconnected, T_A = +25°C, Figure 2		0.01		
Off-Leakage Current	$I_{A/B\_(OFF)}$	$V_{B\_}$ = ±20V, $V_{A\_}$ = -20V, Figure 3	-2.5		+2.5	nA
		$V_{B\_}$ = ±20V, $V_{A\_}$ = -20V, T_A = +25°C, Figure 3		0.01		

MAXIM

Quad SPST +70V Analog Switches

ELECTRICAL CHARACTERISTICS—DUAL SUPPLIES (continued)

(VDD = +35V, VSS = -35V, VGND = 0V, VL = +3.3V, TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC (EN1, EN2, EN3, EN4)						
Input-Voltage Low	VIL				0.25 x VL	V
Input-Voltage High	VIH		0.75 x VL			V
Input Leakage Current		VEN_ = 0V or VL	-1		+1	µA
DYNAMIC CHARACTERISTICS						
VDD/VSS Power-On Time		RL = 10kΩ		1		µs
Enable Turn-On Time	tON	VA_, VB_= ±10V, RL = 10kΩ, Figure 4		35	60	µs
Enable Turn-Off Time	tOFF	VA_, VB_= ±10V, RL = 10kΩ, Figure 4		2	3	µs
Off-Isolation	VISO	VA_, VB_= 1V RMS, f = 100kHz, RL = 1kΩ, CL = 15pF, Figure 5		65		dB
Crosstalk	VCT	RS = RL = 1kΩ, Figure 6		96		dB
-3dB Bandwidth	BW	RS = 50Ω, RL = 1kΩ, Figure 7		145		MHz
Total Harmonic Distortion Plus Noise	THD+N	RS = RL = 1kΩ, f = 20Hz to 20kHz		0.001		%
Charge Injection	Q	A_, B_ = GND, CL = 1nF, Figure 8		580		pC
Switch-On Capacitance	CIN	VDD = +50V, VSS = 0V, VA_, VB_= +4V, f = 1MHz		40		pF
Switch-Off Capacitance	CIN	VDD = +50V, VSS = 0V, VA_, VB_= +4V, f = 1MHz		35		pF

DC ELECTRICAL CHARACTERISTICS—SINGLE SUPPLY

(VDD = +70V, VSS = VGND = 0V, VL = +3.3V, TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
VDD Supply-Voltage Range	VDD		+10		+70	V
SWITCH						
On-Resistance	RON	IA_ = 10mA, VA_, VB_ = +20V, Figure 1		5	10	Ω
On-Resistance Matching Between Channels	ΔRON	IA_, IB_ = 10mA, VA_, VB_ = +70V, 0V (Note 2)		0.3	0.5	Ω
Off-Leakage Current	IA/B_(OFF)	VB_ = +40V, VA_= +10V, Figure 3	-2.5		+2.5	nA

Note 2: Guaranteed by design; not production tested.
Note 3: All parameters in single-supply operation are expected to be the same as in dual-supply operation.
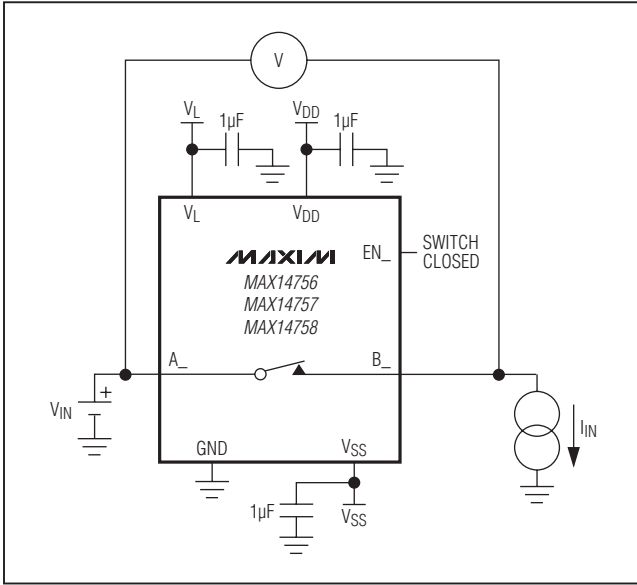
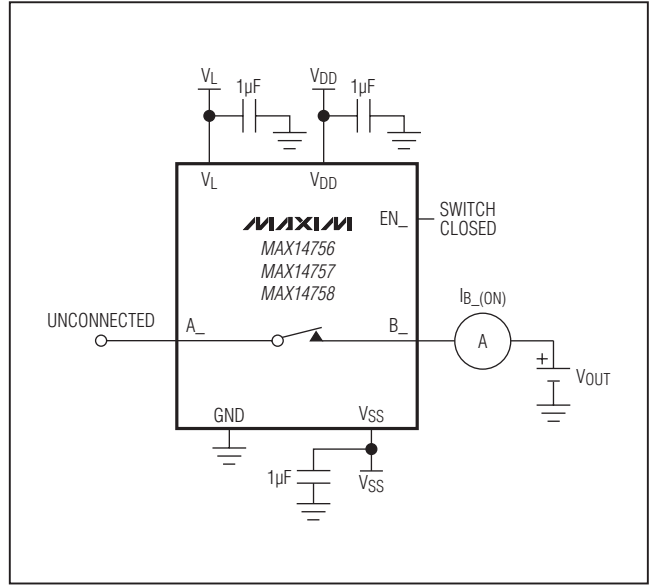# Quad SPST +70V Analog Switches

Figure 1. On-Resistance Measurement

Figure 2. On-Leakage Current

Figure 3. Off-Leakage Current
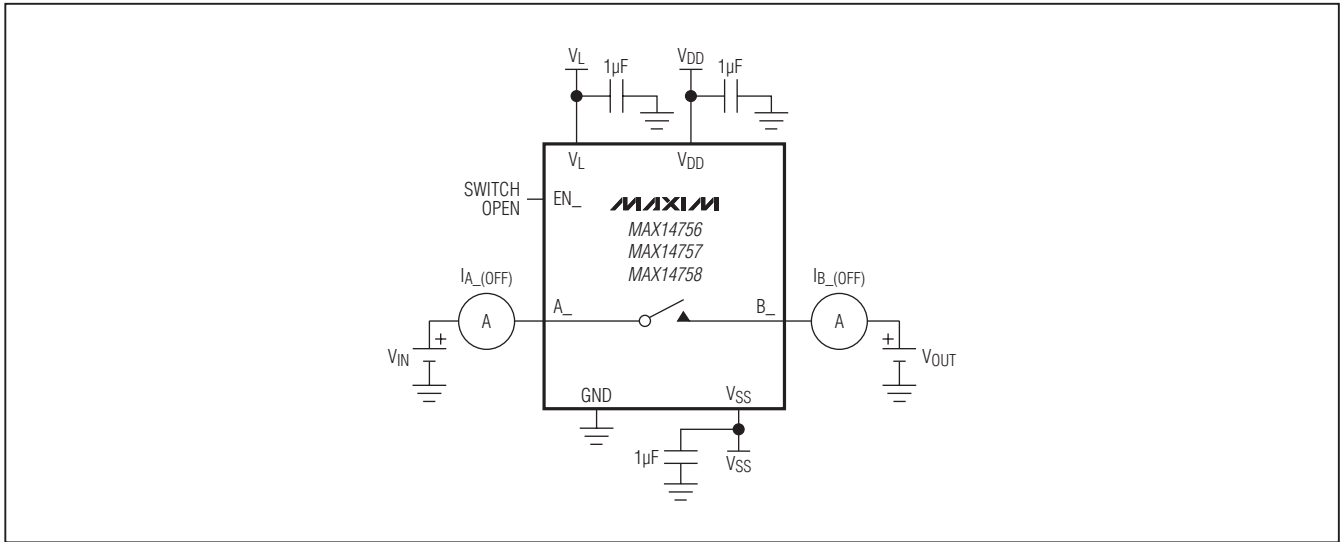
Figure 4. Enable Switching Time
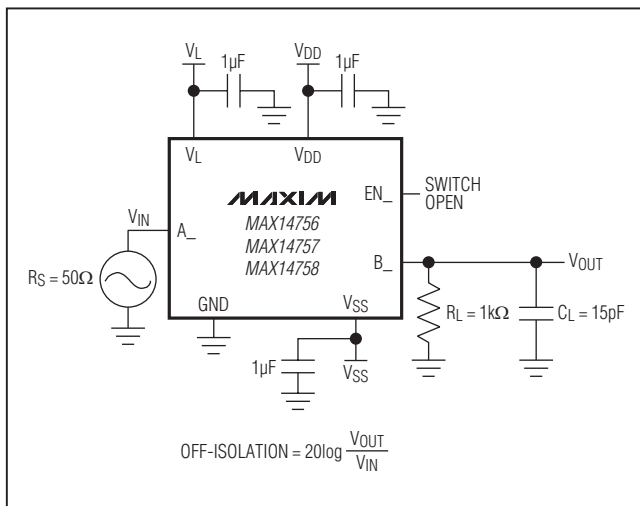
Figure 5. Off-Isolation

$$\text{OFF-ISOLATION} = 20\log\frac{V_{OUT}}{V_{IN}}$$
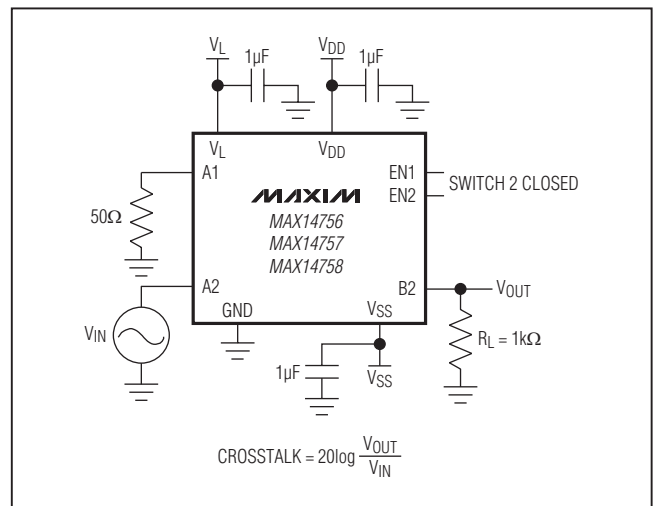
Figure 6. Crosstalk

$$\text{CROSSTALK} = 20\log\frac{V_{OUT}}{V_{IN}}$$
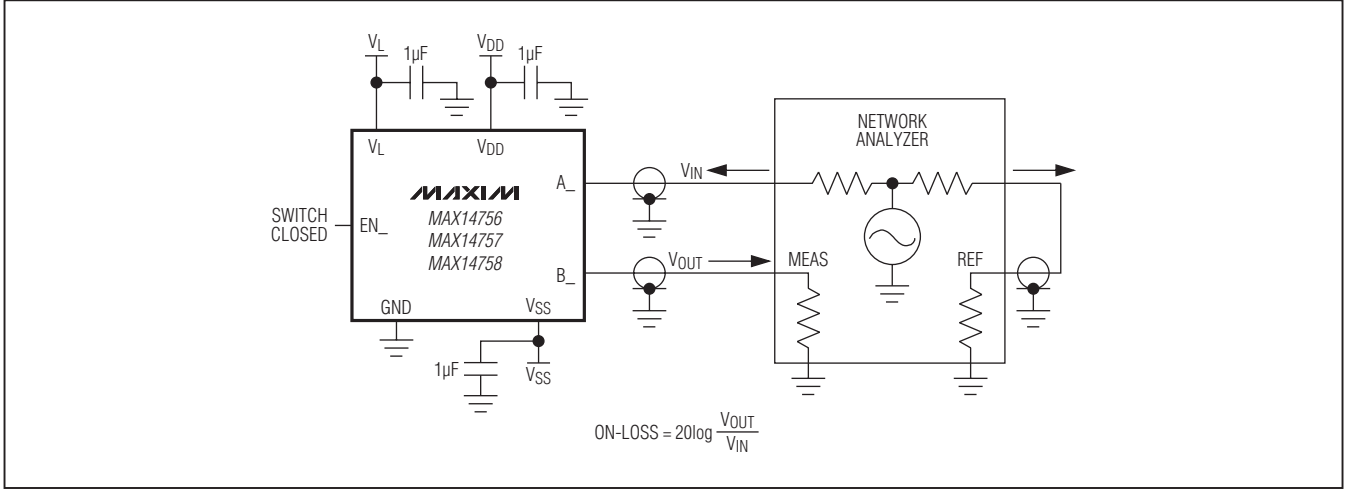
Test Circuits/Timing Diagrams (continued)

ON-LOSS = $20\log \dfrac{V_{OUT}}{V_{IN}}$

Figure 7. Frequency Response

V_{OUT} IS THE MEASURED VOLTAGE DUE TO CHARGE
TRANSFER ERROR Q WHEN THE CHANNEL TURNS OFF.
$Q = C_L \times V_{OUT}$
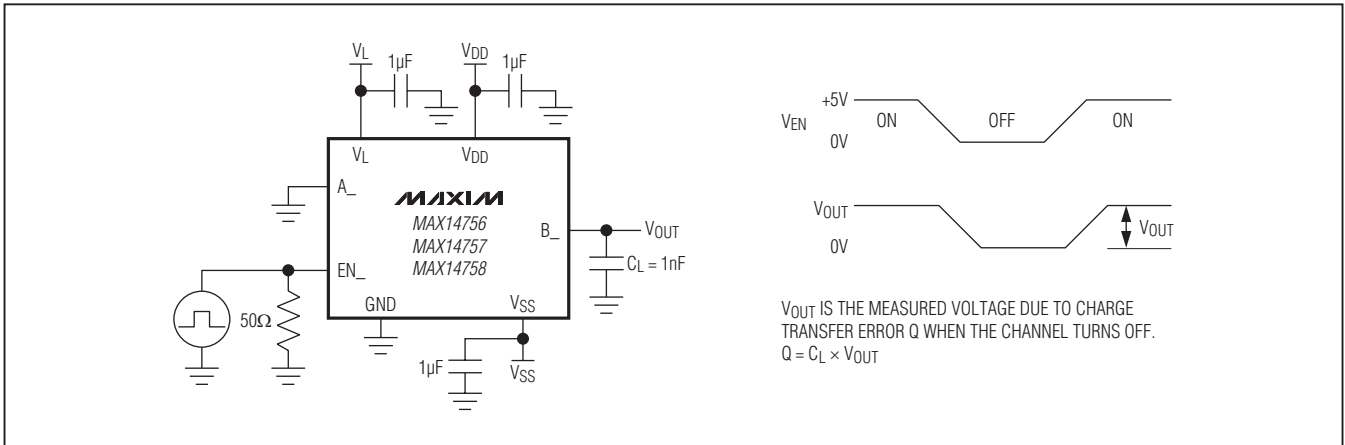
Figure 8. Charge Injection

MAXIM

Typical Operating Characteristics

(T_A = +25°C, V_L = +3.3V, unless otherwise noted.)

ON-RESISTANCE vs. V_B_
(DUAL SUPPLIES)

ON-RESISTANCE vs. V_B_ AND TEMPERATURE
(DUAL SUPPLIES)

ON-RESISTANCE vs. V_B_
(SINGLE SUPPLY)

ON-RESISTANCE vs. V_B_ AND TEMPERATURE
(SINGLE SUPPLY)

ON-LEAKAGE vs. TEMPERATURE

ON-LEAKAGE vs. TEMPERATURE

CHARGE INJECTION vs. TEMPERATURE

SUPPLY CURRENT vs. TEMPERATURE

V_L INPUT CURRENT vs. V_EN_

Quad SPST +70V Analog Switches

(T_A = +25°C, V_L = +3.3V, unless otherwise noted.)

MAX14756/MAX14757/MAX14758
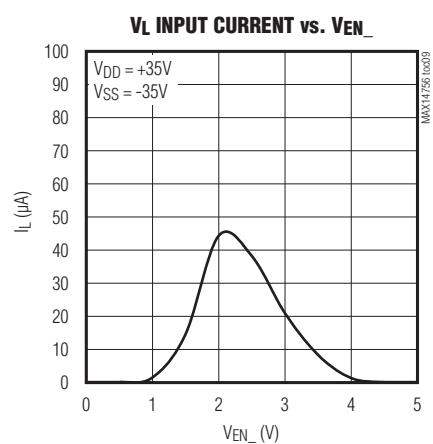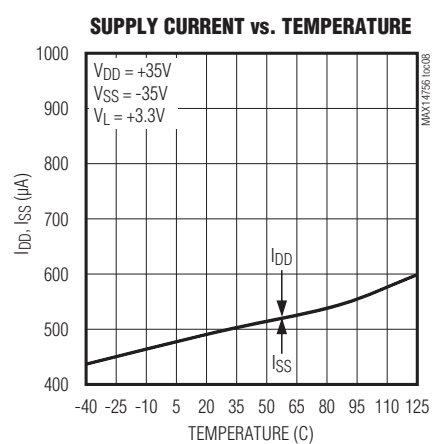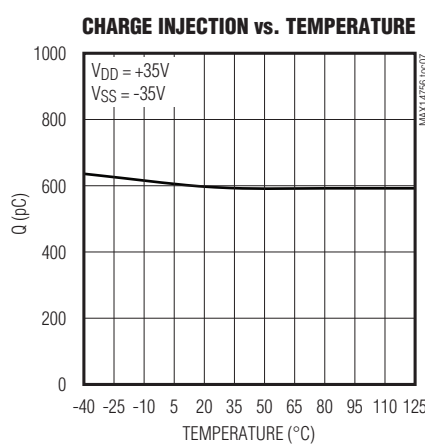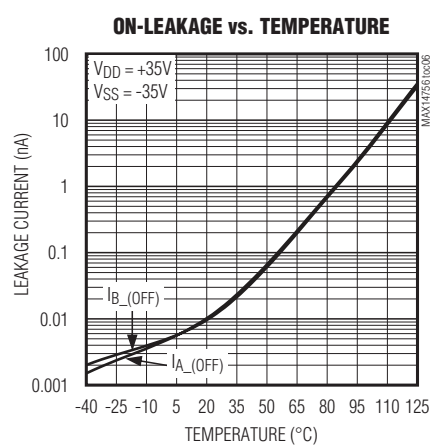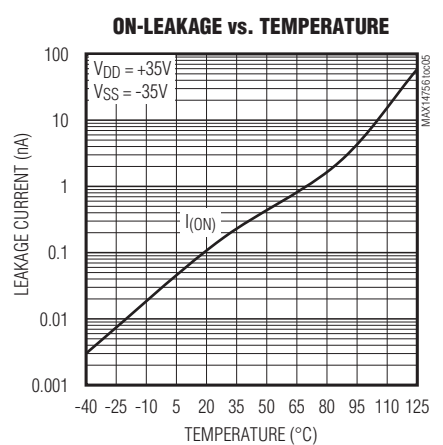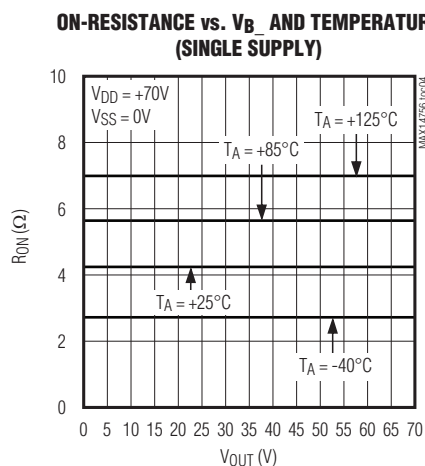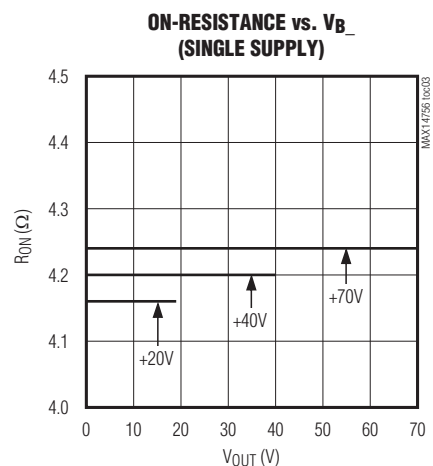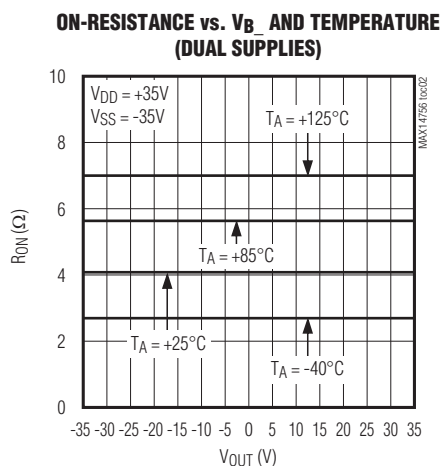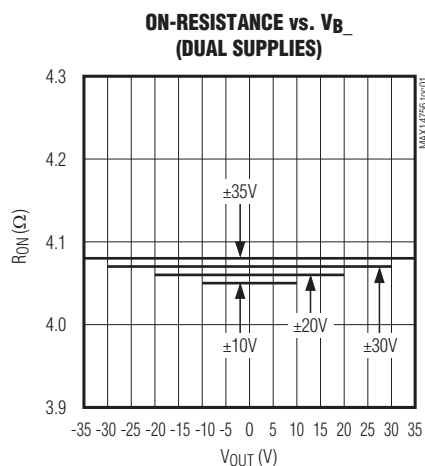
CROSSTALK vs. FREQUENCY

OFF-ISOLATION vs. FREQUENCY

ON-LOSS vs. FREQUENCY

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY

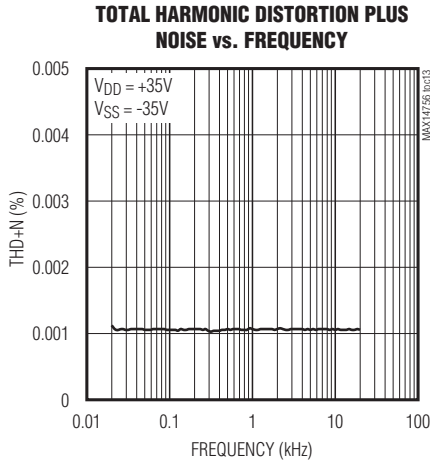**PSRR vs. FREQUENCY**

TURN-ON TIME vs. INPUT VOLTAGE

TURN-OFF TIME vs. INPUT VOLTAGE

MAXIM

Quad SPST +70V Analog Switches

TOP VIEW

A1	1			16	A2
B1	2			15	B2
EN1	3			14	EN2
V$_{SS}$	4			13	V$_{DD}$
GND	5	MAX14756 MAX14757 MAX14758		12	V$_L$
EN4	6			11	EN3
B4	7			10	B3
A4	8			9	A3

TSSOP
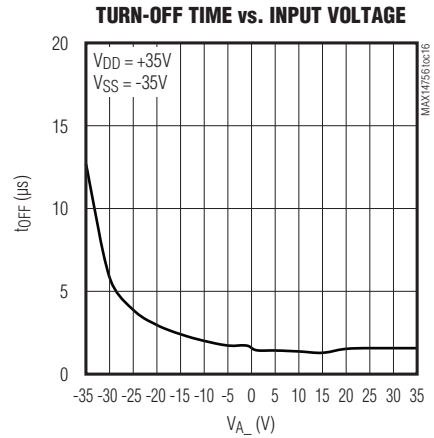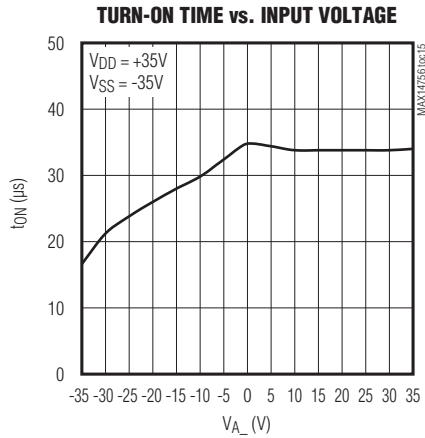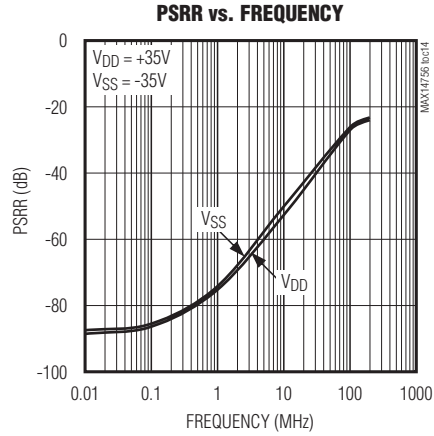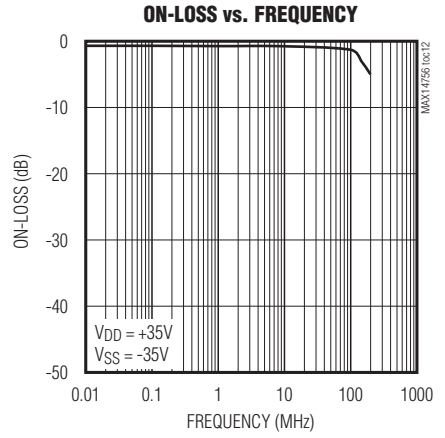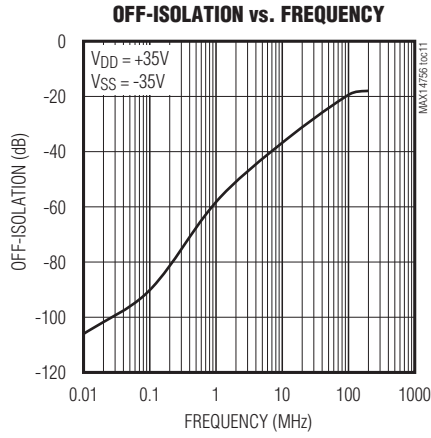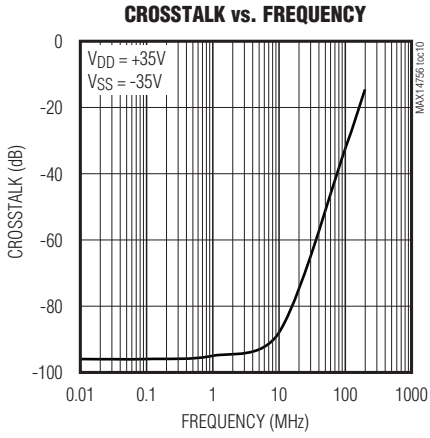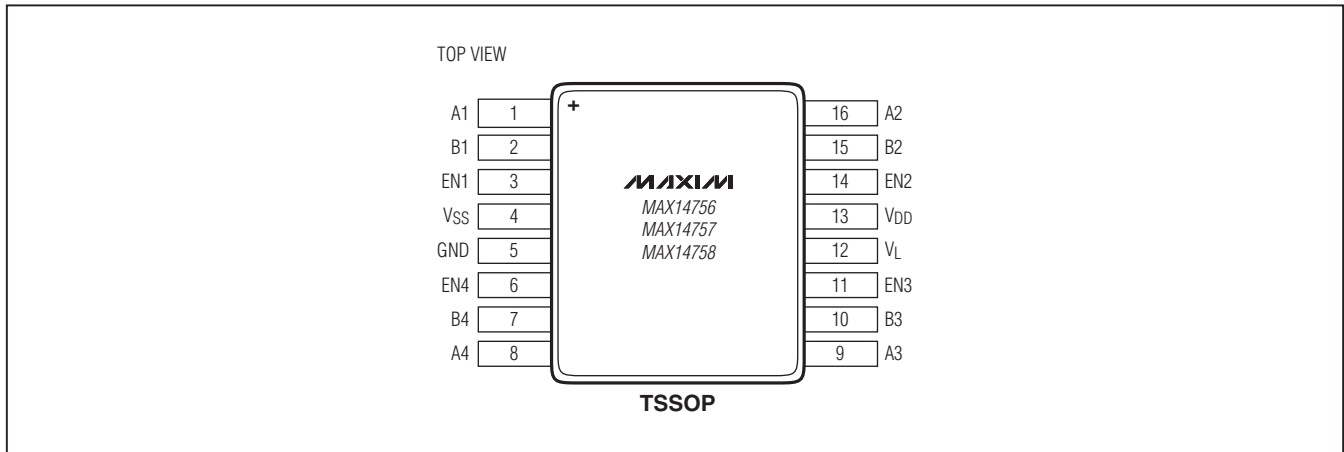
Pin Description

PIN	NAME	FUNCTION
1	A1	Terminal A of Switch 1
2	B1	Terminal B of Switch 1
3	EN1	Enable Input of Switch 1. When EN1 is driven high, the switch's state (NO/NC) changes (see Tables 1, 2, and 3).
4	V$_{SS}$	Negative Supply Voltage. Bypass V$_{SS}$ to GND with a 1µF ceramic capacitor (100V rated) as close as possible to the pin.
5	GND	Ground
6	EN4	Enable Input of Switch 4. When EN4 is driven high, the switch's state (NO/NC) changes (see Tables 1, 2, and 3).
7	B4	Terminal B of Switch 4
8	A4	Terminal A of Switch 4
9	A3	Terminal A of Switch 3
10	B3	Terminal B of Switch 3
11	EN3	Enable Input of Switch 3. When EN3 is driven high, the switch's state (NO/NC) changes (see Tables 1, 2, and 3).
12	V$_L$	Logic Supply Voltage. Bypass V$_L$ to GND with a 1µF ceramic capacitor as close as possible to the pin.
13	V$_{DD}$	Positive Supply Voltage. Bypass V$_{DD}$ to GND with a 1µF ceramic capacitor (100V rated) as close as possible to the pin.
14	EN2	Enable Input of Switch 2. When EN2 is driven high, the switch's state (NO/NC) changes (see Tables 1, 2, and 3).
15	B2	Terminal B of Switch 2
16	A2	Terminal A of Switch 2

Detailed Description

The MAX14756/MAX14757/MAX14758 are analog switches with low on-resistance of 10Ω (max) that conduct equally well in both directions. All devices have a rail-to-rail analog-signal range. They operate with a single +70V supply in unipolar applications or ±35V dual supplies in bipolar applications. The bipolar supplies can be offset and do not have to be symmetrical.

The MAX14756 is a quad NC SPST switch, the MAX14757 is a quad NO SPST switch, and the MAX14758 has two NO and two NC SPST switches. These switches have 5Ω (typ) on-resistances and low on-leakage currents of 5nA (max). The on-resistance flatness is 0.004Ω (typ). These devices are suitable for a multitude of analog-signal routing and switching applications, and are functonally operational up to +125°C with increased leakage currents.

Applications Information

Low-Distortion Audio
The MAX14756/MAX14757/MAX14758 switches, having low R_{ON} and very low R_{ON} variation with signal amplitude, are well suited for low-distortion audio applications. The *Typical Operating Characteristics* show Total Harmonic Distortion (THD) vs. Frequency graphs for several signal amplitudes.

Current Through the Switches
The current flowing through every switch must be limited to ±50mA for normal operation. If the current exceeds this limit, an internal leakage current flows from the switch to V_{SS}. Larger input currents do not destroy the device, as long as the *Absolute Maximum Ratings* are not exceeded.

Input-Voltage Clamping
For applications that require input voltages beyond the supplies rails, the internal input diodes to V_{DD} and V_{SS} can be used to limit the input voltages. As shown in Figure 9, series resistors can be employed at the inputs to limit the currents flowing into the diodes during undervoltage and overvoltage conditions. Choose the limiting resistors such that the input currents are limited to $I_{IN\_}(MAX) = 100mA$. The values of the current-limit resistors can be calculated as the larger of R_{LIM+} and R_{LIM-}.

$$R_{LIM+} = \frac{V_{IN}(MAX) - V_{DD}}{I_{IN\_}(MAX)}$$

$$R_{LIM-} = \frac{V_{SS} - V_{IN}(MIN)}{I_{IN\_}(MAX)}$$

Table 1. MAX14756 Truth Table

LOGIC		SWITCH	
EN1	0	A1/B1	Closed
EN2	0	A2/B2	Closed
EN3	0	A3/B3	Closed
EN4	0	A4/B4	Closed
EN1	1	A1/B1	Open
EN2	1	A2/B2	Open
EN3	1	A3/B3	Open
EN4	1	A4/B4	Open

Table 2. MAX14757 Truth Table

LOGIC		SWITCH	
EN1	0	A1/B1	Open
EN2	0	A2/B2	Open
EN3	0	A3/B3	Open
EN4	0	A4/B4	Open
EN1	1	A1/B1	Closed
EN2	1	A2/B2	Closed
EN3	1	A3/B3	Closed
EN4	1	A4/B4	Closed

Table 3. MAX14758 Truth Table

LOGIC		SWITCH	
EN1	0	A1/B1	Closed
EN2	0	A2/B2	Open
EN3	0	A3/B3	Open
EN4	0	A4/B4	Closed
EN1	1	A1/B1	Open
EN2	1	A2/B2	Closed
EN3	1	A3/B3	Closed
EN4	1	A4/B4	Open

During an undervoltage or overvoltage condition, the input impedance is equal to R_{LIM}. The additional power dissipation due to the fault currents needs to be calculated. During an overvoltage or undervoltage clamping condition on one switch input, the other switches of the MAX14756/MAX14757/MAX14758 operate normally.

Beyond-the-Rail Input
If input voltages are expected to go beyond the supply voltages, but within the absolute maximum supply voltages of the MAX14756/MAX14757/MAX14758, add two diodes in series with the supplies as shown in Figure 10.
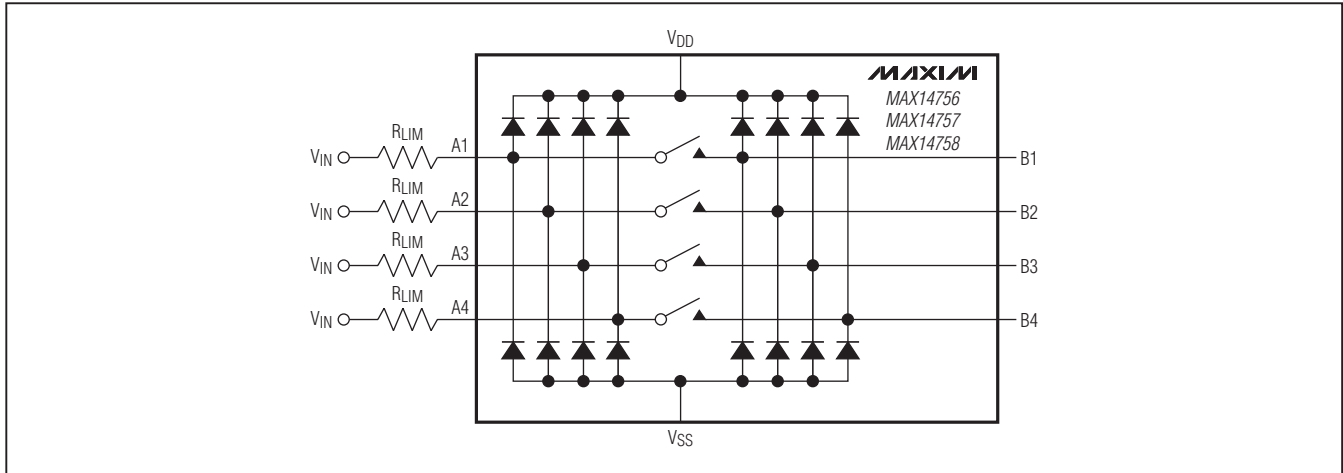
MAXIM

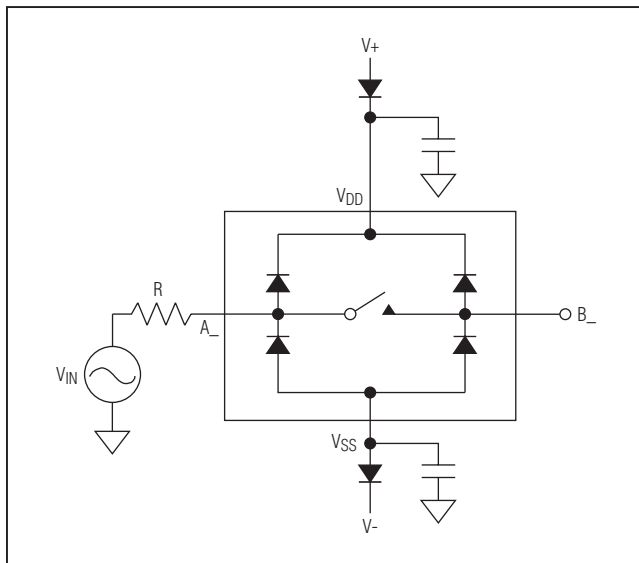Figure 9. Input Overvoltage and Undervoltage Clamping

Figure 10. Beyond-the-Rail Application

During undervoltage and overvoltage events, the internal diodes pull V_{DD}/V_{SS} supplies up/down. An advantage of this scheme is that the input impedance is high and currents do not flow though the MAX14756/MAX14757/MAX14758 during overvoltage and undervoltage events. The input voltages must be limited to the voltages specified in the *Absolute Maximum Ratings* section.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TSSOP	U16+1	**21-0066**	**90-0117**

MAX14756/MAX14757/MAX14758

Quad SPST +70V Analog Switches

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/10	Initial release	—

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600