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General Description

The MAX14912/MAX14913 have eight 640mA smart high-side switches that can also be configured as push-pull drivers for high-speed switching. The propagation delay from input to switching of the high-side/low-side drivers is 1µs (max). Each high-side driver has a low on-resistance of 230mΩ (max) at 500mA load current at T_A = 125°C.

The device is configured and controlled either through pins or the SPI interface. The SPI interface is daisy-chainable, which allows efficient cascading of multiple devices. SPI also supports command mode, for the highest detailed diagnostic information. The MAX14912 allows configuration through SPI in parallel and serial setting modes, while the MAX14913 only supports configuration through SPI in serial setting mode.

Open-load detection in high-side mode detects both open-wire conditions in the switch on/off states, and LED drivers provide indication of per-channel fault and status conditions. Internal active clamps accelerate the shutdown of inductive loads fast in high-side mode.

The MAX14912/MAX14913 are available in a 56-pin QFN 8mm x 8mm package.

Applications

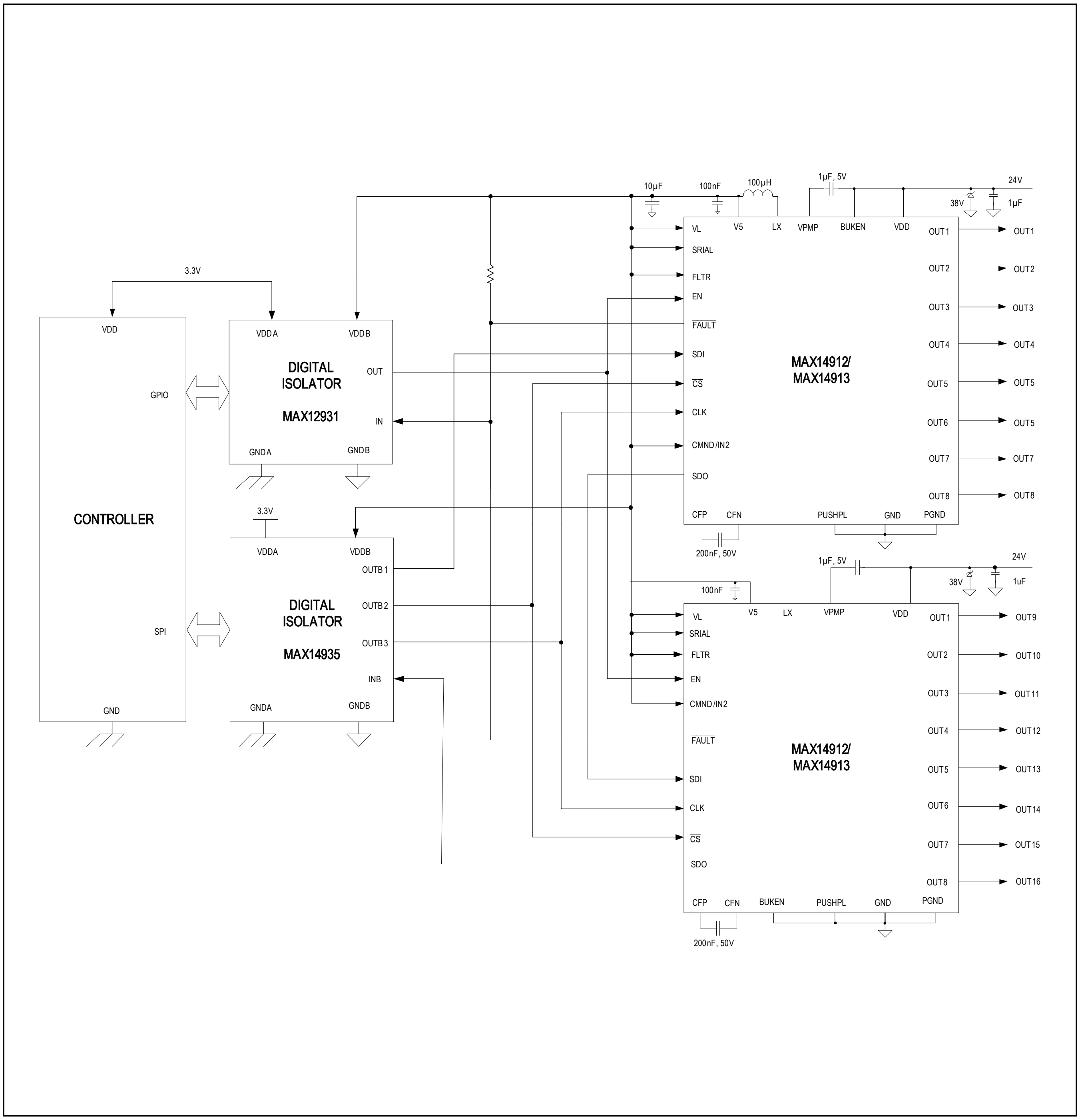
- Industrial Digital Outputs
- PLC Systems
- Building Automation

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Low Power and Heat Dissipation
  - 230mΩ (max) High-Side R_{ON} at T_A = 125°C
  - High-Efficiency 5V/100mA Buck Regulator
- Fast Switching Ideal for High-Speed Control Systems
  - 0.1µs (typ.) Propagation Delay (High-Side Mode)
  - 0.5µs (typ.) Propagation Delay (Push-Pull Mode)
  - 200kHz Switching-Rate Capability in Push-Pull Mode
  - Fast Inductive Load Demagnetization
- Robust Operation
  - 60V Abs Max V_{DD} Rating
  - Safe-Demagnetization: Turn-Off of Unlimited Inductance
  - IEC61000-4-2 8kV Air Gap/6kV Contact ESD Protection
  - ±1kV/42Ω Surge Protection with TVS on VDD
  - Robust SPI Interface with Watchdog and CRC
  - -40°C to +125°C Ambient Operating Temperature Range
- Extensive Diagnostics Reduces System Downtime
  - Per Driver and Chip Thermal Shutdown
  - Open-Wire Detection in High-Side Mode
  - Low Supply Voltage Warning
  - Undervoltage Detection
  - Overvoltage Detection on OUT
  - Overcurrent Detection
  - LED Drivers for Visual Fault and Output State Indication
- Flexible Interface for Ease of Design
  - Serial and/or Parallel Control Interface
  - Per-Channel Configuration and Monitoring
  - Wide Logic Voltage Range (1.6V to 5.5V)
- Small Package and High Integration Enables Compact High-Density I/O Modules
  - 56-Pin QFN 8mm x 8mm Package
  - Eight High-Side Switches/Push-Pull Drivers
  - Daisy-Chainable SPI Interface

Typical Application Circuit



Absolute Maximum Ratings

(All voltages relative to GND.)
V_{DD} .... -0.3V to +60V
PGND .... -0.3V to +0.3V
BUKEN, LX .... -0.3V to (V_{DD} + 0.3V)
V_{PMP} .... (V_{DD} - 0.3V) to (V_{DD} + 6V)
OUT_ (continuous voltage) .... (V_{DD} - 49V) to (V_{DD} + 0.3V)
V_5, V_L .... -0.3V to +6V
CFP .... (V_{DD} - 0.3V) to (V_{PMP} + 0.3V)
CFN .... -0.3V to (V_{PMP} + 0.3V)
SDO .... -0.3V to (V_L + 0.3V)
SDI, CLK, $\overline{CS}$ .... -0.3V to +6V
IN_, PUSHPL, FLTR, SRIAL, EN, $\overline{FAULT}$, $\overline{CERR}$/IN4, WDFLT/IN6 .... -0.3V to +6V
LED_, LD_ .... -0.3V to (V_5 + 0.3V)
Inductive Kickback Energy OUT_ pins: I_L < 0.6A .... Unlimited
OUT_ Load Current .... Internally Limited
Continuous-Current (any other terminal) .... ±100mA
Continuous Power Dissipation (T_A = +70°C)
QFN (derate 47.6mW/°C above 70°C) 3800mW
Junction Temperature .... Internally Limited
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (Soldering, 10sec) .... +300°C

Package Thermal Characteristics (Note 1)

Thermal Resistances QFN56-EP package
Junction-to-Ambient Thermal Resistance (θ_{JA}), Multilayer Board .... 21°C/W
Junction-to-Case Thermal Resistance (θ_{JC}), Multilayer Board .... 1.0°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(V_{DD} = +10V to +36V, V_5 = +4.5V to +5.5V, V_L = +1.6V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{DD} = +24V, CDCDC = 10µF, LDCDC = 100µH, CFLY = 200nF, CPUMP = 10µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY						
V_{DD} Supply Voltage	V_{DD}		10.5		36	V
V_{DD} Supply Current	I_{DD}	HS mode, EN = high, OUT_ outputs high (no switching), no load, V_5 and V_L supplied externally		1.1	1.5	mA
		PP mode, EN = high, 100kHz switching on all OUT_, V_5 and V_L supplied externally, no load		14	22	
V_{DD} Undervoltage-Lockout Threshold	V_{DD_UV}	V_5 = 5V, V_{DD} rising	8.5		9.5	V
V_{DD} Undervoltage-Lockout Hysteresis	V_{DD_UVHYST}	V_5 = 5V		1		V
V_{DD} Low-Voltage Warning Threshold	V_{DD_LV}	V_{DD} falling	12	13	14	V
V_{DD} Low-Voltage Warning Hysteresis	V_{DD_LVHYST}	V_5 = 5V		2		V

Electrical Characteristics (continued)

(V_{DD} = +10V to +36V, V_5 = +4.5V to +5.5V, V_L = +1.6V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{DD} = +24V, CDCDC = 10µF, LDCDC = 100µH, CFLY = 200nF, CPUMP = 10µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_5/V_L Supplies						
V_5 Supply Voltage (Supplied Externally)	V_5		4.5		5.5	V
V_5 Supply Current (V_5 Supplied Externally)	I_{V5}	HS mode, EN = high, OUT_ outputs high, no load, no LEDs connected		2.2	3.2	mA
		PP mode, EN = high, OUT_ switching at 100kHz, no load, no LEDs connected		8.5	11	mA
V_5 Undervoltage-Lockout Threshold	V_{V5_UV}	V_{DD} = 24V, V5 rising	3.8		4.2	V
V_5 Undervoltage-Lockout Hysteresis	V_{V5_UVHYST}	V_{DD} = 24V		0.3		V
V_L Supply Voltage	V_L		1.6		5.5	V
V_L Supply Current	I_{VL}	All logic inputs high or low		24	35	µA
V_L Undervoltage-Lockout Threshold	V_{L_UV}	V_L falling	1.12	1.27	1.52	V
5V DC-DC REGULATOR						
Undervoltage-Lockout Threshold of the DC-DC Regulator	V_{DCDC_UVLO}	V_{DD} rising			6.6	V
Undervoltage-Lockout Threshold of the DC-DC Regulator Hysteresis	V_{DCDC_UVLOHY}			0.5		V
Output Regulated Voltage	V_{DCDC}	0mA to 90mA external load current	4.85	5.0	5.15	V
Current Limit	I_{CL_DCDC}		100			mA
Turn-On Time	T_{ON_DCDC}	Delay from V_{DD} crossing the UVLO threshold until the DC-DC regulator finishes soft-start	3.0	3.4	3.7	ms
Switching Frequency	f_{DCDC}		540	600	660	kHz
DRIVER OUTPUTS (OUT_)						
HS Mode On-Resistance	R_{OUT_HS}	HS mode, HS = on, IOUT_ = -500mA (Note 6)		110	230	mΩ
HS Mode Current Limit	I_{LIM}	EN = high, HS = on, $V_{OUT\_\_}$ = V_{DD} -1V	0.64	0.87	1.2	A
HS Mode Current-Limit V/I Slope		(See *Overcurrent and Short-Circuit Protection* section)		150		Ω
HS Mode Weak Pulldown Current	I_{LKG}	High-side mode, OL detect = off, HS = off, 7V < $V_{OUT\_}$ < V_{DD}	65	100	135	µA

Electrical Characteristics (continued)

(V_{DD} = +10V to +36V, V_5 = +4.5V to +5.5V, V_L = +1.6V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{DD} = +24V, CDCDC = 10µF, LDCDC = 100µH, CFLY = 200nF, CPUMP = 10µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Push-Pull Mode HS On-Resistance	R_{OUT_PP}	PP mode, HS = on, EN = high, $I_{OUT\_}$ = -500mA (Note 6)		110	230	mΩ
Push-Pull Mode LS On-Resistance	V_{OL_PP}	PP mode, LS = on, EN = high, I_{OUT} = 500mA		1	2.5	Ω
Push-Pull Mode Current Limit	I_{LIM_PP}	PP mode, EN = High, OUT_ = high, $V_{OUT\_}$ = V_{DD} - 1V	0.64	0.87	1.2	A
		PP mode, EN = High, OUT_ = low, 3V < $V_{OUT\_}$ < V_{DD}	0.44	0.68	0.81	A
OPEN-LOAD DETECT (OUT_)						
Open-Load Pullup Current, High-Side Off	I_{OL_HSOFF}	OL detect = on, high-side mode, HS = off, 7V < $V_{OUT\_}$ < V_{DD} -1V	50	74	100	µA
Open-Load Detect Threshold, High-Side Off	V_{OL_T}	OL detect = on, high-side mode, HS = off, LED turns off/on	6.4	6.7	7.35	V
Open-Load Detect Threshold Current, High-Side On	I_{OL_HSON}	OL detect = on, high-side mode, HS = on, 0V < $V_{OUT\_}$ < (V_{DD} -1V)	1	2	3	mA
Debounce Filter	T_{DEB_OL}	Reliable open-load detection reading is obtained only if both the switch input state and the load level do not change for T_{DEB_OL}, high-side = on/off		100		ms
LOGIC (I/O)						
Input Voltage High	V_{IH}	V_L < 2.5V	0.8 x V_L			V
		V_L ≥ 2.5V	0.7 x V_L			
Input Voltage Low	V_{IL}	V_L < 2.5V			0.16 x V_L	V
		V_L ≥ 2.5V			0.3 x V_L	
Input Threshold Hysteresis	V_{IHYST}			0.1 x V_L		V
Input Pulldown Resistor	R_I	All logic input pins, except $\overline{CS}$ (Note 2)	140	200	275	kΩ
Input Pullup Resistor	R_I	$\overline{CS}$ input (Note 2)	140	200	275	kΩ
Output Logic-High (SDO)	V_{OH}	I_L = -5mA	V_L - 0.33V			V
Output Logic-Low	V_{OL}	I_L = +5mA			0.33	V
SDO Pulldown Resistor	R_{L_SDO}	$\overline{CS}$ = high	140	200	275	kΩ
OPEN-DRAIN OUTPUTS ($\overline{FAULT}$, $\overline{CERR}$/IN4, WDFLT/IN6)						
Output Logic-Low	V_{ODL}	I_L = +5mA			0.58	V
Leakage	I_{ODL}	Open-drain output off, pins are at 5.5V	-1		+1	µA

Electrical Characteristics (continued)

(V_{DD} = +10V to +36V, V_5 = +4.5V to +5.5V, V_L = +1.6V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{DD} = +24V, CDCDC = 10µF, LDCDC = 100µH, CFLY = 200nF, CPUMP = 10µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LED DRIVERS (LEDH_, LDL_)						
Output Voltage High	V_{OH_LED}	LEDH = on, I_{LED} = 5mA	V_5 - 0.3			V
Output Leakage Current High	I_{LH}	LEDH_ = off, V = 0V	-50			µA
Output Voltage Low	V_{OL_LED}	LDL = on, I_{LED} = 5mA			0.3	V
Output Leakage Current Low	I_{LL}	LDL = off, V = 5V			50	µA
LED Driver Scan Rate	FLED	Update rate for each LED	1.07	1.18	1.31	kHz
Fault-LED Minimum On-Time	t_{FAULT_ON}	Fault LED is turned on for at least t_{FAULT_ON}		200		ms
PROTECTION						
OUT_ Clamp Negative Voltage	V_{CL}	Relative to V_{DD}. EN = high	49	56	64.5	V
Channel Thermal-Shutdown Temperature	T_{JSHDN}	Junction temperature rising. Per channel		167		°C
Channel Thermal-Shutdown Hysteresis	T_{JSHDN_HYST}			17		°C
Chip Thermal Shutdown	T_{CSHDN}	Temperature rising		150		°C
Chip Thermal-Shutdown Hysteresis	T_{CSHDN_HYST}			8		°C

AC Electrical Characteristics

(V_{DD} = +10V to +36V, V_5 = +4.5V to +5.5V, V_L = +1.6V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{DD} = +24V, CDCDC = 10μF, LDCDC = 100μH, CFLY = 200nF, CPUMP = 10μF, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUT_ OUTPUTS						
Power-Up Delay	$t_{POWERUP}$	EN = high time from $V_{DD} > V_{DD\_UV}$ to switches turned-on, $V_{HVBUCKEN}$ = 0V or V_{DD}		5.5		ms
Enable Delay	t_{ENABLE}	All power supplies above UVLO thresholds; time from EN positive edge to switches turned on		0.1		μs
Push-Pull Switchover Delay	t_{D_PPMODE}	Delay from high-side to push-pull switchover		45		μs
Output Propagation Delay LH	t_{PD_LH}	High-side mode, delay from IN_ or positive $\overline{CS}$ edge to OUT_ to 0.8 x V_{DD}. C_L = 100pF, FLTR = low.		0.35	0.7	μs
		Push-pull mode, delay from IN_ or $\overline{CS}$ positive edge to OUT_ rising to 0.8 x V_{DD}. C_L = 100pF, FLTR = low (Figure 2)		0.40	0.7	
Output Propagation Delay HL	t_{PD_HL}	High-side mode, delay from IN_ negative edge or $\overline{CS}$ switching high to OUT_ falling by 0.5V. R_L = 48Ω, FLTR = low (Figure 1, Note 5)		0.1		μs
		Push-pull mode, delay between IN_ switching low or $\overline{CS}$ switching high to OUT_ falling to 0.2 x V_{DD}. C_L = 100pF, FLTR = low (Figure 2)		0.35	0.7	
Output-to-Output Propagation Skew LH	$t_{PD\_SK\_LH}$	Push-pull modes, C_L = 1nF, FLTR = X (Note 3, Note 7)	-100	0	100	ns
Output-to-Output Propagation Skew HL	$t_{PD\_SK\_HL}$	Push-pull modes, R_L = 5kΩ, C_L = 1nF, FLTR = X (Note 7)	-100	0	100	ns
Output Rise Time	t_R	Push-pull mode, 20% to 80% V_{DD}, C_L = 100pF, FLTR = X (Note 7)		0.3		μs
		High-side mode, 20% to 80% V_{DD}, FLTR = X (Note 7)		0.3		μs
Output Fall Time	t_F	Push-pull mode, 80% to 20% V_{DD}, V_{DD} < 30V, C_L = 100pF, FLTR = X (Note 7)		0.05		

AC Electrical Characteristics (continued)

(V_{DD} = +10V to +36V, V_5 = +4.5V to +5.5V, V_L = +1.6V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{DD} = +24V, CDCDC = 10µF, LDCDC = 100µH, CFLY = 200nF, CPUMP = 10µF, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CRC ERROR DETECTION ($\overline{CERR}$/IN4)						
Propagation Delay	t_{PDL_CERR}	SRIAL = high, CRC/IN3 = high, OUT_ detects a CRC error on SDI data, I_{SOURCE} = 5mA		14.5		ns
	t_{PDH_CERR}	SRIAL = high, CRC/IN3 = high, OUT_ clears/CERR/IN4, I_{SOURCE} = 5mA		17		ns
WATCHDOG TIMER						
Watchdog Timeout Accuracy	t_{WD_ACC}	SRIAL = high, WDEN/IN5 = high. See Table 5 for watchdog timeout selection.	-10		+10	%
GLITCH FILTERS						
Pulse Length of Rejected Glitch	t_{FPL_GF}	FLTR = high, on EN, CS, _IN_ pins			80	ns
		FLTR = X, SRIAL and PUSHPL pins			170	
Passes Pulse Length	t_{FD_GF}	FLTR = high, on EN, CS, _IN_ pins	260			ns
		FLTR = X, SRIAL and PUSHPL pins	550			
Glitch Filter Delay Time	t_{D_GF}	FLTR = high, on EN, CS, _IN_ pins		140		ns
		FLTR = X, SRIAL and PUSHPL pins		320		
SPI TIMING CHARACTERISTICS						
2.5V ≤ V_L < 5.5V						
CLK Clock Period	t_{CH+CL}		50			ns
CLK Pulse-Width High	t_{CH}		10			ns
CLK Pulse-Width Low	t_{CL}		10			ns
$\overline{CS}$ Fall-to-CLK Rise Time	t_{CSS}	FLTR = low (Note 5)	12			ns
		FLTR = high	260			
SDI Hold Time	t_{DH}		5			ns
SDI Setup Time	t_{DS}		5			ns
Output Data Propagation Delay	t_{DO}	C_L = 10pF. CLK falling-edge to SDO stable			30	ns
SDO Rise-and-Fall Times	t_{FT}			1		ns
$\overline{CS}$ Hold Time	t_{CSH}		40			ns
$\overline{CS}$ Pulse Width High	t_{CSPW}	FLTR = low (Note 5).	15			ns
		FLTR = high	260			

AC Electrical Characteristics (continued)

(V_{DD} = +10V to +36V, V_5 = +4.5V to +5.5V, V_L = +1.6V to +5.5V, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{DD} = +24V, CDCDC = 10μF, LDCDC = 100μH, CFLY = 200nF, CPUMP = 10μF, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1.6V ≤ V_L < 2.5V						
CLK Clock Period	t_{CH+CL}		60			ns
CLK Pulse-Width High	t_{CH}		13			ns
CLK Pulse-Width Low	t_{CL}		13			ns
$\overline{CS}$ Fall to CLK Rise Time	t_{CSS}	FLTR = low (Note 5)	15			ns
		FLTR = high	260			
SDI Hold Time	t_{DH}		10			ns
SDI Setup Time	t_{DS}		10			ns
Output Data Propagation Delay	t_{DO}	C_L = 10pF. CLK falling-edge to SDO stable			40	ns
SDO Rise-and-Fall Times	t_{FT}			2.5		ns
$\overline{CS}$ Hold Time	t_{CSH}		40			ns
$\overline{CS}$ Pulse-Width High	t_{CSPW}	FLTR = low (Note 5)	20			ns

Note 2: All units are production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 3: Channel-to-channel skew is defined as the difference in propagation delays between channels on the same device with the same polarity.
Note 4: All logic input pins except $\overline{CS}$ have a pulldown resistor. $\overline{CS}$ has a pullup resistor.
Note 5: Specification is guaranteed by design; not production tested.
Note 6: Excludes bond wire resistance.
Note 7: X - means do not care.

ESD Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD	V_{ESD}	OUT_ pins. Contact (Note 8)		±8		kV
		OUT_ pins. Air Discharge		±15		kV
		All other pins. Human Body Model		±2		kV

Note 8: Bypass each V_{DD} pin to AGND with a 1μF capacitor as close as possible to the device for high-ESD protection.

Test Circuits/Timing Diagrams

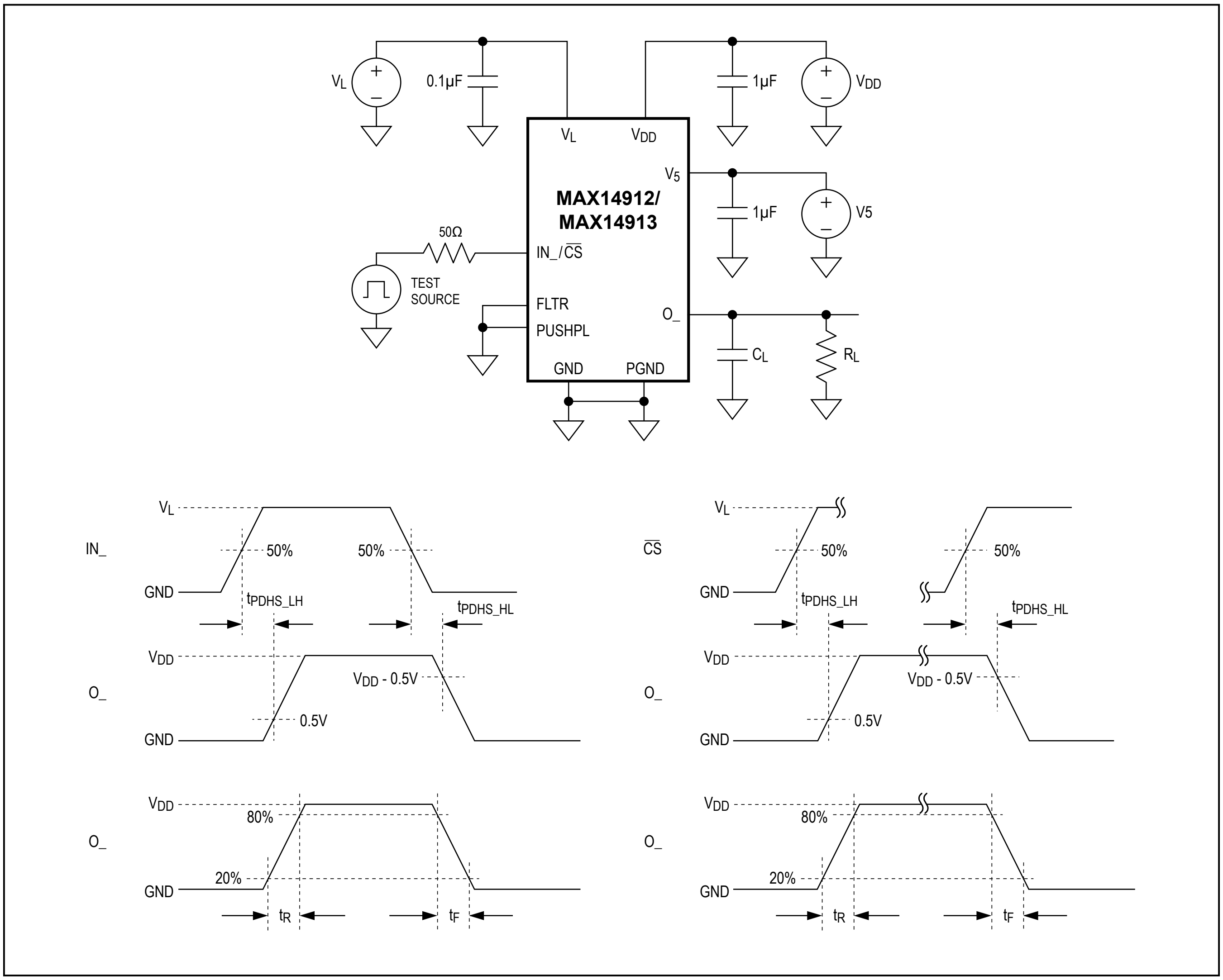


Figure 1. High-Side Mode Timing Characteristics

Test Circuits/Timing Diagrams (continued)

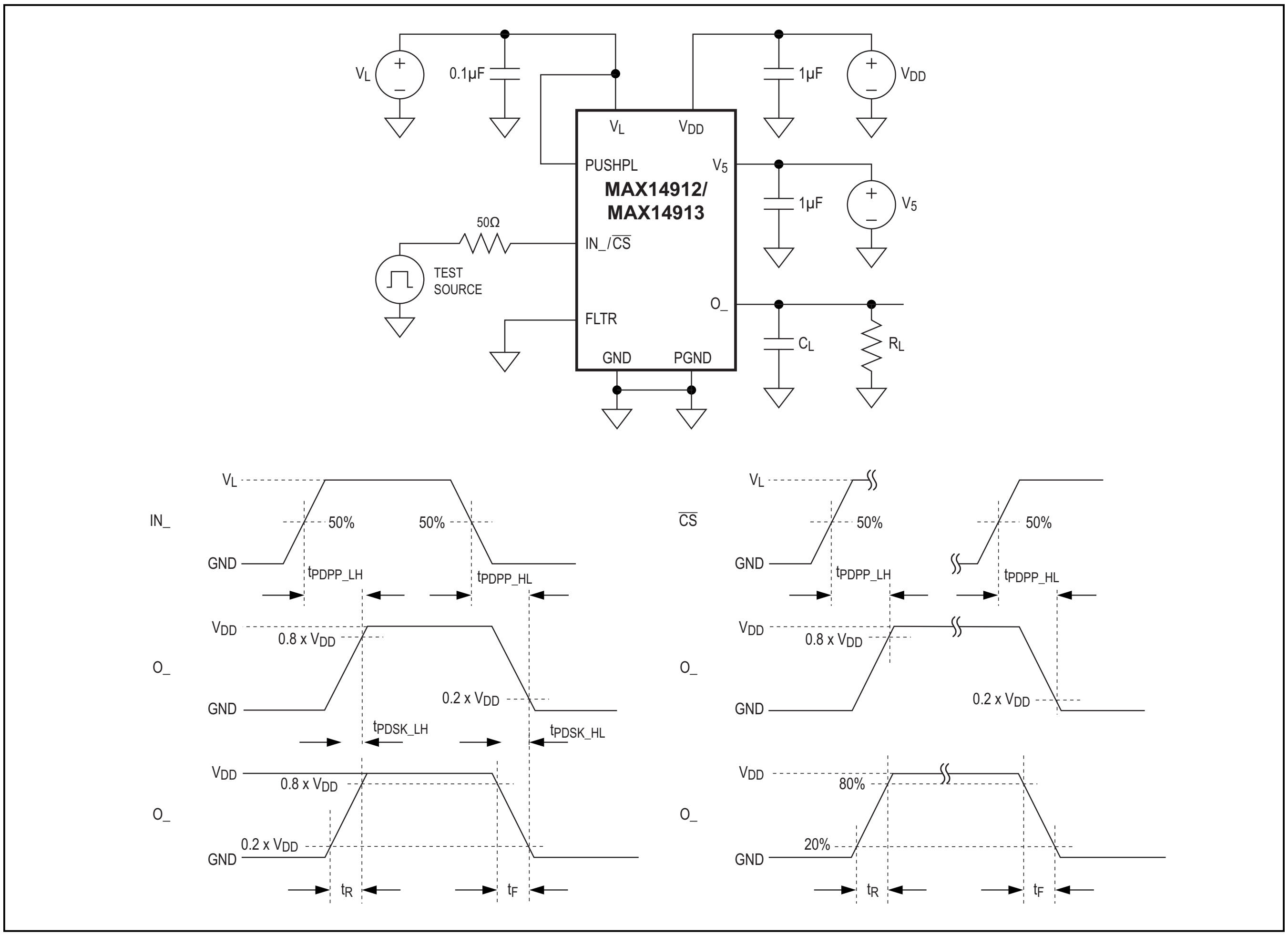


Figure 2. Push-Pull Mode Timing Characteristics

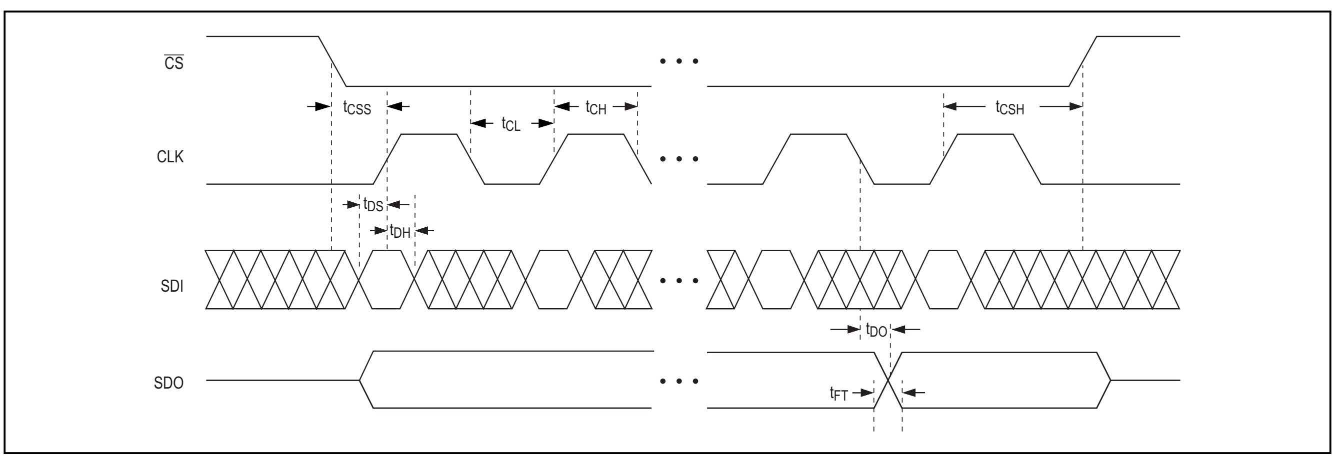
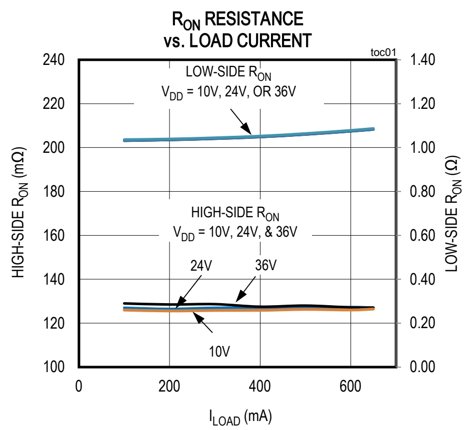
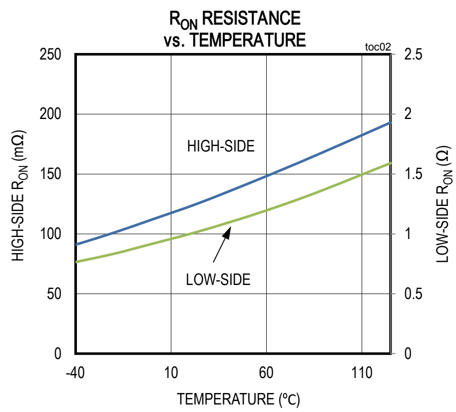


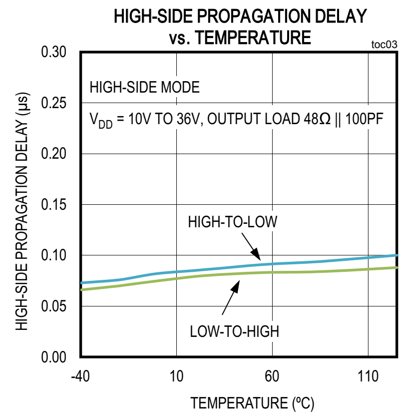
Figure 3. SPI Timing Diagram

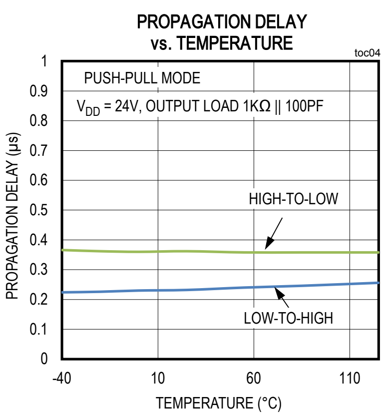
Typical Operating Characteristics

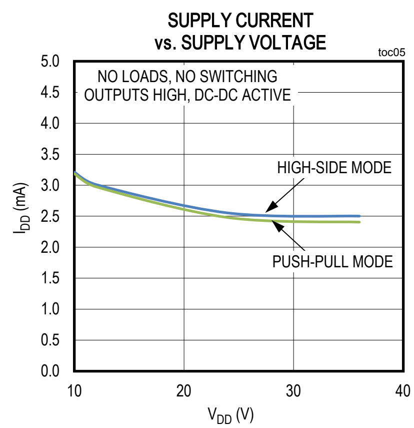
(V_{DD} = 24V; V_5 = 5V, V_L = 3.3V, T_A = +25°C, unless otherwise noted.)

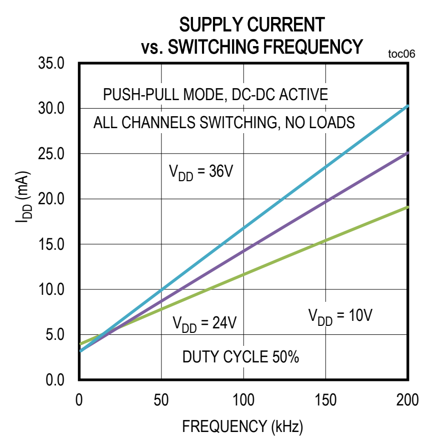


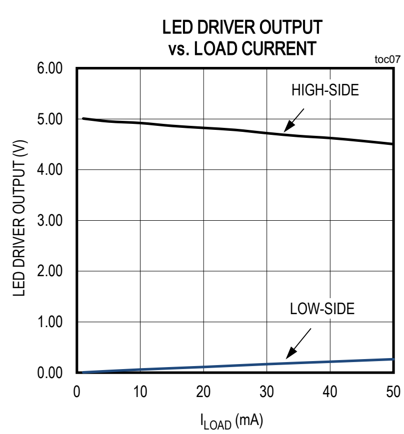




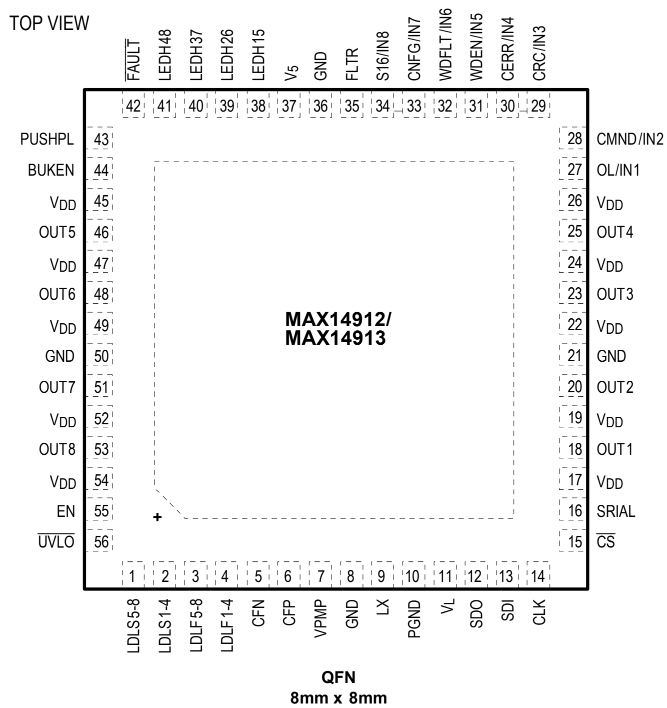








Pin Configuration



Pin Description

PIN	NAME	FUNCTION
LED DRIVERS		
1, 2	LDLS5-8, LDLS1-4	Status LED Cathode Outputs (Open-Drain Low-Side)
3, 4	LDLF5-8, LDLF1-4	Fault LED Cathode Outputs (Open-Drain Low-Side)
38–41	LEDH15, LEDH26, LEDH37, LEDH48	LED Anode Connections (Open-Drain High-Side). Connect a resistor in series to set the diode current.
POWER SUPPLY		
5	CFN	Charge-Pump Flying Capacitor
6	CFP	Charge-Pump Flying Capacitor. Connect a 200nF/50V capacitor to CFN.
7	VPMP	Charge-Pump Output. Connect a 10μF/5V capacitor between VPMP and V_{DD}. VPMP is not intended for use as a power supply for other devices.
8, 21, 36, 50	GND (4x)	Ground. Connect all GND pins together.
9	LX	DC-DC Converter Switching Output. Connect LX to the switching-side of the inductor.

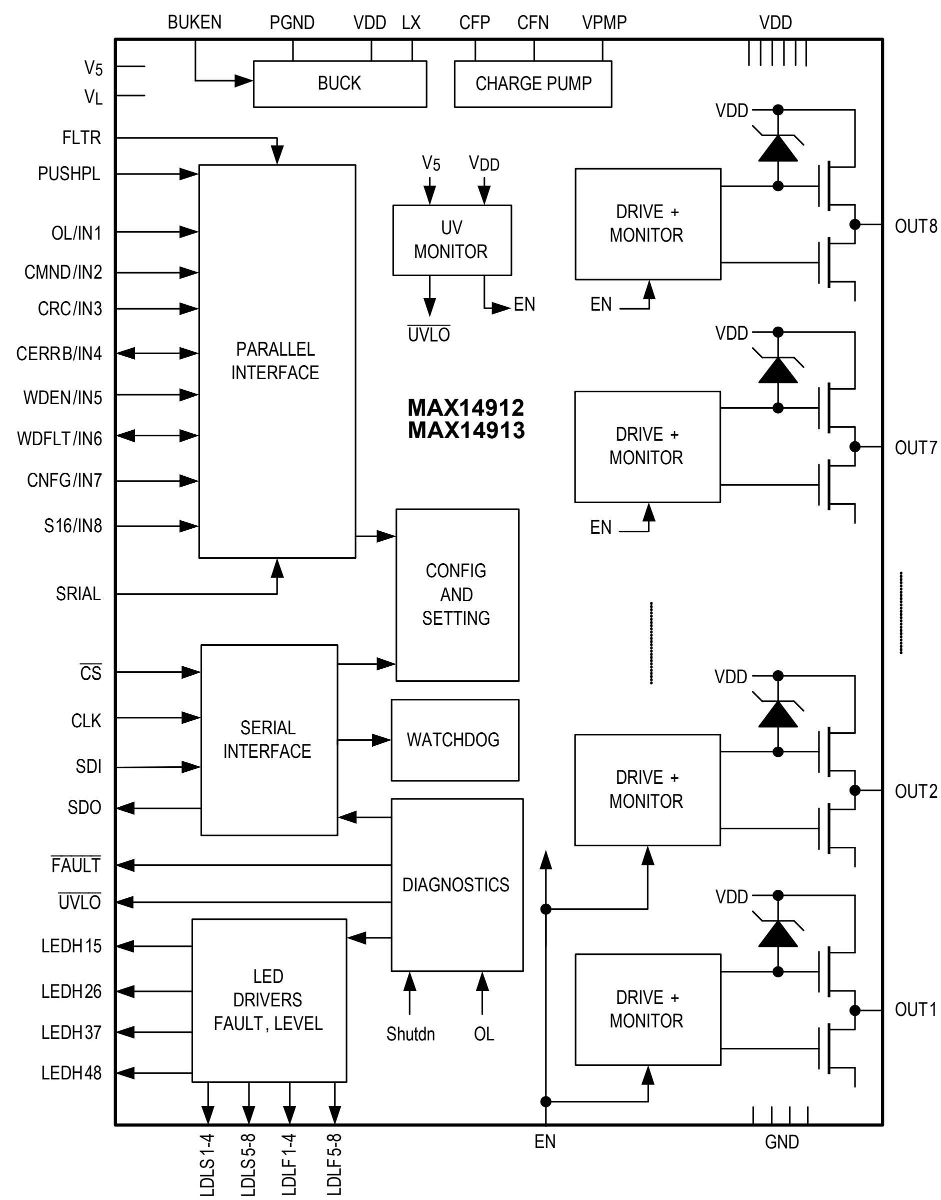
Pin Description (continued)

PIN	NAME	FUNCTION
10	PGND	Ground for the DC-DC Converter. Connect to GND.
11	V_L	Logic Supply Input. V_L defines the levels on all I/O logic interface pins. Bypass V_L to GND through a 100nF ceramic capacitor.
17, 19, 22, 24, 26, 45, 47, 49, 52, 54	V_{DD} (10x)	Supply Voltage, Nominally 24V. Connect all V_{DD} together. Bypass V_{DD} to GND through a 1μF capacitor.
37	V_5	5V Supply Input. V_5 can be powered by an external 5V supply or the internal 5V buck. Bypass V_5 to GND through a 10μF ceramic capacitor.
44	BUKEN	Enable Input for Buck Regulator. BUKEN should be permanently connected to either V_{DD} or GND—do not switch BUKEN. Connect BUKEN to GND if not using the internal buck. Connect BUKEN to V_{DD} to use the internal buck.
56	$\overline{\text{UVLO}}$	$\overline{\text{UVLO}}$ is an Open-Drain, Undervoltage Indicator of the V_{DD} Supply.
SERIAL INTERFACE		
12	SDO	Serial-Data Output. SPI MISO data output to controller.
13	SDI	Serial-Data Input. SPI MOSI data from controller.
14	CLK	Serial-Clock Input from SPI Controller
15	$\overline{\text{CS}}$	Chip-Select Input from Controller
LOGIC INTERFACE		
16	SRIAL	Serial/Parallel Select Input. Drive SRIAL high to set the MAX14912/MAX14913 outputs through the serial interface. Drive SRIAL low to set the MAX14912/MAX14913outputs through the parallel (_/IN) pins. SRIAL does not affect serial readback of diagnostic/status information.
27	OL/IN1	Open-Load Select Input/IN1 Input. In serial mode (SRIAL = high), drive OL/IN1 = high to enable open-load detection on all eight OUT_ outputs when in high-side operation. In parallel mode (SRIAL = low), OL/IN1 sets OUT1 on/off/high/low.
28	CMND/IN2	Command Mode SPI Input/IN2 Logic Input. In serial mode (SRIAL = high), CMND/IN2 enables command-based SPI access (see *Detailed Description* section for details). In parallel mode (SRIAL = low), CMND/IN2 sets OUT2 on/off/high/low.
29	CRC/IN3	CRC Select Input/IN3 Input. In serial mode (SRIAL = high), drive CRC/IN3 = high to enable CRC error detection on serial data. In parallel mode (SRIAL = low), CRC/IN3 sets OUT3 on/off/high/low.
30	CERR/IN4	CRC Error Detection Output/IN4 Input. In serial mode (SRIAL = high) with error checking enabled (CRC/IN3 = high), CERR/IN4 is an open-drain output whose transistor turns on when the device detects an error on SDI data. In parallel mode (SRIAL = low), CERR/IN4 sets OUT4 on/off/high/low.
31	WDEN/IN5	Watchdog Enable Input/ IN5 Input. In serial mode (SRIAL= high), WDEN/IN5 enables the watchdog timer. In parallel mode (SRIAL= low), WDEN/IN5 sets OUT5 on/off/high/low.
32	WDFLT/IN6	Watchdog Fault Output/IN6 Input. In serial mode (SRIAL = high), WDFLT/IN6 is the open-drain watchdog fault output, which turns on when a watchdog fault is detected while WDEN/IN5 is high. In parallel mode (SRIAL = low), WDFLT/IN6 sets OUT6 on/off/high/low.

Pin Description (continued)

PIN	NAME	FUNCTION
33	CNFG/IN7	Configure Input/IN7 Input. In serial mode (SRIAL = high), drive CNFG/IN7 high to enable per-channel configuration through the serial interface. In serial mode, drive CNFG/IN7 low to allow setting the OUT_ outputs through the serial interface. In parallel mode (SRIAL = low), CNFG/IN7 sets OUT7 on/off/high/low.
34	S16/IN8	16-Bit Serial Select/IN8 Input. In serial mode (SRIAL = high), drive S16/IN8 high to select 16-bit serial-interface operation. Drive S16/IN8 low in serial mode for 8-bit serial operation. In parallel mode (SRIAL = low), S16/IN8 sets OUT8 on/off/high/low.
35	FLTR	Glitch Filter Enable Input. Set FLTR high to enable glitch filtering on all parallel logic inputs and $\overline{CS}$.
42	$\overline{FAULT}$	Open-Drain Fault Output. The $\overline{FAULT}$ transistor turns on low when a fault condition (driver shutdown or open-load detect) occurs.
43	PUSHPL	Push-Pull, High Slew-Rate Configuration Input. When PUSHPL is set high, all OUT_ pins operate in push-pull mode. When PUSHPL is set low, all OUT_ pins operate in high-side mode.
55	EN	Output Enable Input. Driving EN low turns all high-side OUT_ switches off, and three-states all push-pull OUT_ drivers and turns all LED drivers off. Driving EN high enables normal operation.
SWITCH/DRIVER OUTPUTS		
18, 20, 23, 25, 46, 48, 51, 53	OUT1–OUT8	Driver Output N. May be configured as a high-side switch or push-pull output.

Functional (or Block) Diagram



Detailed Description

High-Side Mode

The high-side drivers (HS) have 230mΩ (max) on-resistance when sourcing 500mA at T_A = +125°C. The OUT_ output voltage can go below ground, as can occur during inductive load turn-off/demagnetization. Internal clamping diodes limit the negative excursion to (V_{DD} - V_{CL}) and allow free-wheeling currents to demagnetize the inductive loads quickly.

Low-side transistors (LS) can be switched in to provide push-pull operation. Fast discharge of ground-connected RC loads is achieved by push-pull drive. In push-pull mode, the OUT_ outputs are clamped to GND.

Output Parallelization

The devices support paralleling of channels in high-side mode to provide higher current. The channels can be paired (1-2, 3-4, 5-6, and 7-8) by setting two bits of the SPI register 3: joinUP and joinDW (see Table 6).

When joinDW = 1, OUT1 and OUT2 are connected together, and OUT3 and OUT4 are connected together, and:

- Input signals related to channels 2 and 4 are neglected;
- Output status is determined by inputs 1 and 3;
- Push-pull mode is disabled.

When joinUP = 1, OUT5 and OUT6 are connected together, and OUT7 and OUT8 are connected together, and:

- Input signals related to channels 6 and 8 are neglected;
- Output status is determined by inputs 5 and 7;
- Push-pull mode is disabled.

The above configuration can be used without any additional external zener clamping.

Besides pairing of drivers through internal configuration, multiple OUTs can be operated in parallel by tying the OUT_ together and driving the inputs simultaneously. In this case, an external zener clamp is required per output set for quenching the energy during inductive load turn-off. The external clamp voltage of this zener diode must be lower than the minimum internal clamp voltage (V_{CL} (min)). The reason is that there is channel-to-channel variation between the internal clamp voltages. Without an external zener diode, during turn-off of channels connected in parallel, the internal clamp with the lowest clamp voltage turns on and dissipates all the energy.

Channel diagnostics for fault detection remains independent in case of paralleling the outputs.

Open-Load/Wire Detection

Detection of an open-load condition can be enabled on a per-channel basis through serial configuration, or globally in serial mode through the OL/IN1 input. Open-load detection works in high-side mode only. It operates with the HS driver either on or off.

When the HS switch is off, a current source is enabled, which pulls OUT_ to V_{DD} when the wire is open. If the OUT_ voltage is above V_{OL_T}, an open load is signaled.

When the HS switch is on, the voltage across the HS switch is monitored. If this drop is below a load current of I_{OL_HSON}, an open-load fault is reported.

The switch input state and the load condition must both be stable for at least t_{DEB_OL} to get a reliable reading.

When an open-load condition is detected on an output:

1) The F_ bit is set for that output in the serial diagnostic data.
2) The fault LED is turned on for at least 200ms for that channel.
3) The open-drain global $\overline{\text{FAULT}}$ transistor is turned on for at least 200ms.

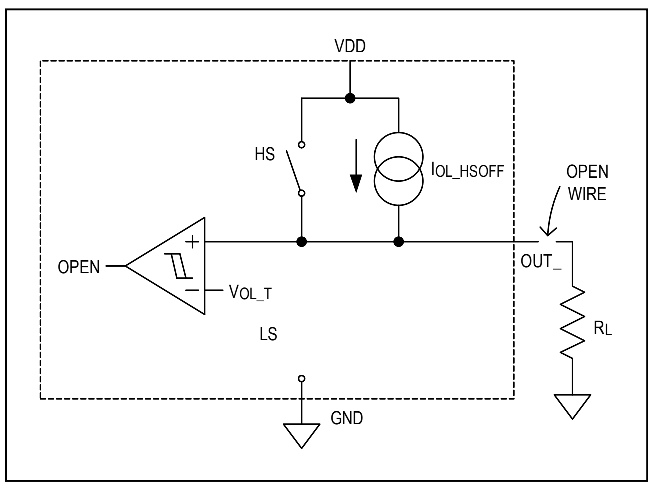


Figure 4. Open-Wire Load Detection

Watchdog

The watchdog timer allows monitoring activity on the $\overline{CS}$ input in serial mode (SRIAL = high). Drive WDEN/IN5 high to enable the watchdog function. The watchdog monitors and expects activity on the $\overline{CS}$ input. The WD timer is reset at every $\overline{CS}$ falling edge. If the timer is not reset after the timeout delay, see Table 8), all OUT_ outputs are turned off and the watchdog fault output (WDFLTB/IN6) transitions low until the next $\overline{CS}$ falling edge.

The watchdog timeout can be selected in SPI command mode (see the *Configuration and Monitoring* section). Bits selection in Register 3: WD[1:0] = 00 for 0.9s, WD[1:0] = 01 for 0.45s and WD[1:0] = 10 for 0.15s. The default value is 0.9s.

Thermal Management

Every driver's temperature is constantly monitored while V_{DD} > V_{DD_UV}. If the temperature of a driver rises above the thermal-shutdown threshold of T_{JSHDN}, that channel is automatically turned off for protection. The drivers are turned on again once the temperature drops by a hysteresis margin of T_{JSHDN_HYST}.

Both high and low-side drivers are thermally protected with a per-driver protection circuit.

When a driver turns off due to thermal shutdown:

1) A fault is indicated through the global $\overline{FAULT}$ output.
2) The F_ bit of that channel is set in the diagnostic byte in the SPI interface.
3) The fault LED driver turns on for that channel.

The device also has a chip thermal shutdown that triggers a $\overline{FAULT}$ output and all the channels shut down if the temperature rises above T_{CSHDN}.

Overcurrent and Short-Circuit Protection

In the event of a short-circuit or high current at an OUT_ output, the load current is limited on a per-channel basis to I_{LIM_HS} for the high-side (HS) driver and to I_{LIM_PP} for the low-side (LS) driver. Additionally, when a short circuit is detected, the affected OUT_ output is put in a safe slow-mode in order to prevent damages in case its IN_ input is switching at a high frequency. In order to restore normal operation, the IN_ input of the affected channel has to be kept low for at least 20ms. While in slow-mode, the low-to-high and high-to-low transitions at OUT_ are slew-rate limited to around 3V/µs. A short-circuit or overcurrent generally creates a temperature rise in the chip; both the HS and LS FETs' temperatures are continuously monitored. When any switch temperature exceeds T_{JSHDN}, the corresponding OUT_ output is put in a high-impedance state until the temperature falls by the hysteresis.

If the case temperature is below T_{CSHDN}, a short circuit on one output will allow the other outputs to operate normally.

The HS current-limit circuit features a controlled dV/dI slope that improves stability with inductive loads. In other words, the current is limited to a nonconstant value that increases with (V_{DD} - V_{OUT}) with a slope of 1A/150V.

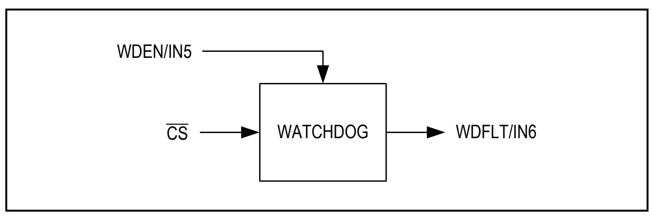


Figure 5. Watchdog Timer

Undervoltage Lockout

When the V_L, V_{DD}, or V_5 supply voltages are under their respective UVLO thresholds, all OUT_ outputs are turned off (three-stated) and the open-load detect current sources are turned off; they automatically turn back on once the V_{DD}/V_5 rises to above the UVLO thresholds.

Undervoltage conditions can be read out through SPI.

The UVLO open-drain output pin indicates whether V_{DD} is below the V_{DD_UV} threshold.

LED Drivers

The 4 x 4 LED driver crossbar matrix offers a pin-optimized configuration for driving 16 LEDs. Per-channel output status and the fault conditions are indicated by individual LEDs. If a FAULT LED is turned on for an output, the corresponding LEVEL LED is always turned off. This mitigates false information about the status of the affected OUT_ pin.

For every current-limiting resistor (R), each of the four LEDs in the vertical string are pulsed so that current only flows through one LED at any given time. Therefore, the resistors (R) determine the LED current through one LED and should be chosen according to the LED's current/light-intensity requirements. Every LED that is on, is pulsed on with a 25% duty cycle.

Configuration and Monitoring

The MAX14912/MAX14913 can be configured, set, and monitored through either a parallel or serial interface. The serial interface allows greater configuration flexibility and provides more monitoring information. For the MAX14913, in parallel setting mode (SRIAL = low), the SPI cannot be used for configuring the device, SPI is only available for monitoring.

Global Configuration

Pin-based configuration does not require the use of the SPI interface. It is global and allows for the configuration of all OUT_ as high-side outputs, push-pull outputs, and enables open-load detection. See Table 1 for details.

In cases where configuration is possible through the parallel and/or serial interface, Table 2 documents the priority.

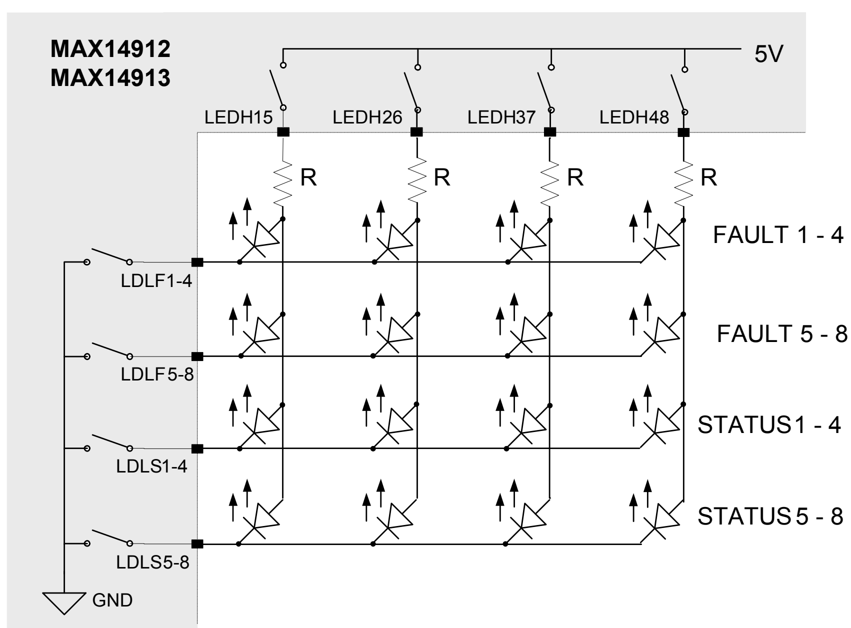


Figure 6. LED Output Status and Fault-Detection Matrix

Table 1. Global Configuration Pins

INPUT	SRIAL	CONFIGURATION
PUSHPL	X	Configures all OUT_ outputs as push-pull or high-side. 0 = All drivers in high-side mode unless configured as push-pull by serial interface. 1 = All drivers in push-pull mode.
OL/IN1	1	Enables global open-load detection in serial mode. 0 = Open-load detection disabled unless enabled by serial interface. 1 = Open-load detection enabled for all high-side mode switches.
CRC/IN3	1	Enables CRC generation and error detection on the serial interface. 0 = CRC error detection disabled. 1 = CRC error detection enabled.
FLTR	X	Enables anti-glitch filtering on all logic input pins except SDI and CLK. (Note 1) 0 = Glitch filtering disabled. 1 = Glitch filtering enabled.
WDEN/IN5	1	Enables watchdog on the SPI interface. 0 = Watchdog disabled. 1 = Watchdog enabled.

Note 1: PUSHPL and SRIAL are always filtered, independent of FLTR logic.

Table 2. Configuration Priority

CONFIGURATION	SRIAL	PRIORITY	
Push-Pull/ High-Side	1	**PUSHPL**	**RESULT**
		Low	OUT_ drivers in high-side mode, unless configured individually as push-pull through the serial interface.
		High	All OUT_ drivers in push-pull mode, independent of serial configuration.
Open-Load Detection	1	**OL/IN1**	**RESULT**
		Low	Open-load detection off, unless configured individually through the serial interface.
		High	Open-load detection enabled on all OUT_ outputs that operate in high-side mode.

Parallel Interface: Setting the OUT_ Output Driver

The parallel mode (SRIAL = low) uses one input pin (IN_) to set each output (OUT_). Table 3 shows the settings that depend on the configured mode.

In parallel setting mode (SRIAL = low), the MAX14913 can only be configured via the global configuration inputs: PUSHPL and FLTR, not on a per-channel basis through SPI. This means that all high-side drivers are either in high-side or push-pull operation. Open-load detection is enabled and cannot be disabled in parallel setting mode.

The MAX14912 can be configured with full flexibility in parallel setting mode.

Serial Controller Interface

The serial interface can be used in all setting modes. It is based on CPOL = low and CPHA = low, meaning that the SDI data is latched-in on the rising edge of CLK and new SDO data is written on the falling edge of CLK. The default idle CLK state needs to be low. The SDO output is only actively driven when the SPI master drives $\overline{CS}$ low, it is otherwise weakly pulled down by an internal 200kΩ resistor when $\overline{CS}$ is high.

Table 3. SRIAL = Low

DRIVER MODE	IN_	OUT_ STATE
High-Side	0	High-side off
High-Side	1	High-side on
Push-Pull	0	Push-pull output low
Push-Pull	1	Push-pull output high

The SPI interface provides per channel and detailed global diagnostics. In serial setting mode (SRIAL = high), the outputs are set on/off/high/low by the serial interface. Serial mode also allows per channel and global configuration. In parallel setting mode (SRIAL = low), the MAX14913 does not allow configuration through SPI, while the MAX1912 can be configured per channel and globally.

The SPI interface can be operated in either command mode or direct mode. Command mode is available in both parallel and serial modes and provides higher information content and supports more configuration options. See Table 4 for details. Direct mode SPI is only available in serial setting mode (SRIAL = high). In direct SPI mode, output setting and per channel configuration is written directly (without a command byte) and diagnostics data is provided either in an 8 or 16-bit SPI cycle.

In both command and direct SPI modes, when the high-side/push-pull drivers are set on/off/high/low via SPI, the outputs change state at the end of the SPI cycle, on the rising $\overline{CS}$ edge, with a sub 1µs propagation delay, as defined in the Electrical Properties Table. In direct and command mode SPI, diagnostic and status information is sampled at the beginning of each SPI cycle, initiated by the falling $\overline{CS}$ edge and is then sequentially written out on SDO on each falling CLK edge. Command SPI mode allows reading back the chip configuration and status and diagnostics, as selected via the command byte. This information is then written out on the following SPI cycle.

Table 4. SPI interface Modes Selection and Description

PIN					RESULT			
SPI MODE	SRIAL	CMND /IN2	CNFG /IN7	S16 /IN8	BITS	SDI	SDO	NOTES
DIRECT SPI 8-BIT/16-BIT OPERATION	1	0	0	0	8	Per-channel OUT_ setting	Per-channel fault	OUT set by SPI. FAULT is the real-time status of the fault (driver shutdown or open-load)
				1	16	Per-channel OUT_ setting and HS/PP selection	Per-channel fault and level	
	1	0	1	0	8	Per-channel config: HS/PP	Per-channel fault	OUT level does not change
				1	16	Per-channel config: HS/PP and OL detection on/off	Per-channel fault and level	
COMMAND MODE	1	1	X	X	16	8-bit-command + 8-bit data	Previous command output	OUT level may or may not change depending on command
	0	X	X	X	16	8-bit-command + 8-bit data	Previous command output	OUT set by INx pins. MAX14912 allows SPI configuration. MAX14913 does not allow SPI configuration.

Daisy-Chain SPI Operation

The device supports daisy-chain operation, allowing control/monitoring of multiple MAX14912/MAX14913 devices from a single serial interface with one common chip-select signal. The identical data that is clocked into SDI, is clocked out of SDO with a one SPI cycle delay. This is illustrated in Figure 8.

Direct SPI Serial Interface: 8-bit Mode

SRIAL = high, CMND = low, S16 = low.

Figure 9 shows an 8-bit cycle that reads the per-channel diagnostic data and sets/configures the outputs in a single 8-bit cycle. Table 5 illustrates the meaning of the SPI bits.

The data returned on SDO is the per-channel fault status.

Pin CNFG is used to select whether the SDI input bits set the output level or the output mode (high-side or push-pull).

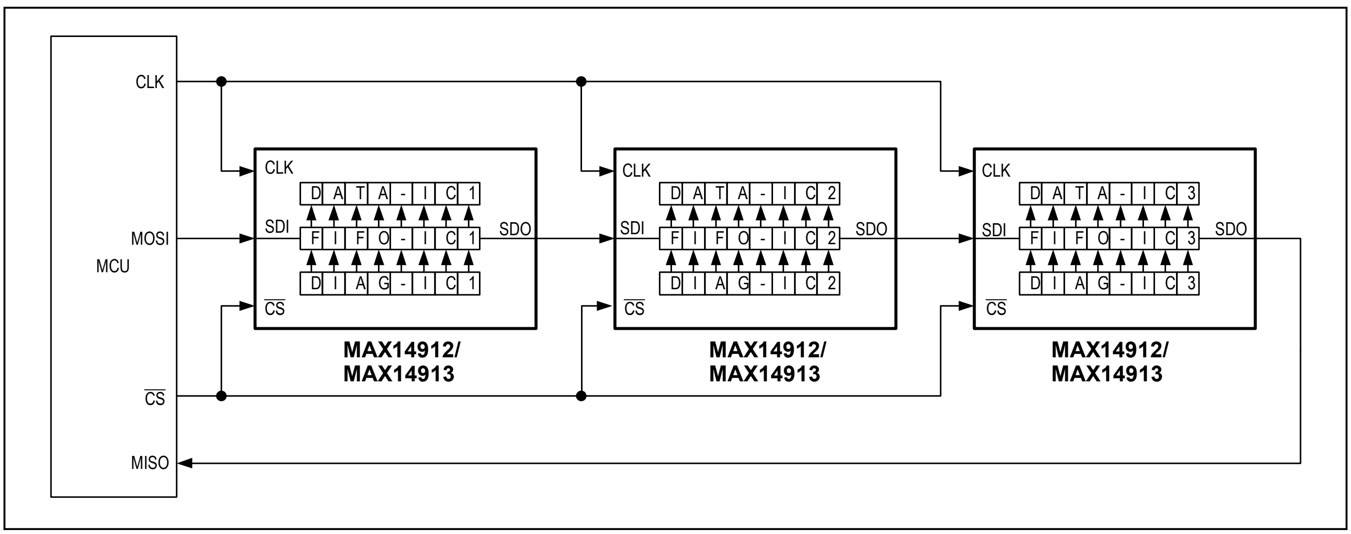


Figure 7. Daisy-Chain Connection

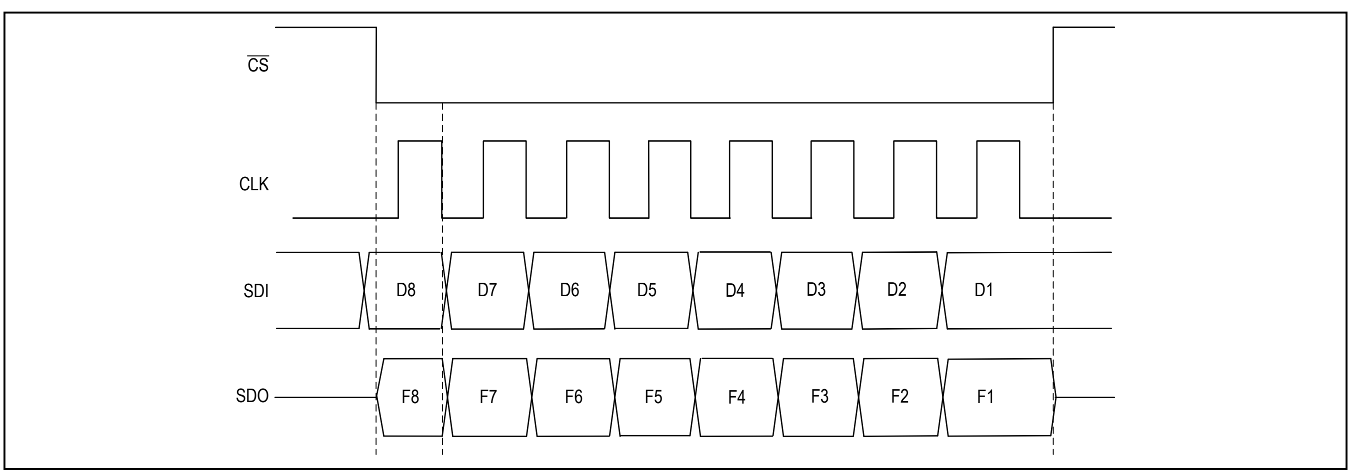


Figure 8. SPI Cycle in 8-Bit Direct SPI Mode

Direct SPI Serial Interface: 16-Bit Mode

SRIAL = High, CMND = Low, S16 = High

Figure 9 shows a 16-bit read/write cycle that reads the per-channel diagnostic data and configures/sets the outputs in a single 16-bit cycle.

The data returned on SDO is the per-channel fault status.

The CNFG pin is used to select whether the input bits sent to SDI set the output level or the output mode (high-side or push-pull). Moreover, in 16-bit mode, the open-load detection can be enabled on a per-channel basis.

Table 5. 8-Bit SPI Direct Mode Bit Definition

BIT	BIT VALUE	CNFG	DEFINITION
D_	0	Low	In high-side mode: set HS off In push-pull mode: HS off, LS on
	1	Low	In high-side mode: set HS switch on In push-pull mode: set HS switch on, LS off
	0	High	Configure high-side mode
	1	High	Configure push-pull mode
F_	0	X	No fault
	1	X	Fault (thermal protection or open load

Table 6. 16-Bit SPI Direct Mode Bit Definition

BIT	BIT VALUE	CNFG	DEFINITION
D_	0	Low	In high-side mode: HS off, LS off In push-pull mode: HS off, LS on
	1	Low	HS on, LS off
C_	0	Low	High-side mode
	1	Low	Push-pull mode
D_C_	00	High	High-side mode; open-load detection defined by OL/IN1 pin
	01	High	Push-pull mode
	10	High	High-side mode with open-load detection
	11	High	*Not used*
F_	0	X	No fault
	1	X	Fault status (thermal protection or open-load)
L_	0	X	Output level < 7V
	1	X	Output level > 7V

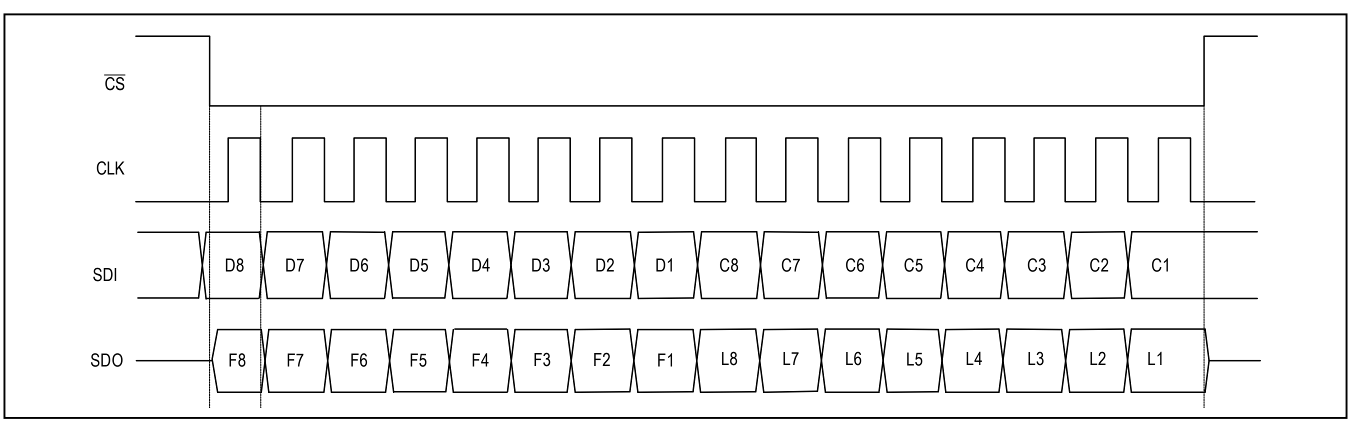


Figure 9. SPI Cycle in 16-Bit Direct SPI Mode

Command Mode SPI

CMND = High

In serial setting mode (SRIAL = high), command SPI mode allows setting, configuration and monitoring. In parallel setting mode (SRIAL = low) command mode allows monitoring. While the MAX14912 supports SPI configuration in parallel mode, configuration is not supported in the MAX14913. In command mode, the input is always a command + data word; pins CNFG, S16, and OL are ignored. The output word returns the information requested during the previous SPI cycle.

Table 7 lists the registers accessible in command mode, while Table 8 lists the commands and their effect.

In command mode, a latched version of all faults is available. In other words, the device keeps any fault in memory until the user decides to clear the fault registers. Each bit of fault registers 4, 5, and 6 is set as soon as its corresponding real-time fault signal goes high. At the end of any SPI cycle during which the SDI MSB (the Z bit) has been set to 1, all fault registers are cleared at once (see Table 8). If [SRIAL = high and CMND = high], the global $\overline{\text{FAULT}}$ signal is latched as well (see Table 9 for more details on the global $\overline{\text{FAULT}}$ signal). Otherwise, it is a real-time global fault status.

In command mode, both the latched and the real-time faults can be read out. All commands except #4 returns the same real-time data as in the 16-bit mode. Command #4 can be used to read any register and, for fault registers 4, 5, and 6, it returns both the latched and real-time value of any fault signal.

Table 7. SPI REGISTERS (Accessible Only in COMMAND Mode)

REG	R/W	PURPOSE	7	6	5	4	3	2	1	0
0	R/W	Switch/Driver Settings (Note 10)	IN8	IN7	IN6	IN5	IN4	IN3	IN2	IN1
		Default	0	0	0	0	0	0	0	0
1	R/W	Push-Pull/High-Side Configuration (Note 11)	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1
		Default	0	0	0	0	0	0	0	0
2	R/W	Open Load Detect Enable (Note 11)	OL_EN8	OL_EN7	OL_EN6	OL_EN5	OL_EN4	OL_EN3	OL_EN2	OL_EN1
		Default	0	0	0	0	0	0	0	0
3	R/W	Watchdog Config. And Channel Paralleling (Note 11)	—	—	—	—	joinUP	joinDW	WD1	WD0
		Default	0	0	0	0	0	0	0	0
4	R	Per-Channel Open-Load Condition	OL8*	OL7*	OL6*	OL5*	OL4*	OL3*	OL2*	OL1*
5	R	Per-Channel Thermal Shutdown	THSD8*	THSD7*	THSD6*	THSD5*	THSD4*	THSD3*	THSD2*	THSD1*
6	R	Global Faults	WDfault	CRCfault	DCDC Current-Limit	8CKmult Error*	THSDglob*	5V UVLO	V_{DD} UVLO	V_{DD} WARN
7	R	OUT Overvoltage Detection (Note 9)	OV8	OV7	OV6	OV5	OV4	OV3	OV2	OV1

Note 9: Bits are set when the OUT_ voltage is higher than V_{DD}. These bits are real-time.

Note 10: Register 0 can be written to, but will not change the output states in Parallel (SRIAL = low) setting mode, since the outputs are then only set through the IN_ pins.

Note 11: Registers 1, 2, 3 can be written to in the MAX14913, but will not change the configuration in Parallel (SRIAL = low) setting mode.

* Faults are stretched in time to a minimum duration of 200ms.

Table 8. COMMAND MODE Protocol

COMMAND NO.	FUNCTION	SDI		SDO VALID ON NEXT CYCLE	COMMENT
		COMMAND	DATA		
0	Set OUT State (Reg 0) (Note 15)	Z0000000	DDDDDDDD	FFFFFFFF.LLLLLLLL	D = 0 : HS off; LS on (in PP) D = 1 : HS on; LS off L: Output Level F: Fault (Real-Time)[12] Z = 1: Clear Fault Registers[13]
1	Set HS/PP Mode (Reg 1) (Note 16)	Z0000001	DDDDDDDD	FFFFFFFF.LLLLLLLL	D = 0 : HS Mode D = 1 : PP Mode
2	Set OL Detection (Reg 2) (Note 16)	Z0000010	DDDDDDDD	FFFFFFFF.LLLLLLLL	D = 0 : OL Detection Off D = 1 : OL Detection On (HS Mode)
3	Set Configuration (Reg 3) (Note 16)	Z0000011	0000JJAB	FFFFFFFF.LLLLLLLL	AB: Watchdog 00 = 0.90s 01 = 0.45s 10 = 0.15s J = 1: Channels are Coupled (PP Disabled)
4	Read Register (Note 14)	Z0100000	00000NNN	AAAAAAAA.QQQQQQQQ	NNN = 0,1,2,3: Q = Reg value, A = 0 NNN = 4,5,6: Q = Reg value, A = Real_time NNN = 7: Q = 0, A = Real_time
5	Read Real-Time Status (Note 12)	Z0110000	—	FFFFFFFF.LLLLLLLL	F-L Status Readout (Real-Time). No Data is Written

Note 12: F bits are the logical OR of thermal protection and open-load detection real-time signals.

Note 13: Any fault bit inside registers 4, 5, and 6 are set as soon as its corresponding event happens. All fault registers are cleared only by setting Z = 1 (this is possible during any command cycle). The registers get cleared at $\overline{CS}$ rising edge. If Z = 1 the registers are not cleared in case of SPI communication error (CRC, 8-CK).
If SRIAL = 1 and CMND = 1, the Z bit clears also the $\overline{FAULT}$ IRQ signal.

Note 14: The Q bits are the value of the fault registers (that need to be cleared by means of the Z bit).
The A bits are the corresponding real-time values (i.e., the real-time fault signals). The real-time values are stretched by 200ms. Therefore, they have a time resolution of ~200ms.

Note 15: In parallel setting mode (SRIAL = low), writing to this registers does not change the real-time values or settings. These can only be changed through pins.

Note 16: For the MAX14913 only, in parallel setting mode (SRIAL = low), writing to these registers does not change the configuration.