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MAX15068

Dual ORing, Single Hot-Swap Controller with Accurate Current Monitoring

General Description

The MAX15068 offers ORing function and hot-swap features for two input-supply-rail applications requiring the safe insertion and removal of circuit line cards from a live backplane. The device integrates dual ORing MOSFET controllers, a single hot-swap controller, electronic circuit-breaker protection, and power monitoring in a single package. The device is designed to operate from 2.9V to 18V supply voltages.

The device regulates the forward voltage drop across the ORing MOSFETs to ensure smooth current transfer from one supply to the other without oscillation. The ORing MOSFET turns on quickly to reduce the load voltage drop during supply switchover. If the input supply fails or is shorted, a fast turn-off minimizes reverse-current transients.

The device implements a foldback current limit during hot-swap startup in order to control inrush current, thereby lowering di/dt and keeping the operation of the hot-swap MOSFET under safe operating area (SOA). An internal 70ms timer starts counting when the device enters the hot-swap startup phase. After the hot-swap startup cycle is completed, on-chip comparators provide active current-limit protection against short-circuit and overcurrent faults. The load is disconnected from the input quickly in the event of a fault condition.

The device provides current monitoring from 3A to 8A (V_{IN} = 12V, T_A = +25°C with R_{SENSE} = 3mΩ) with ±0.5% accuracy. A voltage proportional to the input current delivered to the system could be read directly at the IPMON pin.

The device is factory-calibrated to deliver accurate overcurrent protection with ±5% accuracy. During an overcurrent-fault condition, the device enters an autoretry mode. The device features an adjustable slew-rate control during startup. Additional features include power-good and fault-indicator outputs.

The MAX15068 is available in a 20-pin, (4mm x 5mm) TQFN package and is specified from a -40°C to +125°C operating temperature range.

Benefits and Features

- 2.9V to 18V Operating Voltage Range (ORing and Hot Swap)
- 4.8V to 18V Operating Voltage Range (Current Monitor)
- Seamless Power Transition of Redundant Supplies
- Controls n-Channel MOSFETs
- < 0.5µs Reverse Turn-Off Time
- ±0.5% Current Monitoring (Typ)
- Programmable Slew-Rate Control
- Adjustable Current-Limit Fault Delay
- Programmable Circuit-Breaker Current Threshold
- Inrush Current Regulated at Startup with Programmable SOA Control
- Programmable Undervoltage Lockout
- Small (4mm x 5mm) TQFN Package

Applications

- Baseband Station
- Redundant Power Supplies
- Supply Holdup
- Computer Systems and Servers
- Telecom Networks
- Storage Bridge Bay

Ordering Information ***appears at end of data sheet.***

19-6872; Rev 1; 2/16

maxim integrated™

Absolute Maximum Ratings

IN1, IN2 to GND .....-1V to +24V
$\overline{PG}$, $\overline{EN}$, $\overline{FAULT}$, CSN to GND .....-0.3V to +24V
CSP to GND .....Max (-0.3V, $V_{IN\_}$ - 0.6V) to +24V
V_S to GND .....-0.3V to +6V
ON, $\overline{PC}$, IPMON, CB, CDLY to GND .....-0.3V to (V_S + 0.3V)
CSP to CSN .....-0.3V to +0.3V
OUT to GND .....-0.3V to +24V
GATE to GND .....-0.3V to +36V
GATE to OUT .....-0.3V to +20V
CP1 to GND .....-0.3V to +36V
CP1 to IN1 .....-0.3V to +14V
CP2 to GND .....-0.3V to +36V
CP2 to IN2 .....-0.3V to +14V
OG1 .....(V_{IN1} - 0.3V) to (V_{CP1} + 0.3V)
OG2 .....(V_{IN2} - 0.3V) to (V_{CP2} + 0.3V)
Current into $\overline{EN}$, $\overline{PG}$, $\overline{FAULT}$ 20mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin TQFN (derate 30mW/ºC above +70°C) 2400mW
Operating Temperature Range ..... -40°C to +125°C
Junction Temperature .....+150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....33.5°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN1} = V_{IN2} = 12V, C_{IN1} = C_{IN2} = C_{VS} = 1µF, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE						
Input Supply Voltage	V_{IN}	Hot swap and ORing	2.9		18	V
		Current monitor	4.8		18	
Input Supply Current	I_{IN}			4		mA
Internal LDO Output Voltage	V_S		4.8	5	5.25	V
V_S Undervoltage Lockout	V_{UVLO}	V_S rising	2.5	2.65	2.8	V
V_S Undervoltage-Lockout Hysteresis	V_{UVLO_HYS}			0.07		V
CSP Undervoltage Lockout	V_{CSP_UVLO}	V_{CSP} rising	2.4	2.49	2.58	V
		V_{CSP} falling	2.25	2.35	2.42	
ORING						
ORing MOSFET Forward Regulation Voltage ($V_{IN\_}$ - V_{CSP})	V_{FWD_REG}		7.5	10	12.5	mV
ORing MOSFET Reverse Bias Turn-Off Voltage	V_{REV_OFF}	$V_{IN\_}$ - V_{CSP}, V_{CSP} rising (V_{CSP} > $V_{IN\_}$), $V_{OG\_}$ goes low	-25	-20	-15	mV
ORing MOSFET Reverse Bias Turn-On Voltage	V_{REV_ON}	$V_{IN\_}$ - V_{CSP}, V_{CSP} falling, ($V_{IN\_}$ > $V_{CSP\_}$), $V_{OG\_}$ goes to forward regulation	-20	-15	-10	mV
ORing MOSFET Reverse Bias Hysteresis Voltage	V_{REV_HYS}	V_{REV_OFF} - V_{REV_ON}		5		mV

Electrical Characteristics (continued)

(V_{IN1} = V_{IN2} = 12V, C_{IN1} = C_{IN2} = C_{VS} = 1µF, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Turn-Off Switch Resistance	R_{DS_OFF}	$V_{IN\_}$ - V_{CSP} = -50mV, I = 50mA			0.8		Ω
Turn-On Switch Resistance	R_{DS_ON}	$V_{IN\_}$ - $V_{CSP\_}$ = 120mV, I = 70mA			2		Ω
ORing MOSFET Gate Drive ($V_{OG\_}$ - $V_{IN\_}$)	$V_{OG\_}$	2.9V < $V_{IN\_}$ < 18V		5.2	11	12	V
ORing MOSFET Fast Turn-On Threshold	V_{FWD_ON}	$V_{IN\_}$ - V_{CSP} rising			80		mV
ORing MOSFET Fast Turn-Off	V_{FWD_OFF}	$V_{IN\_}$ - V_{CSP} falling, $V_{OG\_}$ goes to forward regulation			40		mV
ORing MOSFET Turn-On Delay	$t_{ON\_OG\_}$	C_{GATE} = 10nF, $V_{IN\_}$ - V_{CSP} = +0.05V			20		µs
ORing MOSFET Turn-Off Delay	$t_{OFF\_OG\_}$	C_{GATE} = 10nF, $V_{IN\_}$ - V_{CSP} = -0.05V, $V_{OG\_}$ = 0.1 x ($V_{CP\_}$ - $V_{IN\_}$)			300	500	ns
$\overline{PC}$ to OG2 Delay	t_{LH_DLY}	$V_{\overline{PC}}$ falling edge to V_{OG2} going high			40	65	µs
HOT SWAP							
Circuit-Breaker Accuracy	V_{CB_TH}	V_{CSP} - V_{CSN}	V_{CB} = 0V	32.9	35	37.1	mV
			V_{CB} = Hi-Z	47.5	50	52.5	
			V_{CB} = V_S	61.1	65	68.9	
Active Current-Limit Sense Voltage	V_{ACL}				1.3 x V_{CB_TH}		mV
Fast Comparator Threshold	V_{FC_TH}	V_{CSP} - V_{CSN}			3 x V_{CB_TH}		mV
Fast Comparator Response Time	t_{FC_DLY}	V_{CSP} - V_{CSN} = 300mV, C_{GATE} = 10nF (Note 3)			160		ns
GATE Off Delay	t_{OFF_GATE}	$V_{\overline{EN}}$ high to V_{GATE} low			20	40	µs
		V_{ON} low to V_{GATE} low			10	20	
GATE Propagation Delay	$t_{ON\_GATE\_PD}$	V_{ON} = step 0.8V to 2V			10	20	µs
GATE Drive Voltage (V_{GATE} - V_{OUT})	V_{GATE}	2.9V < $V_{IN\_}$ < 18V		6	11		V
GATE Pullup Current	I_{GATE_ON}	V_{GATE} - V_{OUT} = 0V		-13	-10	-7	µA
GATE Pulldown Current (Timeout)	I_{GATE_OFF}	V_{OUT} = 12V, V_{GATE} = V_{OUT} + 5V		350	500	650	µA
GATE Fast Pulldown Current	$I_{GATE\_FAST\_OFF}$	V_{OUT} = 12V, V_{GATE} = V_{OUT} + 5V		75	200	260	mA
HOT-SWAP FOLDBACK							
Minimum CB Voltage	V_{CB_FBMAX}	(V_{CSP} - V_{CSN}) = 12V		3	6.7	10.7	% V_{CB_TH}
Minimum FB Voltage	V_{FBMIN}	V_{CSP} - V_{OUT}, at V_{CB} = V_{CB_FBMAX}		1	2.1	3.2	V
Maximum FB Voltage	V_{FBMAX}	V_{CSP} - V_{OUT}, at V_{CB} = V_{CB_TH}		9	10	11	V

Electrical Characteristics (continued)

(V_{IN1} = V_{IN2} = 12V, C_{IN1} = C_{IN2} = C_{VS} = 1µF, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CURRENT-SENSING INPUT						
CSP Input Current	I_{CSP}	V_{CSP} = 12V		0.5	1.0	mA
CSN Input Current	I_{CSN}	V_{CSN} = 12V	100	200	400	µA
CDLY						
CDLY Upper Threshold	V_{CDLY_U}	V_{CDLY} rising	1.1	1.2	1.3	V
CDLY Lower Threshold Hysteresis	V_{CDLY_L}	V_{CDLY} falling		0.2		V
CDLY Pullup Current	I_{CDLY_UP}		-135	-100	-65	µA
CDLY Pulldown Current	I_{CDLY_DOWN}		1.1	2	2.8	µA
CDLY Ratio	I_{CDLY_RATIO}		1.2	2	3.2	%
POWER-GOOD ($\overline{PG}$)						
$\overline{PG}$ Threshold OUT	$V_{\overline{PG}\_OUT}$	V_{GATE} > (5V + V_{OUT})		0.9 x V_{CSP}		V
$\overline{PG}$ Threshold GATE	$V_{\overline{PG}\_GATE}$	V_{GATE} - V_{OUT}		4.2		V
$\overline{PG}$ Detection Timeout	$t_{\overline{PG}\_STARTUP}$		55	70	85	ms
$\overline{PG}$ Assertion Delay	$t_{\overline{PG}\_DELAY}$		13	16	19	ms
OUTPUTS ($\overline{FAULT}$, $\overline{PG}$)						
$\overline{FAULT}$, $\overline{PG}$ Output Voltage Low	V_{OL}	$I_{\overline{PG}}$ = $I_{\overline{FAULT}}$ = 1mA			0.4	V
$\overline{FAULT}$, $\overline{PG}$ Output Voltage High	V_{OH}	$I_{\overline{PG}}$ = $I_{\overline{FAULT}}$ = 1µA	V_S - 1	V_S - 0.6		V
$\overline{FAULT}$, $\overline{PG}$ Leakage Current	I_{OH}	$V_{\overline{PG}}$ = $V_{\overline{FAULT}}$ = 18V	-1		+20	µA
$\overline{FAULT}$, $\overline{PG}$ Pullup Current	I_{PU}	$V_{\overline{PG}}$ = $V_{\overline{FAULT}}$ = 1.5V	-13	-10	-7	µA
INPUTS						
ON, $\overline{PC}$, $\overline{EN}$ Turn-On Threshold	V_{ON_TH}	V_{ON}, $V_{\overline{PC}}$, $V_{\overline{EN}}$ rising	1.1	1.22	1.32	V
ON, $\overline{PC}$, $\overline{EN}$ Turn-On Threshold Hysteresis	V_{ON_HYS}	V_{ON}, $V_{\overline{PC}}$, $V_{\overline{EN}}$ falling hysteresis	70	123	180	mV
ON Fault Reset Threshold Voltage	V_{ON_RESET}	V_{ON} falling	0.5	0.6	0.7	V
ON, $\overline{PC}$ Input Leakage Current	I_{LEAK}	V_{ON}, $V_{\overline{PC}}$ = 0 to 2.5V	-1		+1	µA
ON, $\overline{PC}$ Clamp Voltage		I_{SINK} = 1µA		3		V
ON, $\overline{PC}$ Clamp Sink		V_{ON}, $V_{\overline{PC}}$ = 5V		300		µA
$\overline{EN}$ Pullup Current	I_{PU}	$V_{\overline{EN}}$ = 0V	-13	-10	-7	µA
CB THREE-STATE INPUT						
CB Input Low Current	I_{IN_LOW}	V_{CB} = 0.4V	-75			µA
CB Input High Current	I_{IN_HIGH}	V_{CB} = V_S - 0.2V			+75	µA
CB Input Open-Current Voltage	V_{CB_OPEN}	Force ±4µA into unconnected CB pin; then measure voltage on the CB pin	1.0		V_S - 1	V
CB Low Voltage	V_{IL}	V_{CB} rising	0.4			V

Electrical Characteristics (continued)

(V_{IN1} = V_{IN2} = 12V, C_{IN1} = C_{IN2} = C_{VS} = 1µF, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CB High Voltage	V_{IH}	V_{CB} falling, relative to V_S				V_S - 0.2	
CURRENT MONITORING							
Current Monitor vs. Undervoltage Lockout	V_{IPMON_UVLO}	V_S rising		4.1	4.16	4.23	V
		Hysteresis			0.1		
IPMON Offset (Note 3)	V_{IPMON_O}	V_{CSP} = 12V	T_A = +25°C	-80		+80	µV
			T_A = 0°C to +85°C	-200		+200	
			T_A = -40°C to +125°C	-240		+240	
		V_{CSP} = 4.8V to 18V	T_A = -40°C to +125°C	-300		+300	
IPMON Gain Error (Note 3)	G_{IM_Error}	V_{CSP} = 12V, G_{IM} = 71.565	T_A = +25°C	-0.35		0.35	%
			T_A = 0°C to +85°C	-0.6		0.6	
			T_A = -40°C to +125°C	-0.8		0.8	
		V_{CSP} = 4.8V to 18V	T_A = -40°C to +125°C	-0.8		0.8	
Current Monitoring Total Accuracy (Note 4)	$V_{IPMON\_ACCURACY}$	V_{CSP} = 12V, R_{SENSE} = 3mΩ, I_{LOAD} = 1A, (V_{CSP} - V_{CSN}) = 3mV, T_A = +25°C, $V_{IPMON\_ACCURACY}$ = ((V_{IPMON} - 214.7mV)/214.7mV) x 100		-3		+3	%
		V_{CSP} = 12V, R_{SENSE} = 3mΩ, I_{LOAD} = 3A, (V_{CSP} - V_{CSN}) = 9mV, T_A = +25°C, $V_{IPMON\_ACCURACY}$ = ((V_{IPMON} - 644.085mV)/644.085mV) x 100		-1		+1	
		V_{CSP} =12V,R_{SENSE} = 3mΩ, I_{LOAD} = 5A, (V_{CSP} - V_{CSN}) = 15mV, T_A = +25°C, $V_{IPMON\_ACCURACY}$ = ((V_{IPMON} -1.073V) /1.073V) x 100		-0.65		+0.65	
		V_{CSP} = 12V, R_{SENSE} = 3mΩ, I_{LOAD} = 8A, (V_{CSP} - V_{CSN}) = 24mV, T_A = +25°C, $V_{IPMON\_ACCURACY}$ = ((V_{IPMON} - 1.7175V)/1.7175V) x 100		-0.5		+0.5	
CMRR (Note 5)	I_{PMON_CMRR}	V_{CSP} = 4.8V to 18V		102			dB
Output Voltage Range	$VIPMON_{MAX}$	V_{CSP} = 4.8V to 18V, -40°C ≤ T_A ≤ +125°C		1.72			V
IPMON Voltage Clamp	V_{IPMON_CLMP}	V_{CSP} - V_{CSN} ≥ 36mV, V_{CSP} = 4.8V to 18V, -40°C ≤ T_A ≤ +125°C		2.1	2.3	2.5	V

Note 2: All devices are 100% production tested at T_A = +25°C. Limits over temperature are guaranteed by design.

Note 3: Gain and offset are defined as V_{IPMON1} = V_{IPMON} with Vi_1 = (V_{CSP} - V_{CSN}) = 3mV, V_{IPMON2} = V_{IPMON} with Vi_2 = (V_{CSP} - V_{CSN}) = 24mV, G_{IM} = (V_{IPMON2} - V_{IPMON1})/(Vi_2 - Vi_1), V_{IPMON_OS} = V_{IPMON1} - G_{IM} x Vi_1.

Note 4: Accuracy over the entire operating range can be determined combining the specified value of the related offset and gain in the range.

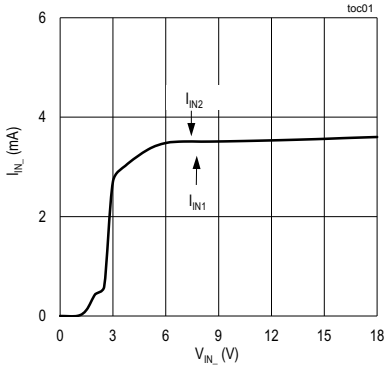
Note 5: CMRR is calculated as:

V_{REF} = V_{IPMON} with V_{CSP} - V_{CSN} = 3mV at V_{REF} = V_{CSP} = 12V,
V_{CM} = V_{IPMON} with V_{CSP} - V_{CSN} = 3mV at 4.8V < V_{CSP} < 18V,
CMRR = 20 x LOG(ABS((12 - V_{CSP})/(V_{REF} - V_{CM})) x G_{IM}),
where G_{IM} is the differential gain defined in the *Electrical Characteristics* table.

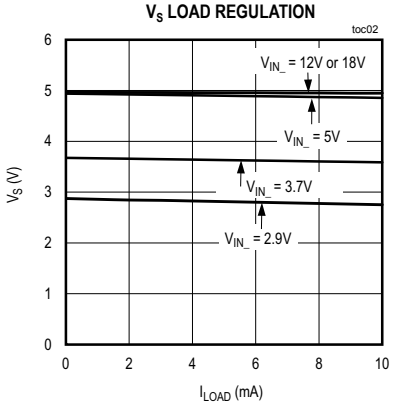
Typical Operating Characteristics

(V_{IN1} = V_{IN2} = 12V, C_{IN1} = C_{IN2} = C_{VS} = 1µF, R_{SENSE} = 3mΩ, unless otherwise noted.)

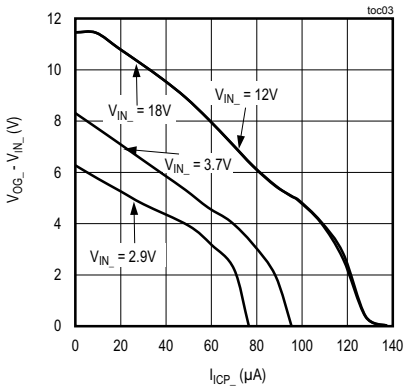
IN_ SUPPLY CURRENT vs. VOLTAGE



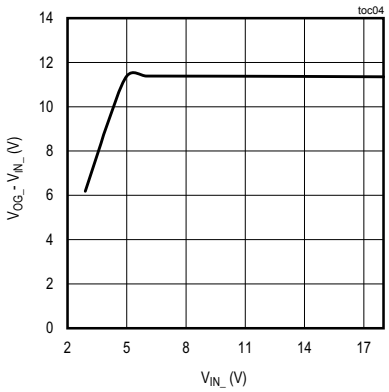
V_S LOAD REGULATION



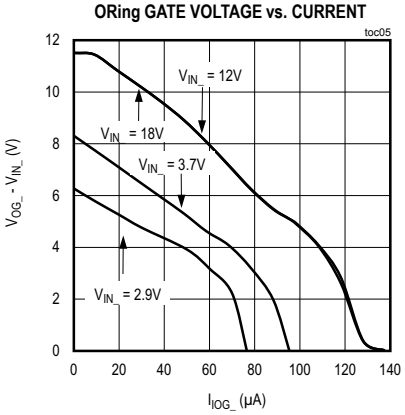
ORing GATE DRIVE vs. CURRENT



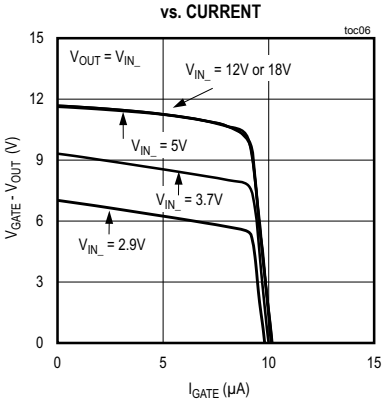
ORing GATE DRIVE vs. INPUT VOLTAGE



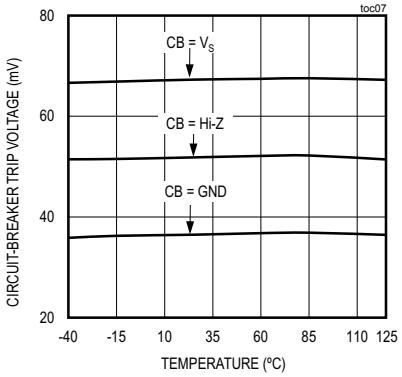
ORing GATE VOLTAGE vs. CURRENT



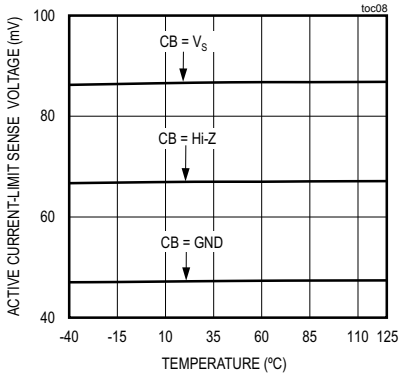
HOT-SWAP MOSFET GATE VOLTAGE vs. CURRENT



CIRCUIT-BREAKER TRIP VOLTAGE vs. TEMPERATURE



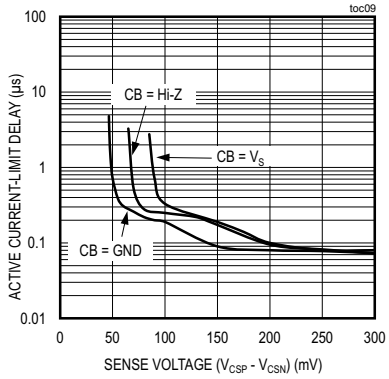
ACTIVE CURRENT-LIMIT SENSE VOLTAGE vs. TEMPERATURE



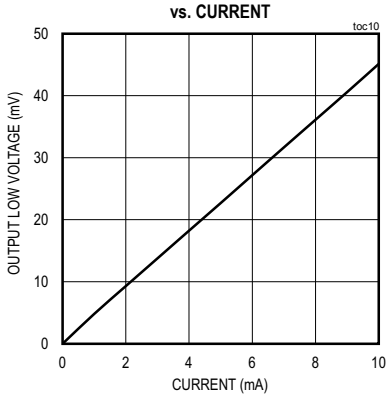
Typical Operating Characteristics (continued)

(V_{IN1} = V_{IN2} = 12V, C_{IN1} = C_{IN2} = C_{VS} = 1µF, R_{SENSE} = 3mΩ, unless otherwise noted.)

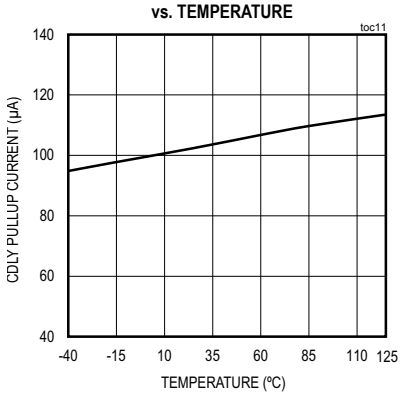
ACTIVE CURRENT-LIMIT DELAY vs. SENSE VOLTAGE



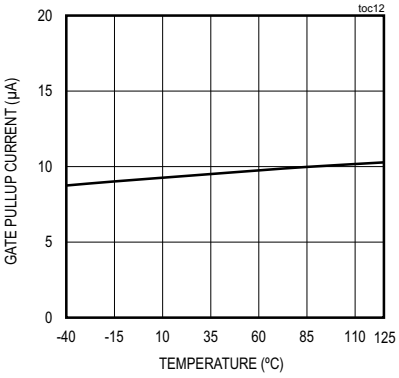
$\overline{PG}$, $\overline{FAULT}$ OUTPUT LOW VOLTAGE vs. CURRENT



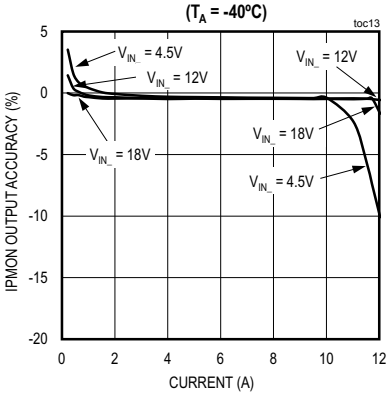
CDLY PULLUP CURRENT vs. TEMPERATURE



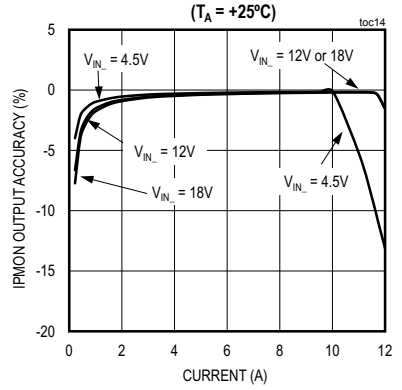
GATE PULLUP CURRENT vs. TEMPERATURE



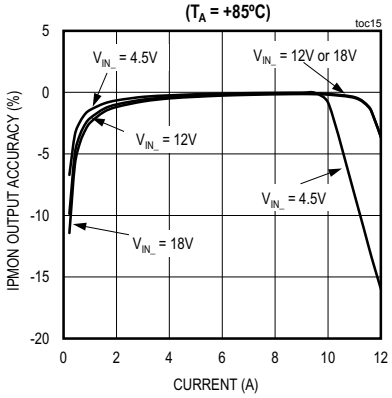
IPMON OUTPUT ACCURACY (T_A = -40ºC)



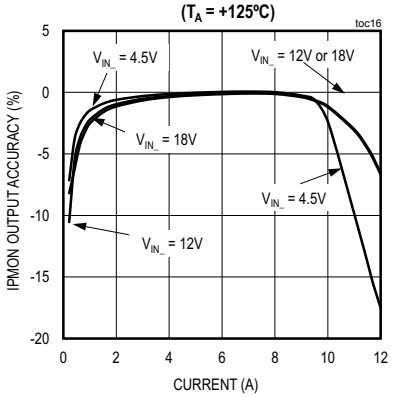
IPMON OUTPUT ACCURACY (T_A = +25ºC)



IPMON OUTPUT ACCURACY (T_A = +85ºC)



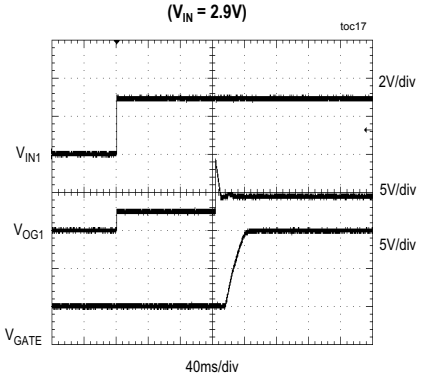
IPMON OUTPUT ACCURACY (T_A = +125ºC)



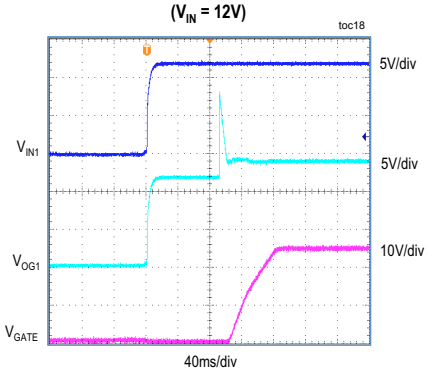
Typical Operating Characteristics (continued)

(V_{IN1} = V_{IN2} = 12V, C_{IN1} = C_{IN2} = C_{VS} = 1µF, R_{SENSE} = 3mΩ, unless otherwise noted.)

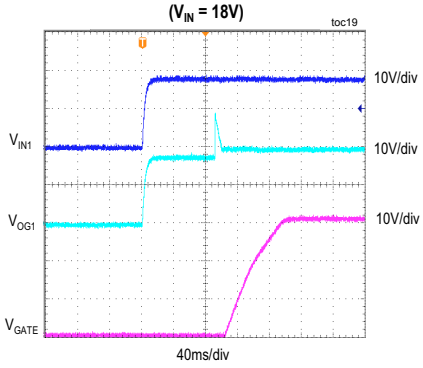
STARTUP WAVEFORM (V_{IN} = 2.9V)



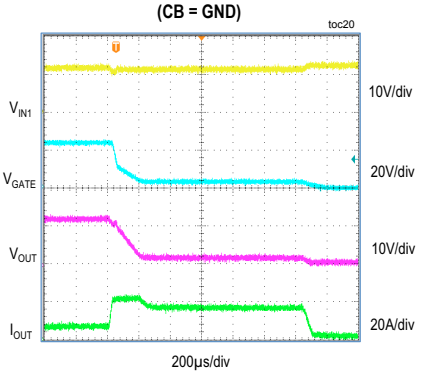
STARTUP WAVEFORM (V_{IN} = 12V)



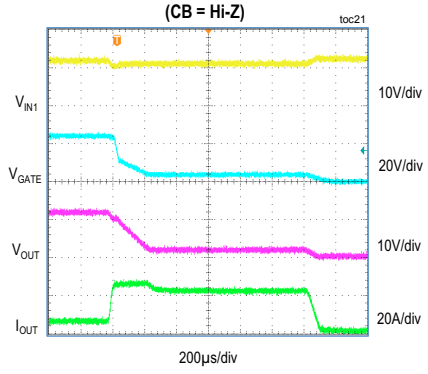
STARTUP WAVEFORM (V_{IN} = 18V)



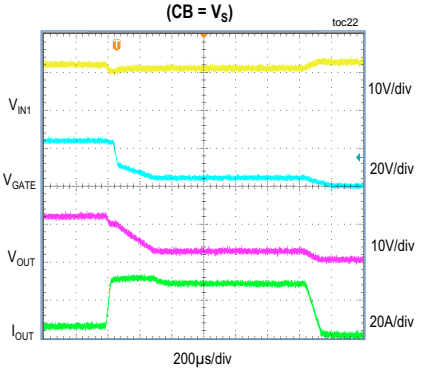
OVERCURRENT-FAULT WAVEFORM (CB = GND)



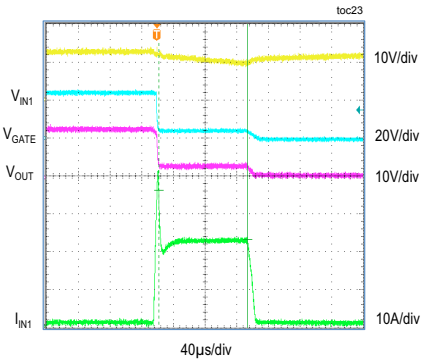
OVERCURRENT-FAULT WAVEFORM (CB = Hi-Z)



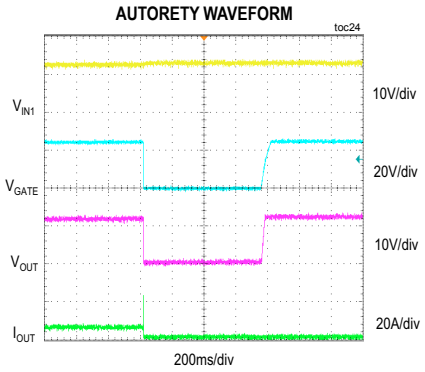
OVERCURRENT-FAULT WAVEFORM ($CB = V_S$)



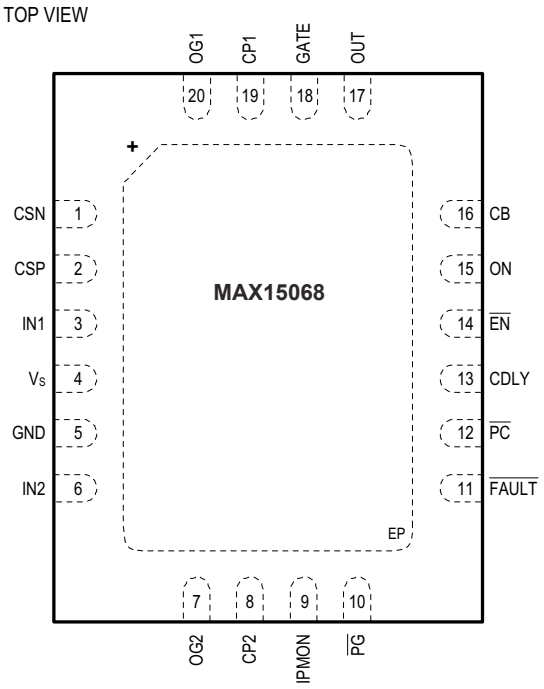
OUT SHORT-CIRCUIT RESPONSE



AUTORETY WAVEFORM



Pin Configuration



TQFN
(4mm × 5mm)

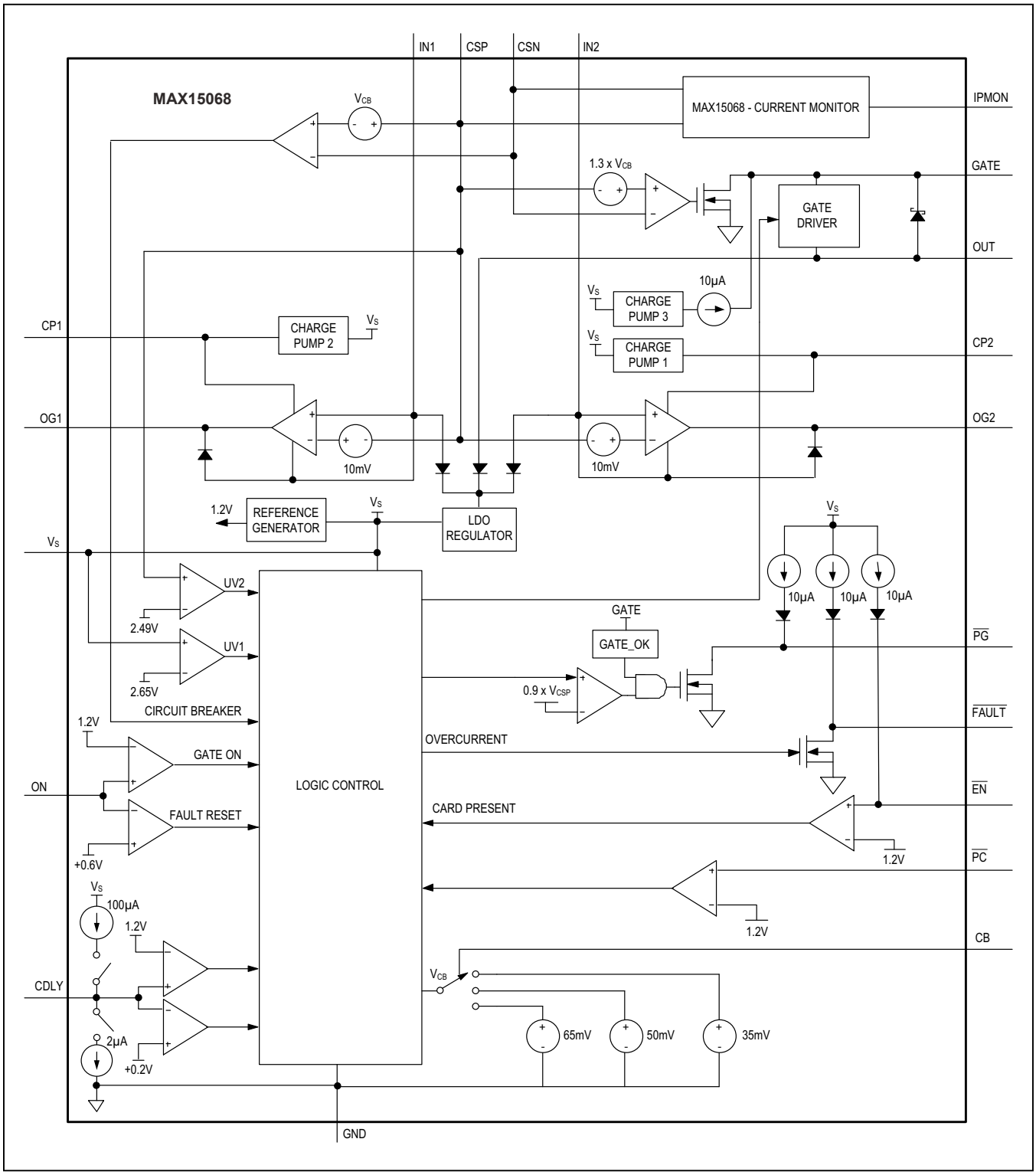
Pin Description

PIN	NAME	FUNCTION
1	CSN	Input Current Sense Negative Input
2	CSP	Input Current Sense Positive Input
3	IN1	Positive Supply 1 Input and MOSFET Gate Drive Return
4	V_S	Internal Regulator Output. Bypass V_S to GND with a 1µF capacitor.
5	GND	Ground
6	IN2	Positive Supply 2 Input and MOSFET Gate Drive Return
7	OG2	ORing MOSFET 2 Gate Control Output. Connect this pin to the gate of an external n-channel MOSFET for ideal diode control. The gate voltage is limited to approximately 11V above and a diode voltage below IN2. During fast turn-on, a 1A pullup switch charges OG2 from CP2. During fast turn-off, a 3A pulldown switch discharges OG2 to IN2.
8	CP2	Charge Pump 2 Output. Connect a capacitor from CP2 to IN2 pin. The value of this capacitor should be approximately 10x the gate capacitance (CISS) of the external MOSFET for ORing diode control. The charge stored on this capacitor is used to pull up the gate during a fast turn-on.
9	IPMON	Analog Current Monitor Output Signal. Connect a 560pF/6.3V ceramic capacitor from IPMON to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
10	$\overline{PG}$	Power Status Output. Open-drain output that is normally pulled high by a 10µA current source to a diode below V_S. $\overline{PG}$ can be pulled above V_S using an external pullup. $\overline{PG}$ pulls low when the MOSFET gate drive between GATE and OUT exceeds the gate-to-source voltage of 4.2V and V_{OUT} is greater than 90% of V_{CSP}. Leave $\overline{PG}$ unconnected if unused.
11	$\overline{FAULT}$	Fault Status Output. Open-drain output that is normally pulled high by a 10µA current source to a diode below V_S. $\overline{FAULT}$ can be pulled above V_S using an external pullup. $\overline{FAULT}$ pulls low when the circuit breaker is tripped after an overcurrent fault timeout. Leave $\overline{FAULT}$ unconnected if unused.
12	$\overline{PC}$	Priority Control Input. When low, it enables the external ideal diode MOSFET in the IN2 supply path and a high turns it off. Connect $\overline{PC}$ to an external resistive divider from IN1 to make IN1 the higher priority input supply when IN1 and IN2 are equal. Connect $\overline{PC}$ to GND if not used.
13	CDLY	Timer Capacitor Terminal. Connect a capacitor between CDLY and GND to set 12ms/µF duration for current limit before the external hot-swap MOSFET is turned off. The duration of the off-time is 600ms/µF, resulting in a 2% duty cycle.
14	$\overline{EN}$	Enable Input. Connect $\overline{EN}$ to GND to enable hot-swap control. If $\overline{EN}$ is pulled high, the hot-swap MOSFET is not allowed to turn on. A 10µA current source pulls up $\overline{EN}$ to a diode below V_S. Upon $\overline{EN}$ going low when ON is high, an internal timer provides a 100ms startup delay for debounce, after which the fault is cleared.
15	ON	On Control Input. When above 1.2V, it turns on the external hot-swap MOSFET and when below 1.1V, it turns it off. Connect ON to an external resistive divider from CSP to monitor the supply undervoltage condition. Pulling voltage of ON pin below 0.6V resets the electronic circuit breaker.
16	CB	Current-Limit Threshold Setting. Connect the CB pin to V_S, GND, or leave CB unconnected to set the circuit-breaker threshold. See Table 1 for details.
17	OUT	Load Output. Connect OUT to the source of the external hot-swap MOSFET.
18	GATE	Hot-Swap MOSFET Gate Drive Output. Connect this pin to the gate of the external n-channel MOSFET for hot-swap control. An internal 10µA current source charges the MOSFET gate. An internal clamp limits the gate voltage to 11V above OUT and a diode voltage below OUT. During turn-off, a 500µA pulldown current discharges GATE to ground. During an output short to ground, a fast 200mA pulldown current discharges GATE to OUT.
19	CP1	Charge Pump 1 Output. Connect a capacitor from CP1 to IN1 pin. The value of this capacitor should be 10x or greater than the gate capacitance of the external MOSFET for ideal diode control. The charge stored on this capacitor is used to pull up the gate during a fast turn-on.
20	OG1	ORing MOSFET 1 Gate Control Output. Connect OG1 to the gate of an external n-channel MOSFET for ideal diode control. The gate voltage is set to approximately 11V above and a diode voltage below IN1. During fast turn-on, a 1A pullup switch charges OG1 from CP1. During fast turn-off, a 3A pulldown switch discharges OG1 to IN1.
—	EP	Exposed Pad. Connect EP to the ground plane to provide a low thermal resistance path from the IC junction to the PCB. Do not use EP as an electrical connection to GND.

Functional Diagram



Detailed Description

Startup

When input voltage is applied to IN_, CSP comes up to one diode below the higher of IN1 or IN2. The internal LDO regulator powers V_S from the higher of two inputs as well. When both V_S and CSP reach their respective UVLO thresholds, the internal charge pumps (CP1 or CP2) for the ORing controller start operating. An internal time starts when both ON is above its threshold and $\overline{EN}$ is below its threshold. After the timer counts 85ms, the ORing control (OG1 or OG2) begins operating. After another 15ms have elapsed, the hot-swap control (GATE) also starts operating.

ORing Control

ORing Control in Startup

During a normal power-up, the ORing MOSFETs turn on first. As soon as the internally generated supply, V_S, rises above its undervoltage lockout threshold, the internal charge pump is allowed to charge up the CP_ pins. Because the ideal diode MOSFETs are connected in parallel as a diode-OR, the CSP pin voltage selects the highest of the supplies at the IN1 and IN2 pins. The MOSFET associated with the lower input supply voltage is turned off by the corresponding gate drive amplifier.

At power-up the CP_ and OG_ pin voltages are at the IN_ voltage level. CP_ starts ramping up after VS clears its undervoltage lockout level. Afterward, OG_ ramps up with CP_.

The gate drive amplifier monitors the voltage between the IN and CSP pins and drives the respective OG_ pin.

If the amplifier senses a forward voltage drop greater than 80mV between IN and CSP then the OG_ pin is pulled to CP to quickly turn on the MOSFET. If the amplifier senses a reverse voltage drop greater than 10mV between CSP and IN_, then the OG_pin is pulled to IN_ to quickly turn off the MOSFET. With the ideal diode MOSFETs acting as an input supply diode-OR, the CSP pin voltage rises to the highest of the supplies at the IN1 and IN2 pins. The stored charge in an external capacitor connected between the CP_ and IN_ pins provides the charge needed to quickly turn on and off the ideal diode MOSFET. An internal charge pump charges the external capacitors at the CP pins. The OG_ pin sources current from the CP_ pin and sinks current into the IN_ and GND pins.

ORing MOSFET Regulation Mode

When the ideal diode MOSFET is turned on, the gate drive amplifier controls OG_ to servo the forward voltage drop (V_{IN} - V_{CSP}) across the MOSFET to 10mV. If the load current causes more than 10mV of voltage drop, across the FET, then the OG voltage rises to enhance the MOSFET. For large output currents, the MOSFET's gate is driven fully on and the voltage drop is equal to I_{LOAD} x $R_{DS(ON)}$ of the MOSFET.

Hot-Swap Control

Hot-Swap in Startup

Once the output is enabled, the device provides controlled application of power to the load. The voltage at OUT begins to rise until the internal selected final maximum current limit is reached, which is programmed through the CB pin (Table 1). The low limit is approximately 1/12th of the upper limit as shown in Figure 1. Once the power-good threshold is achieved, the normalized hot-swap electronic circuit-breaker (ECB) threshold goes to its full value.

An external capacitor connected to the GATE pin allows the user to program the slew rate to a value lower than the default. During startup, a foldback current limit is active to protect the external hot-swap MOSFET to operate within the SOA (Figure 1).

An internal timer is activated to count for 70ms, which is the maximum time duration for the startup phase. The startup phase is completed when the voltage at OUT rises above the power-good threshold (0.9 x V_{CSP} typical) and hot-swap GATE to OUT voltage exceeds 4.2V even though the 70ms timeout has not yet elapsed.

Programmable Speed Circuit-Breaker Response on Hot-Swap MOSFET

The device features an adjustable current limit with circuit-breaker function that protects the external MOSFETs against short circuits or excessive load current. The voltage across the external sense resistor (R_{SENSE}) is monitored by an electronic circuit breaker (ECB) and

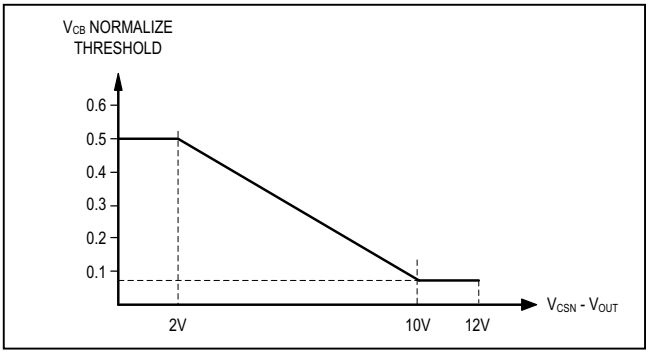


Figure 1. Inrush Current vs. Voltage Drop Across the Hot-Swap Switch During Startup Period

active current limit amplifier (ACL). The electronic circuit breaker turns off the hot-swap MOSFET with a 500µA current from GATE to OUT if the voltage across the sense resistor exceeds V_{CB_TH} (ECB) for longer than the fault filter delay configured at the CDLY pin. Active current limiting begins when the sense voltage exceeds the ACL threshold V_{ACL} (ACL) (which is 1.3x the ECB threshold). The gate of the hot-swap MOSFET is brought under control by the ACL amplifier and the output current is regulated to maintain the ACL threshold across the sense resistor. At this point, the fault filter starts the timeout with a 100µA current charging the CDLY pin capacitor. If the CDLY pin voltage exceeds its threshold (1.2V), the external MOSFET is turned off and the $\overline{FAULT}$ pin pulls low.

After the hot-swap MOSFET turns off, the CDLY pin capacitor is discharged with a 2µA pulldown current until it reaches 0.2V. This is followed by a cool-off period of 14 timing cycles at the CDLY pin. For the autoretry part, the latched fault is cleared automatically at the end of the cool-off period and the GATE pin restarts charging up the gate of the MOSFET.

In the event of a severe short-circuit fault on the 12V output, the output current can surge to tens of amperes. The device responds within 1µs to bring the current under control by pulling the GATE to OUT voltage down with a 200mA current. Almost immediately, the gate of the hot-swap MOSFET recovers rapidly due to the R_{GATE} and C_{GATE} network, and load current is actively limited until the electronic circuit breaker times out. Due to parasitic supply lead inductance, an input supply without any bypass capacitor may collapse during the high current surge and then spike upwards when the current is interrupted.

Circuit-Breaker Comparator and Current Limit

The device features a programmable circuit-breaker threshold. The current limit can be selected by the connection of the CB pin. During startup, a foldback current limit is active to protect the internal MOSFET to operate within the SOA (Figure 1).

Programmable Circuit-Breaker Current Threshold

The device features a programmable current limit with circuit-breaker function that protects the external MOSFETs against short circuits or excessive load current. The voltage across the external sense resistor, (R_{SENSE}) is monitored by an electronic circuit breaker (ECB) and active current limit (ACL) amplifier. Connect the CB pin to GND, V_S, or leave unconnected to select the electronics circuit-breaker threshold (Table 1).

The electronic circuit breaker turns off the hot-swap MOSFET with a 500µA current from GATE to GND if the voltage across the sense resistor exceeds $V_{CB\_TH\ (CB)}$ (50mV) for longer than the fault filter delay configured at the CDLY pin.

Timer (CDLY)

An external capacitor connected from the CDLY pin to GND serves as fault filtering when the supply output is in active current limit. When the voltage across the sense resistor exceeds the circuit-breaker trip threshold (50mV), CDLY pulls up with 100µA. Otherwise, it pulls down with 2µA. The fault filter times out when the 1.2V CDLY threshold is exceeded, causing the corresponding $\overline{FAULT}$ pin to pull low. The fault filter delay or circuit-breaker time delay is:

$$t_{CB} = C_{CDLY} \times 12[ms/\mu F]$$

After the circuit-breaker timeout, the CDLY pin capacitor pulls down with 2µA from the 1.2V CDLY threshold until it reaches 0.2V. Then it completes 14 cooling cycles consisting of the CDLY pin capacitor charging to 1.2V with a 100µA current and discharging to 0.2V with a 2µA current. At that point, the GATE pin voltage is allowed to start up if the fault has been cleared as described in the *Resetting Faults* section. When the latched fault is cleared during the cool-off period, the corresponding $\overline{FAULT}$ pin pulls high. The total cool-off time for the MOSFET after an overcurrent fault is:

$$t_{COOL} = C_{CDLY} \times 7.13[s/\mu F]$$

ORing/Hot-Swap Response in Overload Condition

In the case where an overcurrent fault occurs on the output, the current is limited to a programmed current limit set through the CB pin. After a fault filter delay set by 100µA current source in to the CDLY pin capacitor, the circuit breaker trips, pulls the GATE pin low, and turns off the hot-swap MOSFET. The $\overline{FAULT}$ output is latched low. During the fault condition, the ORing MOSFET remains on.

Control Inputs

$\overline{ON}$ Input

The device drives the OG_ as soon as the V_{IN1} - V_{F1} (V_{F1} is the forward voltage drop of ORing MOSFET connected to IN1) or V_{IN2} - V_{F2} (V_{F2} is the forward voltage drop of the ORing MOSFET connected to IN2) supply voltage generates a V_{ON} above the threshold voltage. An external resistive divider from CSP to ON and ground is used to set the turn-on voltage to any desired voltage from 2.9V to 5.5V. The IC turns on the corresponding ORing MOSFET and then turns on the hot-swap MOSFET when V_{ON} > 1.22V.

The device turns off the output when V_{ON} falls below V_{UV_REF} (1.22V - V_{ON_HYS}). An external resistive divider from CSP to ON and ground is used to set the undervoltage-lockout threshold to any desired level between V_{UVLO} and 18V. Pulling the ON pin voltage below 0.6V resets the electronic circuit breaker.

Monitoring

Analog Current Monitor Output

IPMON monitors the system input current and provides the best accuracy when V_{IPMON} is less than 1.7V. For best performance, add a 560pF/6.3V ceramic capacitor between IPMON and GND.

The voltage at IPMON (V_{IPMON}) is proportional to the input current (V_{SYS}) given by the following equation:

$$V_{IPMON} = G_{IM} \times I_{SYS} \times R_{SENSE}$$

where G_{IM} = 71.565, a fixed voltage gain.

Adding an RC network at the IPMON output (Figure 2) allows the overall V_{IPMON} gain (G) to be adjusted per the following equation:

$$G = G_{IM} \times R2/(R1+R2)$$

where R1 = 20kΩ, C1 = 560pF, and C2 = 1nF. The resistive-divider equivalent resistance R1||R2 needs to be carefully selected, as it affects accuracy due to the input bias current of the system readout.

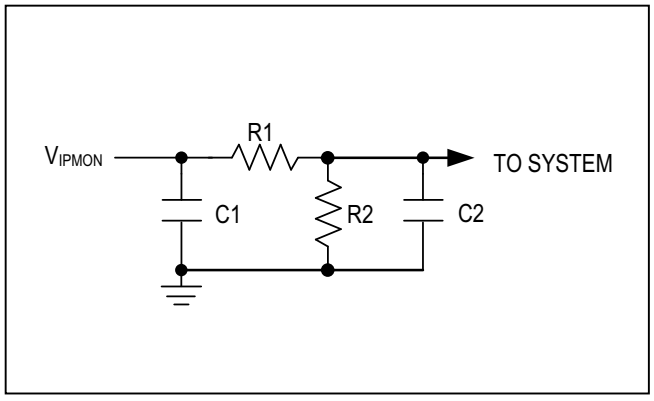


Figure 2. External RC Network to Adjust V_{IPMON}

Output Signals

Fault Status Output ($\overline{FAULT}$)

$\overline{FAULT}$ is an open-drain output that is internally pulled high by a 10µA current source to a diode below V_S, and can be pulled above V_S using an external pullup. $\overline{FAULT}$ asserts low when the circuit breaker is tripped after an overcurrent fault timeout. Leave $\overline{FAULT}$ unconnected if unused.

Power-Good Output ($\overline{PG}$)

Internal circuitry monitors the hot-swap MOSFET gate overdrive between the GATE and OUT pins and the voltage at the OUT pin. The power-good status for the supply is reported by the $\overline{PG}$ open-drain output. It is normally pulled high by an external pullup resistor or the internal 10µA pullup. The power-good output asserts low when the gate overdrive exceeds 4.2V during the GATE startup and the voltage at the OUT pin exceeds (0.9 x V_{CSP}). The $\overline{PG}$ signal is delayed by 16ms once conditions for power-good are met.

Fault Management

Autoretry

When an overcurrent fault is latched after tripping the circuit breaker, the $\overline{FAULT}$ pin is asserted low. Only the hot-swap MOSFET is turned off, and the ideal diode MOSFETs are not affected. The latched fault is reset automatically after a cool-off timing cycle as described in the *Timer (CDLY)* section. At the end of the cool-off period, the fault latch is cleared and $\overline{FAULT}$ pulls high. The GATE pin voltage is allowed to start up and turn on the hot-swap MOSFET. If the output short persists, the supply powers up into a short with active current limiting until the circuit breaker times out and $\overline{FAULT}$ again pulls low. A new cool-off cycle begins with CDLY ramping down with a 2µA current. The whole process repeats itself until the output short is removed. Since t_{CB} and t_{COOL} are a function of CDLY capacitance, C_{CDLY}, the autoretry duty cycle is equal to 0.1%, irrespective of C_{CDLY}.

Table 1. Electronics Circuit-Breaker Threshold Programming

CB PIN CONNECTION	ELECTRONIC CIRCUIT-BREAKER THRESHOLD (V_{CSP} - V_{CSN}) [mV]
CB = GND	35
CB = Hi-Z (unconnected)	50
CB = V_S	65

Applications Information

Prioritizing Supplies with $\overline{PC}$

Figure 2 shows an ORing application where a resistive divider connected from IN1 at the $\overline{PC}$ pin controls the turn-on of the ORing MOSFET, MD2, in the IN2 supply path. When the IN1 supply voltage falls below 4.5V, it turns on the ORing MOSFET, MD2, causing the ORing output to be switched from the main 5.0V supply at IN1 to the auxiliary 5.0V supply at IN2. This configuration permits the load to be supplied from a lower IN1 supply as compared to IN2 until IN1 falls below the MD2 turn-on threshold. The threshold value used should not allow the IN1 supply to be operated at more than one diode voltage below IN2. Otherwise, MD2 conducts through the MOSFET's body diode. The resistive divider connected from CSP at the ON pin provides the undervoltage threshold of 2.6V for the ORing output supply.

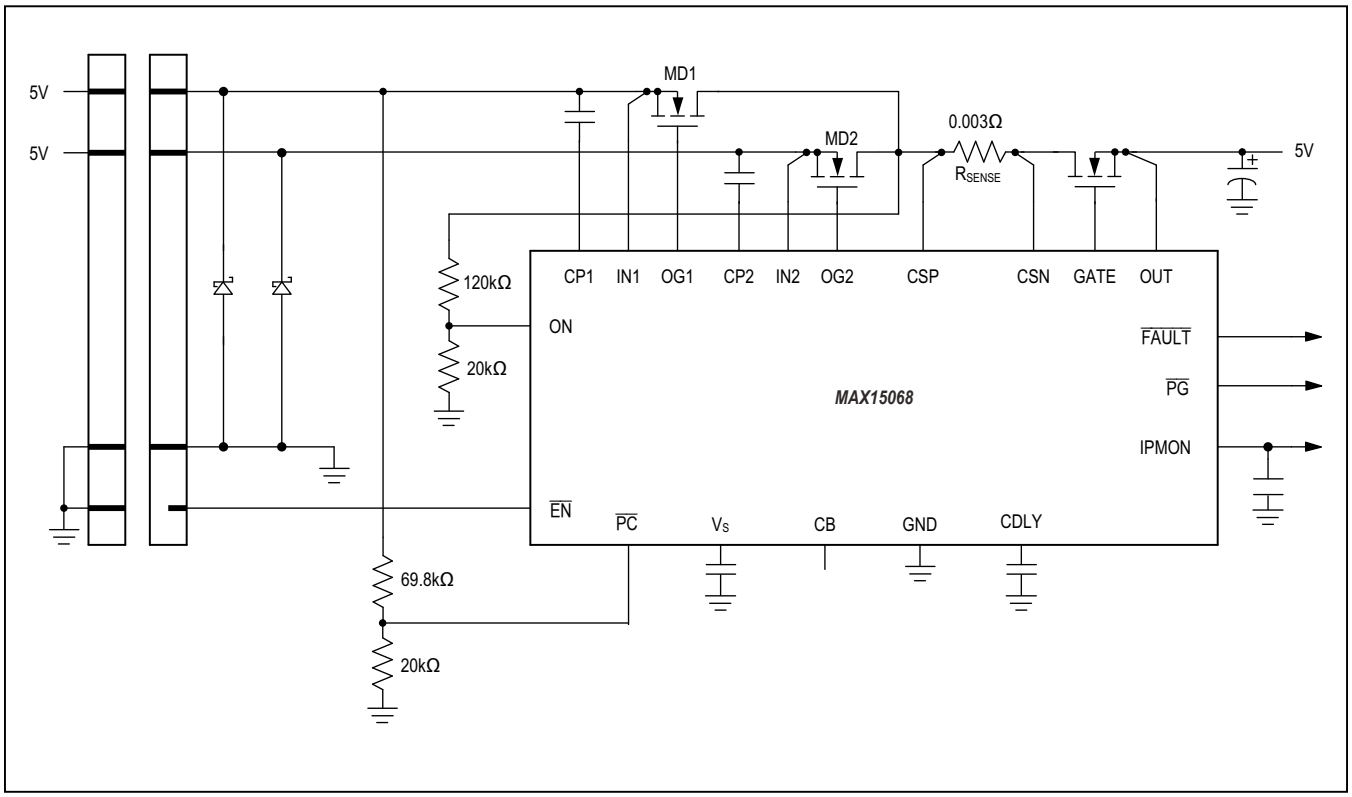
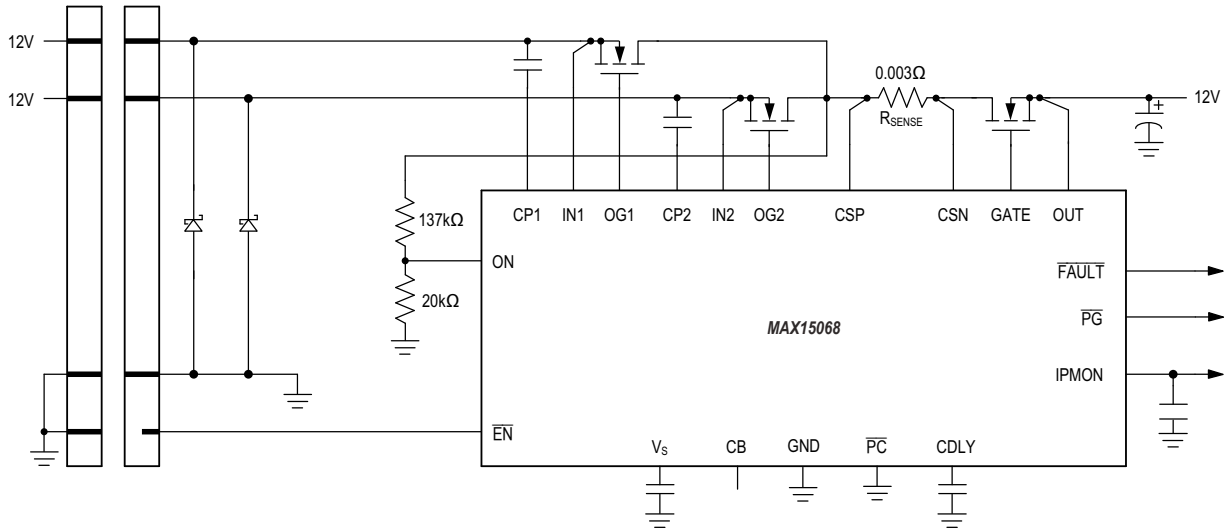


Figure 3. Plug-in Card IN1 Supply Controls the IN2 Supply Turn-On through the $\overline{PC}$ Pin

Typical Application Circuit



Ordering Information

PART	OPERATING RANGE	FUNCTION	TEMP RANGE	PIN-PACKAGE
MAX15068ATP+	2.9V to 18V	Autoretry, Current Monitor	-40°C to +125°C	20 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN	T2045+1C	21-0726	—

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/13	Initial release	—
1	2/16	Customer test spec changes: Updated *General Description*, B*enefits and Features*, *Electrical Characteristics* table; replaced TOC2–TOC6, TOC17, and changed TOC13–TOC16 titles in *Typical Operating Characteristics* section; updated IPMON pin 9 function in *Pin Description* table; updated 2nd equation in *Timer (CDLY)* section; replaced *Analog Current Monitor Output* section, adding a new Figure 2; renumbered and replaced new Figure 3 and replaced *Typical Application Circuit*; updated operating range in *Ordering Information* table	1–9, 13–16

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