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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# MAX1530/MAX1531

# Multiple-Output Power-Supply Controllers for LCD Monitors

## General Description

The MAX1530/MAX1531 multiple-output power-supply controllers generate all the supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) monitors. Both devices include a high-efficiency, fixed-frequency, step-down regulator. The low-cost, all N-channel, synchronous topology enables operation with efficiency as high as 93%. High-frequency operation allows the use of small inductors and capacitors, resulting in a compact solution. The MAX1530 includes three linear regulator controllers and the MAX1531 includes five linear regulator controllers for supplying logic and LCD bias voltages. A programmable startup sequence enables easy control of the regulators.

The MAX1530/MAX1531 include soft-start functions to limit inrush current during startup. An internal stepdown converter current-limit function and a versatile overcurrent shutdown protect the power supplies against fault conditions. The MAX1530/MAX1531 use a currentmode control architecture, providing fast load transient response and easy compensation. An internal linear regulator provides MOSFET gate drive and can be used to power small external loads.

The MAX1530/MAX1531 can operate from inputs as high as 28V and are well suited for LCD monitor and TV applications running directly from AC/DC wall adapters. Both devices are available in a small (5mm x 5mm), ultra-thin (0.8mm), 32-pin QFN package and operate over the -40°C to +85°C temperature range.

## Applications

- LCD Monitors and TVs

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX1530ETJ+** | -40°C to +125°C | 32 TQFN-EP* |
| MAX1530ETJ+T | -40°C to +125°C | 32 TQFN-EP* |
| **MAX1531ETJ+** | -40°C to +125°C | 32 TQFN-EP* |
| MAX1531ETJ+T | -40°C to +125°C | 32 TQFN-EP* |

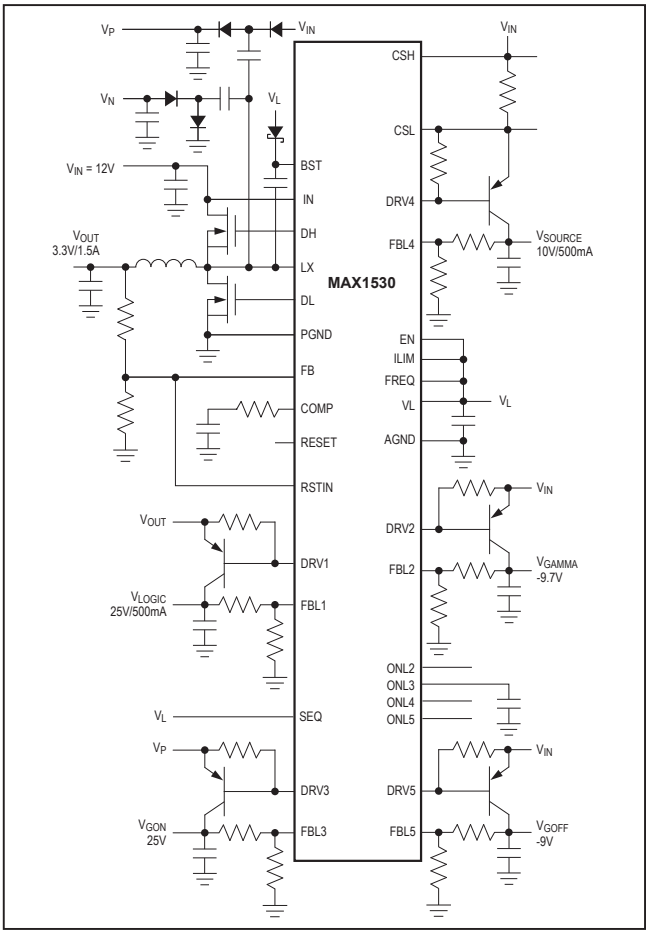
*+Denotes a lead(Pb)-free/RoHS-compliant package.*
*T = Tape and reel.*
**EP = Exposed pad.*

***Pin Configuration* appears at end of data sheet.**

## Features

- 4.5V to 28V Input Voltage Range
- 250kHz/500kHz Current-Mode Step-Down Converter
  - Small Inductor/Capacitors
  - No Sense Resistor
- Three Positive Linear Regulator Controllers
  - One Positive and One Negative Additional Controller (MAX1531)
  - Small Input and Output Capacitors
- Timed Reset Output
- Uncommitted Overcurrent Protection (MAX1531)
- Soft-Start for All Regulators
- Programmable Input Undervoltage Comparator
- Programmable Startup Sequencing

## Minimal Operating Circuit



## Absolute Maximum Ratings

IN, DRV1, DRV2, DRV3, DRV4, CSH, CSL to AGND .....-0.3V to +30V
DRV5 to VL .....-28V to +0.3V
CSH to CSL .....-0.3V to +6V
VL to AGND.....-0.3V to +6V
PGND to AGND.....±0.3V
LX to BST.....-6V to +0.3V
BST to AGND.....-0.3V to +36V
DH to LX .....-0.3V to (BST + 0.3V)
DL to PGND .....-0.3V to (VL + 0.3V)
SEQ, ONL2, ONL3, ONL4, ONL5, COMP, ILIM to AGND.....-0.3V to (VL + 0.3V)
RSTIN, RESET, EN, FB, FBL1, FBL2, FBL3, FBL4, FBL5, FREQ to AGND.....-0.3V to +6V
VL Short Circuit to AGND .....Momentary
Continuous Power Dissipation ($T_A$ = +70°C)
32-Pin Thin QFN (derate 21.3mW/°C above +70°C) ...1702mW
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Electrical Characteristics

(Circuit of Figure 1, $V_{IN}$ = 12V, $V_{EN}$ = $V_{SEQ}$ = 5V, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **GENERAL** | | | | | |
| Operating Input Voltage Range | (Note 1) | 4.5 | | 28.0 | V |
| Quiescent Supply Current | $V_{FB}$ = $V_{FBL1}$ = $V_{FBL2}$ = $V_{FBL3}$ = $V_{FBL4}$ = 1.5V, $V_{FBL5}$ = 0V | | 1.7 | 3.0 | mA |
| IC Disable Supply Current | EN = AGND | | 200 | 400 | µA |
| **VL REGULATOR** | | | | | |
| VL Output Voltage | 5.5V < $V_{IN}$ < 28V, 0 < $I_{VL}$ < 30mA | 4.75 | 5 | 5.25 | V |
| VL Undervoltage Lockout Threshold | VL rising, 3% hysteresis | 3.2 | 3.5 | 3.8 | V |
| **CONTROL AND SEQUENCE** | | | | | |
| SEQ, FREQ Input Logic High Level | | 2.0 | | | V |
| SEQ, FREQ Input Logic Low Level | | | | 0.6 | V |
| SEQ, FREQ Input Leakage Current | | -1 | | +1 | µA |
| ONL_ Input Threshold | ONL_ rising, 25mV hysteresis | 1.201 | 1.238 | 1.275 | V |
| ONL_ Source Current | SEQ = EN = VL, $V_{ONL\_}$ = 0 to 1.24V | 1.8 | 2.0 | 2.2 | µA |
| ONL_ Input Leakage Current | SEQ = EN = VL, ONL_ = VL | -500 | | +500 | nA |
| ONL_ Input Discharge Clamp Resistance | $V_{SEQ}$ = 0V | 800 | 1500 | 3000 | Ω |
| EN Input Threshold | EN rising, 5% hysteresis | 1.201 | 1.238 | 1.275 | V |
| EN Input Leakage Current | | -50 | | +50 | nA |
| **FAULT DETECTION** | | | | | |
| FB, FBL1, FBL2, FBL3, FBL4 Undervoltage Fault Trip Level | FB, FBL1, FBL2, FBL3, FBL4 falling, 25mV hysteresis | 1.081 | 1.114 | 1.147 | V |
| FBL5 Undervoltage Fault Trip Level | FBL5 rising, 25mV hysteresis | 300 | 400 | 500 | mV |

## Electrical Characteristics (continued)

(Circuit of Figure 1, $V_{IN}$ = 12V, $V_{EN}$ = $V_{SEQ}$ = 5V, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Comparator Bandwidth | For EN, FB, FBL_ | | 10 | | kHz |
| Duration to Trigger Fault Latch | For FB, FBL_ | 51 | 64 | 77 | ms |
| Overcurrent Protection Threshold | ($V_{CSH}$ - $V_{CSL}$) | 270 | 300 | 330 | mV |
| Overcurrent Sense Common-Mode Range | $V_{CSH}$, $V_{CSL}$ | 2.7 | | 28.0 | V |
| CSH Input Current | $V_{CSH}$ = 2.7V to 28V | | | 100 | µA |
| CSL Input Current | $V_{CSL}$ = $V_{CSH}$ = 12V | -50 | | +50 | nA |
| Overcurrent Sense Filter RC Time Constant | | | 50 | | µs |
| **THERMAL PROTECTION** | | | | | |
| Thermal Shutdown | Temperature rising, 15°C hysteresis | | 160 | | °C |
| **RESET FUNCTION** | | | | | |
| RSTIN Reset Trip Level | RSTIN falling, 25mV hysteresis | 1.081 | 1.114 | 1.147 | V |
| RSTIN Input Leakage Current | $V_{RSTIN}$ = 1.5V | -50 | | +50 | nA |
| Comparator Bandwidth | | | 10 | | kHz |
| Reset Timeout Period | | 102 | 128 | 154 | ms |
| RESET Output Low Level | $I_{RESET}$ = -1mA | | | 0.4 | V |
| RESET Output High Leakage | $V_{RESET}$ = 5V | | | 1 | µA |
| **STEP-DOWN CONTROLLER** | | | | | |
| **ERROR AMPLIFIER** | | | | | |
| FB Regulation Voltage | | 1.223 | 1.238 | 1.253 | V |
| Transconductance | FB to COMP | 70 | 100 | 140 | µS |
| Voltage Gain | FB to COMP | | 200 | | V/V |
| Minimum Duty Cycle | | | 15 | | % |
| FB Input Leakage Current | $V_{FB}$ = 1.5V | -50 | | +50 | nA |
| FB Input Common-Mode Range | (Note 2) | -0.1 | | +1.5 | V |
| COMP Output Minimum Voltage | $V_{FB}$ = 1.5V | | 1 | | V |
| COMP Output Maximum Voltage | $V_{FB}$ = 1.175V | | 3 | | V |
| Current-Sense Amplifier Voltage Gain | $V_{IN}$ - $V_{LX}$ | 2.75 | 3.5 | 4.0 | V/V |
| Current-Limit Threshold (Default Mode) | PGND - LX, ILIM = VL | 190 | 250 | 310 | mV |
| Current-Limit Threshold (Adjustable Mode) | PGND - LX, $V_{ILIM}$ = 1.25V | 190 | 250 | 310 | mV |
| ILIM Input Dual Mode™ Threshold | | 3.0 | 3.5 | 4.00 | V |
| **OSCILLATOR** | | | | | |
| Switching Frequency | FREQ = AGND | 200 | 250 | 300 | kHz |
| | FREQ = VL | 425 | 500 | 575 | |
| Maximum Duty Cycle | FREQ = AGND | 75 | 80 | 88 | % |
| | FREQ = VL | 75 | 80 | 88 | |

## Electrical Characteristics (continued)

(Circuit of Figure 1, $V_{IN}$ = 12V, $V_{EN}$ = $V_{SEQ}$ = 5V, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **SOFT-START** | | | | | |
| Step Size | Measured at FB | | 1.238/32 | | V |
| Period | FREQ = GND | | $1024/f_{OSC}$ | | s |
| | FREQ = VL | | $2048/f_{OSC}$ | | |
| **FET DRIVERS** | | | | | |
| DH, DL On-Resistance | | | 3 | 10 | Ω |
| DH, DL Output Drive Current | Sourcing or sinking, $V_{DH}$ or $V_{DL}$ = $V_{VL}$ / 2 | | 0.5 | | A |
| LX, BST Leakage Current | $V_{BST}$ = $V_{LX}$ = $V_{IN}$ = 28V | | | 20 | µA |
| **LINEAR REGULATOR CONTROLLERS** | | | | | |
| **POSITIVE LINEAR REGULATOR (LR1)** | | | | | |
| FBL1 Regulation Voltage | $V_{DRV1}$ = 5V, $I_{DRV1}$ = 100µA | 1.226 | 1.245 | 1.264 | V |
| FBL1 Input Bias Current | $V_{FBL1}$ = 1.5V | -50 | | +50 | nA |
| FBL1 Effective Load Regulation Error (Transconductance) | $V_{DRV1}$ = 5V, $I_{DRV1}$ = 100µA to 2mA | | -15 | -2 | % |
| FBL1 Line Regulation Error | $I_{DRV1}$ = 100µA, 5.5V < $V_{IN}$ < 28V | | | 5 | mV |
| DRV1 Sink Current | $V_{FBL1}$ = 1.175V, $V_{DRV1}$ = 5V | 3 | 10 | | mA |
| DRV1 Off-Leakage Current | $V_{FBL}$1 = 1.5V, $V_{DRV1}$ = 28V | | 0.1 | 10 | µA |
| FBL1 Input Common-Mode Range | (Note 2) | -0.1 | | +1.5 | V |
| Soft-Start Step Size | Measured at FBL1 | | 1.238 / 32 | | V |
| Soft-Start Period | FREQ = GND | | $1024/f_{OSC}$ | | s |
| | FREQ = VL | | $2048/f_{OSC}$ | | |
| **POSITIVE LINEAR REGULATORS (LR2 AND LR3)** | | | | | |
| FBL_ Regulation Voltage | $V_{DRV\_}$ = 5V, $I_{DRV\_}$ = 100µA | 1.226 | 1.245 | 1.264 | V |
| FBL_ Input Bias Current | $V_{FBL\_}$ = 1.5V | -50 | | +50 | nA |
| FBL_ Effective Load Regulation Error (Transconductance) | $V_{DRV\_}$ = 5V, $I_{DRV\_}$ = 50µA to 1mA | | -1.5 | -2 | % |
| FBL_ Line Regulation Error | $I_{DRV\_}$ = 100µA, 5.5V < $V_{IN}$ < 28V | | | 5 | mV |
| DRV_ Sink Current | $V_{FBL\_}$ = 1.175V, $V_{DRV\_}$ = 5V | 2 | 4 | | mA |
| DRV_ Off-Leakage Current | $V_{FBL\_}$ = 1.5V, $V_{DRV\_}$ = 28V | | 0.1 | 10 | µA |
| FBL_ Input Common-Mode Range | (Note 2) | -0.1 | | +1.5 | V |
| Soft-Start Step Size | Measured at FBL_ | | 1.238 / 32 | | V |

## Electrical Characteristics (continued)

(Circuit of Figure 1, $V_{IN}$ = 12V, $V_{EN}$ = $V_{SEQ}$ = 5V, **$T_A$ = 0°C to +85°C**, unless otherwise noted. Typical values are at $T_A$ = +25°C.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Soft-Start Period | FREQ = GND | | 1024 / $f_{OSC}$ | | s |
| | FREQ = VL | | 2048 / $f_{OSC}$ | | |
| **POSITIVE LINEAR REGULATOR (LR4)** | | | | | |
| FBL4 Regulation Voltage | $V_{DRV4}$ = 5V, $I_{DRV4}$ = 500µA | 1.226 | 1.245 | 1.264 | V |
| FBL4 Input Bias Current | $V_{FBL4}$ = 1.5V | -50 | | +50 | nA |
| FBL4 Effective Load Regulation Error (Transconductance) | $V_{DRV4}$ = 5V, $I_{DRV4}$ = 500µA to 10mA | | -1.5 | -2 | % |
| FBL4 Line Regulation Error | $I_{DRV4}$ = 500µA, 5.5V < $V_{IN}$ < 28V | | | 5 | mV |
| DRV4 Sink Current | $V_{FBL4}$ = 1.175V, $V_{DRV4}$ = 5V | 10 | 28 | | mA |
| DRV4_Off-Leakage Current | $V_{FBL4}$ = 1.5V, $V_{DRV4}$ = 28V | | 0.1 | 10 | µA |
| FBL4 Input Common-Mode Range | (Note 2) | -0.1 | | +1.5 | V |
| Soft-Start Step Size | Measured at FBL4 | | 1.238 / 32 | | V |
| Soft-Start Period | FREQ = GND | | 1024 / $f_{OSC}$ | | s |
| | FREQ = VL | | 2048 / $f_{OSC}$ | | |
| **NEGATIVE LINEAR REGULATOR (LR5)** | | | | | |
| FBL5 Regulation Voltage | $V_{DRV5}$ = -10V, $I_{DRV5}$ = 100µA | 100 | 125 | 150 | mV |
| FBL5 Input Bias Current | $V_{FBL5}$ = 0V | -50 | | +50 | nA |
| FBL5 Effective Load Regulation Error (Transconductance) | $V_{DRV5}$ = -10V, $I_{DRV5}$ = 50µA to 1mA | | -1.5 | -2 | % |
| FBL5 Line Regulation Error | $I_{DRV5}$ = 100µA, 5.5V < $V_{IN}$ < 28V | | | 5 | mV |
| DRV5 Source Current | $V_{FBL5}$ = 200mV, $V_{DRV5}$ = -10V | 2 | 9 | | mA |
| DRV5 Off-Leakage Current | $V_{FBL5}$ = 0V, $V_{DRV5}$ = -20V | | 0.1 | 10 | µA |
| FBL5 Input Common-Mode Range | (Note 2) | -0.1 | | +15 | V |
| Soft-Start Step Size | Measured at FBL5 | | 1.238 / 32 | | V |
| Soft-Start Period | FREQ = AGND | | 1024 / $f_{OSC}$ | | s |
| | FREQ = VL | | 2048 / $f_{OSC}$ | | |

## Electrical Characteristics

(Circuit of Figure 1, $V_{IN}$ = 12V, $V_{EN}$ = $V_{SEQ}$ = 5V, **$T_A$ = -40°C to +85°C**, unless otherwise noted.) (Note 3)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **GENERAL** | | | | | |
| Operating Input Voltage Range | (Note 1) | 4.5 | | 28.0 | V |
| **VL REGULATOR** | | | | | |
| VL Output Voltage | 5.5V < $V_{IN}$ < 28V, 0 < $I_{VL}$ < 30mA | 4.75 | | 5.25 | V |
| VL Undervoltage Lockout Threshold | VL rising, 3% hysteresis | 3.2 | | 3.8 | V |

## Electrical Characteristics (continued)

(Circuit of Figure 1, $V_{IN}$ = 12V, $V_{EN}$ = $V_{SEQ}$ = 5V, **$T_A$ = -40°C to +85°C**, unless otherwise noted.) (Note 3)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **CONTROL AND SEQUENCE** | | | | | |
| ONL_ Input Threshold | ONL_ rising, 25mV hysteresis | 1.201 | | 1.275 | V |
| EN Input Threshold | EN rising, 5% hysteresis | 1.201 | | 1.275 | V |
| FAULT DETECTION | | | | | |
| FB, FBL1, FBL2, FBL3, FBL4 Fault Trip Level | FB, FBL1, FBL2, FBL3, FBL4 falling, 25mV hysteresis | 1.081 | | 1.147 | V |
| FBL5 Fault Trip Level | FBL5 rising, 25mV hysteresis | 300 | | 500 | mV |
| Overcurrent Protection Threshold | ($V_{CSH}$ - $V_{CSL}$) | 270 | | 330 | mV |
| **RESET FUNCTION** | | | | | |
| RSTIN Reset Trip Level | RSTIN falling, 25mV hysteresis | 1.081 | | 1.147 | V |
| **STEP-DOWN CONTROLLER** | | | | | |
| **ERROR AMPLIFIER** | | | | | |
| FB Regulation Voltage | | 1.215 | | 1.260 | V |
| Current-Limit Threshold (Default Mode) | PGND - LX, ILIM = VL | 170 | | 330 | mV |
| Current-Limit Threshold (Adjustable Mode) | PGND - LX, $V_{ILIM}$ = 1.25V | 170 | | 330 | mV |
| **LINEAR REGULATOR CONTROLLERS** | | | | | |
| **POSITIVE LINEAR REGULATOR (LR1)** | | | | | |
| FBL1 Regulation Voltage | $V_{DRV1}$ = 5V, $I_{DRV1}$ = 100µA | 1.220 | | 1.270 | V |
| FBL1 Input Bias Current | $V_{FBL1}$ = 1.5V | -50 | | +50 | nA |
| **POSITIVE LINEAR REGULATORS (LR2 AND LR3)** | | | | | |
| FBL_ Regulation Voltage | $V_{DRV\_}$ = 5V, $I_{DRV\_}$ = 100µA | 1.220 | | 1.270 | V |
| FBL_ Input Bias Current | $V_{FBL\_}$ = 1.5V | -50 | | +50 | nA |
| **POSITIVE LINEAR REGULATOR (LR4)** | | | | | |
| FBL4 Regulation Voltage | $V_{DRV4}$ = 5V, $I_{DRV4}$ = 500µA | 1.220 | | 1.270 | V |
| FBL4 Input Bias Current | $V_{FBL4}$ = 1.5V | -50 | | +50 | nA |
| **NEGATIVE LINEAR REGULATOR (LR5)** | | | | | |
| FBL5 Regulation Voltage | $V_{DRV5}$ = -10V, $I_{DRV5}$ = 100µA | 100 | | 150 | mV |
| FBL5 Input Bias Current | $V_{FBL5}$ = 0V | -50 | | +50 | nA |
| DRV5 Source Current | $V_{FBL5}$ = 200mV, $V_{DRV5}$ = -10V | 2 | | | mA |

**Note 1:** Operating supply range is guaranteed by VL line regulation test for the range of 5.5V to 28V. Between 4.5V and 5.5V, the$V_L$ regulator might be in dropout; however, the part continues to operate properly.

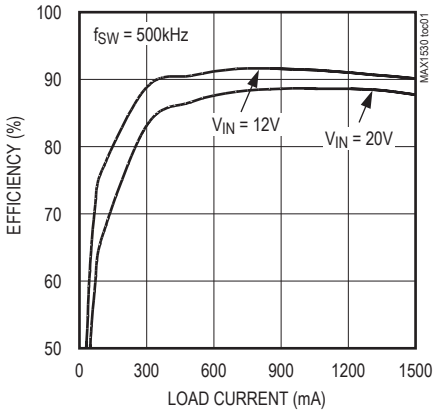
**Note 2:** Guaranteed by design and not production tested.

**Note 3:** Specifications to -40°C are guaranteed by design and not production tested.

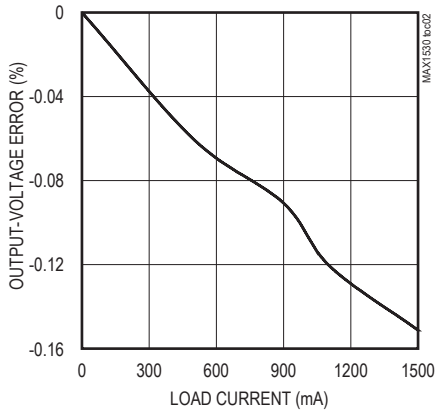
## Typical Operating Characteristics

(Circuit of Figure 1; including R5, R6, and D2; $T_A$ = +25°C, unless otherwise noted.)

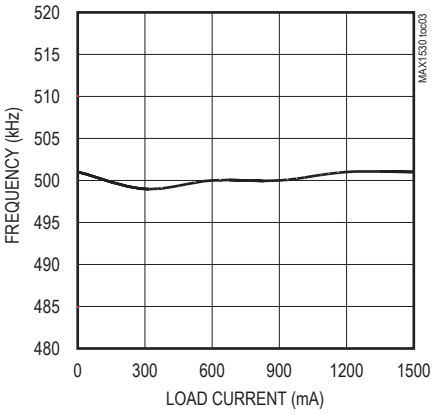
**STEP-DOWN EFFICIENCY vs. LOAD CURRENT**



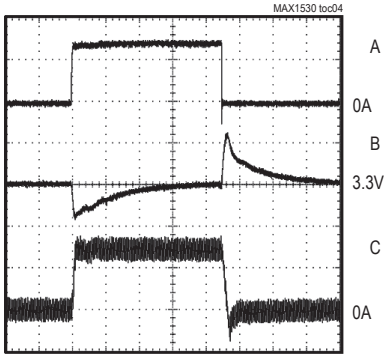

**STEP-DOWN LOAD REGULATION**




**SWITCHING FREQUENCY vs. LOAD CURRENT**



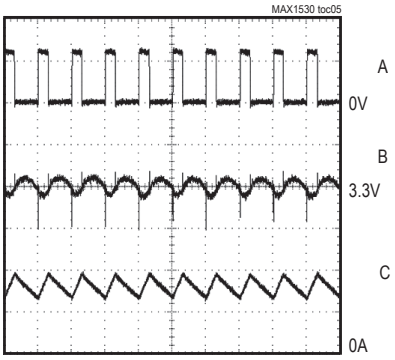

**STEP-DOWN REGULATOR LOAD TRANSIENT**




40µs/div

A: LOAD CURRENT, 1A/div
B: OUTPUT VOLTAGE, 200mV/div, AC-COUPLED
C: INDUCTOR CURRENT, 1A/div

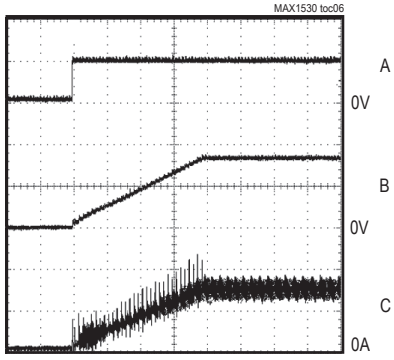
**STEP-DOWN REGULATOR SWITCHING WAVEFORM**




2µs/div

A: LX, 10V/div
B: OUTPUT VOLTAGE, 20 mV/div, AC-COUPLED
C: INDUCTOR CURRENT, 1A/div

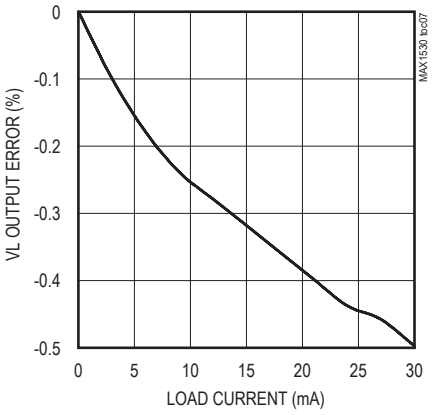
**STEP-DOWN REGULATOR SOFT-START**



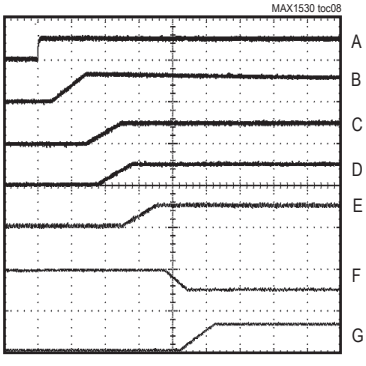

1µs/div

A: EN, 2V/div
B: OUTPUT VOLTAGE, 2V/div
C: INDUCTOR CURRENT, 1A/div

**VL LOAD REGULATION**



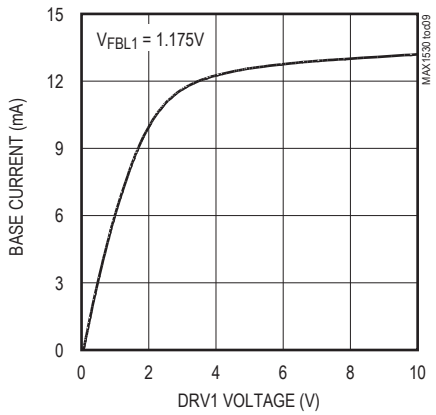

**STARTUP SEQUENCE**




4ms/div

A: $V_L$, 10V/div
B: $V_{OUT}$, 5V/div
C: $V_{LOGIC}$, 5V/div
D: $V_{SOURCE}$, 20V/div
E: $V_{GAMMA}$, 20V/div
F: $V_{GOFF}$, 20V/div
G: $V_{GON}$, 40V/div

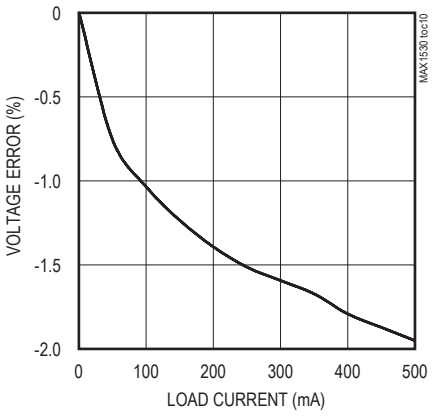
**LR1 BASE CURRENT vs. DRV1 VOLTAGE**



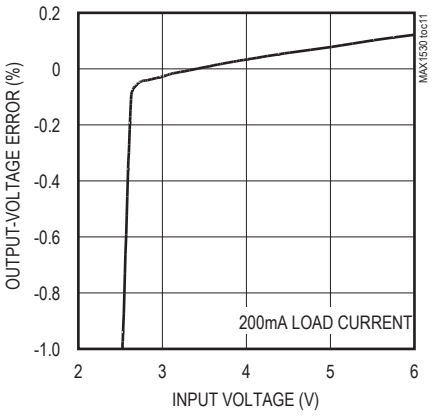
## Typical Operating Characteristics (continued)

(Circuit of Figure 1; including R5, R6, and D2; $T_A$ = +25°C, unless otherwise noted.)

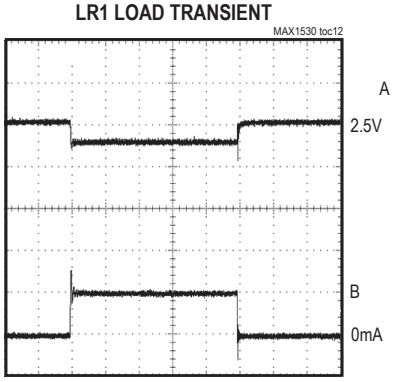
**LR1 NORMALIZED LOAD REGULATION**




**LR1 NORMALIZED LINE REGULATION**

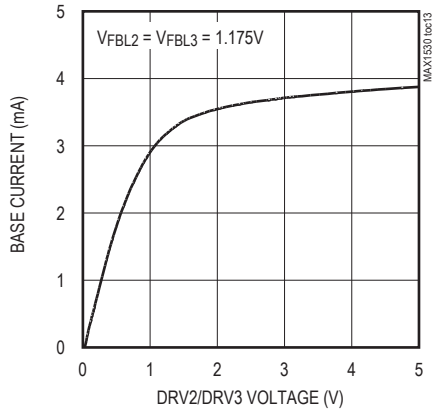



**LR1 LOAD TRANSIENT**

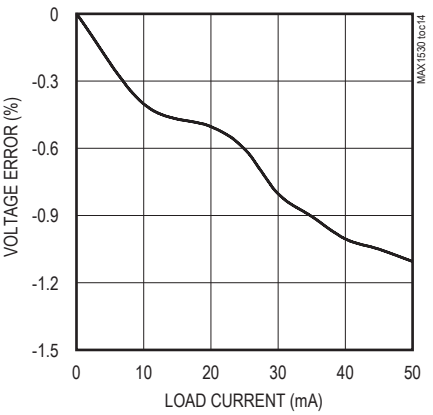



A: LR1 OUTPUT VOLTAGE, 100mV/div, AC-COUPLED
B: LR1 LOAD CURRENT, 500mA/div

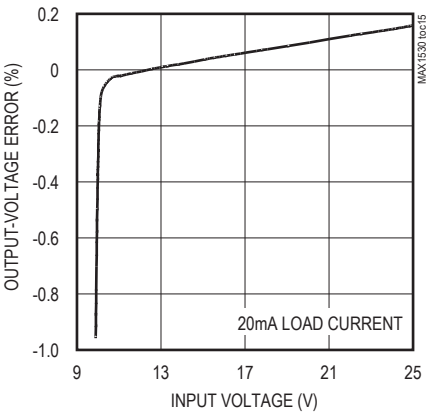
**LR2/LR3 BASE CURRENT vs. DRV2/DRV3 VOLTAGE**



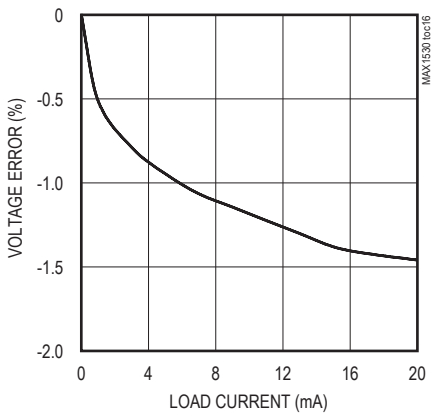

**LR2 NORMALIZED LOAD REGULATION**



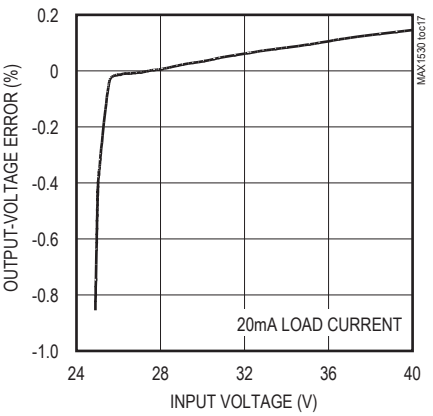

**LR2 NORMALIZED LINE REGULATION**



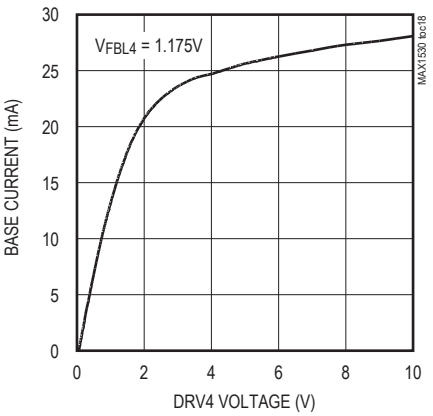

**LR3 NORMALIZED LOAD REGULATION**




**LR3 NORMALIZED LINE REGULATION**



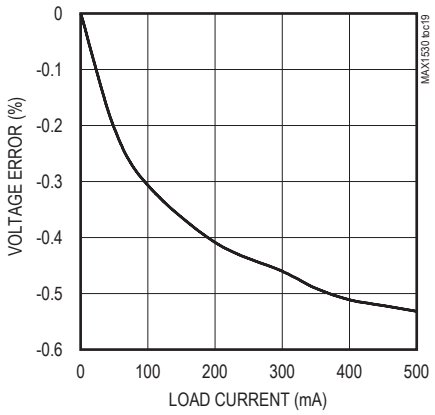

**LR4 BASE CURRENT vs. DRV VOLTAGE**



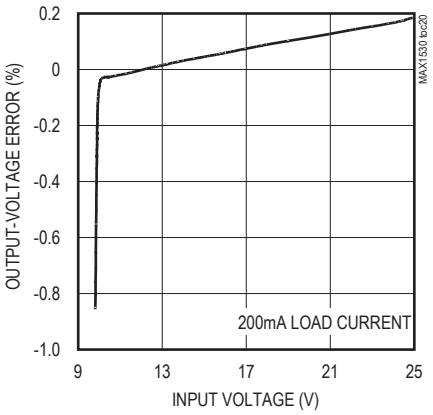
## Typical Operating Characteristics (continued)

(Circuit of Figure 1; including R5, R6, and D2; $T_A$ = +25°C, unless otherwise noted.)

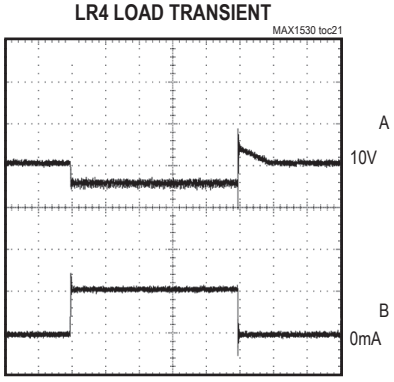
**LR4 NORMALIZED LOAD REGULATION**




**LR4 NORMALIZED LINE REGULATION**

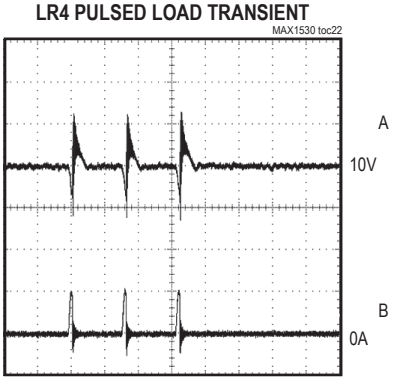



**LR4 LOAD TRANSIENT**



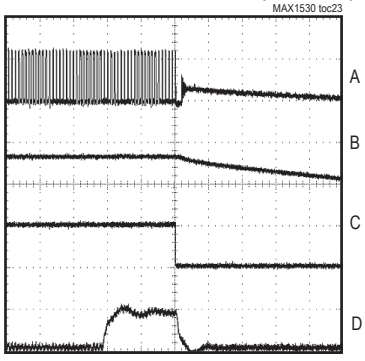

40µs/div
A: LR4 OUTPUT VOLTAGE, 100mV/div, AC-COUPLED
B: LR4 LOAD CURRENT, 500mA/div

**LR4 PULSED LOAD TRANSIENT**



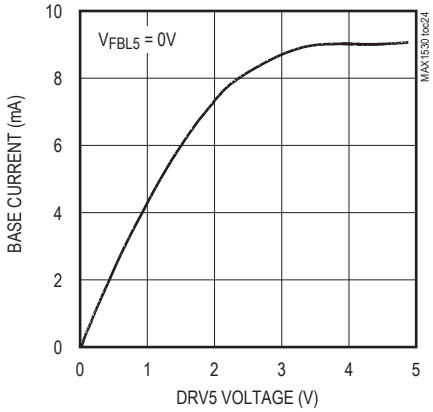

10µs/div
A: LR4 OUTPUT VOLTAGE, 100mV/div, AC-COUPLED
B: LR4 LOAD CURRENT, 1A/div

**MAX1531**
**OVERCURRENT PROTECTION (CSH, CSL)**



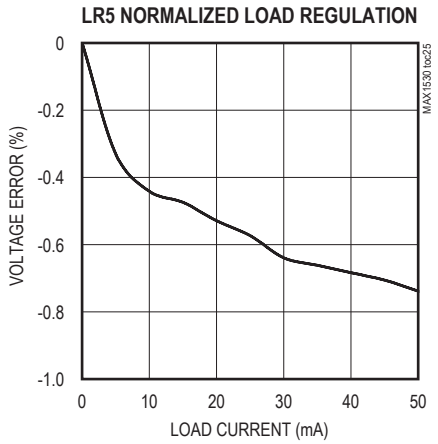

20µs/div
A: $V_{LX}$, 10V/div
B: $V_{OUT}$, 5V/div
C: $V_{RESET}$, 5V/div
D: $V_{CSH}$ - $V_{CSL}$, 500mV/div

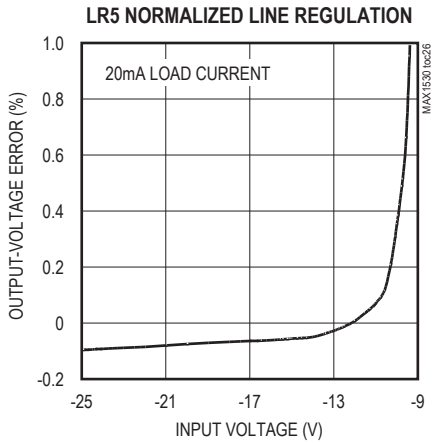
**LR5 BASE CURRENT**
**vs. DRV5 VOLTAGE**



## Typical Operating Characteristics (continued)

(Circuit of Figure 1; including R5, R6, and D2; $T_A$ = +25°C, unless otherwise noted.)




## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX1530 | MAX1531 | | |
| 1 | 1 | DRV2 | Gamma Linear Regulator (LR2) Base Drive. Open drain of an internal N-channel MOSFET. Connect DRV2 to the base of an external PNP pass transistor to form a positive linear regulator. (See the *Pass Transistor Selection* section.) |
| 2 | 2 | FBL2 | Gamma Linear Regulator (LR2) Feedback Input. FBL2 regulates at 1.245V nominal. Connect FBL2 to the center tap of a resistive voltage-divider between the LR2 output and AGND to set the output voltage. Place the divider close to the FBL2 pin. |
| 3 | 3 | FBL3 | Gate-On Linear Regulator (LR3) Feedback Input. FBL3 regulates at 1.245V nominal. Connect FBL3 to the center tap of a resistive voltage-divider between the LR3 output and AGND to set the output voltage. Place the divider close to the FBL3 pin. |
| 4 | 4 | DRV3 | Gate-On Linear Regulator (LR3) Base Drive. Open drain of an internal N-channel MOSFET. Connect DRV3 to the base of an external PNP pass transistor to form a positive linear regulator. (See the *Pass Transistor Selection* section.) |
| 5–10, 18, 19 | — | N. C. | No Connection. Not internally connected. |
| 11 | 11 | RSTIN | Adjustable Reset Input. RESET asserts low when the monitored voltage is less than the reset trip threshold. RESET goes to a high-impedance state only after the monitored voltage remains above the reset trip threshold for the duration of the reset timeout period. Connect RSTIN to the center tap of a resistive voltage-divider between the monitored output voltage and AGND to set the reset trip threshold. The internal RSTIN threshold of 90% of 1.238V allows direct connection of RSTIN to any of the device's positive feedback pins. |

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX1530 | MAX1531 | | |
| 12 | 12 | RESET | Open-Drain Reset Output. RESET asserts low when the monitored voltage is less than the reset trip threshold. RESET goes to a high-impedance state only after the monitored voltage remains above the reset trip threshold for the duration of the reset timeout period. RESET also asserts low when VL is less than the VL undervoltage lockout threshold, EN is low, or the thermal, overcurrent or undervoltage fault latches are set. |
| 13 | 13 | COMP | Step-Down Regulator Compensation Input. A pole-zero pair must be added to compensate the control loop by connecting a series resistor and capacitor from COMP to AGND. (See the *Compensation Design* section.) |
| 14 | 14 | FB | Step-Down Regulator Feedback Input. FB regulates at 1.238V nominal. Connect FB to the center tap of a resistive voltage-divider between the step-down regulator output and AGND to set the output voltage. Place the divider close to the FB pin. |
| 15 | 15 | ILIM | Step-Down Regulator Current-Limit Control Input. Connect this dual-mode input to VL to set the current-limit threshold to its default value of 250mV. The overcurrent comparator compares the voltage across the low-side N-channel MOSFET with the current-limit threshold. Connect ILIM to the center tap of a resistive voltage-divider between VL and AGND to adjust the current-limit threshold to other values. In adjustable mode, the actual current-limit threshold is 1/5th of the voltage at ILIM over a 0.25V to 3.0V range. The dual- mode threshold for switchover to the 250mV default value is approximately 3.5V. |
| 16 | 16 | ONL2 | Gamma Linear Regulator (LR2) Enable Input. When EN is above its enable threshold, VL is above its UVLO threshold, and ONL2 is greater than the internal reference, LR2 is enabled. Drive ONL2 with a logic signal or, for automatic sequencing, connect a capacitor from ONL2 to AGND. If SEQ is high, EN is above its threshold, and VL is above its UVLO threshold, an internal 2µA (typ) current source charges the capacitor. Otherwise, an internal switch discharges the capacitor. Connecting various capacitors to each ONL_ pin allows the programming of the startup sequence. |
| 17 | 17 | ONL3 | Gate-On Linear Regulator (LR3) Enable Input. When EN is above its enable threshold, VL is above its UVLO threshold, and ONL3 is greater than the internal reference, LR3 is enabled. Drive ONL3 with a logic signal or, for automatic sequencing, connect a capacitor from ONL3 to AGND. If SEQ is high, EN is above its threshold, and VL is above its UVLO threshold, an internal 2µA (typ) current source charges the capacitor. Otherwise, an internal switch discharges the capacitor. Connecting various capacitors to each ONL_ pin allows the programming of the startup sequence. |
| 20 | 20 | PGND | Power Ground |
| 21 | 21 | DL | Low-Side Gate Driver Output. DL drives the synchronous rectifier of the step-down regulator. DL swings from PGND to VL. DL remains low until VL rises above the UVLO threshold. |
| 22 | 22 | LX | Step-Down Regulator Current-Sense Input. The IC's current-sense amplifier inputs for current-mode control connect to IN and LX. Connect IN and LX directly to the high-side N- channel MOSFET drain and source, respectively. The low-side current-limit comparator inputs connect to LX and PGND to sense voltage across a low-side N-channel MOSFET. |

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX1530 | MAX1531 | | |
| 23 | 23 | DH | High-Side Gate Driver Output. DH drives the main switch of the step-down regulator. DH swings from LX to BST. |
| 24 | 24 | BST | Step-Down Regulator Boostrap Capacitor Connection for High-Side Gate Driver. Connect a 0.1µF ceramic capacitor from BST to LX. |
| 25 | 25 | SEQ | Sequence Control Input for LR2, LR3, LR4, and LR5. Controls the current sources and switches that charge and discharge the capacitors connected to the ONL_ pins. |
| 26 | 26 | FREQ | Oscillator Frequency Select Input. Connect FREQ to VL for 500kHz operation. Connect FREQ to AGND for 250kHz operation. |
| 27 | 27 | IN | Main Input Voltage (+4.5V to 28V). Bypass IN to AGND with a 1µF ceramic capacitor close to the pins. IN powers the VL linear regulator. Connect IN to the drain of the high-side MOSFET (for current sense) through a 1Ω resistor. |
| 28 | 28 | VL | Internal 5V Linear Regulator Output. Connect a minimum 1µF ceramic capacitor from VL to AGND. Place the capacitor close to the pins. VL can supply up to 30mA for gate drive and external loads. VL remains active when EN is low. |
| 29 | 29 | AGND | Analog Ground |
| 30 | 30 | EN | Enable Input. This general-purpose on/off control input has an accurate 1.238V (typ) rising threshold with 5% hysteresis. This allows EN to monitor an input voltage level or other analog parameter. If EN is less than its threshold, then the main step-down and all linear regulators are turned off. VL and the internal reference remain active when EN is low. The rising edge of EN clears any latched faults except for a thermal fault, which is cleared only by cycling the input power. An internal filter with a 10µs time constant prevents short glitches from accidentally clearing the fault latch. |
| 31 | 31 | FBL1 | Low-Voltage Logic Linear Regulator (LR1) Feedback Input. FBL1 regulates at 1.245V nominal. Connect FBL1 to the center tap of a resistive voltage-divider between LR1 output AGND to set the output voltage. Place the divider close to the FBL1 pin. LR1 starts automatically after the step-down converter soft-start ends. |
| 32 | 32 | DRV1 | Low-Voltage Logic Linear Regulator (LR1) Base Drive. Open drain of an internal N-channel MOSFET. Connect DRV1 to the base of an external PNP pass transistor. (See the *Pass Transistor Selection* section.) |
| — | 5 | CSH | Overcurrent Protection Positive Input. CSH is also the supply input for the overcurrent sense block. CSH and CSL can be used to sense any current in the application circuit and to shut the device down in an overcurrent condition. This feature is typically used to protect the main input or the input to one of the linear regulators since they do not have their own current limits. Insert an appropriate sense resistor in series with the protected input and connect CSH and CSL to its positive and negative terminals. The controller sets the fault latch when $V_{CSH}$ - $V_{CSL}$ exceeds the 300mV (typ) overcurrent threshold. An internal lowpass filter prevents large currents of short duration (less than 50µs) or noise glitches from setting the latch. If the overcurrent protection is not used, connect CSH and CSL to VL. |
| — | 6 | CSL | Overcurrent Protection Negative Input. See CSH above. |

## Pin Description (continued)

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX1530 | MAX1531 | | |
| — | 7 | FBL4 | Source Drive Linear Regulator (LR4) Feedback Input. FBL4 regulates at 1.245V nominal. Connect FBL4 to the center tap of a resistive voltage-divider between the LR4 output and AGND to set the output voltage. Place the divider close to the FBL4 pin. |
| — | 8 | DRV4 | Source Drive Linear Regulator (LR4) Base Drive. Open drain of an internal N-channel MOSFET. Connect DRV4 to the base of an external PNP pass transistor to form a positive linear regulator. (See the *Pass Transistor Selection* section.) |
| — | 9 | FBL5 | Gate-Off Linear Regulator (LR5) Feedback Input. FBL5 regulates at 125mV nominal. Connect FBL5 to the center tap of a resistive voltage-divider between the LR5 output and the internal 5V linear regulator output (VL) to set the output voltage. Place the divider close to the FBL5 pin. |
| — | 10 | DRV5 | Gate-Off Linear Regulator (LR5) Base Drive. Open drain of an internal P-channel MOSFET. Connect DRV5 to the base of an external NPN pass transistor to form a negative linear voltage regulator. (See the *Pass Transistor Selection* section.) |
| — | 18 | ONL4 | Source Drive Linear Regulator (LR4) Enable Input. When EN is above its enable threshold, VL is above its UVLO threshold, and ONL4 is greater than the internal reference, LR4 is enabled. Drive ONL4 with a logic signal or, for automatic sequencing, connect a capacitor from ONL4 to AGND. If SEQ is high, EN is above its threshold, and VL is above its UVLO threshold, an internal 2µA (typ) current source charges the capacitor. Otherwise, an internal switch discharges the capacitor. Connecting various capacitors to each ONL_ pin allows the programming of the startup sequence. |
| — | 19 | ONL5 | Gate-Off Linear Regulator (LR5) Enable Input. When EN is above its enable threshold, VL is above its UVLO threshold, and ONL5 is greater than the internal reference, LR5 is enabled. Drive ONL5 with a logic signal or, for automatic sequencing, connect a capacitor from ONL5 to AGND. If SEQ is high, EN is above its threshold, and VL is above its UVLO threshold, an internal 2µA (typ) current source charges the capacitor. Otherwise, an internal switch discharges the capacitor. Connecting various capacitors to each ONL_ pin allows the programming of the startup sequence. |
| — | — | EP | Exposed Paddle. Internally connected to GND. Connect EP to a large ground plane to improve thermal dissipation. Do not use as the main ground connection of the IC. |

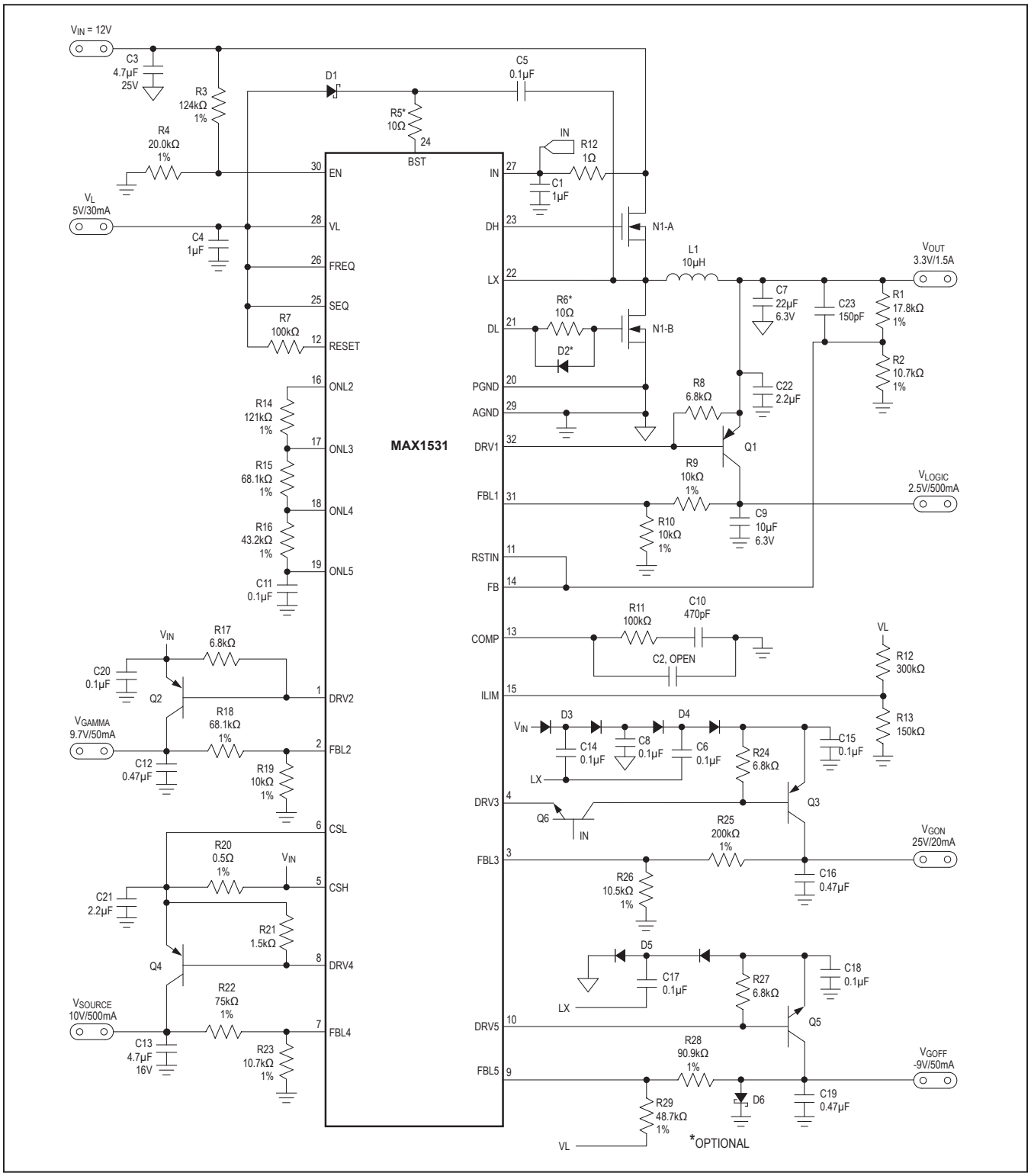



*Figure 1. MAX1531 Standard Application Circuit*

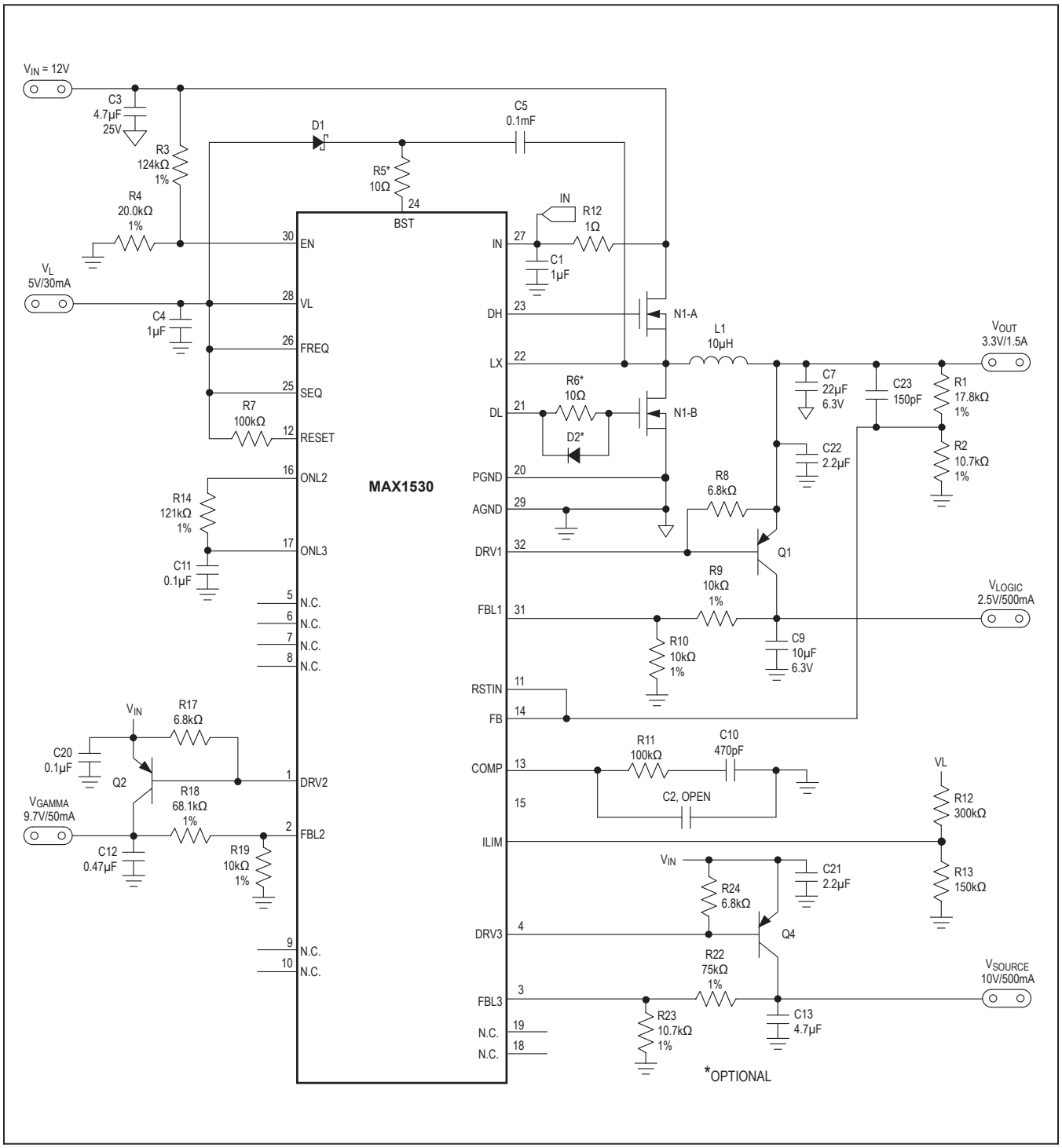



*Figure 2. MAX1530 Standard Application Circuit*

## Table 1. Selected Component List

| DESIGNATION | DESCRIPTION |
|---|---|
| C3 | 4.7µF, 25V X7R ceramic capacitor (1210) TDK C3225X7R1E475K |
| C7 | 22µF, 6.3V X7R ceramic capacitor TDK C3216X7R0J226M |
| C9 | 10µF, 6.3V X5R ceramic capacitor TDK C2012X5R0J106M |
| C12, C19* | 0.47µF, 16V X7R ceramic capacitors (0805) TDK C2012X7R1C474K |
| C13 | 4.7µF, 16V X7R ceramic capacitor TDK C3216X7R1C475K |
| C21, C22 | 2.2µF, 25V X7R ceramic capacitors (1206) TDK C3216X7R1C475M |
| D1, D6* | 100mA, 30V Schottky diodes (SOD523) Central Semiconductor CMOSH-3 |
| D2 | 100mA, 75V, small-signal switching diode, SOT23 Fairchild Semiconductor MMBD4148 |
| D3*, D4*, D5* | 200mA, 25V dual Schottky diodes (SOT23) Fairchild BAT54S |
| L1 | 10µH, 2.3A (DC) inductor Sumida CDR7D28MN-100 |
| N1 | 2.5A, 30V dual N-channel MOSFET (6-pin Super SOT) Fairchild FDC6561AN |
| Q1, Q4 | 3A, 60V low-saturation PNP bipolar transistors (SOT-223) Fairchild NZT660A |
| Q2, Q3* | 200mA, 40V PNP bipolar transistors (SOT23) Fairchild MMBT3906 |
| Q5*, Q6* | 200mA, 40V NPN bipolar transistors (SOT23) Fairchild MMBT3904 |

**For MAX1531 only.*

## Table 2. Component Suppliers

| SUPPLIER | PHONE | FAX | WEBSITE |
|---|---|---|---|
| Central Semi | 516-435-1110 | 516-435-1824 | www.centralsemi.com |
| Fairchild | 888-522-5372 | 972-910-8036 | www.fairchildsemi.com |
| Sumida | 847-956-0666 | 847-956-0702 | www.sumida.com |
| TDK | 847-803-6100 | 847-390-4405 | www.components.tdk.com |

## Standard Application Circuit

The standard application circuit (Figure 1) of the MAX1531 is a complete power-supply system for TFT LCD monitors. The circuit generates a 3.3V/1.5A main output, a 2.5V/500mA output for the timing controller and digital sections of source/gate drive ICs, a 10V/500mA source drive supply voltage, a 9.7V/50mA gamma reference, a 25V/20mA gate-on voltage, and a -10V/50mA gate-off voltage. The input voltage is 12V ±10%. Table 1 lists the selected components and Table 2 lists the component suppliers. The standard application circuit (Figure 2) of the MAX1530 is similar to the MAX1531 application circuit except that gate-on and gate-off voltages are eliminated.

## Detailed Description

The MAX1530/MAX1531 power-supply controllers provide logic and bias power for LCD monitors. Figure 3 shows the IC functional diagram. The main step-down controller employs a current-mode PWM control method to ease compensation requirements and provide excellent load- and line-transient response. The use of synchronous rectification yields excellent efficiency.

The MAX1530 includes three analog gain blocks to control three auxiliary positive linear regulators, and the MAX1531 includes five analog gain blocks to control four positive and one negative linear regulators. Use the positive gain blocks to generate low-voltage rails directly from the input voltage or the main step-down converter output, or higher voltages using charge pumps attached to the switching node or

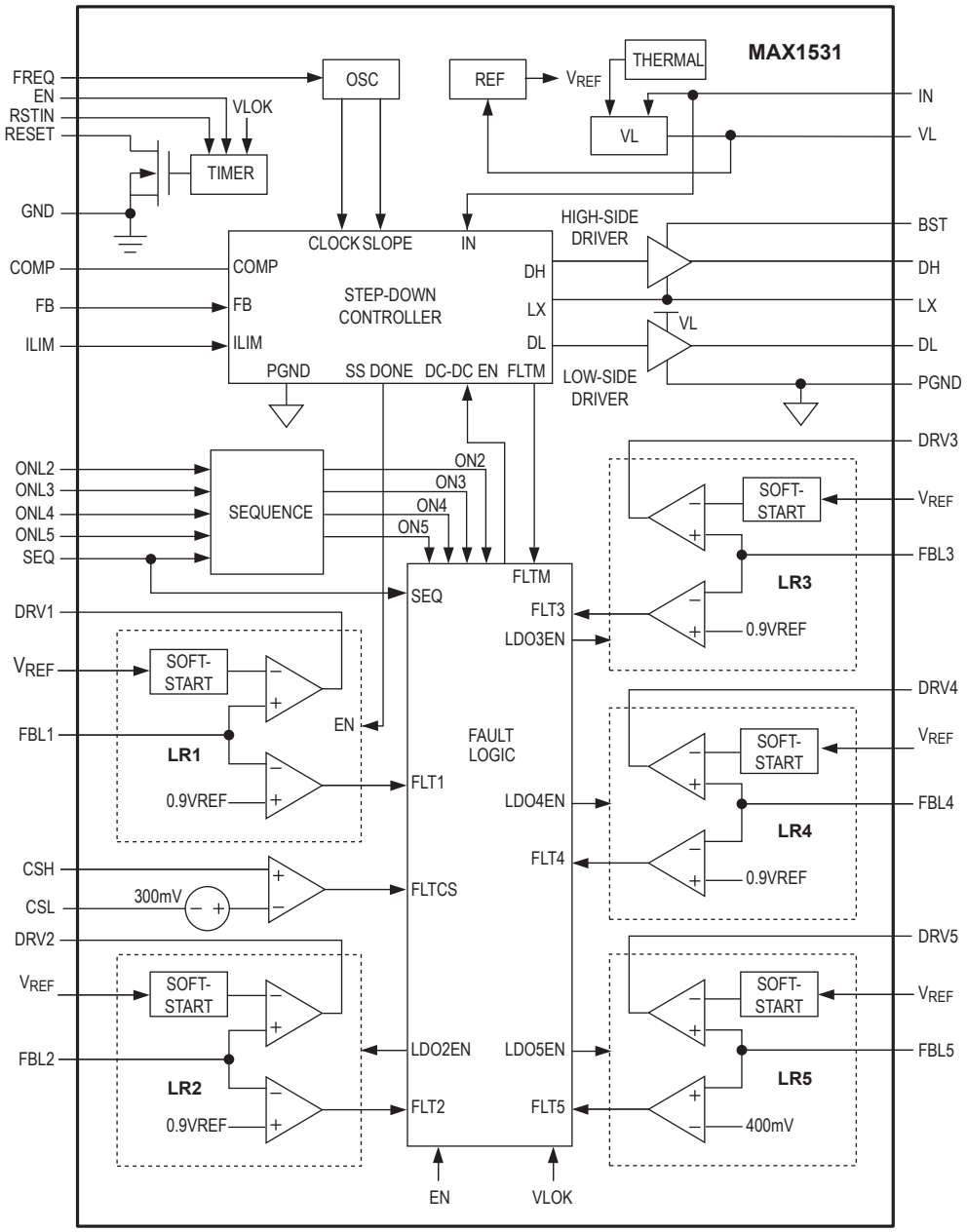



*Figure 3. IC Functional Diagram*

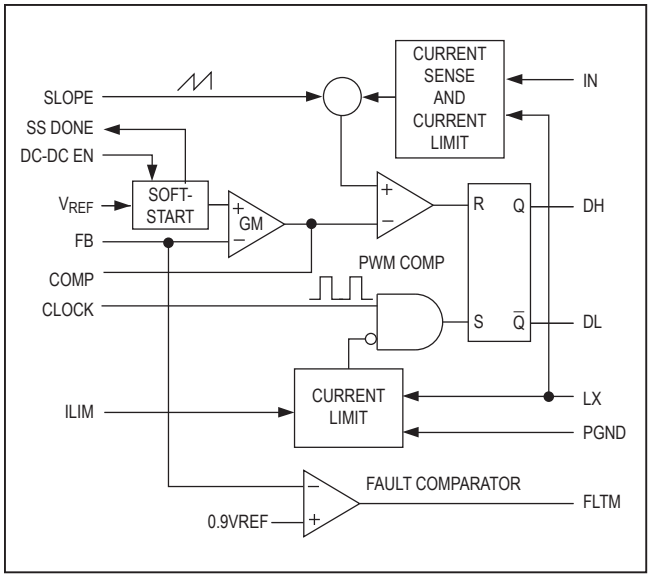



*Figure 4. Step-Down Controller Block Diagram*

extra windings coupled to the step-down converter inductor. The negative gain block (MAX1531) can be used in conjunction with a charge pump or coupled winding to generate the LCD gate-off voltage or other negative supplies.

## Step-Down Controller

The MAX1530/MAX1531 include step-down controllers that use a fixed-frequency current-mode PWM control scheme (Figure 4). An internal transconductance amplifier establishes an integrated error voltage at the COMP pin. The heart of the current-mode PWM controller is an open-loop comparator that compares an integrated voltage-feedback signal with an amplified current-sense signal plus a slope-compensation ramp. At each rising edge of the internal clock, the high-side MOSFET turns on until the PWM comparator trips or the maximum duty cycle is reached. During this on-time, current ramps up through the inductor, sourcing current to the output and storing energy in a magnetic field. The current-mode feedback system regulates the peak inductor current as a function of the output voltage error signal. Since the average inductor current is nearly the same as the peak inductor current (assuming that the inductor value is relatively high to minimize ripple current), the circuit acts as a switch-mode transconductance amplifier. That pushes the output LC filter pole, normally found in a voltage-mode PWM, to a higher frequency. To preserve loop stability, the slopecompensation ramp is summed into the main PWM comparator.

During the second half of the cycle, the high-side MOSFET turns off and the low-side N-channel MOSFET turns on. Now the inductor releases the stored energy as its current ramps down, providing current to the output. The output capacitor stores charge when the inductor current exceeds the load current and discharges when the inductor current is lower, smoothing the voltage across the load. Under overload conditions, when the inductor current exceeds the selected current limit (see *Current Limit Circuit*), the high-side MOSFET is not turned on at the rising edge of the clock and the lowside MOSFET remains on to let the inductor current ramp down.

Under light-load conditions, the MAX1530/MAX1531 maintain a constant switching frequency to minimize cross-regulation errors in applications that use a transformer. The low-side gate-drive waveform is the complement of the high-side gate-drive waveform, which causes the inductor current to reverse under light loads.

### Current-Sense Amplifier

The MAX1530/MAX1531s' current-sense circuit amplifies the current-sense voltage generated by the highside MOSFET's on-resistance. This amplified current-sense signal and the internal slope compensation signal are summed together and fed into the PWM comparator's inverting input. Place the high-side MOSFET near the controller, and connect IN and LX to the MOSFET using Kelvin-sense connections to guarantee current-sense accuracy and improve stability.

### Current-Limit Circuit

The MAX1530/MAX1531 include two current-limit circuits that use the two MOSFETs' on-resistances as current-sensing elements (Figure 4). The high-side MOSFET's voltage is used with a fixed 400mV (typ) current- limit threshold during the high-side on-times. The low-side MOSFET's voltage is used with an adjustable current-limit threshold during the low-side on-times. Using both circuits together ensures that the current is always measured and controlled.

The high-side MOSFET current limit employs a peak current limit. If the voltage across the high-side MOSFET, measured from IN to LX, exceeds the 400mV threshold during an on-time, the high-side MOSFET turns off and the low-side MOSFET turns on.

The low-side MOSFET current-limit circuit employs a "valley" current limit. If the voltage across the low-side MOSFET, measured from LX to PGND, exceeds the low-side threshold at the end of a low-side on-time, the low-side MOSFET remains on and the high-side MOSFET stays off for the entire next cycle.

The ILIM pin is a dual-mode input. When ILIM is connected to VL, a default low-side current limit of 250mV typ) is used. If ILIM is connected to a voltage between 250mV and 3V, the low-side current limit is typically 1/5th the ILIM voltage.

The MAX1530/MAX1531s' current limits are comparatively inaccurate, since the maximum load current is a function of the MOSFETs' on-resistances and the inductor value, as well as the accuracy of the two thresholds. However, using MOSFET current sensing reduces both cost and circuit size and increases efficiency, since sense resistors are not needed.

### MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderate-size high-side and low-side MOSFETs. Adaptive dead-time circuits monitor the DL and DH drivers and prevent either FET from turning on until the other is fully off. This algorithm allows operation without shoot- through with a wide range of MOSFETs, minimizing delays and maintaining efficiency. When the gates are turning off, there must be low-resistance, low-induc- tance paths from the gate drivers to the MOSFET gates for the adaptive dead-time circuit to work properly. Otherwise, the sense circuitry in the MAX1530/ MAX1531 interpret the MOSFET gate as "off" while gate charge actually remains. Use short, wide traces mea- suring less than 50 squares (at least 20 mil wide if the MOSFET is 1in from the device). It is advantageous to slow down the turn-on of both gate drivers if there is noise coupling between the switching regulator and the linear regulators. The noise coupling can result in excessive switching ripple on the linear regulator outputs. Slowing down the turn-on of the gate drivers proves to be an effective way of reduc- ing the output ripple. Take care to ensure that the turn- off times are not affected at the same time. As explained above, slowing down the turn-off times may result in shoot-through problems. In Figure 1, a 10Ω resistor (R5) is inserted in series with the BST pin to slow down the turn-on of the high-side MOSFET (N1-B) without affecting the turn-off. A 10Ω resistor (R6) is also inserted between DL and the gate of the low-side MOS- FET (N1-A) to slow its turn-on. Because the gate resis- tor would slow down the turn-off time, connect a switching diode (D2) (such as 1N4148) in parallel with the gate resistor as shown in Figure 1 to prevent poten- tial shoot-through.

### High-Side Gate-Drive Supply (BST)

A flying-capacitor bootstrap circuit generates gate- drive voltage for the high-side N-channel switch (Figure 1). The capacitor C5 between BST and LX is alternately charged from the VL supply and placed parallel to the high-side MOSFET's gate-source terminals.

On startup, the synchronous rectifier (low-side MOSFET) forces LX to ground and charges the boost capacitor from VL through diode D1. On the second half-cycle, the switch-mode power supply turns on the high-side MOSFET by closing an internal switch between BST and DH. This provides the necessary gate-to-source voltage to turn on the high-side switch, an action that boosts the 5V gate-drive signal above the input voltage.

### Oscillator Frequency Selection (FREQ)

The FREQ pin can be used to select the switching frequency of the step-down regulator. Connect FREQ to VL for 500kHz operation. Connect FREQ to AGND for 250kHz operation. The 500kHz operation minimizes the size of the inductor and capacitors. The 250kHz operation improves efficiency by 2% to 3%.

## Linear Regulator Controllers

The MAX1530/MAX1531 include three positive linear regulator controllers, LR1, LR2, and LR3. These linear regulator controllers can be used with external pass transistors to regulate supplies for TFT LCDs. The MAX1531 includes an additional positive linear regula- tor controller (LR4) and a negative linear regulator con- troller (LR5).

### Low-Voltage Logic Regulator Controller (LR1)

LR1 is an analog gain block with an open-drain N- channel output. It drives an external PNP pass transis- tor with a 6.8kΩ base-to-emitter resistor. Its guaranteed base drive sink current is at least 3mA. The regulator including transistor Q1 in Figure 1 uses a 10µF output capacitor and is designed to deliver 500mA at 2.5V.

LR1 is typically used to generate low-voltage logic supplies for the timing controller and the digital sections of the TFT LCD source/gate driver ICs.

LR1 is enabled when the soft-start of the main step-down regulator is complete. (See the Startup Sequence (ONL_,SEQ) section.) Each time it is enabled, the controller goes through a soft-start routine that ramps up its internal reference DAC. (See the *Soft-Start* section.)

### Gamma Regulator Controller (LR2) LR2

is an analog gain block with an open-drain N- channel output. It drives an external PNP pass transis- tor with a 6.8kΩ base-to-emitter resistor. Its guaranteed base drive sink current is at least 2mA. The regulator including transistor Q2 in Figure 1 uses a 0.47µF output capacitor and is designed to deliver 50mA at 9.7V.

LR2 is typically used to generate the TFT LCD gamma reference voltage, which is usually 0.3V below the source drive supply voltage.

LR2 is enabled when the step-down regulator is enabled and the voltage on ONL2 exceeds ONL2 input threshold (1.238V typ). (See the *Startup Sequence (ONL_,SEQ)* section.) Each time it is enabled, the controller goes through a soft-start routine that ramps up its internal reference DAC. (See the *Soft-Start* section).

## Linear Regulator Controller (LR3)

LR3 is an analog gain block with an open-drain Nchannel output. It drives an external PNP pass transistor with a 6.8kΩ base-to-emitter resistor. Its guaranteed base drive sink current is at least 2mA. The regulator, including Q3 in Figure 1, uses a 0.47µF output capacitor and is designed to deliver 20mA at 25V. The regulator including Q3 in Figure 2 uses a 4.7µF output capacitor and is designed to deliver 500mA at 10V.

For the MAX1531 (Figure 1), LR3 is typically used to generate the TFT LCD gate driver's gate-on voltage. A sufficient input voltage can be produced using a charge-pump circuit as shown in Figure 1. Note that the voltage rating of the DRV3 output is 28V. If higher voltages are present, an external cascode NPN transistor (Q6) should be used with the emitter connected to DRV3, the base to $V_{IN}$ (which is the connection point of C1 and R12 in Figure 1), and the collector to the base of the PNP pass transistor (Figure 1). For the MAX1530 (Figure 2), LR3 is typically used to generate the TFT LCD source drive supply voltage. The input for this regulator can come directly from the input supply, be produced from an external step-up regulator, or from an extra windingcoupled to the main step-down regulator inductor.

LR3 is enabled when the step-down regulator is enabled and the voltage on ONL3 exceeds the ONL3 input threshold (1.238V typ). (See the *Startup Sequence (ONL_,SEQ)* section.) Each time it is enabled, the controller goes through a soft-start routine that ramps up its internal reference DAC. (See the *Soft-Start* section.)

### Source Drive Regulator Controller (LR4) (MAX1531 Only)

LR4 is an analog gain block with an open-drain Nchannel output. It drives an external PNP pass transistor with a 1.5kΩ base-to-emitter resistor. Its guaranteed base drive sink current is at least 10mA. The regulator including Q4 in Figure 1 uses a 4.7µF output capacitor and is designed to deliver 500mA at 10V. The regulator's fast transient response allows it to handle brief peak currents up to 2A.

LR4 is typically used to generate the TFT LCD source drive supply voltage. The input for this regulator can come directly from the input supply, be produced from an external step-up regulator, or from an extra winding coupled to the main step-down regulator inductor. LR4 is enabled when the step-down regulator is enabled and the voltage on ONL4 exceeds the ONL4 input threshold (1.238V typ). (See the *Startup Sequence (ONL_,SEQ*) section.) Each time it is enabled, the regulator goes through a soft-start routine that ramps up its internal reference DAC from 0V to 1.238V (typ). (See the *Soft-Start* section.)

The standard application circuit in Figure 1 powers the LR4 regulator directly from the input supply and uses the MAX1531's general-purpose overcurrent protection function to protect the input supply from excessive load currents. (See the *Overcurrent Protection* section.)

### Gate-Off Regulator Controller (LR5) (MAX1531 Only)

LR5 is an analog gain block with an open-drain P-channel output. It drives an external NPN pass transistor with a 6.8kΩ base-to-emitter resistor. Its guaranteed base drive sink current is at least 2mA. The regulator including Q5 in Figure 1 uses a 0.47µF output capacitor and is designed to deliver 10mA at -10V.

LR5 is typically used to generate the TFT LCD gate driver's gate-off voltage. A negative input voltage can be produced using a charge-pump circuit as shown in Figure 1. Use as many stages as necessary to obtain the required output voltage.

LR5 is enabled when the step-down regulator is enabled and the voltage on ONL5 exceeds the ONL5 input threshold (1.238V typ). (See the *Startup Sequence (ONL_,SEQ)* section.) Each time it is enabled, the regulator goes through a soft-start routine that ramps down its internal reference DAC from VL to 125mV (typ). (See the *Soft-Start* section.)

## Internal 5V Linear Regulator (VL)

All MAX1530/MAX1531 functions, except the thermal sensor, are internally powered from the on-chip, lowdropout 5V regulator. The maximum regulator input voltage ($V_{IN}$) is 28V. Bypass the regulator's output (VL) with at least a 1µF ceramic capacitor to AGND. The $V_{IN}$-to-VL dropout voltage is typically 200mV, so when $V_{IN}$ is less than 5.2V, VL is typically $V_{IN}$ - 200mV. The internal linear regulator can source up to 30mA to supply the device, power the low-side gate driver, charge the external boost capacitor, and supply small external loads. When driving particularly large MOSFETs, little or no regulator current may be available for external loads. For example, when

switched at 500kHz, large MOSFETs with a total of 40nC total gate charge would require 40nC × 500kHz, which is approximately 20mA.

## On/Off Control (EN)

The EN pin has an accurate 1.238V (typ) rising threshold with 5% hysteresis. The accurate threshold allows it to be used to monitor the input voltage or other analog signals of interest. If $V_{EN}$ voltage is less than its threshold, then the step-down regulator and all linear regulators are turned off. VL and the internal reference remain active when EN is low to allow an accurate EN threshold.A rising edge on the pin clears any latched faults except for a thermal fault, which is cleared only by cycling the input power.

## Undervoltage Lockout

If VL drops below 3.4V (typ), the MAX1530/MAX1531 assume that the supply voltage is too low to make valid decisions. Therefore, the undervoltage lockout (UVLO) circuitry turns off all the internal bias supplies. Switching is inhibited, and the DL and DH gate drivers are forced low. After VL rises above 3.5V (typ), the fault and thermal shutdown latches are cleared and startup begins if EN is above its threshold.

## Startup Sequence (ONL_, SEQ)

The MAX1530/MAX1531 are not enabled unless all four of the following conditions are met: 1) VL exceeds the UVLO threshold, 2) EN is above 1.238V, 3) the fault latch is not set, and 4) the thermal shutdown latch is not set. After all four conditions are met, the step-down controller starts switching and enables soft-start (Figure 5). After the step-down regulator soft-start is done, the lowvoltage logic linear regulator controller (LR1) soft-starts.

The remaining linear regulator controllers and the sequence block that can be used to control them are enabled at the same time as the step-down regulator. The SEQ logic input is used in combination with the ONL_ pins to control the startup sequence. When SEQ is high and the sequence block is enabled, each ONL_ pin sources 2µA (typ). When the voltage on an ONL_ pin reaches 1.238V (typ), its respective linear regulator controller (LR_) is enabled. When SEQ is low or the sequence block is not enabled, each ONL_ pin is connected to ground through a 1.5kΩ internal MOSFET.

The sequence block allows the user to program the startup of LR2 to LR5 in any desired sequence. If no capacitor is placed on an ONL_ pin, its LR_ controller starts immediately after the sequence block is enabled and SEQ goes high. Placing a 1.5nF capacitor on an ONL_ pin provides about 1ms delay for the respective LR_ controller. Placing

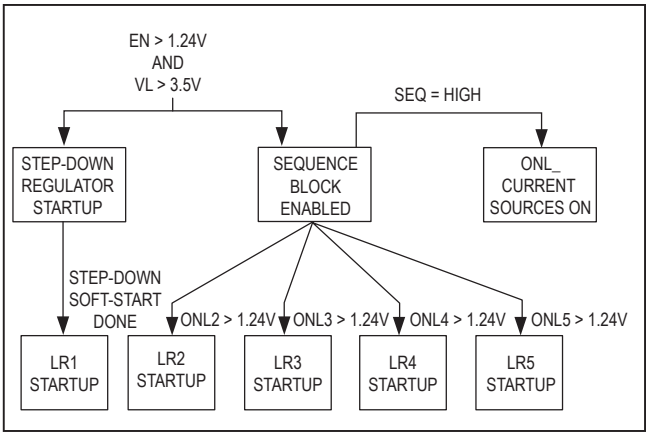



*Figure 5. Startup Conditions*

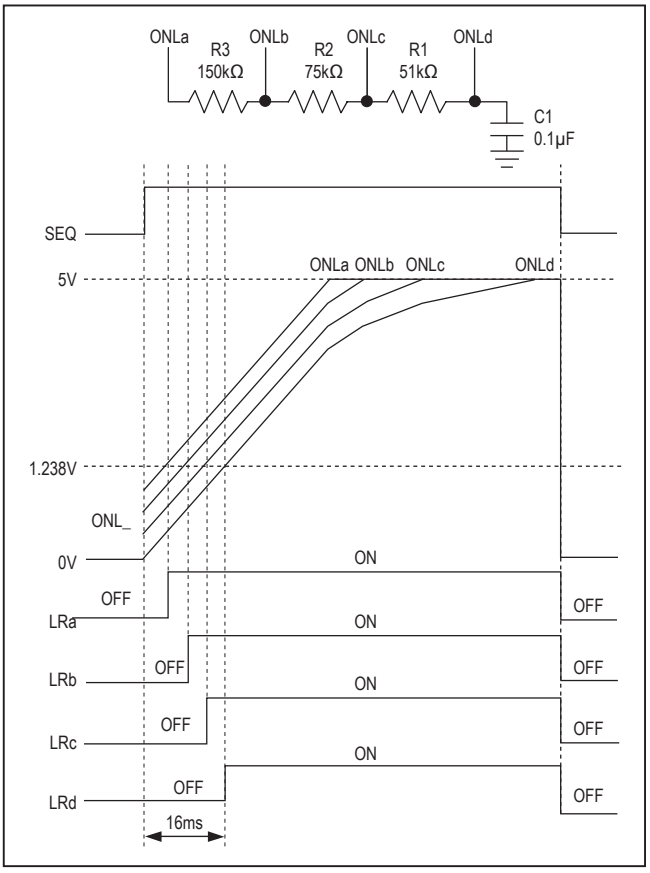



*Figure 6. Single-Capacitor Sequence Configuration*

different size capacitors on each ONL_ pin allows any arbitrary startup sequence.

An arbitrary startup sequence can also be created witha single capacitor (Figure 6). Capacitor C1, together with the 8µA current (2µA per ONL_ pin), is chosen to provide

the desired delay for the controller that starts last (ONLd). Using 0.1µF for C1 provides about 16ms total delay. Because of the 6µA current flowing through R1 (51kΩ), the voltage on ONLc is 0.31V greater than the voltage on ONLd and it crosses the 1.238V threshold and enables its LR_ controller about 4ms before ONLd's controller. Similarly, the 4µA current through R2 (75kΩ) and the 2µA current through R3 (150kΩ) cause their LR_ controllers to each start about 4ms before the next one. Any desired sequence and delay can be programmed by calculating the charge rate of C1 and voltage drops across R1 through R3.

### Soft-Start

The soft-start function controls the slew rate of the output voltages and reduces inrush currents during startup. Each regulator (step-down, LR1 to LR5) goes through a soft-start routine after it is enabled. During soft-start, the reference voltage for each positive regulator gradually ramps up from 0V to the internal reference in 32 steps. The reference voltage of the negative regulator ramps down from VL to 125mV in 32 steps. The total soft-start period for each regulator is 1024 clock cycles for 250kHz switching frequency and 2048 clock cycles for 500kHz switching frequency.

### Reset

The MAX1530/MAX1531 include an open-drain timed microprocessor supervisor function to ensure proper startup of digital circuits. The RESET output asserts low whenever RSTIN is less than the RSTIN trip threshold. RESET also asserts low when VL is less than the VL UVLO threshold, EN is low, or the thermal, undervoltage or overcurrent fault latches are set. RESET enters the high-impedance state only after RSTIN remains above the trip threshold for the duration of the reset timeout period. The state of RESET has no effect on other portions of the IC.

The RSTIN threshold (1.114V typ) is designed to allow RSTIN to directly connect to any of the MAX1530/MAX1531s' feedback input pins, eliminating the need for an additional resistive divider. Typically, RSTIN is connected to FB or FBL1 to monitor the supply voltage for digital logic ICs, but it can be used to monitor any desired output voltage or it can even be used as a general- purpose comparator.

### Fault Protection

#### Undervoltage Protection

After its soft-start is done, if the output of the main step-down regulator or any of the linear-regulator outputs (LR1 to LR5) are below 90% of their normal regulation point, the MAX1530/MAX1531 activate an internal fault timer. If the fault condition remains continuously for the entire fault timer duration, the MAX1530/MAX1531 set the fault latch, shutting down all the regulator outputs. Undervoltage faults do not turn off VL. Once the fault condition is removed, cycling the input voltage or applying a rising edge on SEQ or EN clears the fault latch and reactivates the device.

#### Thermal Protection

The thermal protection limits total power dissipation in the MAX1530/MAX1531. If the junction temperature exceeds +160°C, a thermal sensor immediately sets the thermal fault latch, shutting off all the IC's outputs including VL, allowing the device to cool down. The only way to clear the thermal fault latch is to cycle the input voltage after the device cools down by at least 15°C.

#### Overcurrent Protection Block (CSH, CSL) (MAX1531 Only)

The MAX1531 includes an uncommitted overcurrent protection block that can be used to measure any input or output current, using a current-sense resistor or other sense element. If the measured current exceeds the overcurrent protection threshold (300mV typ), the MAX1531 immediately sets the undervoltage fault latch, shutting down all the regulator outputs. Overcurrent faults do not turn off VL. An internal lowpass filter prevents large current transients of short duration (less than 50µs) from setting the latch. Once the overcurrent condition is removed, cycling the input voltage clears the fault latch and reactivates the device. A rising edge on SEQ or EN also clears the fault latch.

In Figure 1's circuit, the overcurrent protection is used with the LR4 source driver regulator since that regulator is powered directly from the input supply and has no current limit of its own. The current-sense resistor is placed in series with the input supply, before the linear regulator's external PNP pass transistor. CSH and CSL are connected to the positive and negative sides of the sense resistor.

## Design Procedures

### Main Step-Down Regulator

#### Inductor Selection

Three key inductor parameters must be specified: inductance value (L), peak current ($I_{PEAK}$), and DC resistance ($R_{DC}$). The following equation includes a constant, LIR, which is the ratio of peak-to-peak inductor ripple current to DC load current. A higher LIR value allows smaller inductance, but results in higher losses and higher ripple.

A good compromise between size and losses is typically found at a 30% ripple current to load current ratio (LIR = 0.3), which corresponds to a peak inductor current 1.15 times the DC load current:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times I_{LOAD(MAX)} \times LIR}$$

where $I_{LOAD(MAX)}$ is the maximum DC load current, and the switching frequency fSW is 500kHz when FREQ is tied to VL, and 250kHz when FREQ is tied to AGND. The exact inductor value is not critical and can be adjusted to make trade-offs among size, cost, and efficiency. Lower inductor values minimize size and cost, but they also increase the output ripple and reduce the efficiency due to higher peak currents. On the other hand, higher inductor values increase efficiency, but at some point increased resistive losses due to extra turns of wire will exceed the benefit gained from lower AC current levels.

The inductor's saturation current must exceed the peak inductor current. The peak current can be calculated by:

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{f_{SW} \times L \times V_{IN}}$$

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's DC resistance should be low for good efficiency. Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, though powdered iron is inexpensive and can work well at 250kHz. Shielded-core geometries help keep noise, EMI, and switching waveform jitter low.

### MOSFET Selection and Current-Limit Setting

The MAX1530/MAX1531s' step-down controller drives two external logic-level N-channel MOSFETs. Since the $R_{DS(ON)}$ of each MOSFET is used as a sense resistor to provide current-sense signals to the PWM, their $R_{DS(ON)}$ values are important considerations in component selection.

The $R_{DS(ON)}$ of the high-side MOSFET (N1) provides an inductor current-sense signal for current-mode operation and also provides a crude maximum current limit during the high-side on-time that prevents runaway currents if the inductor saturates. The MOSFET voltage is measured across the high-side MOSFET from VIN to LX and is limited to 400mV (typ). To ensure the desired output current with sufficient margin, choose a MOSFET with $R_{DS(ON)}$ low enough that the peak current does not generate more than 340mV across the MOSFET, even when the MOSFET is hot. If the MOSFET's $R_{DS(ON)}$ is not specified at a suitable temperature, use the maximum room temperature specification and add 0.5% per °C for the $R_{DS(ON)}$ increase with temperature:

$$I_{PEAK} \times R_{DS(ON)\_HOT} < 340mV$$

To ensure stable operation of the current-mode PWM, the minimum current-sense ripple signal should exceed 12mV. Since this value depends on the minimum $R_{DS(ON)}$ of the high-side MOSFET, which is not typically a specified parameter, a good rule of thumb is to choose the typical room temperature $R_{DS(ON)}$ about 2 times the amount needed for this:

$$I_{RIPPLE} \times R_{DS(ON)\_TYP} > 24mV$$

For example, Figure 6's circuit is designed for 1.5A and uses a dual MOSFET (N1) for both the high-side and low-side MOSFETs. Its maximum $R_{DS(ON)}$ at room temperature is 145mΩ and an estimate of its maximum $R_{DS(ON)}$ at our chosen maximum temperature of +85°C is 188mΩ. Since the inductor ripple current is 0.5A, the peak current through the MOSFET is 1.75A. So the maximum peak current-sense signal is 330mV, which is less than 340mV. Using the typical $R_{DS(ON)}$ of 113mΩ and the ripple current of 0.5A, the current ripple signal for the PWM is 56mV, much greater than the required 24mV.

The $R_{DS(ON)}$ of the low-side MOSFET (also N1) provides current-limit information during the low-side ontime that inhibits a high-side on-time if the MOSFET voltage is too high. The voltage is measured across the low-side MOSFET from PGND to LX and the threshold is set by ILIM. To use the preset 250mV (typ) threshold, connect ILIM to VL and choose a MOSFET with $R_{DS(ON)}$ low enough that the "valley" current does not generate more than 190mV across the MOSFET, even when the MOSFET is hot. If the MOSFET's $R_{DS(ON)}$ is not specified at a suitable temperature, use the maximum room temperature specification and add 0.5% per °C for the $R_{DS(ON)}$ increase with temperature:

$$I_{VALLEY} = I_{OUT} - I_{RIPPLE} / 2$$

$$I_{VALLEY} \times R_{DS(ON)\_HOT} < 190mV$$

If the MOSFET's $R_{DS(ON)}$ is lower than necessary, there is no need to adjust the current-limit threshold using ILIM. If the MOSFET's $R_{DS(ON)}$ is too high, adjust the current-limit threshold using a resistive-divider between VL and

AGND at ILIM. The threshold is approximately 1/5th the voltage on ILIM over a range of 0.25V to 3V:

$$I_{VALLEY} \times R_{DS(ON)\_HOT} < 0.2 \times V_{ILIM} \times (1 - K)$$

K is the accuracy of the current-limit threshold, which is 20% when the threshold is 250mV.

For example, Figure 1's N1 MOSFET has a maximum $R_{DS(ON)}$ at room temperature of 145mΩ and an estimate of its maximum at our chosen maximum temperature of +85°C is 188mΩ. Since the inductor ripple current is 0.5A, the valley current through the MOSFET is 1.25A. So the maximum valley current-sense signal is 235mV, which is too high to work with the 190mV minimum of the default current-limit threshold. Adding a divider at ILIM (R12 and R13) adjusts the ILIM voltage to 1.7V and the current-limit threshold to 340mV, providing more than adequate margin for threshold accuracy.

### Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduce noise and voltage ripple on the input caused by the regulator's switching. It is usually selected according to input ripple current requirements and voltage rating, rather than capacitance value. The input voltage and load current determine the RMS input ripple current ($I_{RMS}$):

$$I_{RMS} = I_{LOAD} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

The worst case is $I_{RMS} = 0.5 \times I_{LOAD}$, which occurs at $V_{IN} = 2 \times V_{OUT}$.

For most applications, ceramic capacitors are used because of their high ripple current and surge current capabilities. For long-term reliability, choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current corresponding to the maximum load current.

### Output Capacitor

The output capacitor and its equivalent series resistance (ESR) affect the regulator's loop stability, output ripple voltage, and transient response. The *Compensation Design* section discusses the output capacitance requirement based on the loop stability. This section deals with how to determine the output capacitance and ESR needs according to the ripple voltage and load transient requirements.

The output voltage ripple has two components: variations in the charge stored in the output capacitor, and the voltage drop across the capacitor's ESR caused by the current into and out of the capacitor:

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} = I_{RIPPLE} \times R_{ESR}$$

$$V_{RIPPLE(C)} = \frac{I_{RIPPLE}}{8 \times C_{OUT} \times f_{SW}}$$

where $C_{OUT}$ is the output capacitance, and $R_{ESR}$ is the ESR of the output capacitor. In Figure 1's circuit, the inductor ripple current is 0.5A. Assume the voltage-ripple requirement is 2% (peak-to-peak) of the 3.3V output, which corresponds to 66mV total peak-to-peak ripple. Assuming that the ESR ripple component and the capacitive ripple component each should be less than 50% of the 66mV total peak-to-peak ripple, then the ESR should be less than 66mΩ and the output capacitance should be more than 7.6µF to meet the total ripple requirement. A 22µF ceramic capacitor with ESR (including PC board trace resistance) of 10mΩ is selected for the standard application circuit in Figure 1, which easily meets the voltage ripple requirement.

The step-down regulator's output capacitance and ESR also affect the voltage undershoot and overshoot when the load steps up and down abruptly. The undershoot and overshoot have three components: the voltage steps caused by ESR, the voltage undershoot and overshoot due to the current-mode control's AC load regulation, and the voltage sag and soar due to the finite capacitance and inductor slew rate.

The amplitude of the ESR steps is a function of the load step and the ESR of the output capacitor:

$$V_{ESR\_STEP} = \Delta I_{LOAD} \times R_{ESR}$$

The amplitude of the sag due to the finite output capacitance and inductor slew rate is a function of the load step, the output capacitor value, the inductor value, the input-to-output voltage differential, and the maximum duty cycle:

$$V_{SAG\_LC} = \frac{L \times (\Delta I_{LOAD})^2}{2 \times C_{OUT} \times (V_{IN(MIN)} \times D_{MAX} - V_{OUT})}$$

The amplitude of the undershoot due to the AC load regulation is a function of the high-side MOSFET $R_{DS(ON)}$, the gain of the current-sense amplifier $A_{VCS}$, the change of the slope compensation during the undershoot ($\Delta SC_{UNDER}$), the transconductance of the error amplifier $g_m$, the com-

pensation resistor $R_{COMP}$, the FB regulation $V_{FB}$, and the output voltage set point $V_{OUT}$:

$$V_{UNDER\_AC} = \frac{V_{OUT} \times \left( \begin{matrix} A_{VCS} \times R_{DS(ON)} \times \Delta I_{LOAD} \\ +\Delta SC_{UNDER} \end{matrix} \right)}{V_{FB} \times R_{COMP} \times g_m}$$

Use the following to calculate the slope compensation change during the sag:

$$\Delta SC_{UNDER} = 437.5mV \times \left( D_{UNDER} - \frac{V_{OUT}}{V_{IN}} \right)$$

where $D_{UNDER}$ is the duty cycle at the valley of the sag, which is usually 50%.

The actual undershoot is always equal to or bigger than the worst of $V_{ESR\_STEP}$, $V_{SAG\_LC}$, and $V_{UNDER\_AC}$.

The amplitude of the soar due to the finite output capacitance and inductor slew rate is a function of the load step, the output capacitor value, the inductor value, and the output voltage:

$$V_{SOAR\_LC} = \frac{L \times (\Delta I_{LOAD})^2}{2 \times C_{OUT} \times V_{OUT}}$$

The amplitude of the overshoot due to the AC load regulation is:

$$V_{OVER\_AC} = \frac{V_{OUT} \times \left( \begin{matrix} A_{VCS} \times R_{DS(ON)} \times \Delta I_{LOAD} \\ +\Delta SC_{OVER} \end{matrix} \right)}{V_{FB} \times R_{COMP} \times g_m}$$

where $\Delta SC_{OVER}$ is the change of the slope compensation during the overshoot, given by:

$$\Delta SC_{OVER} = 437.5mV \times \left( \frac{V_{OUT}}{V_{IN}} - D_{OVER} \right)$$

where $D_{OVER}$ is the duty cycle at the peak of the overshoot, which is typically 0%.

Similarly, the actual overshoot is always equal to or bigger than the worst of $V_{ESR\_STEP}$, $V_{SOAR\_LC}$, and $V_{OVER\_AC}$.

Given the component values in the circuit of Figure 1, during a 1.5A step load transient, the voltage step due to capacitor ESR is negligible. The voltage sag due to finite capacitance and inductor slew rate is 81mV, and the voltage undershoot due to the AC load regulation is 170mV. The total undershoot seen in the *Typical Operating Characteristics* is 170mV. The voltage soar due to finite capacitance and inductor slew rate is 155mV, and the voltage overshoot due to the AC load regulation is 167mV. The total overshoot seen the in the Typical Operating Characteristics is 200mV.

### Compensation Design

The step-down controller of the MAX1530/MAX1531 uses a peak current-mode control scheme that regulates the output voltage by forcing the required current through the inductor. The MAX1530/MAX1531 use the voltage across the high-side MOSFET's $R_{DS(ON)}$ to sense the inductor current. Using the current-sense amplifier's output signal and the amplified feedback voltage sensed at FB, the control loop sets the peak inductor current by:

$$I_{PEAK} = \frac{(V_{OUT} - V_{OUT(SET)}) \times V_{FB} \times A_{VEA}}{V_{OUT(SET)} \times R_{DS(ON)} \times A_{VCS}}$$

where $V_{FB}$ = 1.238V is the FB regulation voltage, $A_{VCS}$ is the gain of the current-sense amplifier (3.5 typical), AVEA is the DC gain of the error amplifier (2000 typ), $V_{OUT(SET)}$ is the output voltage set point, and $R_{DS(ON)}$ is the on-resistance of the high-side MOSFET.

The total DC loop gain ($A_{DC}$) is approximately:

$$A_{DC} = \frac{V_{FB} \times R_{LE} \times A_{VEA}}{V_{OUT(SET)} \times R_{DS(ON)} \times A_{VCS}}$$

RLE is the equivalent load resistance, given by:

$$R_{LE} = \left( \frac{V_{OUT}}{I_{LOAD(MAX)}} \right) \left\| \left( \frac{L \times f_{SW}}{n \times D' - D} \right) \right.$$

In the above equation, D' = 1 - D, n is a factor determined-by the slope compensation mc and the inductor current ramp m1, as shown below:

$$n = 1 + \frac{m_C}{m_1}$$

The slope compensation of the MAX1530/MAX1531 is 219mV/µs. The inductor current ramp is a function of the input voltage, output voltage, inductance, high-side MOSFET on-resistance $R_{DS(ON)}$, and the gain of the current-sense amplifier $A_{VCS}$, and is:

$$m_1 = \frac{V_{IN} - V_{OUT}}{L} \times R_{DS(ON)} \times A_{VCS}$$