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19-2741; Rev 0; 4/03

EVALUATION KIT AVAILABLE

TFT LCD DC-to-DC Converter with Operational Amplifiers

MAX1542/MAX1543

General Description

The MAX1542/MAX1543 include a high-performance boost regulator and two high-current operational amplifiers for active matrix, thin-film transistor (TFT), liquid-crystal displays (LCDs). Also included is a logic-controlled, high-voltage switch with adjustable delay. The MAX1543 includes an additional high-voltage load switch and features pin-selectable boost regulator switching frequency.

The step-up DC-to-DC converter is a high-frequency 640kHz (MAX1543)/1.2MHz (MAX1542/MAX1543) current-mode regulator with a built-in power MOSFET that allows the use of ultra-small inductors and ceramic capacitors. It provides fast transient response to pulsed loads while producing efficiencies over 85%.

The two easy-to-use, high-performance operational amplifiers can drive the LCD backplane (V_{COM}) and/or the gamma correction divider string. The devices feature high short-circuit current (150mA), fast slew rate (7.5V/µs), wide bandwidth (12MHz), and Rail-to-Rail® inputs and outputs.

The MAX1542/MAX1543 are available in 20-pin thin QFN packages with a maximum thickness of 0.8mm for ultra-thin LCD panel design.

Applications

Notebook Computer Displays

LCD Monitor Panels

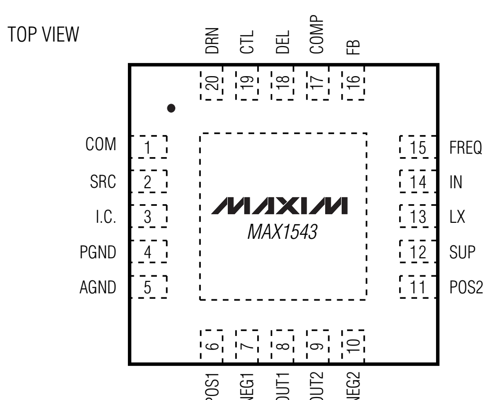
PDAs

Car Navigation Displays

Features

- **Ultra-High-Performance Step-Up Regulator**
  - **Fast Transient Response to Pulsed Load Using Current-Mode Control Architecture**
  - **High-Accuracy Output Voltage (1.3%)**
  - **Built-In 14V, 1.2A, 0.2Ω N-Channel Power MOSFET with Lossless Current-Sensing**
  - **High Efficiency (85%)**
  - **8-Step Current-Controlled Digital Soft-Start**
- **Two High-Performance Operational Amplifiers**
  - **150mA Output Short-Circuit Current**
  - **7.5V/µs Slew Rate**
  - **12MHz -3dB Bandwidth**
  - **Rail-to-Rail Inputs/Outputs**
  - **Unity Gain Stable**
- **Logic-Controlled High-Voltage Switch with Adjustable Delay**
- **Timer Delay Latch FB Fault Protection**
- **Thermal Protection**
- **2.6V to 5.5V Input Operating Voltage Range**
- **3.6mA (Switching), 0.45mA (Not Switching) Quiescent Current**
- **Ultra-Thin 20-Pin Thin QFN Package (5mm x 5mm x 0.8mm)**

Pin Configurations



THIN QFN (5mm x 5mm)

Pin Configurations continued at end of data sheet.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1542ETP	-40°C to +85°C	20 Thin QFN (5mm x 5mm)
MAX1543ETP	-40°C to +85°C	20 Thin QFN (5mm x 5mm)

Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

TFT LCD DC-to-DC Converter with Operational Amplifiers

ABSOLUTE MAXIMUM RATINGS

IN, CTL, COMP, FB, DEL, FREQ (MAX1543)
to AGND ....-0.3V to +6V
COMP, FB, DEL to AGND ....-0.3V to (IN + 0.3V)
PGND to AGND ....±0.3V
LX to PGND ....-0.3V to +14V
SUP, POS1, NEG1, OUT1, POS2,
NEG2, OUT2 to AGND ....-0.3V to +14V
POS1, NEG1, OUT1, POS2, NEG2,
OUT2 to AGND ....-0.3V to (SUP + 0.3V)
SRC, COM to AGND..-0.3V to +30V
SRC to COM...-0.3V to +30V
SRC to DRN (MAX1543)...-0.3V to +30V
COM to AGND ....-0.3V to (SRC + 0.3V)
DRN (MAX1543) to AGND ....-0.3V to (SRC + 0.3V)
DRN (MAX1543) to COM..-30V to +30V
MAX1542 COM RMS Output Current ....+75mA
MAX1543 COM RMS Output Current ....±50mA
OUT1, OUT2 Continuous Output Current.........................±75mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin Thin QFN 5mm x 5mm
(derate 20.8mW/°C above +70°C)............................1667mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, V_{SUP} = 8V, V_{SRC} = 28V, FREQ = IN (MAX1543), PGND = AGND = 0, **T_A = 0°C to +85°C**, typical values at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN Supply Range	V_{IN}			2.6		5.5	V
IN Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising		2.3	2.5	2.7	V
		V_{IN} falling		2.2	2.35	2.5	
IN Quiescent Current	I_{IN}	V_{FB} = 1.3V, LX not switching			0.45	0.65	mA
		V_{FB} = 1.1V, LX switching			3.6	6.5	
Duration to Trigger Fault Condition		MAX1542			55		ms
		MAX1543	FREQ = AGND		51		
			FREQ = IN		55		
Thermal Shutdown		Rising edge			160		°C
		Hysteresis			15		
MAIN STEP-UP REGULATOR							
Output Voltage Range	V_{MAIN}			V_{IN}		13	V
Operating Frequency	f_{OSC}	MAX1542		1020	1200	1380	kHz
		MAX1543	FREQ = AGND	512	600	768	
			FREQ = IN	1020	1200	1380	
Oscillator Maximum Duty Cycle				82	87	92	%
FREQ Input Low Voltage		MAX1543, V_{IN} = 2.6V to 5.5V				0.3 x V_{IN}	V
FREQ Input High Voltage		MAX1543, V_{IN} = 2.6V to 5.5V		0.7 x V_{IN}			V
FREQ Pulldown Current		MAX1543, V_{FREQ} = 1.0V		3.5	5	6.5	µA
FB Regulation Voltage	V_{FB}	No load	T_A = +85°C	1.224	1.240	1.256	V
			T_A = 0°C to +85°C	1.222	1.240	1.258	
FB Fault Trip Level		V_{FB} falling		0.96	1	1.04	V
FB Load Regulation		0 ≤ I_{MAIN} ≤ full load			-1		%
FB Line Regulation		V_{IN} = 2.6V to 5.5V			-0.08	±0.15	%/V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, V_{SUP} = 8V, V_{SRC} = 28V, FREQ = IN (MAX1543), PGND = AGND = 0, **T_A = 0°C to +85°C**, typical values at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
FB Input Bias Current		V_{FB} = 1.5V	-40		+40	nA
FB Transconductance		ΔI_{COMP} = 5µA	75	160	280	µS
FB Voltage Gain		FB to COMP		700		V/V
LX On-Resistance	$R_{LX(ON)}$			210	400	mΩ
LX Leakage Current	I_{LX}	V_{LX} = 13V		0.01	20	µA
LX Current Limit	I_{LIM}	V_{FB} = 1V, duty cycle = 65%	1.2	1.5	1.8	A
Current-Sense Transresistance			0.30	0.50	0.65	Ω
Soft-Start Period	t_{SS}	MAX1542		14		ms
		MAX1543, FREQ = AGND		13		
		MAX1543, FREQ = IN		14		
Soft-Start Step Size				I_{LIM} / 8		A
OPERATIONAL AMPLIFIERS						
SUP Supply Range	V_{SUP}		4.5		13.0	V
SUP Supply Current	I_{SUP}	Buffer configuration, $V_{POS\_}$ = 4V, no load		1.3	1.9	mA
Input Offset Voltage	V_{OS}	V_{CM} = V_{SUP}/2, T_A = +25°C		0	12	mV
Input Bias Current	I_{BIAS}	NEG1, NEG2, POS1, POS2		+1	±50	nA
Input Common-Mode Voltage Range	V_{CM}		0		V_{SUP}	V
Common-Mode Rejection Ratio	CMRR	0 ≤ $V_{NEG\_}$, $V_{POS\_}$ ≤ V_{SUP}	50	90		dB
Open-Loop Gain				125		dB
Output Voltage Swing High	V_{OH}	$I_{OUT\_}$ = 100µA	V_{SUP} - 15	V_{SUP} - 2		mV
		$I_{OUT\_}$ = 5mA	V_{SUP} - 150	V_{SUP} - 80		
Output Voltage Swing Low	V_{OL}	$I_{OUT\_}$ = -100µA		2	15	mV
		$I_{OUT\_}$ = -5mA		80	150	
Short-Circuit Current		To V_{SUP}/2, Source	50	150		mA
		To V_{SUP}/2, Sink	50	140		
Output Source-and-Sink Current		Buffer configuration, $V_{POS\_}$ = 4V, $\lvert\Delta V_{OS}\rvert$ < 10mV	40			mA
Power-Supply Rejection Ratio	PSRR	DC, 6V ≤ V_{SUP} ≤ 13V, $V_{NEG\_}$, $V_{POS\_}$ = V_{SUP}/2	60	100		dB
Slew Rate				7.5		V/µs
-3dB Bandwidth		R_L = 10kΩ, C_L =10pF, buffer configuration		12		MHz
Gain-Bandwidth Product	GBW	Buffer configuration		8		MHz
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES						
DEL Capacitor Charge Current		During startup, V_{DEL} = 1V	4	5	6	µA

TFT LCD DC-to-DC Converter with Operational Amplifiers

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, V_{SUP} = 8V, V_{SRC} = 28V, FREQ = IN (MAX1543), PGND = AGND = 0, **T_A = 0°C to +85°C**, typical values at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DEL Turn-On Threshold	$V_{TH(DEL)}$			1.178	1.240	1.302	V
DEL Discharge Switch On-Resistance		During UVLO, V_{IN} = 2.2V			20		Ω
CTL Input Low Voltage		V_{IN} = 2.6V to 5.5V				0.6	V
CTL Input High Voltage		V_{IN} = 2.6V to 5.5V		2			V
CTL Input Leakage Current		CTL = AGND or IN		-1		+1	µA
CTL-to-SRC Propagation Delay					100		ns
SRC Input Voltage Range						28	V
SRC Input Current	I_{SRC}	V_{DRN} = 8V, CTL = IN, V_{DEL} = 1.5V	MAX1542		70	130	µA
			MAX1543		100	180	
		V_{DRN} = 8V, CTL = AGND, V_{DEL} = 1.5V			15	30	
DRN Input Current	I_{DRC}	V_{DRN} = 8V, CTL = AGND, V_{DEL} = 1.5V, MAX1543			90	150	µA
SRC to COM Switch On-Resistance	$R_{SRC(ON)}$	V_{DEL} = 1.5V, CTL = IN	MAX1542		5	10	Ω
			MAX1543		15	30	
DRN to COM Switch On-Resistance (MAX1543)	$R_{DRN(ON)}$	V_{DEL} = 1.5V, CTL = AGND			30	60	Ω
COM to PGND Switch On-Resistance (MAX1543)	$R_{COM(ON)}$	V_{DEL} = 1.1V		350	1000	1800	Ω

ELECTRICAL CHARACTERISTICS

(V_{IN} = 3V, V_{SUP} = 8V, V_{SRC} = 28V, FREQ = IN (MAX1543), PGND = AGND = 0, **T_A = -40°C to +85°C,** unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IN Supply Range	V_{IN}			2.6		5.5	V
IN Undervoltage Lockout Threshold	V_{UVLO}	V_{IN} rising		2.3		2.7	V
		V_{IN} falling		2.2		2.5	
IN Quiescent Current	I_{IN}	V_{FB} = 1.3V, LX not switching				0.65	mA
		V_{FB} = 1.1V, LX switching				6.5	
MAIN STEP-UP REGULATOR							
Output Voltage Range	V_{MAIN}			V_{IN}		13	V
Operating Frequency	f_{OSC}	MAX1542		1000		1400	kHz
		MAX1543	FREQ = AGND	512		768	
			FREQ = IN	1000		1400	
FB Regulation Voltage	V_{FB}	No load		1.215		1.260	V
FB Fault Trip Level		V_{FB} falling		0.96		1.04	V
FB Line Regulation		V_{IN} = 2.6V to 5.5V				0.15	%/V
FB Transconductance		ΔI_{COMP} = 5µA		75		300	µS
LX On-Resistance	$R_{LX(ON)}$					400	mΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 3V, V_{SUP} = 8V, V_{SRC} = 28V, FREQ = IN (MAX1543), PGND = AGND = 0, **T_A = -40°C to +85°C,** unless otherwise noted.)

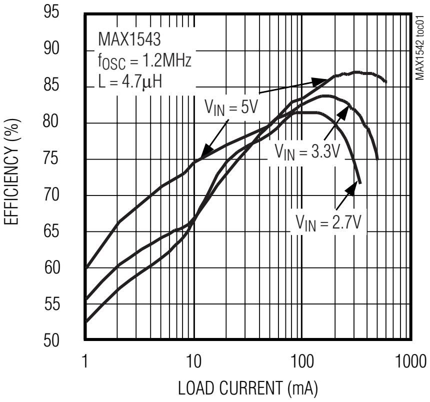
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LX Current Limit	I_{LIM}	V_{FB} = 1V, duty cycle = 65%		1.2		1.8	A
Current-Sense Transresistance				0.30		0.65	Ω
OPERATIONAL AMPLIFIERS							
SUP Supply Range	V_{SUP}			4.5		13.0	V
SUP Supply Current	I_{SUP}	Buffer configuration, $V_{POS\_}$ = 4V, no load				2.1	mA
Input Offset Voltage	V_{OS}	V_{CM} = V_{SUP}/2, T_A = +25ºC				12	mV
Input Bias Current	I_{BIAS}	NEG1, NEG2, POS1, POS2				±50	nA
Input Common-Mode Voltage Range	V_{CM}			0		V_{SUP}	V
Output Voltage Swing High	V_{OH}	$I_{OUT\_}$ = 100µA		V_{SUP} - 15			mV
		$I_{OUT\_}$ = 5mA		V_{SUP} - 150			
Output Voltage Swing Low	V_{OL}	$I_{OUT\_}$ = -100µA				15	mV
		$I_{OUT\_}$ = -5mA				150	
Short-Circuit Current		To V_{SUP}/2	Source	50			mA
			Sink	50			
Output Source-and-Sink Current		Buffer configuration, $V_{POS\_}$ = 4V, $\lvert \Delta V_{OS} \rvert$ < 10mV		40			mA
POSITIVE GATE-DRIVER TIMING AND CONTROL SWITCHES							
DEL Capacitor Charge Current		During startup, V_{DEL} = 1.0V		4		6	µA
DEL Turn-On Threshold	$V_{TH\ (DEL)}$			1.178		1.302	V
CTL Input Low Voltage		V_{IN} = 2.6V to 5.5V				0.6	V
CTL Input High Voltage		V_{IN} = 2.6V to 5.5V		2			V
SRC Input Voltage Range						28	V
SRC Input Current	I_{SRC}	V_{DRN} = 8V, CTL = IN, V_{DEL} = 1.5V	MAX1542			130	µA
			MAX1543			180	
		V_{DRN} = 8V, CTL = AGND, V_{DEL} = 1.5V				30	
DRN Input Current	I_{DRN}	V_{DRN} = 8V, CTL = AGND, V_{DEL} = 1.5V, MAX1543				150	µA
SRC to COM Switch On-Resistance	$R_{SRC(ON)}$	V_{DEL} = 1.5V, CTL = IN	MAX1542			10	Ω
			MAX1543			30	
DRN to COM Switch On-Resistance (MAX1543)	$R_{DRN(ON)}$	V_{DEL} = 1.5V, CTL = AGND				60	Ω
COM to PGND Switch On-Resistance (MAX1543)	$R_{COM(ON)}$	V_{DEL} = 1.1V		350		1800	Ω

TFT LCD DC-to-DC Converter with Operational Amplifiers

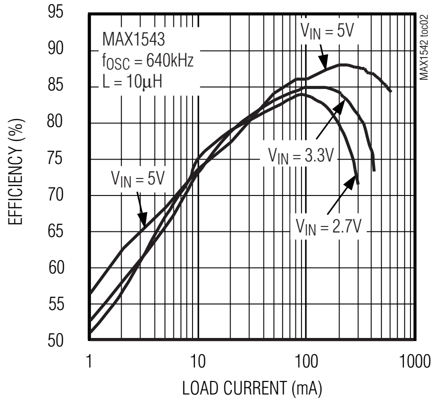
Typical Operating Characteristics

(V_{IN} = 3.3V, V_{MAIN} = 8V, f_{OSC} = 1.2MHz, T_A = +25°C, unless otherwise noted.)

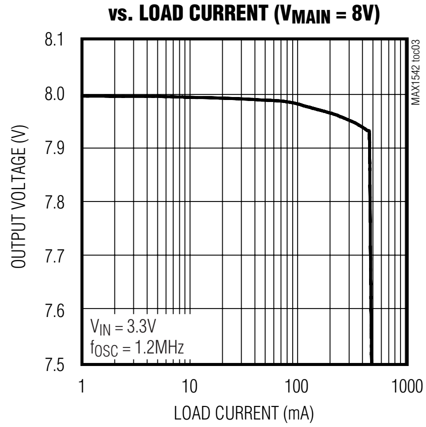
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT (V_{MAIN} = 8V)



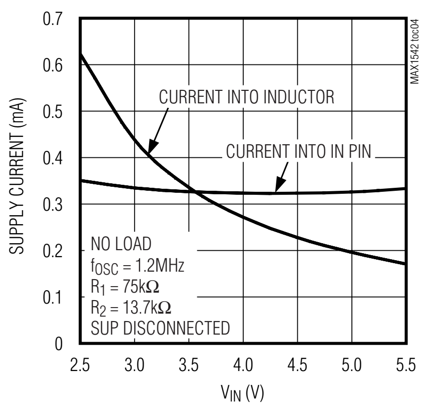
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT (V_{MAIN} = 8V)



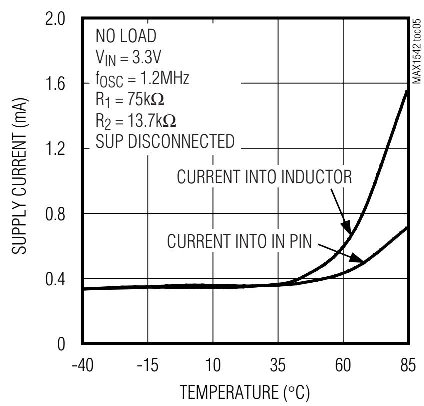
STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT (V_{MAIN} = 8V)



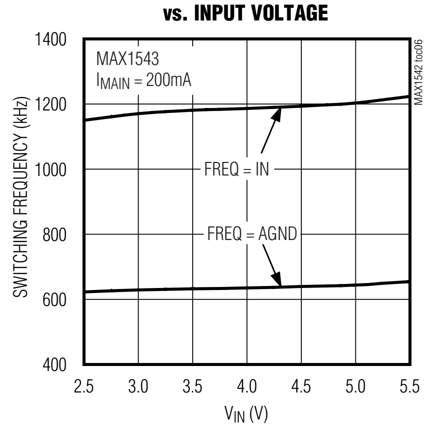
STEP-UP REGULATOR SUPPLY CURRENT vs. SUPPLY VOLTAGE



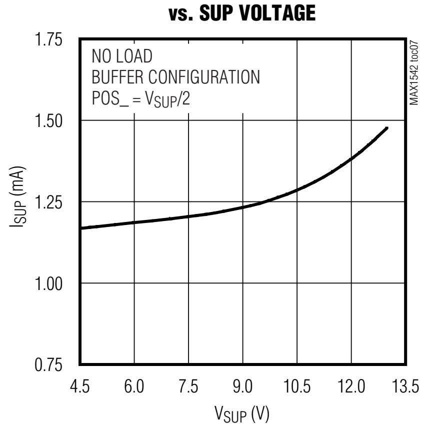
STEP-UP REGULATOR SUPPLY CURRENT vs. TEMPERATURE



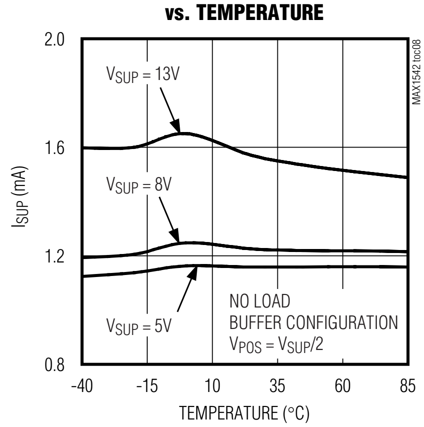
SWITCHING FREQUENCY vs. INPUT VOLTAGE



SUP SUPPLY CURRENT vs. SUP VOLTAGE



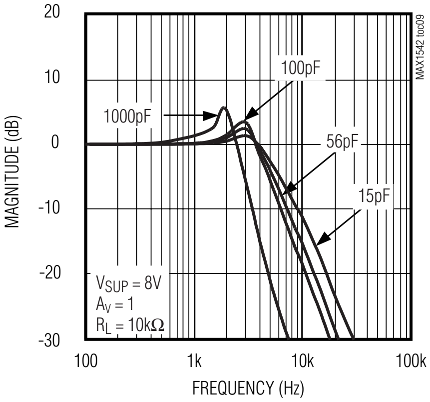
SUP SUPPLY CURRENT vs. TEMPERATURE



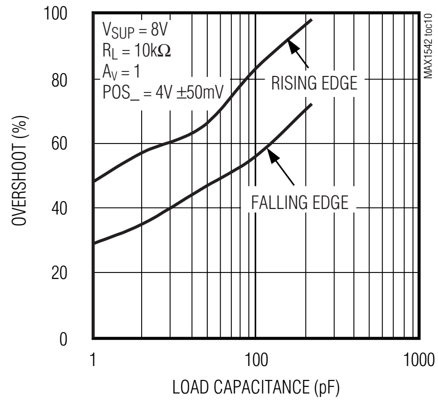
Typical Operating Characteristics (continued)

(V_{IN} = 3.3V, V_{MAIN} = 8V, f_{OSC} = 1.2MHz, T_A = +25°C, unless otherwise noted.)

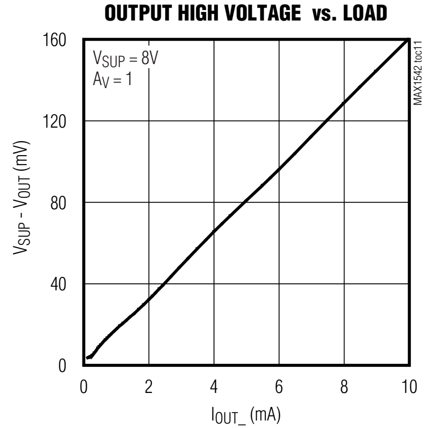
OPERATIONAL AMPLIFIER FREQUENCY RESPONSE FOR VARIOUS C_{LOAD}



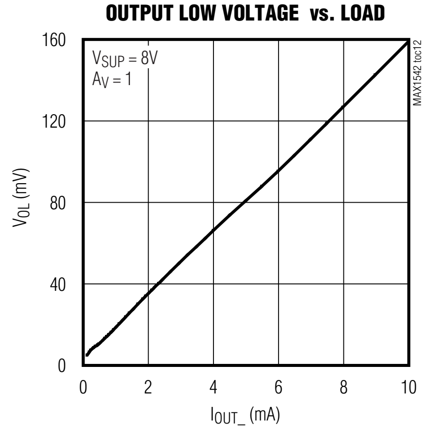
OPERATIONAL AMPLIFIER OVERSHOOT vs. LOAD CAPACITANCE



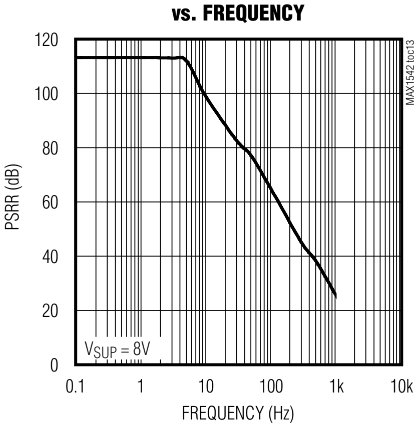
OPERATIONAL AMPLIFIER OUTPUT HIGH VOLTAGE vs. LOAD



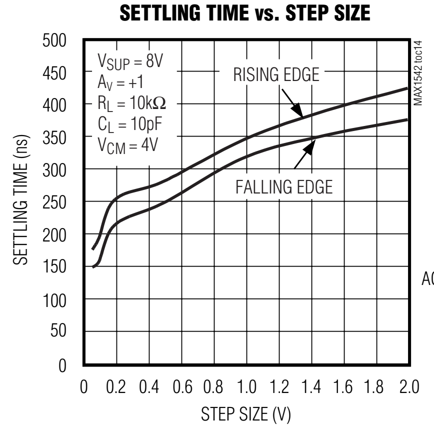
OPERATIONAL AMPLIFIER OUTPUT LOW VOLTAGE vs. LOAD



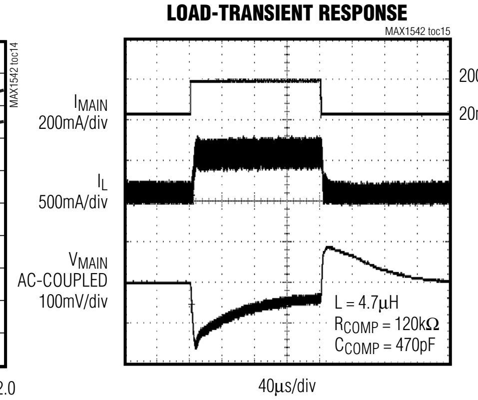
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



OPERATIONAL AMPLIFIER SETTLING TIME vs. STEP SIZE



STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE

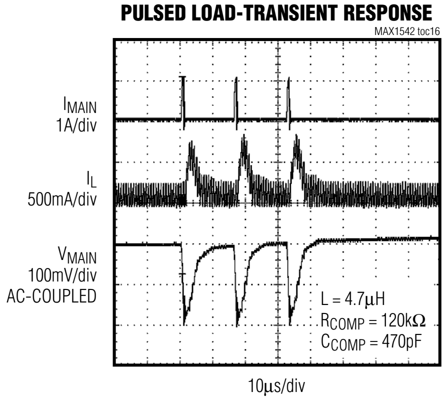


TFT LCD DC-to-DC Converter with Operational Amplifiers

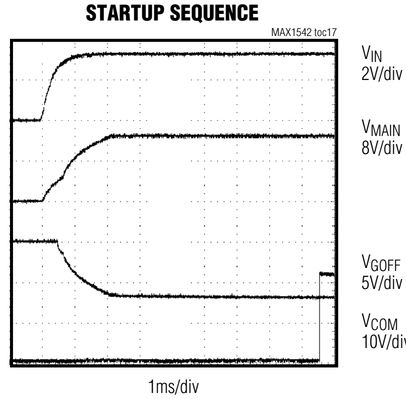
Typical Operating Characteristics (continued)

(V_{IN} = 3.3V, V_{MAIN} = 8V, f_{OSC} = 1.2MHz, T_A = +25°C, unless otherwise noted.)

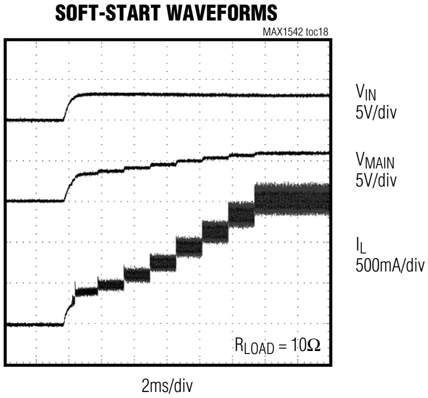
STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE



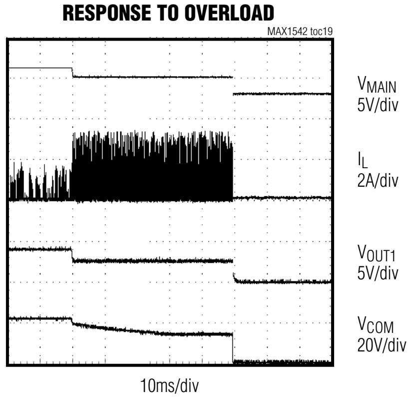
STARTUP SEQUENCE



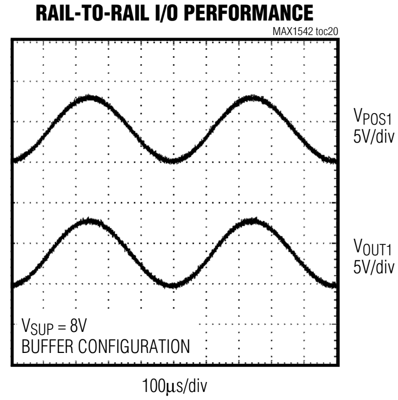
HEAVY-LOAD SOFT-START WAVEFORMS



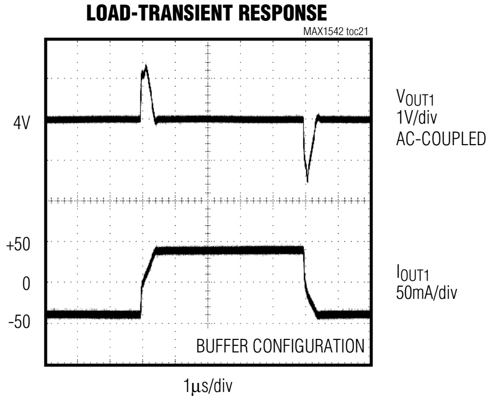
TIMER DELAY LATCH RESPONSE TO OVERLOAD



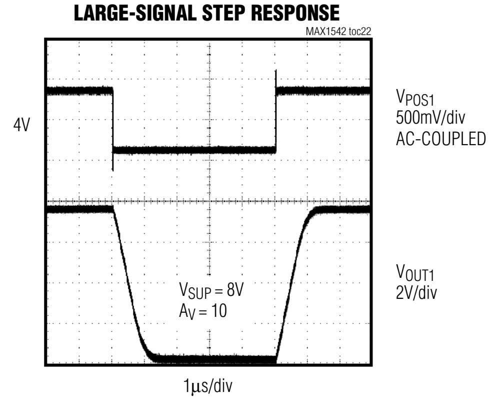
OPERATIONAL AMPLIFIER RAIL-TO-RAIL I/O PERFORMANCE



OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE

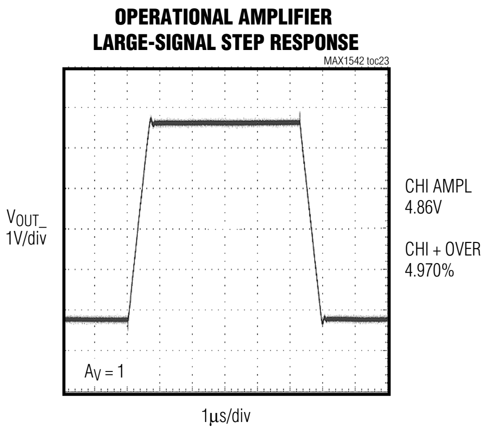


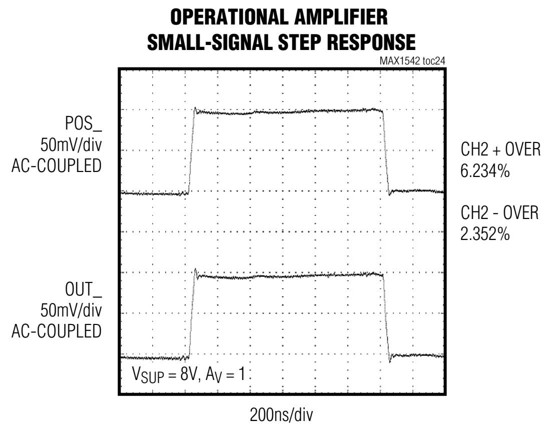
OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE



Typical Operating Characteristics (continued)

(V_{IN} = 3.3V, V_{MAIN} = 8V, f_{OSC} = 1.2MHz, T_A = +25°C, unless otherwise noted.)





Pin Description

PIN		NAME	FUNCTION
MAX1542	MAX1543		
1	1	COM	Internal High-Voltage MOSFET Switch Common Terminal. Do not allow the voltage on COM to exceed V_{SRC}.
2	2	SRC	Switch Input. Source of the internal high-voltage P-channel MOSFET. Bypass SRC to PGND with a minimum of 0.1µF close to the pins.
3, 15, 20	—	N.C.	No Connection. Not internally connected.
—	3	I.C.	Internal Connection. Make no connection to this pin.
4	4	PGND	Power Ground. PGND is the source of the main boost N-channel power MOSFET. Connect PGND to the output capacitor ground terminals through a short, wide PC board trace. Connect to analog ground (AGND) underneath the IC.
5	5	AGND	Analog Ground. Connect to power ground (PGND) underneath the IC.
6	6	POS1	Operational Amplifier 1 Noninverting Input
7	7	NEG1	Operational Amplifier 1 Inverting Input
8	8	OUT1	Operational Amplifier 1 Output
9	9	OUT2	Operational Amplifier 2 Output
10	10	NEG2	Operational Amplifier 2 Inverting Input
11	11	POS2	Operational Amplifier 2 Noninverting Input
12	12	SUP	Operational Amplifier Power Input. Positive supply rail for the OUT1 and OUT2 amplifiers. Typically connected to V_{MAIN}. Bypass SUP to AGND with a 0.1µF capacitor.
13	13	LX	Power MOSFET N-Channel Drain and Switching Node. Connect the inductor and catch diode to LX and minimize the trace area for lowest EMI.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX1542	MAX1543		
14	14	IN	Supply Voltage. IN can range from 2.6V to 5.5V.
—	15	FREQ	Oscillator Frequency Select Input. Pull FREQ low or leave it unconnected for 640kHz operation. Connect FREQ high for 1.2MHz operation. This input has a 5µA pulldown current.
16	16	FB	Step-Up Converter Feedback Input. Regulates to 1.24V (nominal). Connect a resistor-divider from the output (V_{MAIN}) to FB to analog ground (AGND). Place the resistor-divider within 5mm of FB.
17	17	COMP	Step-Up Regulator Error Amplifier Compensation Point. Connect a series RC from COMP to AGND. See the *Loop Compensation* section for component selection guidelines.
18	18	DEL	High-Voltage Switch Delay Input. Connect a capacitor from DEL to AGND to set the high-voltage switch startup delay. A 5µA current source charges C_{DEL}. For the MAX1542, the high-voltage switch between SRC and COM is disabled until V_{DEL} exceeds 1.24V. Following the delay period, CTL controls the state of the high-voltage switch. For the MAX1543, the switches between SRC, COM, and DRN are disabled and a 1kΩ pulldown between COM and PGND is enabled until V_{DEL} exceeds 1.24V. Following the delay period, the 1kΩ pulldown is released and CTL controls the state of the high-voltage switches (see the *Delay Control Circuit* section).
19	19	CTL	High-Voltage Switch Control Input. When CTL is high, the high-voltage switch between COM and SRC is on and the high-voltage switches between COM and DRN (MAX1543) are off. When CTL is low, the high-voltage switch between COM and SRC is off and the high-voltage switches between COM and DRN (MAX1543) are on. CTL is inhibited by the undervoltage lockout and when V_{DEL} is less than 1.24V.
—	20	DRN	Switch Input. Drain of the internal high-voltage back-to-back P-channel MOSFETs connected to COM.

Typical Application Circuits

The MAX1542 typical application circuit (Figure 1) and the MAX1543 typical application circuit (Figure 2) generate an +8V source driver supply and approximately +22V and -7V gate driver supplies for TFT displays. The input voltage is from +2.6V to +5.5V. Table 1 lists recommended components and Table 2 lists contact information for component suppliers.

Detailed Description

The MAX1542/MAX1543 include a high-performance step-up regulator, two high-current operational amplifiers, and startup timing and level-shifting functionality useful for active matrix TFT LCDs. Figure 3 shows the MAX1542/MAX1543 functional diagram.

Main Step-Up Converter

The MAX1542/MAX1543 main step-up converter switches at 1.2MHz or 640kHz (MAX1543 only) (see the *Oscillator Frequency (FREQ)* section). The devices employ a current-mode, fixed-frequency, pulse-width modulation (PWM) architecture to maximize loop bandwidth providing fast transient response to pulsed loads found in source drivers for TFT LCD panels. The high-switching frequency also allows the use of low-profile inductors and capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET and the IC's built-in digital soft-start function reduce the number of external components required while controlling inrush current. The output voltage of the main step-up converter (V_{MAIN}) can be set from V_{IN} to 13V with an external resistive voltage-divider at FB.

Table 1. Component List

DESIGNATION	DESCRIPTION	PART
C1	10µF ±10%, 6.3V X5R ceramic capacitor	TDK C3216X5R0J106K
C8, C9	4.7µF ±10%, 10V X5R ceramic capacitors	TDK C3225X5R1A475K
D1	1A, 30V Schottky diode	Toshiba CRS02
D2, D3, D4	200mA, 100V dual ultra-fast diodes	Fairchild MMBD4148SE
L1	4.7µH, 1.3A inductor	Sumida CLS5D11HP-4R7

Table 2. Component Suppliers

SUPPLIER	PHONE	FAX	WEBSITE
Inductors			
Sumida USA	847-956-0666	847-956-0702	www.sumida.com
Capacitors			
TDK	847-803-6100	847-803-6296	www.component.tdk.com
Diodes			
Fairchild	888-522-5372	408-822-2104	www.fairchildsemi.com
Toshiba	949-455-2000	949-859-3963	www.toshiba.com/taec/

The regulator controls the output voltage and the power delivered to the outputs by modulating the duty cycle (D) of the power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

The device regulates the output voltage through a combination of an error amplifier, two comparators, and several signal generators (Figure 3). The error amplifier compares the signal at FB to 1.24V and varies the COMP output. The voltage at COMP determines the current trip point each time the internal MOSFET turns on. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope compensation signal is summed with the current-sense signal.

Operational Amplifiers

The MAX1542/MAX1543 include two operational amplifiers that are typically used to drive the LCD backplane VCOM and/or the gamma correction divider string. The operational amplifiers feature ±150mA output short-circuit current, 7.5V/µs slew rate, and 12MHz bandwidth. The rail-to-rail inputs and outputs maximize flexibility.

Short-Circuit Current Limit

The MAX1542/MAX1543 operational amplifiers limit short-circuit current to ±150mA if the output is directly shorted to SUP or AGND. In such a condition, the junction temperature of the IC rises until it reaches the thermal shutdown threshold, typically +160°C. Once it reaches this threshold, the IC shuts down and remains inactive until IN falls below V_{UVLO}.

Driving Pure Capacitive Loads

The operational amplifiers are typically used to drive the LCD backplane (VCOM) or the gamma correction divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load easily driven by the operational amplifiers. However, if the operational amplifiers are used in an application with a pure capacitive load, steps must be taken to ensure stable operation.

As the operational amplifier's capacitive load increases, the amplifier bandwidth decreases and gain peaking increases. A small 5Ω to 50Ω resistance placed between OUT_ and the capacitive load reduces peaking but reduces the amplifier gain. An alternative method of reducing peaking is the use of a snubber circuit. A 150Ω and 10nF (typ) shunt load, or snubber, does not continuously load the output or reduce amplifier gain.

TFT LCD DC-to-DC Converter with Operational Amplifiers

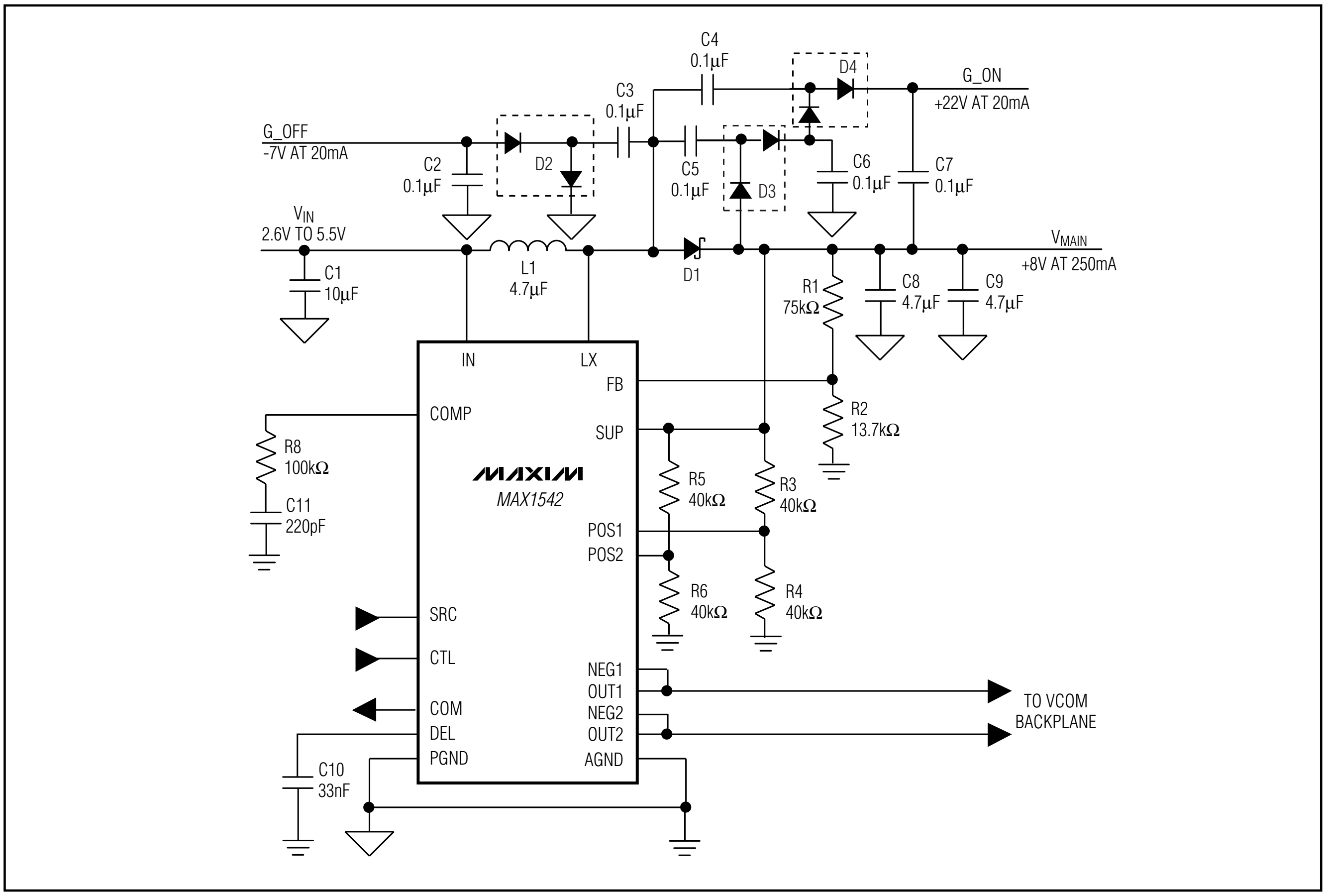


Figure 1. MAX1542 Typical Application Circuit

Delay Control Circuit

A capacitor from DEL to AGND selects the switch control block supply startup delay. After the input voltage exceeds V_{UVLO}, a 5µA current source charges C_{DEL}. Once the capacitor voltage exceeds the turn-on threshold (1.24V) COM can be connected to SRC, depending on the state of CTL. Before startup and when IN is less than V_{UVLO}, DEL is internally connected to AGND to discharge C_{DEL}. Select C_{DEL} using the following equation:

$$C_{DEL} = (\text{DELAY TIME}) \times \frac{5\mu A}{1.24V}$$

MAX1542 Control Block Switch

The switch control input (CTL) is not activated until V_{DEL} exceeds the turn-on voltage (1.24V) and the input voltage (V_{IN}) exceeds V_{UVLO} (2.5V). Once activated, CTL controls the P-channel MOSFET, between COM and SRC. A high at CTL turns on Q1 between SRC and COM, and a low at CTL turns Q1 off (Figure 4).

MAX1543 Control Block Switch

The switch control input (CTL) is not activated until the input voltage (V_{IN}) exceeds V_{UVLO} (2.5V) and V_{DEL} exceeds the turn-on voltage (1.24V). During UVLO or when DEL is below the turn-on threshold, COM is pulled low to PGND through Q3 and a 1kΩ resistance. Once activated, CTL controls the COM MOSFETs, switching COM between SRC and DRN. A high at CTL turns on Q1 and disables Q2. A low at CTL turns on Q2 and turns off Q1 (Figure 4).

Undervoltage Lockout (UVLO)

The UVLO comparator of the MAX1542/MAX1543 compares the input voltage at IN with the UVLO threshold

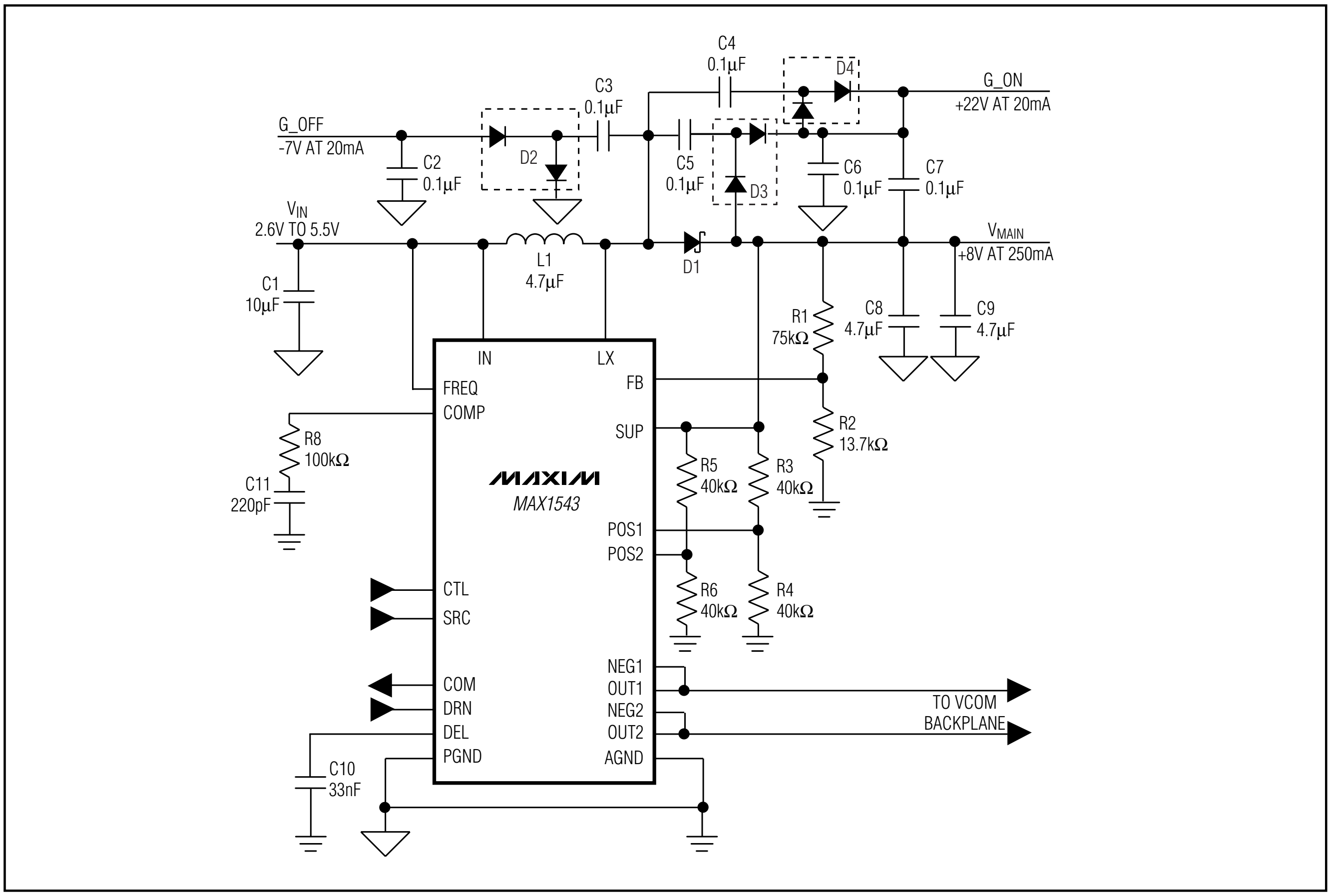


Figure 2. MAX1543 Typical Application Circuit

(2.5V rising, 2.35V falling, typ) to ensure that the input voltage is high enough for reliable operation. The 150mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO threshold, startup begins. When the input voltage falls below the UVLO threshold, the controller turns off the N-channel MOSFET, the switch control block turns off Q1, and the operational amplifier outputs float. For the MAX1543, the switch control block also turns off Q2 and turns on Q3 when the input voltage falls below the UVLO threshold (Figure 4).

Oscillator Frequency (FREQ)

The MAX1542 internal oscillator is preset to 1.2MHz. The internal oscillator frequency is pin programmable for the MAX1543. Connect FREQ to ground or leave it unconnected for 640kHz operation and connect it to V_{IN} for 1.2MHz operation. FREQ has a 5μA (typ) pulldown current.

Fault Protection

Once the soft-start routine is complete, if the output of the main regulator is below the fault detection threshold, the MAX1542/MAX1543 activate the fault timer. If the fault condition continuously exists throughout the fault timer duration, the MAX1542/MAX1543 set the fault latch, which shuts down the device. After removing the fault condition, cycle the input voltage (IN) below V_{UVLO} to clear the fault latch and reactivate the device.

Digital Soft-Start

The MAX1542/MAX1543 digital soft-start period duration is 14ms (typ). During this time, the MAX1542/MAX1543 directly limit the peak inductor current, allowing from zero up to the full current-limit value in eight equal current steps ($I_{LIM}/8$). The maximum load current is available after output voltage reaches the full regulation threshold (which terminates soft-start), or after the soft-start timer expires.

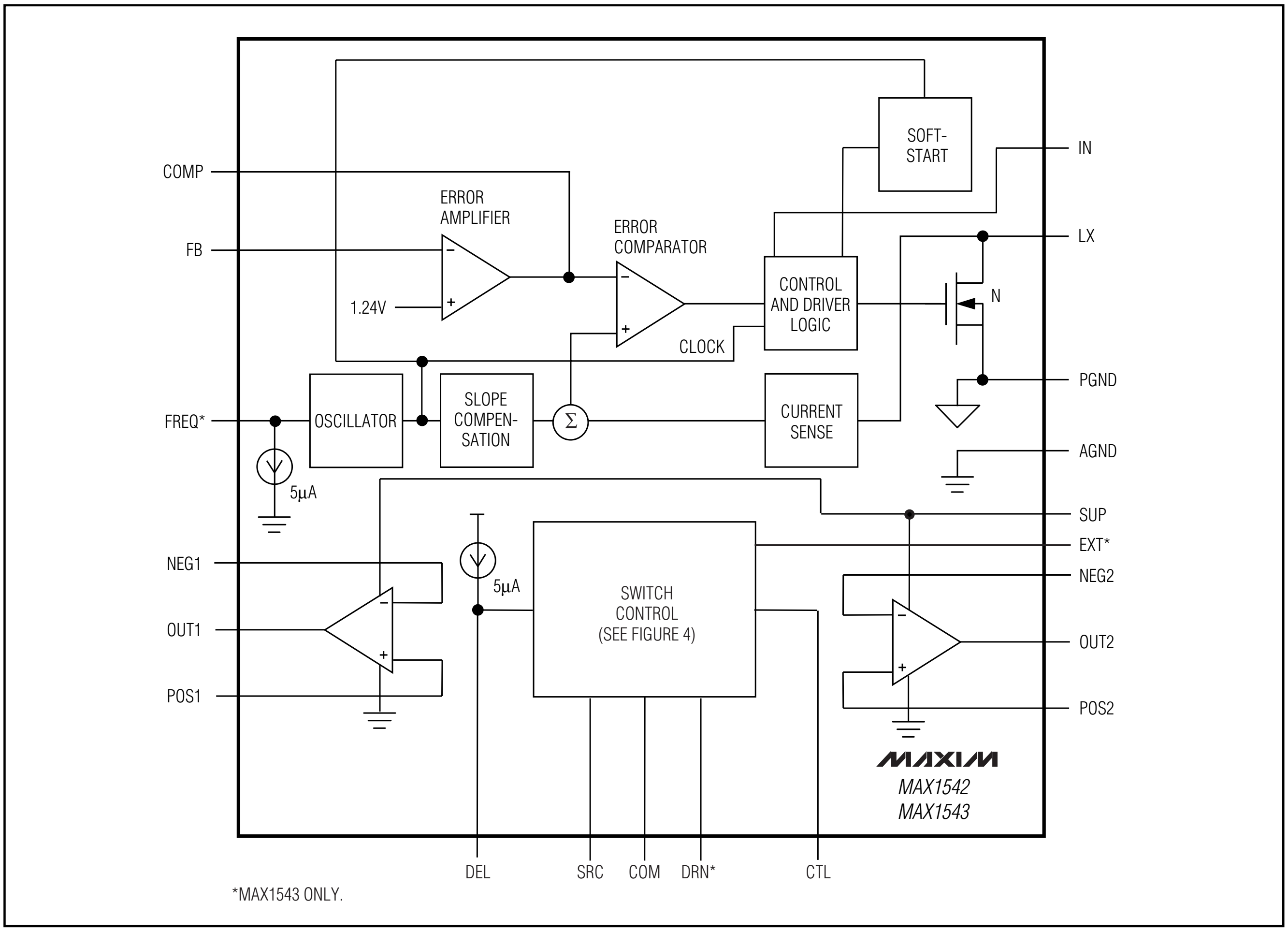


Figure 3. Functional Diagram

Thermal-Overload Protection

Thermal-overload protection prevents excessive power dissipation from overheating the MAX1542/MAX1543. When the junction temperature exceeds T_J = +160°C, a thermal sensor immediately activates the fault protection, which shuts down the device, allowing the IC to cool. The input voltage must fall (below V_{UVLO}) to clear the fault latch and reactivate the controller.

Thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction-temperature rating of T_J = +150°C.

Applications Information

Inductor Selection

The primary considerations in inductor selection are inductor physical shape, circuit efficiency, and cost. The factors that determine the inductance value are input voltage, output voltage, switching frequency, and maximum output current. Final inductor selection includes ensuring the chosen inductor meets the application's peak current and RMS current requirements.

Very high inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the circuit's entire power path. However, large inductance

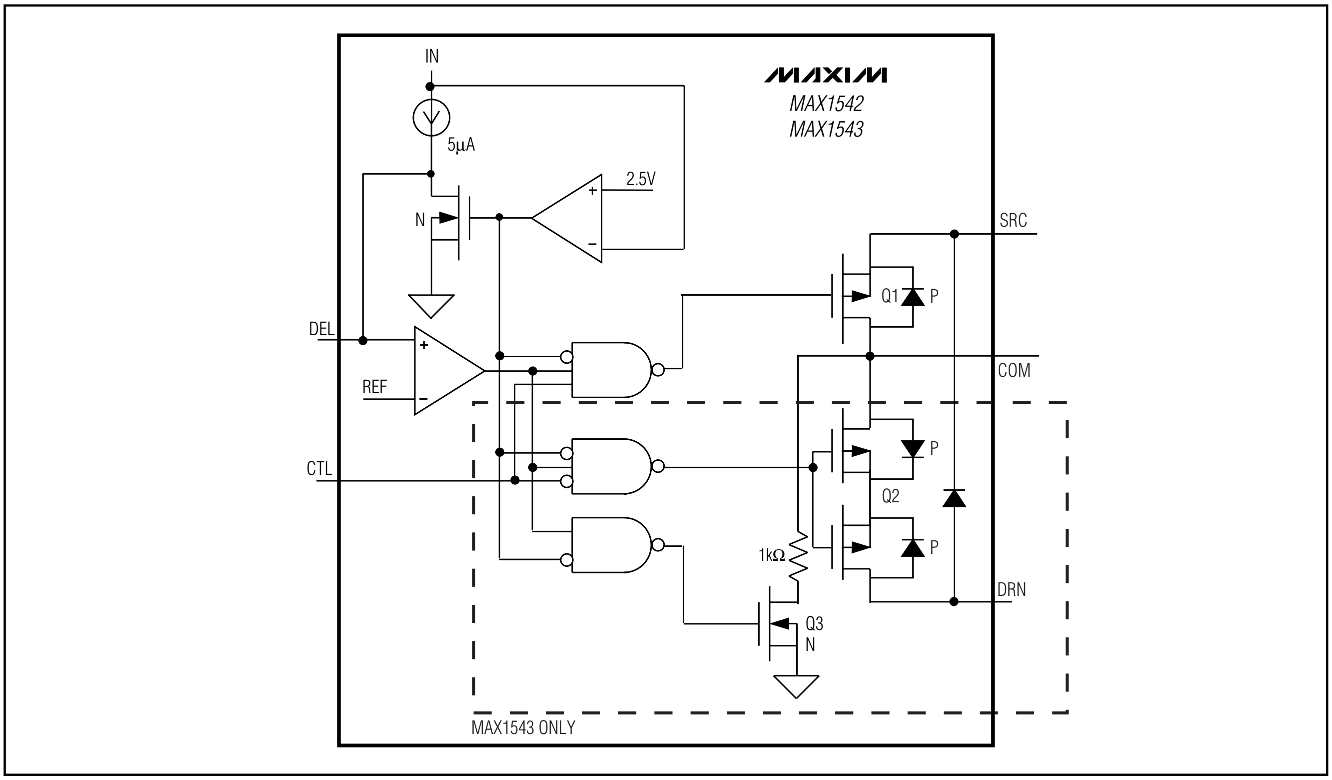


Figure 4. Switch Control

values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise between circuit efficiency, inductor size, and cost.

The equations used here include a constant, LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full output current. The best trade-off between inductor size and circuit efficiency for step-up converters generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin, high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of that inductor should be evaluated for efficiency improvements in typical operating regions.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(MAX)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, and an estimate for LIR based on the above paragraphs:

$$L \cong V_{IN}^2 \times \eta_{TYP} \times (V_{MAIN} - V_{IN}) / (V_{MAIN}^2 \times LIR \times I_{MAIN(MAX)} \times f_{OSC})$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = I_{MAIN(MAX)} \times V_{MAIN} / (V_{IN(MIN)} \times \eta_{MIN})$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = V_{IN(MIN)} \times (V_{MAIN} - V_{IN(MIN)}) / (L \times f_{OSC} \times V_{MAIN})$$

$$I_{PEAK} = I_{IN(DC,MAX)} + (I_{RIPPLE}) / 2$$

The inductor's saturation current rating and the MAX1542/MAX1543s' LX current limit (I_{LIM}) should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For reasonable efficiency, choose an inductor with less than 0.5Ω series resistance.

Considering the *Typical Application Circuits*, the maximum load current ($I_{MAIN(MAX)}$) is 200mA with an 8V output and a typical input voltage of 3.3V.

Choosing an LIR of 0.6 and estimating efficiency of 85% at this operating point:

$$L = (3.3V)^2 \times 0.85 \times (8V - 3.3V) / ((8V)^2 \times 0.6 \times 0.2A \times 1.2MHz) = 4.7\mu H$$

Using the circuit's minimum input voltage (2.7V) and estimating efficiency of 80% at that operating point,

$$I_{IN(DC,MAX)} = (0.2A \times 8V / (2.7V \times 0.8)) = 741mA$$

The ripple current and the peak current are:

$$I_{RIPPLE} = 2.7V \times (8V - 2.7V) / (4.7\mu H \times 1.2MHz \times 8V) = 317mA$$

$$I_{PEAK} = 741mA + (317mA / 2) = 900mA$$

Output Capacitor Selection

The total output voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(ESR)} + V_{RIPPLE(C)}$$

$$V_{RIPPLE(ESR)} \cong I_{PEAK} \times R_{ESR(COUT)}, \text{ and}$$

$$V_{RIPPLE(C)} \cong \frac{I_{MAIN}}{C_{OUT}} \left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} \times f_{OSC}} \right)$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input Capacitor Selection

The input capacitor (C_{IN}) reduces the current peaks drawn from the input supply and reduces noise injection into the device. A 10µF ceramic capacitor is used in the *Typical Application Circuits* (Figures 1 and 2) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply. Typically, C_{IN} can be reduced below the values used in the *Typical Application Circuits*. Ensure a low-noise supply at IN by using adequate C_{IN}.

Output Voltage

The MAX1542/MAX1543 operate with an adjustable output from V_{IN} to 13V. Connect a resistive voltage-divider to FB (*Typical Application Circuits*) from the output (V_{MAIN}) to AGND. Select the resistor values as follows:

$$R_1 = R_2 \left(\frac{V_{MAIN}}{V_{FB}} - 1 \right)$$

where V_{FB}, the step-up converter feedback set point, is 1.24V. Since the input bias current into FB is typically zero, R_2 can have a value up to 100kΩ without sacrificing accuracy, although lower values provide better noise immunity. Connect the resistor-divider as close to the IC as possible.

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \cong \frac{500 \times V_{IN} \times V_{OUT} \times C_{OUT}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \cong \frac{V_{OUT} \times C_{OUT}}{10 \times I_{MAIN(MAX)} \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient response waveforms.

Charge Pumps

Selecting the Number of Charge-Pump Stages

For highest efficiency, always choose the lowest number of charge-pump stages that meet the output requirements. Figures 5 and 6 show the positive and

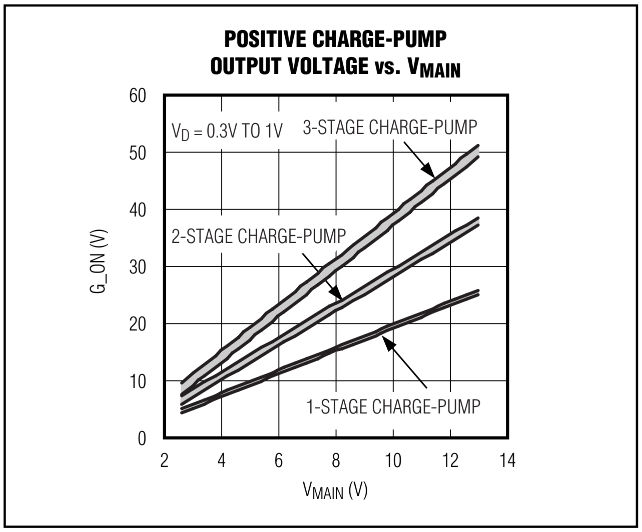


Figure 5. Positive Charge-Pump Output Voltage vs. V_{MAIN}

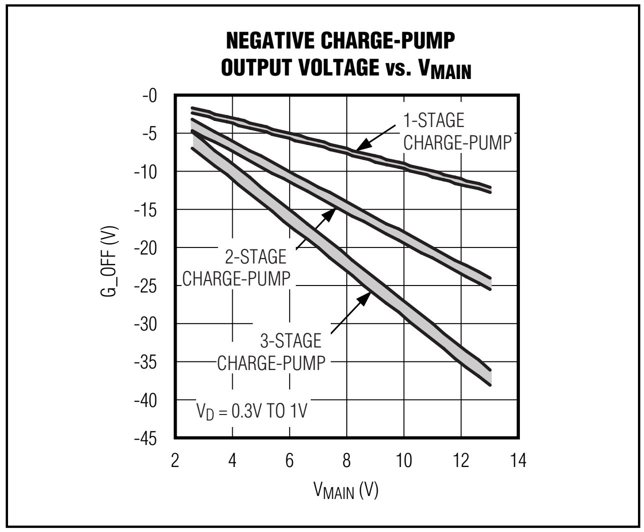


Figure 6. Negative Charge-Pump Output Voltage vs. V_{MAIN}

negative charge-pump output voltages for a given V_{MAIN} for one-, two-, and three-stage charge pumps, based on the following equations:

$$G\_ON = V_{MAIN} + n(V_{MAIN} - V_D)$$
$$G\_OFF = -n(V_{MAIN} - V_D)$$

where G_ON is the positive charge-pump output voltage, G_OFF is the negative charge-pump output voltage, n is the number of charge-pump stages, and V_D is the voltage drop across each diode.

V_D is the forward voltage drop of the charge-pump diodes.

Flying Capacitors

Increasing the flying capacitor (C3, C4, and C5) value increases the output current capability. Increasing the capacitance indefinitely has a negligible effect on output current capability because the internal switch resistance and the diode impedance limit the source impedance. A 0.1µF ceramic capacitor works well in most low-current applications. The flying capacitor's voltage rating must exceed the following:

$$V_{CX} > n \times V_{MAIN}$$

Where n is the stage number in which the flying capacitor appears, and V_{MAIN} is the main output voltage. For example, the two-stage positive charge pump in the *Typical Application Circuits* (Figures 1 and 2) where V_{MAIN} = 8V contains two flying capacitors. The flying capacitor in the first stage (C5) requires a voltage rating greater than 8V. The flying capacitor in the second stage (C4) requires a voltage rating greater than 16V.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. With ceramic capacitors, the output voltage ripple is dominated by the capacitance value. Use the following equation to approximate the required capacitor value:

$$C_{OUT} \geq \frac{I_{LOAD}}{2 \times F_{OSC} \times V_{RIPPLE}}$$

where V_{RIPPLE} is the acceptable peak-to-peak output-voltage ripple.

Charge-Pump Rectifier Diodes

To maximize the available output voltage, use Schottky diodes with a current rating equal to or greater than two times the average charge-pump input current. If the loaded charge-pump output voltage is greater than required, some or all of the Schottky diodes can be replaced with low-cost silicon switching diodes with an equivalent current rating. The charge-pump input current is:

$$I_{CP\_IN} = I_{CP\_OUT} \times n$$

where n is the number of charge-pump stages.

TFT LCD DC-to-DC Converter with Operational Amplifiers

Power Dissipation

The MAX1542/MAX1543s' maximum power dissipation depends on the thermal resistance from the IC die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PC board copper area, other thermal mass, and airflow. The MAX1542/MAX1543, with their exposed backside pad soldered to $1in^2$ of PC board copper, can dissipate about 1.7W into +70°C still air. More PC board copper, cooler ambient air, and more airflow increase the possible dissipation while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the step-up converter and the power dissipated by the operational amplifiers.

Step-Up Converter

The largest portions of power dissipation in the step-up converter are the internal MOSFET, inductor, and the output diode. If the step-up converter has 90% efficiency, about 3% to 5% of the power is lost in the internal MOSFET, about 3% to 4% in the inductor, and about 1% in the output diode. The rest of the 1% to 3% is distributed among the input and output capacitors and the PC board traces. If the input power is about 3W, the power lost in the internal MOSFET is about 90mW to 150mW.

Operational Amplifiers

The power dissipated in the operational amplifiers depends on their output current, the output voltage, and the supply voltage:

$$PD_{SOURCE} = I_{OUT\_(SOURCE)} \times (V_{SUP} - V_{OUT\_})$$

$$PD_{SINK} = I_{OUT\_(SINK)} \times V_{OUT\_}$$

where $I_{OUT\_(SOURCE)}$ is the output current sourced by the operational amplifier, and $I_{OUT\_(SINK)}$ is the output current that the operational amplifier sinks.

In a typical case where the supply voltage is 8V and the output voltage is 4V with an output source current of 30mA, the power dissipated is 120mW.

Layout Procedure

Careful PC board layout and routing are required for high-frequency switching power supplies to achieve good regulation, high efficiency, and stability. Use the following guidelines for good PC board layout:

1) Place the input capacitors close enough to the IC to provide adequate bypassing (within 1.5cm). Connect the input capacitors to IN with a wide trace.

   Minimize the area of high-current loops by placing the inductor, output diode, and output capacitors near the input capacitors and near LX and PGND. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out PGND, and to the input capacitor negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the catch diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components together with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.

2) Create a power ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and the SRC bypass capacitor and other charge-pump components. Connect all of these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output voltage ripple and noise spikes.

   Create an analog ground island (AGND) consisting of the AGND pin, FB divider, the operation amplifier dividers, the COMP and DEL capacitor ground connections, and the device's exposed backside pad.

   Connect the AGND and PGND islands by connecting the PGND pin directly to the exposed backside pad. Make no other connections between these separate ground planes.

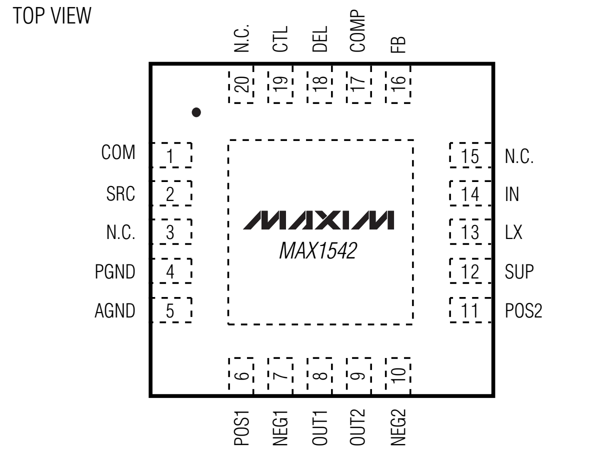
3) Place the feedback voltage-divider resistors close to FB. The divider's center trace should be kept short. Placing the resistors far away causes their FB traces to become antennas that can pick up switching noise. Avoid running the feedback trace near LX or the switching nodes in the charge pumps.

4) Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient response.

5) Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node (FB) and analog ground. Use DC traces as shields if necessary.

Refer to the MAX1543 Evaluation Kit for an example of proper board layout.

Pin Configurations (continued)



THIN QFN

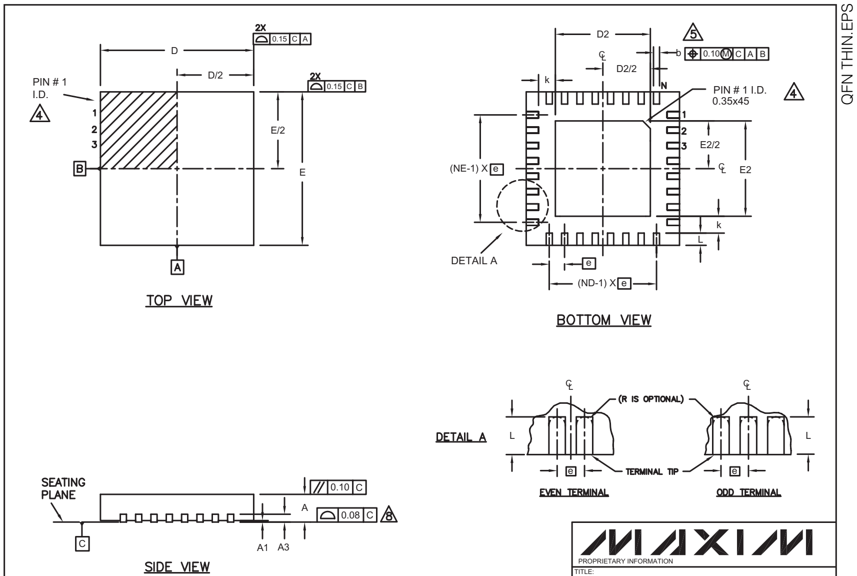
Chip Information

TRANSISTOR COUNT: 2508

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

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COMMON DIMENSIONS												
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A3	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50
N	16			20			28			32		
ND	4			5			7			8		
NE	4			5			7			8		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-2	3.00	3.10	3.20	3.00	3.10	3.20
T2855-1	3.15	3.25	3.35	3.15	3.25	3.35
T2855-2	2.60	2.70	2.80	2.60	2.70	2.80
T3255-2	3.00	3.10	3.20	3.00	3.10	3.20

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
16, 20, 28, 32L, QFN THIN, 5x5x0.8 mm

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