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19-3048; Rev 2; 10/07

Low-Input-Voltage, 500mA LDO Regulator with RESET in SOT and TDFN

General Description

The MAX1589 low-dropout linear regulator operates from a +1.62V to +3.6V supply and delivers a guaranteed 500mA continuous load current with a low 175mV dropout. The high-accuracy (±0.5%) output voltage is preset to internally trimmed voltages from +0.75V to +3.0V. An active-low, open-drain reset output remains asserted for at least 70ms after the output voltage reaches regulation. This device is offered in 6-pin thin SOT23 and 6-pin 3mm x 3mm thin DFN packages.

An internal PMOS pass transistor maintains low supply current, independent of load and dropout voltage, making the MAX1589 ideal for portable battery-powered equipment such as personal digital assistants (PDAs), digital still cameras, cell phones, cordless phones, and notebook computers. Other features include logic-controlled shutdown, short-circuit protection, and thermal-overload protection.

Applications

Notebook Computers

Cellular and PCS Telephones

Personal Digital Assistants (PDAs)

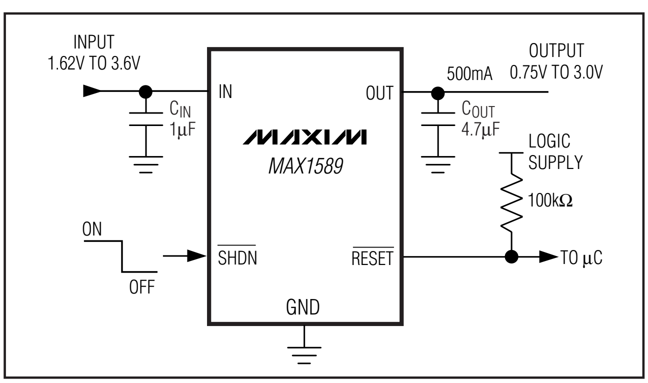
Hand-Held Computers

Digital Still Cameras

PCMCIA Cards

CD and MP3 Players

Typical Operating Circuit



Features

- ♦ **Low 1.62V Minimum Input Voltage**
- ♦ **Guaranteed 500mA Output Current**
- ♦ **±0.5% Initial Accuracy**
- ♦ **Low 175mV Dropout at 500mA Load**
- ♦ **70ms RESET Output Flag**
- ♦ **Supply Current Independent of Load and Dropout Voltage**
- ♦ **Logic-Controlled Shutdown**
- ♦ **Thermal-Overload and Short-Circuit Protection**
- ♦ **Preset Output Voltages (0.75V, 1.0V, 1.2V, 1.3V, 1.5V, 1.8V, 2.5V, and 3.0V)**
- ♦ **Tiny 6-Pin Thin SOT23 Package (<1.1mm High)**
- ♦ **Thin 6-Pin TDFN Package (<0.8mm High)**

Ordering Information

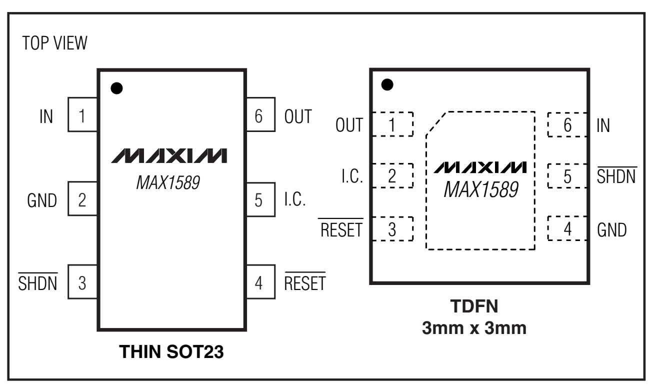
PART*	TEMP RANGE	PIN-PACKAGE
MAX1589EZT_ _ _-T	-40°C to +85°C	6 Thin SOT23-6
MAX1589ETT_ _ _	-40°C to +85°C	6 TDFN

**Insert the desired three-digit suffix (see the Selector Guide) into the blanks to complete the part number. Contact the factory for other output voltages.*

Selector Guide

V_{OUT} (V)	SUFFIX	TOP MARK	
		SOT	TDFN
0.75	075	AAAT	AFJ
1.00	100	AAAU	AFK
1.20	120	—	ATM
1.30	130	AAAV	AFL
1.50	150	AAAW	AFM
1.80	180	AAAX	AFN
2.50	250	AAAY	AFO
3.00	300	AAAZ	AFP

Pin Configurations



ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, $\overline{RESET}$ to GND ....-0.3V to +4.0V
OUT to GND ....-0.3V to (V_{IN} + 0.3V)
Output Short-Circuit Duration....................................Continuous
Continuous Power Dissipation (T_A = +70°C)
6-Pin Thin SOT23 (derate 9.1mW/°C above +70°C)....727mW
6-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range ....-40°C to +85°C
Junction Temperature.. +150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = (V_{OUT} + 0.5V) or V_{IN} = 1.8V, whichever is greater; $\overline{SHDN}$ = IN, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage	V_{IN}		1.62		3.60	V
Input Undervoltage Lockout	V_{UVLO}	V_{IN} rising (180mV typical hysteresis)	1.30		1.60	V
Output Voltage Accuracy		I_{OUT} = 150mA, T_A = +25°C	-0.5		+0.5	%
		I_{OUT} = 1mA to 500mA, V_{IN} = (V_{OUT} + 0.5V) to +3.6V	-1.5		+1.5	
Maximum Output Current	I_{OUT}	Continuous	500			mA_{RMS}
Current Limit	I_{LIM}	V_{OUT} = 96% of nominal value	550	850	1150	mA
Ground Current	I_Q	No load		70	140	µA
		I_{OUT} = 500mA		90		
		Dropout (Note 2)		70		
Dropout Voltage	V_{IN} - V_{OUT}	I_{OUT} = 500mA, V_{OUT} ≥ 1.8V (Note 2)		175	350	mV
Load Regulation	ΔV_{LDR}	I_{OUT} = 1mA to 500mA		0.02	0.5	%
Line Regulation	ΔV_{LNR}	V_{IN} = (V_{OUT} + 0.5V) to +3.6V, I_{OUT} = 100mA	-0.15	+0.01	+0.15	%/V
Output Noise		10Hz to 100kHz, I_{OUT} = 10mA		86		$µV_{RMS}$
PSRR		f < 1kHz, I_{OUT} = 10mA		70		dB
SHUTDOWN						
Shutdown Supply Current	I_{OFF}	$\overline{SHDN}$ = GND, T_A = +25°C		0.001	1	µA
		$\overline{SHDN}$ = GND, T_A = +85°C		0.01		
$\overline{SHDN}$ Input Logic Levels	V_{IH}	V_{IN} = 1.62V to 3.6V	1.4			V
	V_{IL}	V_{IN} = 1.62V to 3.6V			0.6	
$\overline{SHDN}$ Input Bias Current	I_{SHDN}	$V_{\overline{SHDN}}$ = 0 or 3.6V, T_A = +25°C		1	300	nA
		$V_{\overline{SHDN}}$ = 0 or 3.6V, T_A = +85°C		5		
Turn-On Delay		From $\overline{SHDN}$ high to OUT high, V_{OUT} = 1.5V		90		µs
$\overline{RESET}$ OUTPUT						
Reset Threshold Accuracy		V_{OUT} falling (1.7% typical hysteresis)	80	82.5	85	$\%V_{OUT}$
$\overline{RESET}$ Output Low Voltage	V_{OL}	$I_{\overline{RESET}}$ = 100µA		1.5	100	mV
		V_{IN} = +1.0V, $I_{\overline{RESET}}$ = 100µA		3	100	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = (V_{OUT} + 0.5V) or V_{IN} = 1.8V, whichever is greater; $\overline{SHDN}$ = IN, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

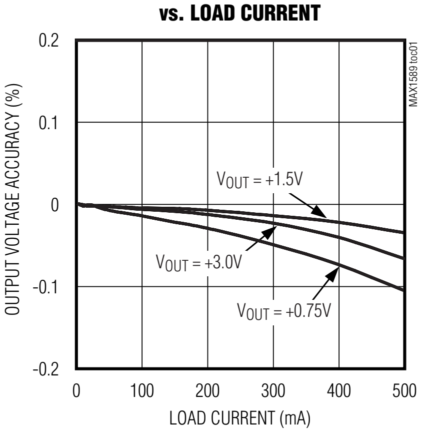
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{RESET}$ Output High Leakage Current	I_{OH}	$V_{\overline{RESET}}$ = 3.6V, $\overline{RESET}$ not asserted	T_A = +25°C		0.001	1	µA
			T_A = +85°C		0.01		
Reset Delay	t_{RP}	From V_{OUT} high to $\overline{RESET}$ rising		70	100	160	ms
THERMAL PROTECTION							
Thermal-Shutdown Temperature	$T_{\overline{SHDN}}$				+165		°C
Thermal-Shutdown Hysteresis	$\Delta T_{\overline{SHDN}}$				15		°C

Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 2: The dropout voltage is defined as V_{IN} - V_{OUT}, when V_{OUT} is 4% lower than the value of V_{OUT} when V_{IN} = V_{OUT} + 0.5V.

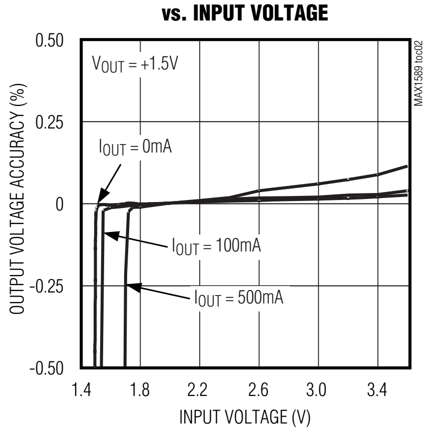
Typical Operating Characteristics

(V_{IN} = (V_{OUT} + 0.5V) or 1.8V, whichever is greater; $\overline{SHDN}$ = IN, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

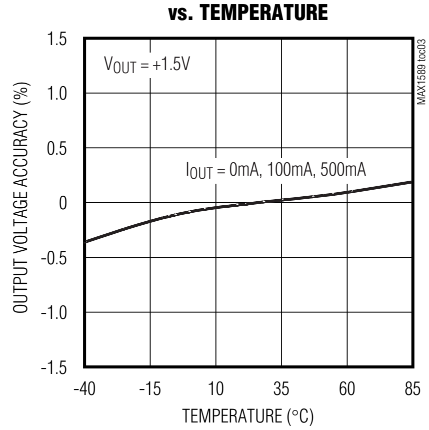
OUTPUT VOLTAGE ACCURACY vs. LOAD CURRENT



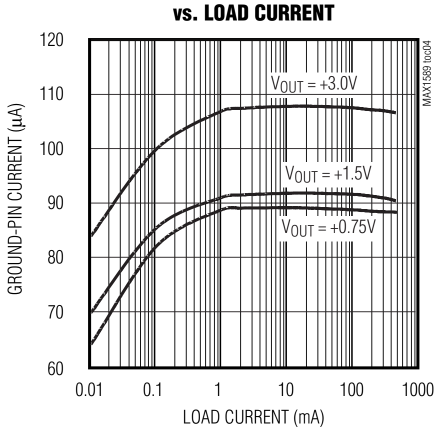
OUTPUT VOLTAGE ACCURACY vs. INPUT VOLTAGE



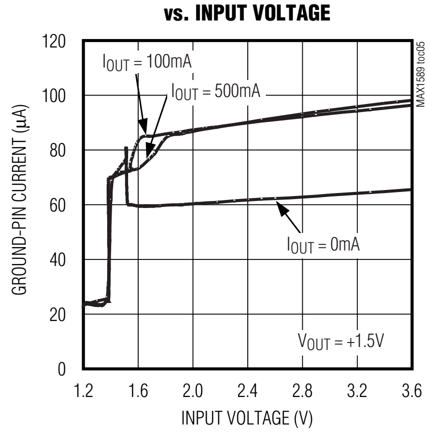
OUTPUT VOLTAGE ACCURACY vs. TEMPERATURE



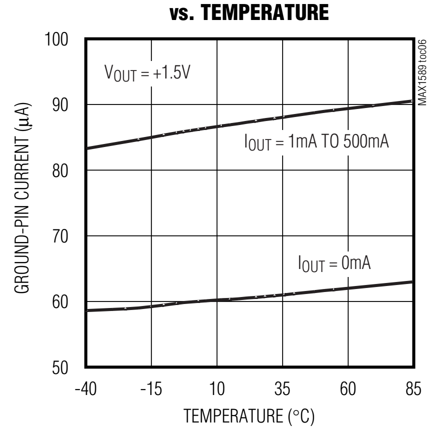
GROUND-PIN CURRENT vs. LOAD CURRENT



GROUND-PIN CURRENT vs. INPUT VOLTAGE



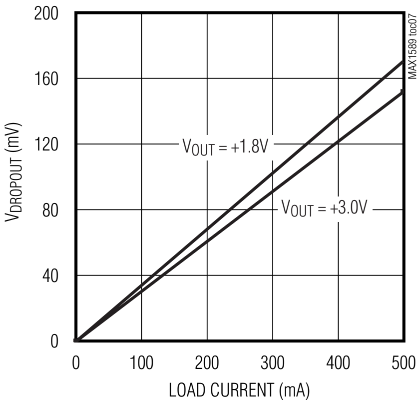
GROUND-PIN CURRENT vs. TEMPERATURE



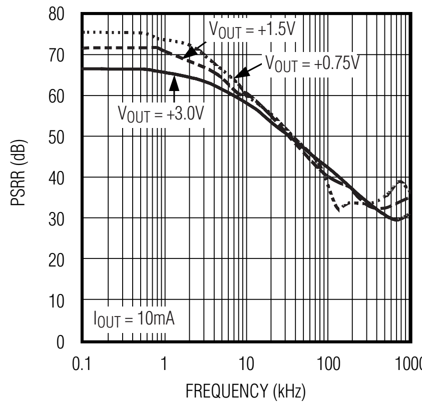
Typical Operating Characteristics (continued)

(V_{IN} = (V_{OUT} + 0.5V) or 1.8V, whichever is greater; $\overline{SHDN}$ = IN, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)

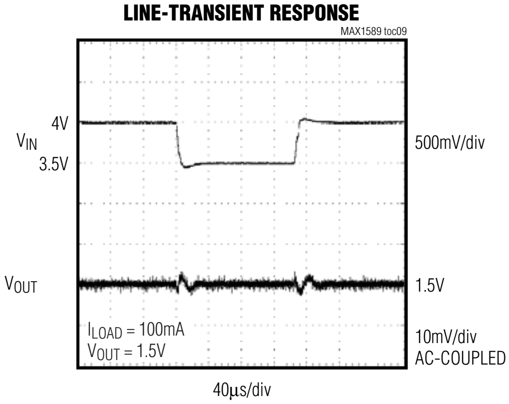
DROPOUT VOLTAGE vs. LOAD CURRENT



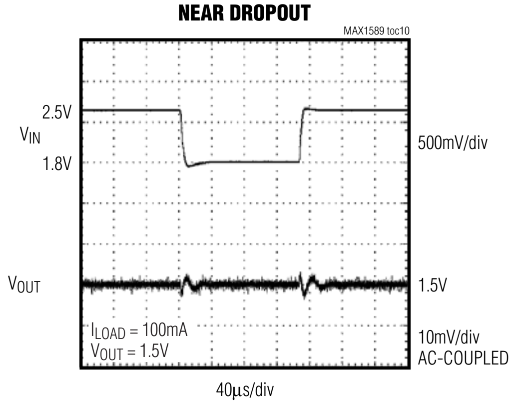
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



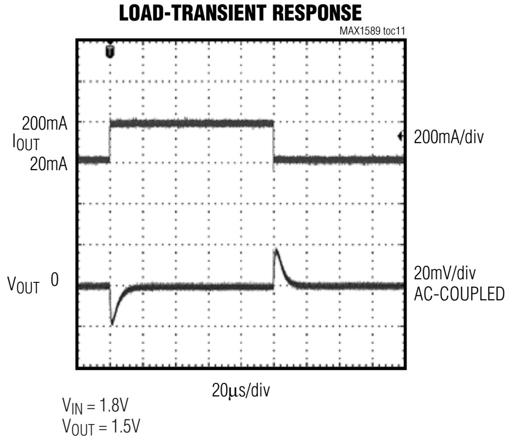
LINE-TRANSIENT RESPONSE



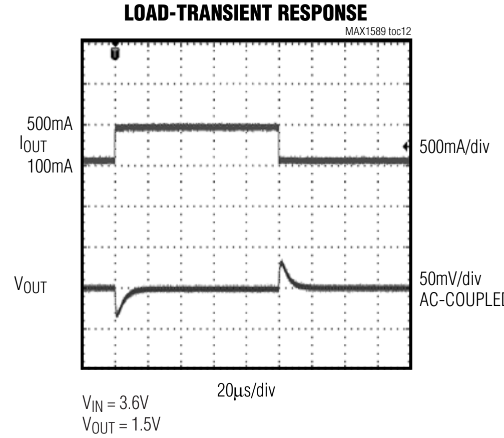
LINE-TRANSIENT RESPONSE NEAR DROPOUT



LOAD-TRANSIENT RESPONSE

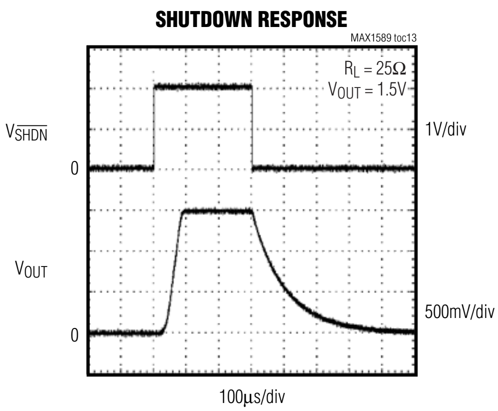


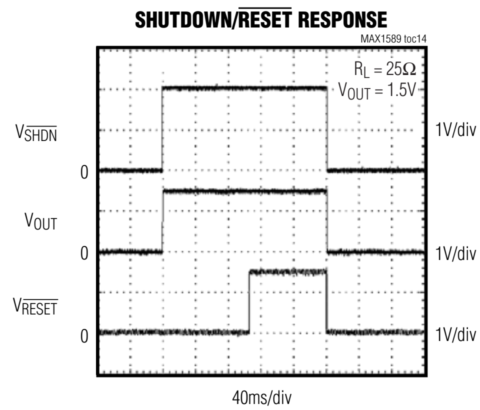
LOAD-TRANSIENT RESPONSE

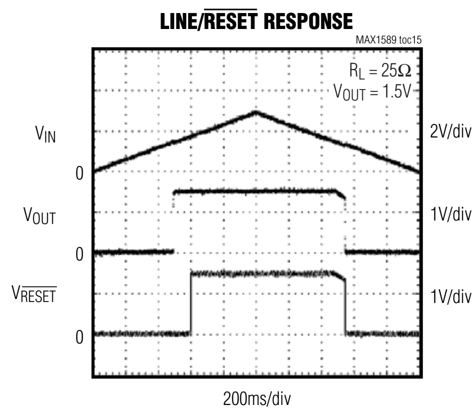


Typical Operating Characteristics (continued)

(V_{IN} = (V_{OUT} + 0.5V) or 1.8V, whichever is greater; $\overline{SHDN}$ = IN, C_{IN} = 1µF, C_{OUT} = 4.7µF, T_A = +25°C, unless otherwise noted.)







Low-Input-Voltage, 500mA LDO Regulator with $\overline{RESET}$ in SOT and TDFN

Pin Description

PART		NAME	FUNCTION
SOT23	TDFN		
1	6	IN	Regulator Input. Supply voltage can range from +1.62V to +3.6V. Bypass IN with at least a 1µF ceramic capacitor to GND (see the *Capacitor Selection and Regulator Stability* section).
2	—	GND	Ground. GND also functions as a heatsink. Solder GND to a large pad or circuit-board ground plane to maximize SOT23 power dissipation.
—	4	GND	Ground
3	5	$\overline{SHDN}$	Active-Low Shutdown Input. A logic low reduces supply current to below 1µA. Connect to IN or logic high for normal operation.
4	3	$\overline{RESET}$	Active-Low, Open-Drain Reset Output. $\overline{RESET}$ rises 100ms after the output has achieved regulation. $\overline{RESET}$ falls immediately if V_{OUT} drops below 82.5% of its nominal voltage, or if the MAX1589 is shut down.
5	2	I.C.	Internally Connected. Leave floating or connect to GND.
6	1	OUT	Regulator Output. Sources up to 500mA. Bypass with a 4.7µF low-ESR ceramic capacitor to GND.
—	Exposed Pad	EP	Ground. EP also functions as a heatsink. Solder EP to a large pad or circuit-board ground plane to maximize TDFN power dissipation.

Detailed Description

The MAX1589 is a low-dropout, low-quiescent-current, high-accuracy linear regulator designed primarily for battery-powered applications. The device supplies loads up to 500mA and is available with preset output voltages from +0.75V to +3.0V. As illustrated in Figure 1, the MAX1589 contains a reference, an error amplifier, a P-channel pass transistor, an internal feedback voltage-divider, and a power-good comparator.

The error amplifier compares the reference with the feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, allowing more current to pass to the output and increasing the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output.

Internal P-Channel Pass Transistor

The MAX1589 features a 0.33Ω ($R_{DS(ON)}$) P-channel MOSFET pass transistor. Unlike similar designs using PNP pass transistors, P-channel MOSFETs require no base drive, which reduces quiescent current. PNP-based regulators also waste considerable current in dropout when the pass transistor saturates and use high base-drive currents under large loads. The MAX1589 does not suffer from these problems and consumes only 90µA (typ) of quiescent current under heavy loads, as well as in dropout.

Shutdown

Pull $\overline{SHDN}$ low to enter shutdown. During shutdown, the output is disconnected from the input, an internal 1.5kΩ resistor pulls OUT to GND, $\overline{RESET}$ is actively pulled low, and supply current drops below 1µA.

$\overline{RESET}$ Output

The MAX1589's microprocessor (µP) supervisory circuitry asserts a guaranteed logic-low reset during power-up, power-down, and brownout conditions down to +1V. $\overline{RESET}$ asserts when V_{OUT} is below the reset threshold and remains asserted for at least 70ms (t_{RP}) after V_{OUT} rises above the reset threshold.

Current Limit

The MAX1589 monitors and controls the pass transistor's gate voltage, limiting the output current to 850mA (typ). If the output current exceeds I_{LIM}, the MAX1589 output voltage drops.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX1589. When the junction temperature exceeds +165°C, a thermal sensor turns off the pass

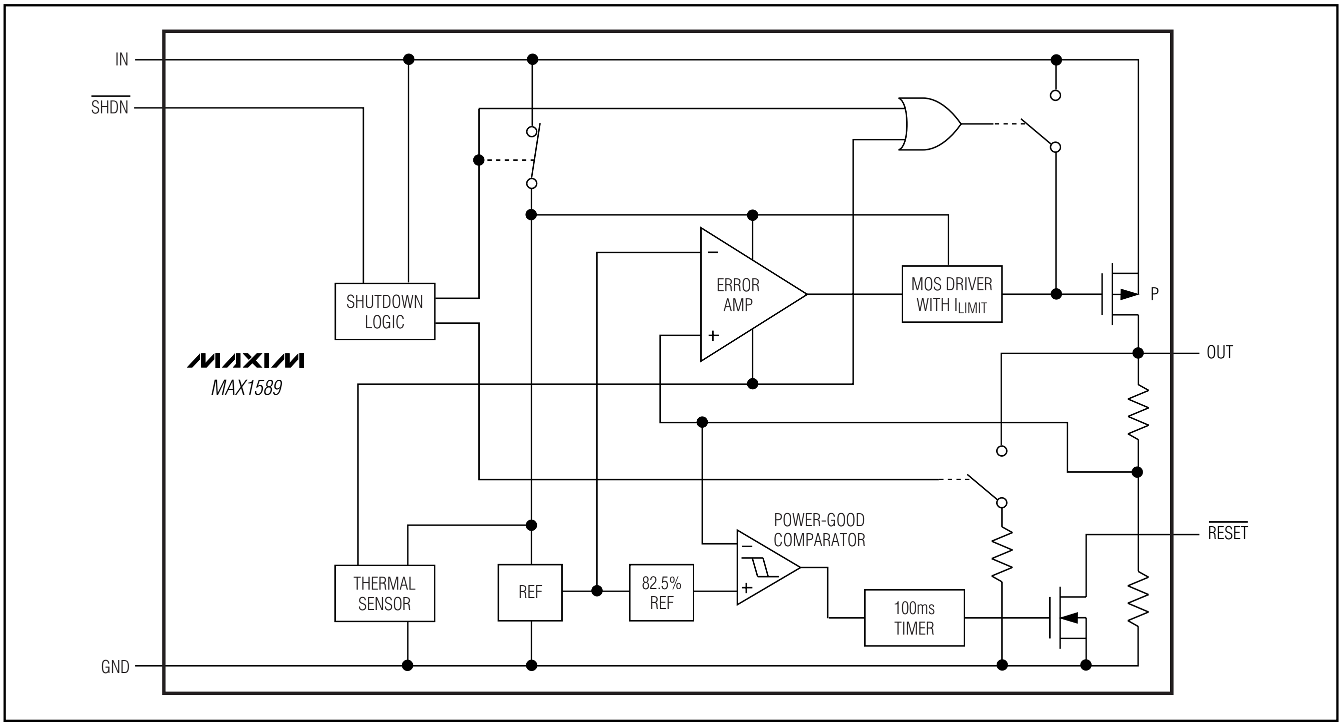


Figure 1. Functional Diagram

transistor, allowing the IC to cool. The thermal sensor turns the pass transistor on again after the junction temperature cools by 15°C, resulting in a pulsed output during continuous thermal-overload conditions. Thermal-overload protection safeguards the MAX1589 in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction-temperature rating of +150°C.

Operating Region and Power Dissipation

The MAX1589's maximum power dissipation depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of airflow. The power dissipated in the device is $P = I_{OUT} \times (V_{IN} - V_{OUT})$. The maximum allowed power dissipation is:

$$P_{MAX} = (T_{J(MAX)} - T_A) / (\theta_{JC} + \theta_{CA})$$

where $T_{J(MAX)} - T_A$ is the temperature difference between the MAX1589 die junction and the surrounding air, θ_{JC} is the thermal resistance of the junction to the case, and θ_{CA} is the thermal resistance from the case through the PC board, copper traces, and other materials to the surrounding air. Typical thermal resistance ($\theta_{JC} + \theta_{JA}$) for a device mounted to a 1in square, 1oz copper pad is 41°C/W for the 3mm x 3mm TDFN package, and 110°C/W for the 6-pin thin SOT23 package. For best heatsinking, expand the copper connected to GND, or the exposed paddle.

The MAX1589 delivers up to 500mA and operates with an input voltage up to +3.6V. However, when using the 6-pin SOT23 version, high output currents can only be sustained when the input-output differential voltage is low, as shown in Figure 2.

The maximum allowed power dissipation for the 6-pin TDFN is 1.951W at T_A = +70°C. Figure 3 shows that the maximum input-output differential voltage is not limited by the TDFN package power rating.

Applications Information

Capacitor Selection and Regulator Stability

Capacitors are required at the MAX1589's input and output for stable operation over the full temperature range and with load currents up to 500mA. Connect a 1µF ceramic capacitor between IN and GND and a 4.7µF low-ESR ceramic capacitor between OUT and GND. The input capacitor (C_{IN}) lowers the source impedance of the input supply. Use larger output

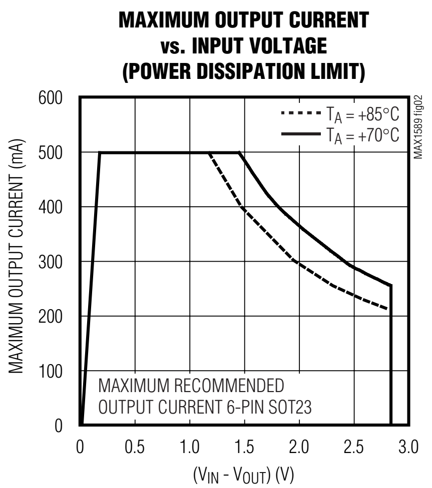


Figure 2. Power Operating Regions for 6-Pin SOT23: Maximum Output Current vs. Input Voltage

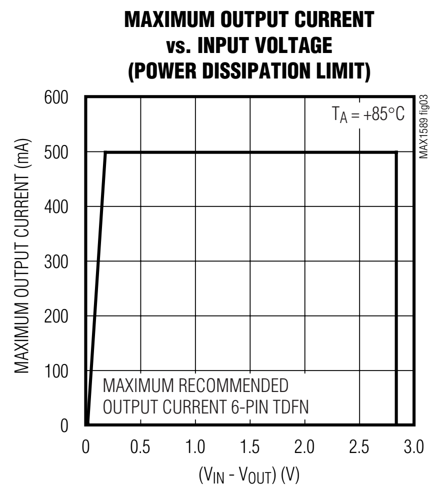


Figure 3. Power Operating Region for 6-Pin TDFN: Maximum Output Current vs. Input Voltage

capacitors to reduce noise and improve load-transient response, stability, and power-supply rejection.

The output capacitor's equivalent series resistance (ESR) affects stability and output noise. Use output capacitors with an ESR of 30mΩ or less to ensure stability and optimize transient response. Surface-mount ceramic capacitors have very low ESR and are commonly available in values up to 10µF. Connect C_{IN} and C_{OUT} as close to the MAX1589 as possible to minimize the impact of PC board trace inductance.

Noise, PSRR, and Transient Response

The MAX1589 is designed to operate with low dropout voltages and low quiescent currents in battery-powered systems, while still maintaining good noise, transient response, and AC rejection. See the *Typical Operating Characteristics* for a plot of Power-Supply Rejection Ratio (PSRR) vs. Frequency. When operating from noisy sources, improved supply-noise rejection and transient response can be achieved by increasing the values of the input and output bypass capacitors and through passive filtering techniques.

The MAX1589 load-transient response (see the *Typical Operating Characteristics*) shows two components of the output response: a near-zero DC shift from the output impedance due to the load-current change, and the transient response. A typical transient response for a step change in the load current from 100mA to 500mA is 35mV. Increasing the output capacitor's value and decreasing the ESR attenuates the overshoot.

Input-Output (Dropout) Voltage

A regulator's minimum input-output voltage difference (dropout voltage) determines the lowest usable supply voltage. In battery-powered systems, this determines the useful end-of-life battery voltage. Because the MAX1589 uses a P-channel MOSFET pass transistor, its dropout voltage is a function of drain-to-source on-resistance ($R_{DS(ON)}$ = 0.33Ω) multiplied by the load current (see the *Typical Operating Characteristics*):

$$V_{DROPOUT} = V_{IN} - V_{OUT} = 0.33\Omega \times I_{OUT}$$

The MAX1589 ground current reduces to 70µA in dropout.

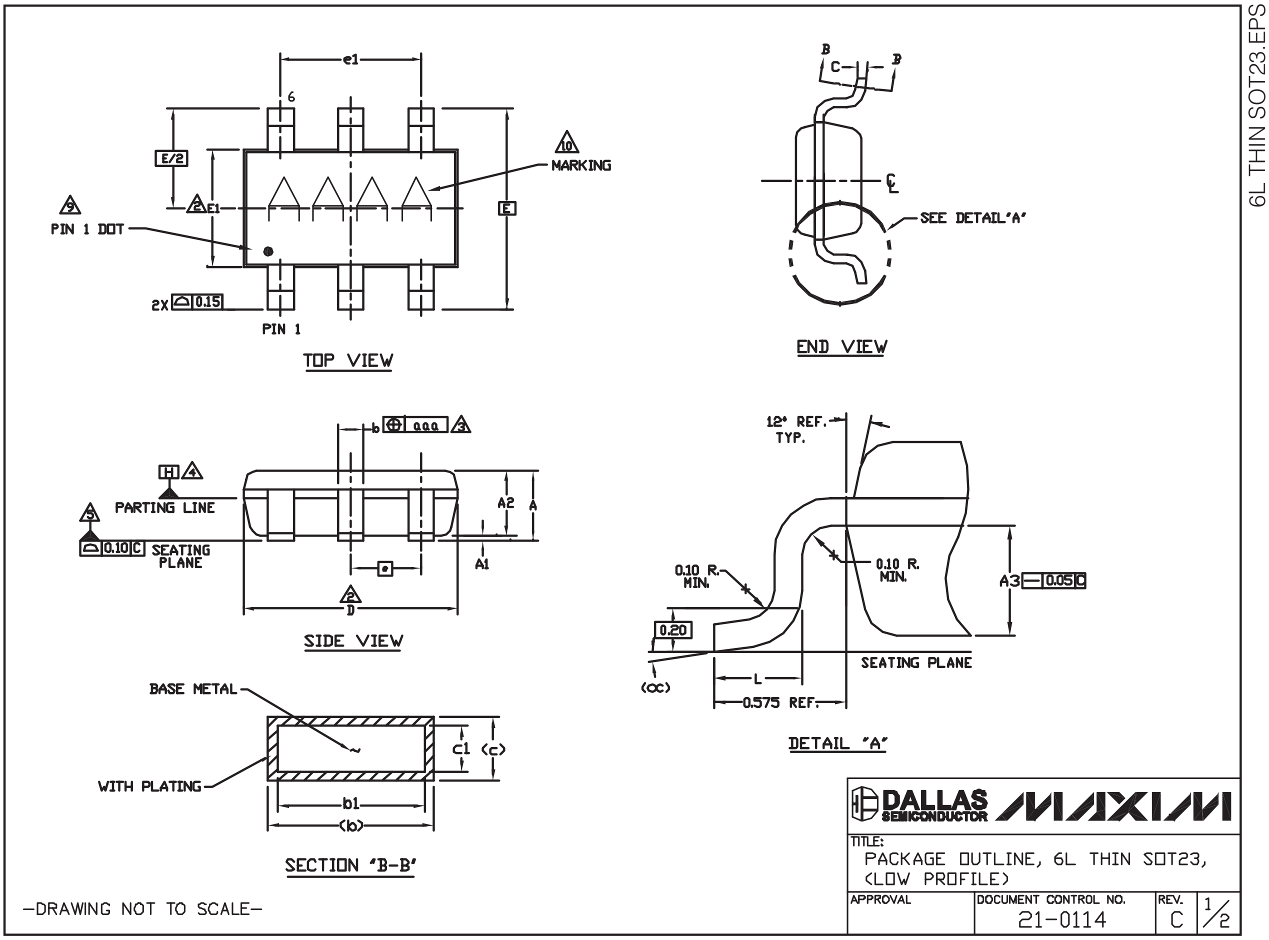
Chip Information

TRANSISTOR COUNT: 2556

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Low-Input-Voltage, 500mA LDO Regulator with $\overline{RESET}$ in SOT and TDFN

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. "D" AND "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15mm ON "D" AND 0.25mm ON "E" PER SIDE.
3. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DATUM PLANE "H" LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT THE BOTTOM OF PARTING LINE.
5. THE LEAD TIPS MUST LINE WITHIN A SPECIFIED TOLERANCE ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL LINES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; AND THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITH 0.10mm AT SEATING PLANE.
6. THIS PART IS COMPLIANT WITH JEDEC SPECIFICATION MO-193 EXCEPT FOR THE "e" DIMENSION WHICH IS 0.95mm INSTEAD OF 1.00mm. THIS PART IS IN FULL COMPLIANCE TO EIAJ SPECIFICATION SC-74.
7. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
8. WARPAGE SHALL NOT EXCEED 0.10mm.
9. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 PP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

SYMBOLS	MIN	NOM	MAX
A	-	-	1.10
A1	0.00	0.075	0.10
A2	0.85	0.88	0.90
A3	0.50 BSC		
b	0.30	-	0.45
b1	0.25	0.35	0.40
c	0.15	-	0.20
c1	0.12	0.127	0.15
D	2.80	2.90	3.00
E	2.75 BSC		
E1	1.55	1.60	1.65
L	0.30	0.40	0.50
e1	1.90 BSC		
e	0.95 BSC		
α	0°	4°	8°
aaa	0.20		
Pkg. codes: Z6-1; Z6-2			

DALLAS SEMICONDUCTOR MAXIM

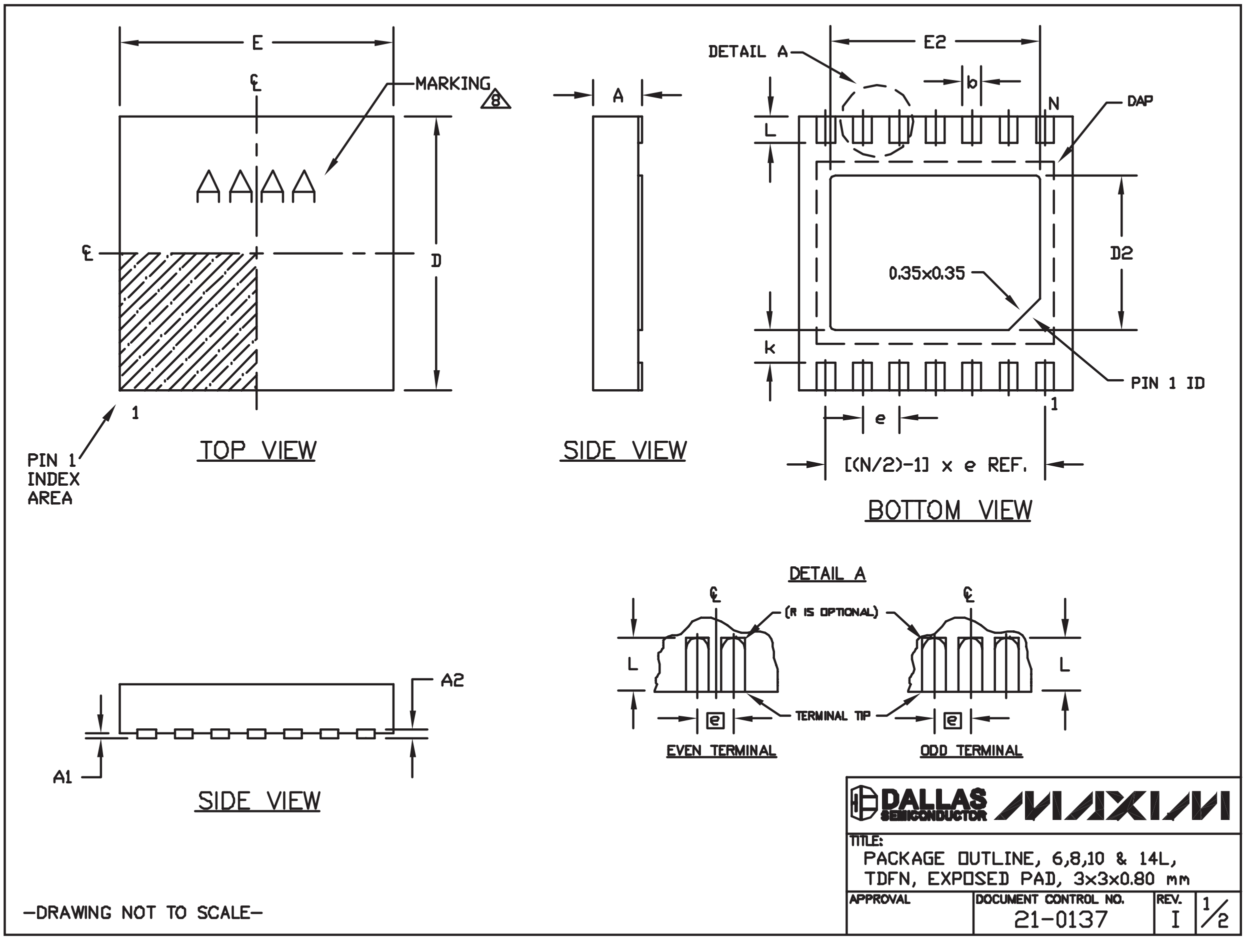
TITLE: PACKAGE OUTLINE, 6L THIN SOT23, (LOW PROFILE)

APPROVAL | DOCUMENT CONTROL NO. 21-0114 | REV. C | 2/2

-DRAWING NOT TO SCALE-

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



6, 8, &10L, DFN THIN.EPS

Low-Input-Voltage, 500mA LDO Regulator with RESET in SOT and TDFN

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-2	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-2	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T833-3	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1033-2	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF
T1433-1	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF
T1433-2	14	1.70±0.10	2.30±0.10	0.40 BSC	- - - -	0.20±0.05	2.40 REF

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2", AND T1433-1 & T1433-2.
6. "N" IS THE TOTAL NUMBER OF LEADS.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 6,8,10 & 14L, TDFN, EXPOSED PAD, 3x3x0.80 mm

APPROVAL | DOCUMENT CONTROL NO. 21-0137 | REV. I | 2/2

Revision History

Pages changed at Rev 2: 1, 8–12