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19-5250; Rev 1; 9/10

EVALUATION KIT AVAILABLE

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

General Description

The MAX16047A/MAX16049A EEPROM-configurable system managers monitor, sequence, and track multiple system voltages. The MAX16047A manages up to twelve system voltages simultaneously, and the MAX16049A manages up to eight supply voltages. These devices integrate an analog-to-digital converter (ADC) for monitoring supply voltages, and configurable outputs for sequencing and tracking supplies (during power-up and power-down). Nonvolatile EEPROM registers are configurable for storing upper and lower voltage limits, setting timing and sequencing requirements, and for storing critical fault data for read back following failures.

An internal 1% accurate 10-bit ADC measures each input and compares the result to one upper, one lower, and one selectable upper or lower limit. A fault signal asserts when a monitored voltage falls outside the set limits. Up to three independent fault output signals are configurable to assert under various fault conditions.

The integrated sequencer/tracker allows precise control over the power-up and power-down order of up to twelve (MAX16047A) or up to eight (MAX16049A) power supplies. Four channels (EN_OUT1–EN_OUT4) support closed-loop tracking using external series MOSFETs. Six outputs (EN_OUT1–EN_OUT6) are configurable with charge-pump outputs to directly drive MOSFETs without closed-loop tracking.

The MAX16047A/MAX16049A include six programmable general-purpose inputs/outputs (GPIOs). In addition to serving as EEPROM-configurable I/O pins, the GPIOs are also configurable as dedicated fault outputs, as a watchdog input or output (WDI/WDO), or as a manual reset ($\overline{MR}$).

The MAX16047A/MAX16049A feature two methods of fault management for recording information during critical fault events. The fault logger records a failure in the internal EEPROM and sets a lock bit protecting the stored fault data from accidental erasure.

An I²C/SMBus™-compatible or a JTAG serial interface configures the MAX16047A/MAX16049A. These devices are offered in a 56-pin, 8mm x 8mm TQFN package and are fully specified from -40°C to +125°C.

SMBus is a trademark of Intel Corp.

Features

- **Operate from 3V to 14V**
- **1% Accurate 10-Bit ADC Monitors 12/8 Inputs**
- **12/8 Monitored Inputs with One Overvoltage/One Undervoltage/One Selectable Limit**
- **Nonvolatile Fault Event Logger**
- **Power-Up and Power-Down Sequencing Capability**
- **12/8 Outputs for Sequencing/Power-Good Indicators**
- **Closed-Loop Tracking for Up to Four Channels**
- **Two Programmable Fault Outputs and One Reset Output**
- **Six General-Purpose Input/Outputs Configurable as:**
  - **Dedicated Fault Output**
  - **Watchdog Timer Function**
  - **Manual Reset**
- **I²C/SMBus-Compatible and JTAG Interface**
- **EEPROM-Configurable Time Delays and Thresholds**
- **100 Bytes of Internal User EEPROM**
- **56-Pin (8mm x 8mm) TQFN Package**
- **-40°C to +125°C Operating Temperature Range**

Applications

Servers

Workstations

Storage Systems

Networking/Telecom

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16047ATN+	-40°C to +125°C	56 TQFN-EP*
MAX16049ATN+	-40°C to +125°C	56 TQFN-EP*

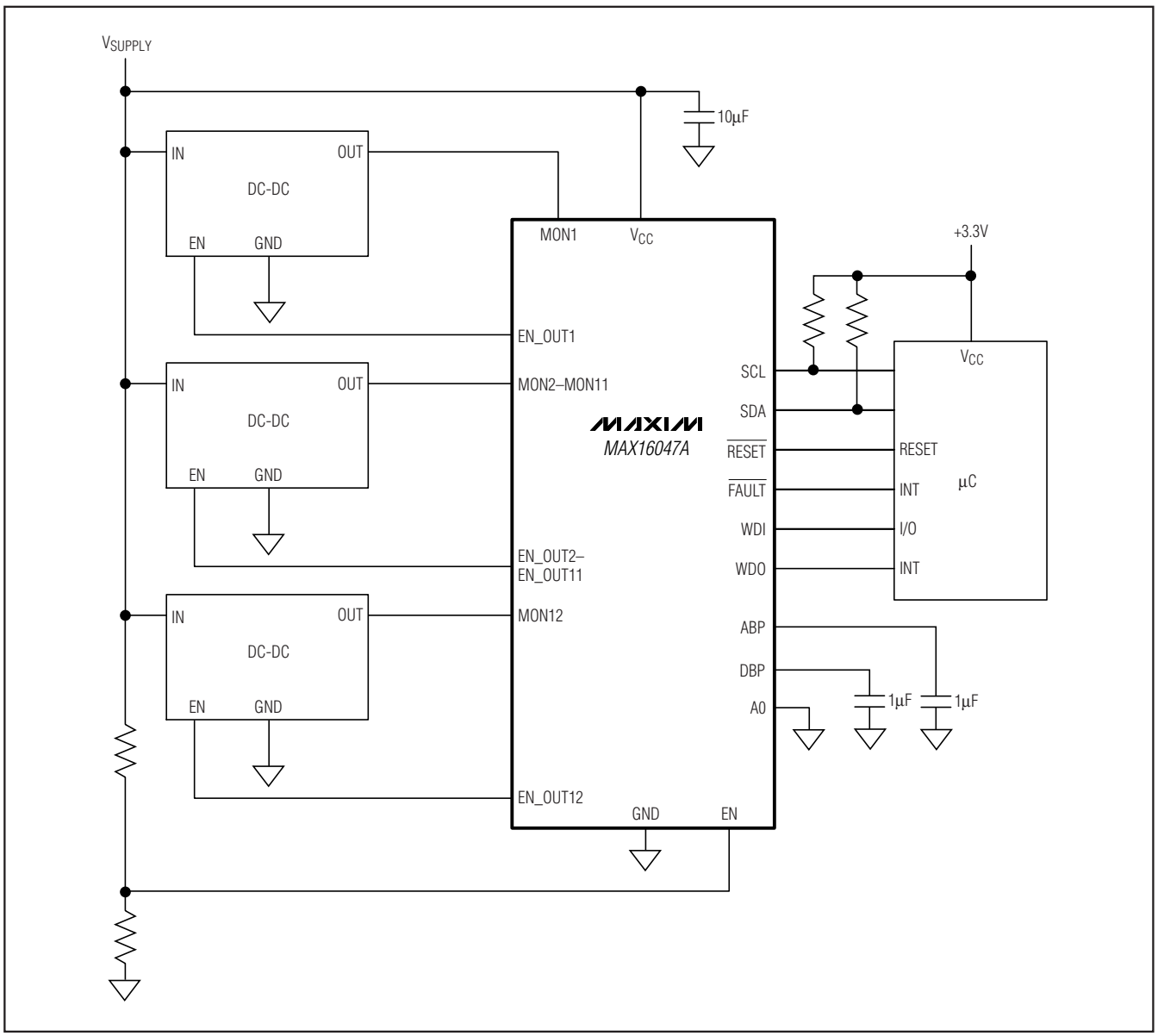
+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed Pad.*

Selector Guide appears at end of data sheet.

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +15V
EN, MON_, SCL, SDA, A0 .....-0.3V to +6V
GPIO_, EN_OUT7–EN_OUT12, $\overline{RESET}$
(configured as open drain) to GND.....-0.3V to +6V
EN_OUT1–EN_OUT6
(configured as open-drain) to GND .....-0.3V to +12V
GPIO_, EN_OUT, $\overline{RESET}$
(configured as push-pull) to GND .....-0.3V to (V_{DBP} + 0.3V)
DBP, ABP to GND .....-0.3V to the lower of 3V and (V_{CC} + 0.3V)
TCK, TMS, TDI.....-0.3V to +3.6V
TDO .....-0.3V to (V_{DBP} + 0.3V)
EN_OUT1–EN_OUT6
(configured as charge pump) .....-0.3V to (V_{MON1-6} + 6V)
Continuous Current (all pins).....±20mA
Continuous Power Dissipation (T_A = +70°C)
56-Pin TQFN (derate 47.6mW/°C above +70°C).....3810mW*
Thermal Resistance
θ_{JA} .....21°C/W
θ_{JC} .....0.6°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

**As per JEDEC 51 Standard, Multilayer Board (PCB).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 3V to 14V, T_A = -40°C to +125°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	$\overline{RESET}$ output asserted low		1.4			V
				3		14	
Undervoltage Lockout	V_{UVLO}	(Note 2)				2.85	V
Undervoltage-Lockout Hysteresis	$UVLO_{HYS}$				50		mV
Supply Current	I_{CC}	V_{CC} = 14V, V_{EN} = 3.3V, no load on any output			3.8	5	mA
DBP Regulator Voltage	V_{DBP}	C_{DBP} = 1µF, no load on any output		2.6	2.7	2.8	V
ABP Regulator Voltage	V_{ABP}	C_{ABP} = 1µF, no load		2.78	2.88	2.96	V
Boot Time	t_{BOOT}	V_{CC} > V_{UVLO}			0.8	1.5	ms
Internal Timing Accuracy		(Note 3)		-10		+10	%
ADC							
ADC Resolution					10		Bits
ADC Total Unadjusted Error (Note 4)	ADC_{ERR}	T_A = -40°C to +85°C	MON_ range set to '00'			0.65	%FSR
			MON_ range set to '01'			0.75	
			MON_ range set to '10'			0.95	
		T_A = -40°C to +125°C	MON_ range set to '00'			0.85	
			MON_ range set to '01'			0.95	
			MON_ range set to '10'			1.15	
ADC Integral Nonlinearity	ADC_{INL}					0.8	LSB
ADC Differential Nonlinearity	ADC_{DNL}					0.8	LSB
ADC Total Monitoring Cycle Time	t_{CYCLE}	All channels monitored, no MON_ fault detected (Note 5)			120	150	µs
MON_ Input Impedance	R_{IN}	MON1–MON4		46.5		100	kΩ
		MON5–MON12		65		140	

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC MON_ Ranges	ADC_{RNG}	MON_ range set to '00' in r0Fh–r11h		5.6		V
		MON_ range set to '01' in r0Fh–r11h		2.8		
		MON_ range set to '10' in r0Fh–r11h		1.4		
ADC LSB Step Size	ADC_{LSB}	MON_ range set to '00' in r0Fh–r11h		5.46		mV
		MON_ range set to '01' in r0Fh–r11h		2.73		
		MON_ range set to '10' in r0Fh–r11h		1.36		
EN Input-Voltage Threshold	$V_{TH\_EN\_R}$	EN voltage rising		0.525		V
	$V_{TH\_EN\_F}$	EN voltage falling	0.486	0.500	0.517	
EN Input Current	I_{EN}		-0.5		+0.5	µA
EN Input Voltage Range			0		5.5	V
CLOSED-LOOP TRACKING						
Tracking Differential Voltage Stop Ramp	V_{TRK}	$V_{INS\_} > V_{TH\_PL}$, $V_{INS\_} < V_{TH\_PG}$		150		mV
Tracking Differential Voltage Hysteresis				20		$\%V_{TRK}$
Tracking Differential Fault Voltage	V_{TRK_F}	$V_{INS\_} > V_{TH\_PL}$, $V_{INS\_} < V_{TH\_PG}$	280	325	370	mV
Track/Sequence Slew-Rate Rising or Falling	TRK_{SLEW}	Slew-rate register set to '00'	640	800	960	V/s
		Slew-rate register set to '01'	320	400	480	
		Slew-rate register set to '10'	150	200	230	
		Slew-rate register set to '11'	70	100	115	
INS_ Power-Good Threshold	V_{TH_PG}	Power-good register set to '00,' $V_{MON\_}$ = 3.5V	94	95	96	$\%V_{MON\_}$
		Power-good register set to '01,' $V_{MON\_}$ = 3.5V	91.5	92.5	93.5	
		Power-good register set to '10,' $V_{MON\_}$ = 3.5V	89	90	91	
		Power-good register set to '11,' $V_{MON\_}$ = 3.5V	86.5	87.5	88.5	
Power-Good Threshold Hysteresis	V_{PG_HYS}			0.5		$\%V_{TH\_PG}$
Power-Low Threshold	V_{TH_PL}	INS_ falling	125	142	160	mV
Power-Low Hysteresis	$V_{TH\_PL\_HYS}$			10		mV
GPIO_ Input Impedance	$GPIO_{INR}$	GPIO_ configured as INS_	75	100	145	kΩ
INS_ to GND Pulldown Impedance when Enabled	INS_{RPD}	$V_{INS\_}$ = 2V		100		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS (EN_OUT_, $\overline{\text{RESET}}$, GPIO_)						
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
Output-Voltage High (Push-Pull)		I_{SOURCE} = 100µA	2.4			V
Output Leakage (Open Drain)	I_{OUT_LKG}				1	µA
		GPIO1–GPIO4, $V_{GPIO\_}$ = 3.3V		1		
		GPIO1–GPIO4, $V_{GPIO\_}$ = 5V			23	
EN_OUT_ Overdrive (Charge Pump) (EN_OUT1 to EN_OUT6 Only) Volts above $V_{MON\_}$	V_{OV}	$I_{GATE\_}$ = 0.5µA	4.6	5.1	5.6	V
EN_OUT_ Pullup Current (Charge Pump)	I_{CHG_UP}	During power-up/power-down, $V_{GATE\_}$ = 1V	4.5	6		µA
EN_OUT_ Pulldown Current (Charge Pump)	I_{CHG_DOWN}	During power-up/power-down, $V_{GATE\_}$ = 5V		10		µA
INPUTS (A0, GPIO_)						
Logic-Input Low Voltage	V_{IL}				0.8	V
Logic-Input High Voltage	V_{IH}		2.0			V
SMBus INTERFACE						
Logic-Input Low Voltage	V_{IL}	Input voltage falling			0.8	V
Logic-Input High Voltage	V_{IH}	Input voltage rising	2.0			V
Input Leakage Current		V_{CC} shorted to GND, SCL/SDA at 0V or 3.3V	-1		+1	µA
			-1		+1	
Output-Voltage Low	V_{OL}	I_{SINK} = 3mA			0.4	V
Input Capacitance	C_{IN}			5		pF
SMBus TIMING						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		200			ns
Output Fall Time	t_{OF}	10pF ≤ C_{BUS} ≤ 400pF, T_A = -40°C to +85°C			250	ns
		10pF ≤ C_{BUS} ≤ 400pF, T_A = -40°C to +125°C			500	
Data Hold Time	$t_{HD:DAT}$	Receive	0			µs
		Transmit	0.3		0.9	
Pulse Width of Spike Suppressed	t_{SP}			30		ns

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 3V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
JTAG INTERFACE						
TDI, TMS, TCK Logic-Low Input Voltage	V_{IL}	Input voltage falling			0.55	V
TDI, TMS, TCK Logic-High Input Voltage	V_{IH}	Input voltage rising	2			V
TDO Logic-Output Low Voltage	V_{OL_TDO}	$V_{DBP} \geq 2.5V$, I_{SINK} = 2mA			0.4	V
TDO Logic-Output High Voltage	V_{OH_TDO}	$V_{DBP} \geq 2.5V$, I_{SOURCE} = 200µA	2.4			V
TDO Leakage Current		TDO high impedance	-1		+1	µA
TDI, TMS Pullup Resistors	R_{JPU}	Pullup to V_{DBP}	7	10	13	kΩ
Input/Output Capacitance	$C_{I/O}$			5		pF
JTAG TIMING						
TCK Clock Period	t_1				1000	ns
TCK High/Low Time	t_2, t_3		50	500		ns
TCK to TMS, TDI Setup Time	t_4		15			ns
TCK to TMS, TDI Hold Time	t_5		15			ns
TCK to TDO Delay	t_6				500	ns
TCK to TDO High-Z Delay	t_7				500	ns
EEPROM TIMING						
EEPROM Byte Write Cycle Time	t_{WR}	(Note 6)		16	20	ms

Note 1: Specifications are guaranteed for the stated global conditions, unless otherwise noted. 100% production tested at T_A = +25°C and T_A = +125°C. Specifications at T_A = -40°C are guaranteed by design.

Note 2: V_{UVLO} is the minimum voltage on V_{CC} to ensure the device is EEPROM configured.

Note 3: Applies to $\overline{RESET}$, fault, delay, and watchdog timeouts.

Note 4: Total unadjusted error is a combination of gain, offset, and quantization error.

Note 5: Guaranteed by design.

Note 6: An additional cycle is required when writing to configuration memory for the first time.

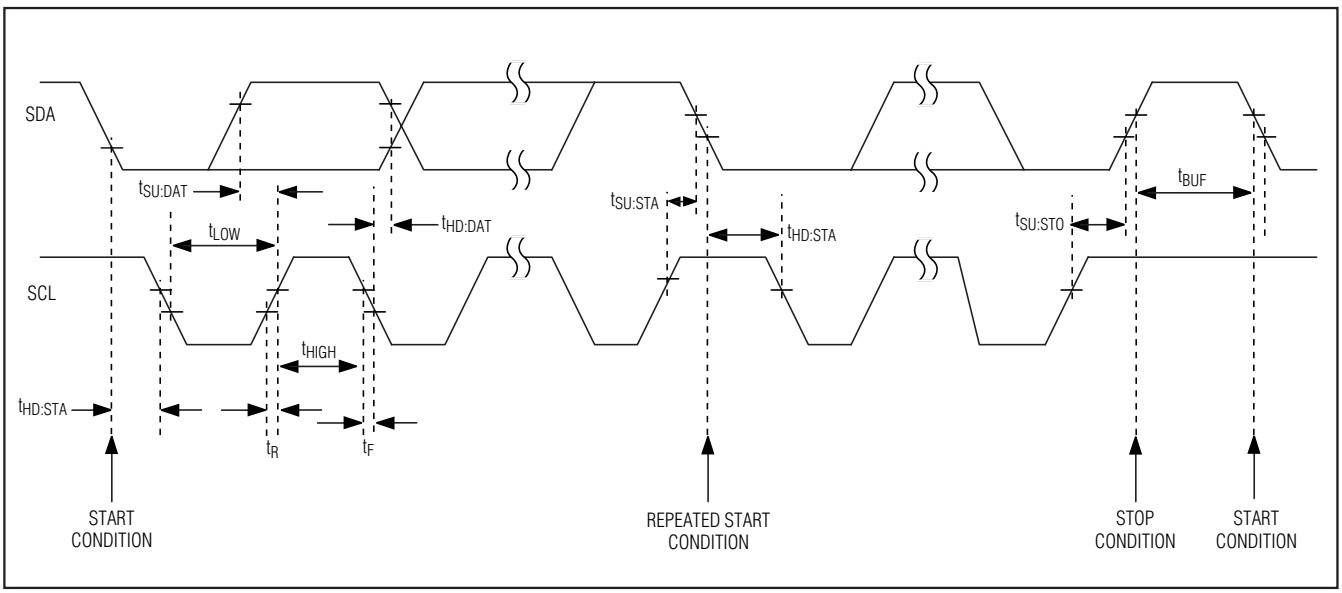


Figure 1. I²C/SMBus Timing Diagram

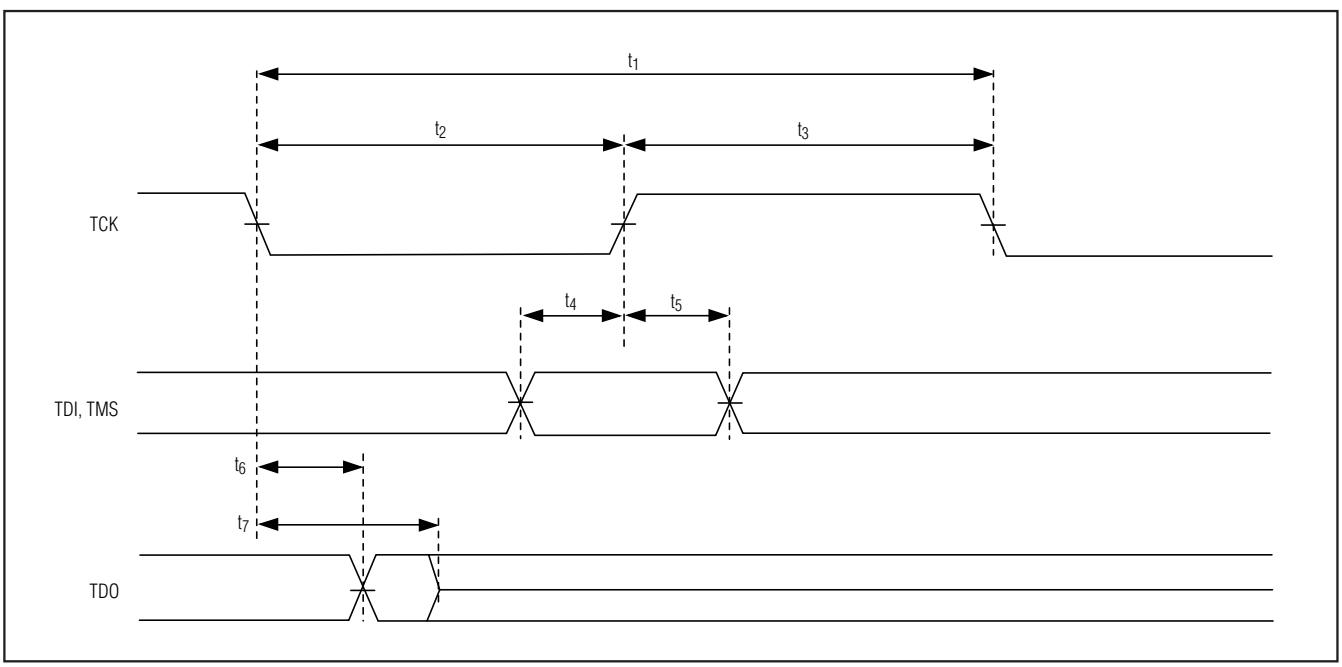


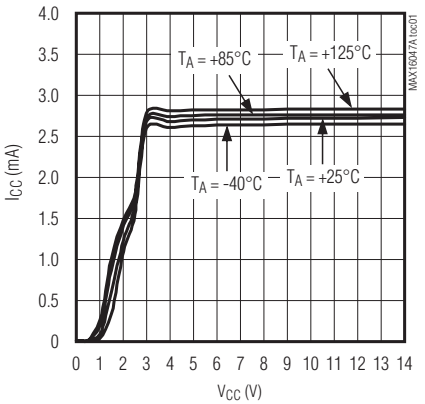
Figure 2. JTAG Timing Diagram

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

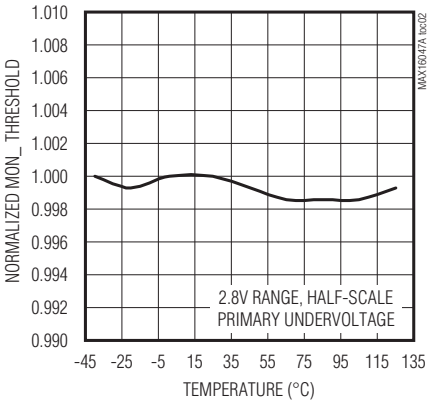
Typical Operating Characteristics

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

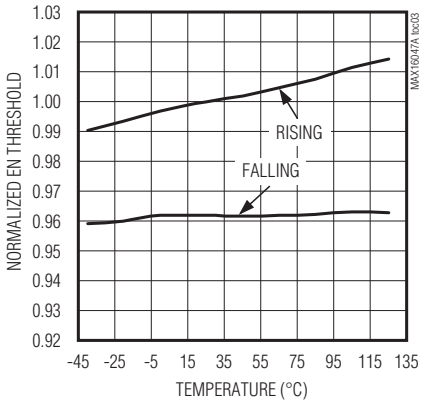
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE



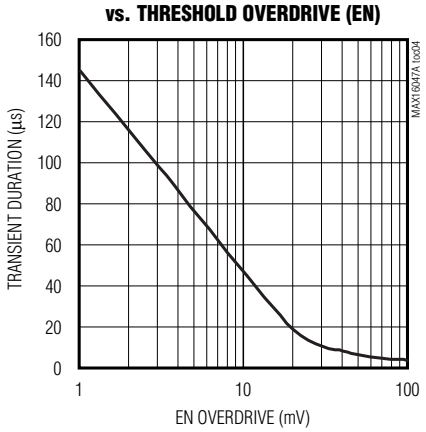
NORMALIZED MON_ THRESHOLD vs. TEMPERATURE



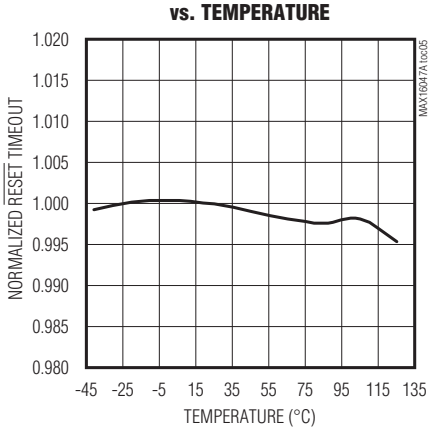
NORMALIZED EN THRESHOLD vs. TEMPERATURE



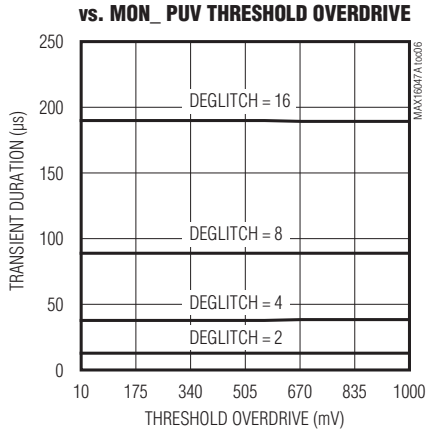
TRANSIENT DURATION vs. THRESHOLD OVERDRIVE (EN)



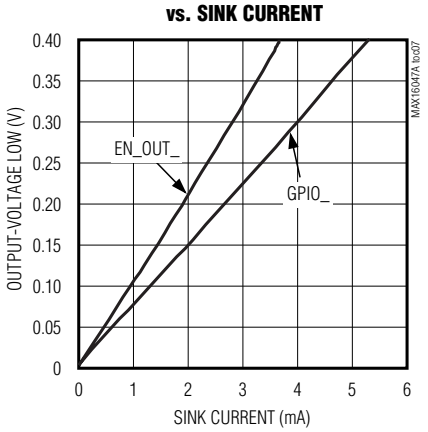
NORMALIZED $\overline{RESET}$ TIMEOUT PERIOD vs. TEMPERATURE



MINIMUM TRANSIENT DURATION vs. MON_ PUV THRESHOLD OVERDRIVE



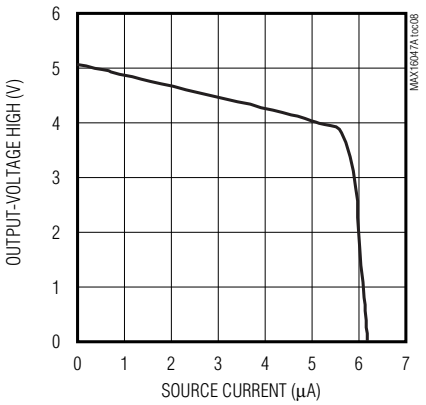
OUTPUT-VOLTAGE LOW vs. SINK CURRENT



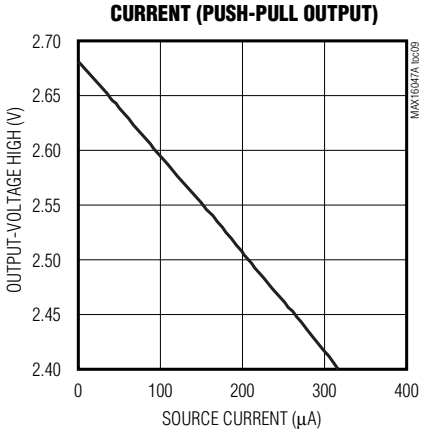
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

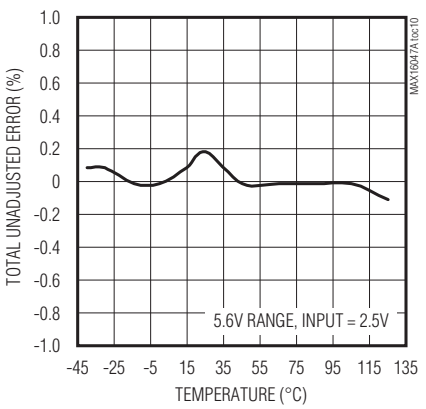
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (CHARGE-PUMP OUTPUT)



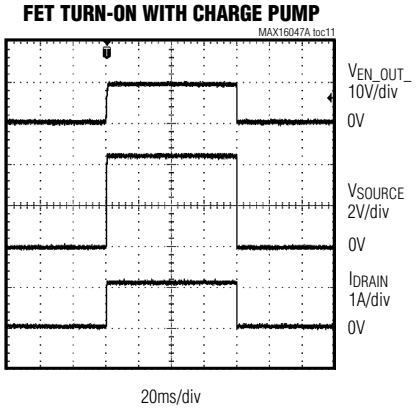
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (PUSH-PULL OUTPUT)



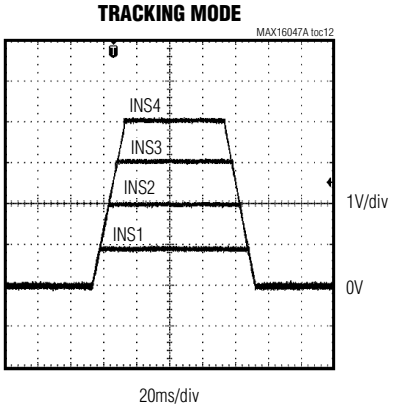
ADC ACCURACY vs. TEMPERATURE



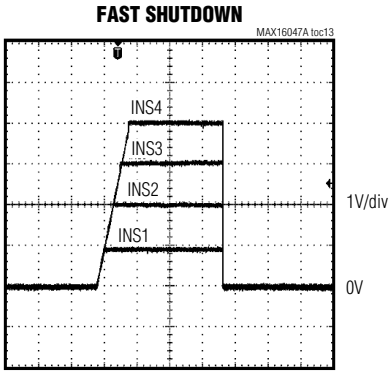
FET TURN-ON WITH CHARGE PUMP



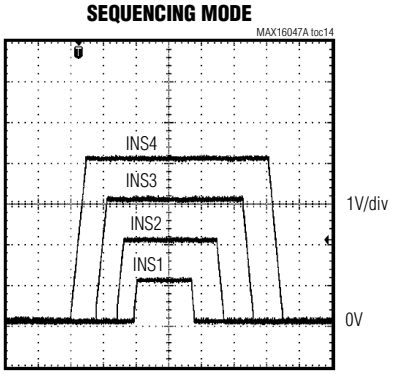
TRACKING MODE



TRACKING MODE WITH FAST SHUTDOWN



SEQUENCING MODE

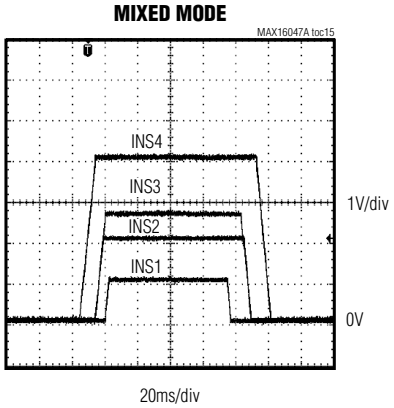


12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

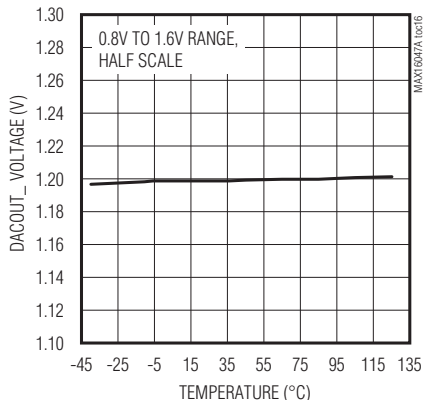
Typical Operating Characteristics (continued)

(V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

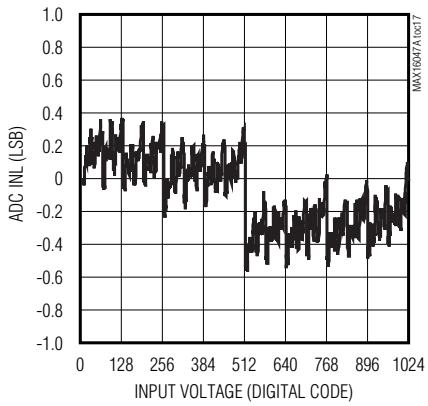
MIXED MODE



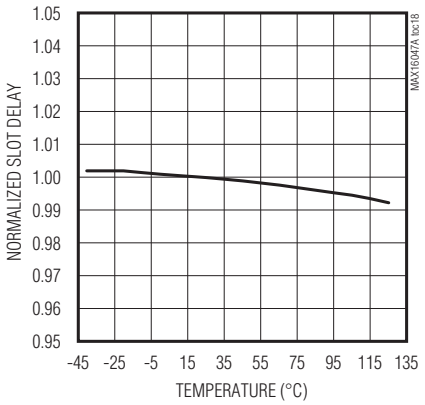
DACOUT_ VOLTAGE vs. TEMPERATURE



ADC INL



INTERNAL TIMING ACCURACY vs. TEMPERATURE



Pin Description

PIN		NAME	FUNCTION
MAX16047A	MAX16049A		
1–8	1–8	MON1–MON8	ADC Monitored Voltage Inputs. Set ADC input range for each MON_ through configuration registers. Measured values are written to ADC registers and can be read back through the I^2C or JTAG interface.
9–12	—	MON9–MON12	ADC Monitored Voltage Inputs. Set ADC input range through configuration registers. Measured values are written to ADC registers and can be read back through the I^2C or JTAG interface.
13	13	$\overline{\text{RESET}}$	Configurable Reset Output
14	14	A0	Four-State SMBus Address. Address sampled upon POR. Connect A0 to ground, DBP, SCL, or SDA to program an individual address when connecting multiple devices. See the *I^2C/SMBus-Compatible Serial Interface* section.
15	15	SCL	SMBus Serial Clock Input
16	16	SDA	SMBus Serial Data Open-Drain Input/Output
17	17	TMS	JTAG Test Mode Select
18	18	TDI	JTAG Test Data In
19	19	TCK	JTAG Test Clock
20	20	TDO	JTAG Test Data Out
21, 40	21, 40	GND	Ground. Connect all GND connections together.
22	22	GPIO6	General-Purpose Input/Output. GPIO6 and GPIO5 are configurable as open-drain or push-pull outputs, dedicated fault outputs, or for watchdog functionality. GPIO5 is configurable as a watchdog input (WDI). GPIO6 is configurable as a watchdog output (WDO). GPIO6 is also configurable for margining. Use the EEPROM to configure GPIO5 and GPIO6. See the *General-Purpose Inputs/Outputs* section.
23	23	GPIO5	
24	24	EN	Analog Enable Input. Apply a voltage greater than the 0.525V (typ) threshold to enable all outputs. The power-down sequence is triggered when EN falls below 0.5V (typ) and all outputs are deasserted.
25–36	9–12, 25–36, 53–56	N.C.	No Connection. Must be left unconnected.

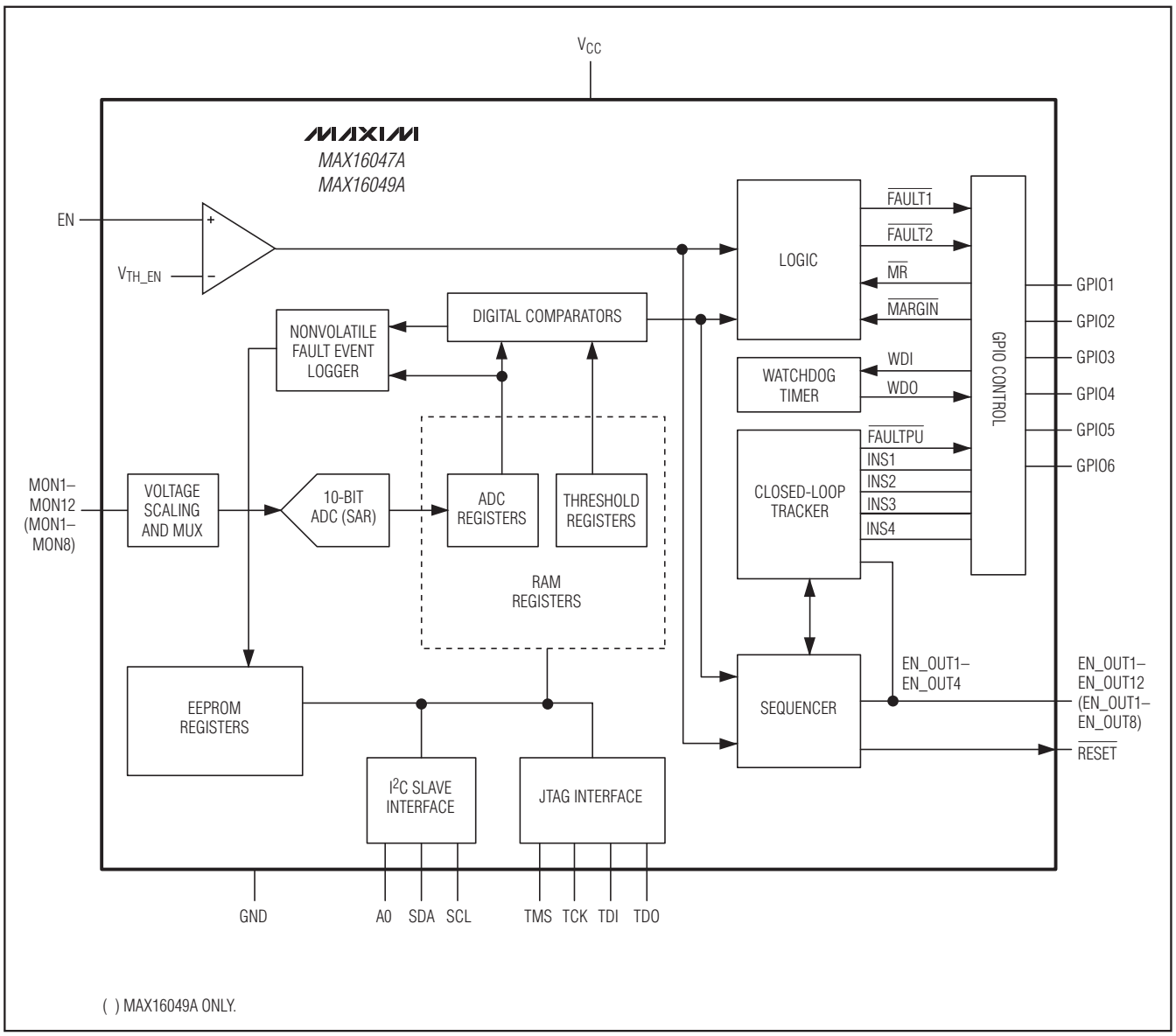
12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Pin Description (continued)

PIN		NAME	FUNCTION
MAX16047A	MAX16049A		
37	37	ABP	Internal Analog Voltage Bypass. Bypass ABP to GND with a 1µF ceramic capacitor. ABP powers the internal circuitry of the MAX16047A/MAX16049A. Do not use ABP to power any external circuitry.
38	38	V_{CC}	Power-Supply Input. Bypass V_{CC} to GND with a 10µF ceramic capacitor.
39	39	DBP	Internal Digital Voltage Bypass. Bypass DBP to GND with a 1µF ceramic capacitor. DBP supplies power to the EEPROM memory, to the internal logic circuitry, and to the internal charge pumps when the programmable outputs are configured as charge pumps. All push-pull outputs are referenced to DBP. Do not use DBP to power any external circuitry.
41	41	GPIO1	General-Purpose Input/Output 1. Configure GPIO1 as a logic input, a return sense line for closed-loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. Use the EEPROM to configure GPIO1. See the *General-Purpose Inputs/Outputs* section.
42	42	GPIO2	General-Purpose Input/Output 2. GPIO2 is configurable as a logic input, a return sense line for closed-loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. Use the EEPROM to configure GPIO2. See the *General-Purpose Inputs/Outputs* section.
43	43	GPIO3	General-Purpose Input/Output 3. GPIO3 is configurable as a logic input, a return sense line for closed-loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. Use the EEPROM to configure GPIO3. See the *General-Purpose Inputs/Outputs* section.
44	44	GPIO4	General-Purpose Input/Output 4. GPIO4 is configurable as a logic input, a return sense line for closed-loop tracking, an open-drain/push-pull fault output, or an open-drain/push-pull output port. GPIO4 is also configurable as an active-low manual reset, $\overline{MR}$. Use the EEPROM to configure GPIO4. See the *General-Purpose Inputs/Outputs* section.
45–50	45–50	EN_OUT1–EN_OUT6	Output. EN_OUT1–EN_OUT6 are configurable with active-high/active-low logic and with an open-drain or push-pull configuration. Program the EEPROM to configure EN_OUT1–EN_OUT6 as a charge-pump output 5V greater than the monitored input voltage ($V_{MON\_}$ + 5V). EN_OUT1–EN_OUT4 can also be used for closed-loop tracking.
51, 52	51, 52	EN_OUT7–EN_OUT8	Output. Configure EN_OUT_ with active-low/active-high logic and with an open-drain or push-pull configuration.
53–56	—	EN_OUT9–EN_OUT12	Output. Configure EN_OUT_ with active-low/active-high logic and with an open-drain or push-pull configuration.
—	—	EP	Exposed Pad. Internally connected to GND. Connect to GND. EP also functions as a heatsink to maximize thermal dissipation. Do not use as the main ground connection.

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Functional Diagram



( ) MAX16049A ONLY.

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Register Summary (All Registers 8-Bits Wide)

Note: This data sheet uses a specific convention for referring to bits within a particular address location. As an example, r0Fh[3:0] refers to bit 3 through 0 in register with address 15 decimal.

PAGE	REGISTER	DESCRIPTION
Extended	ADC Conversion Results (Registers r00h to r17h)	Input ADC conversion results. ADC writes directly to these registers during normal operation. ADC input ranges (MON1–MON12) are selected with registers r0Fh to r11h.
	Failed Line Flags (Registers r18h to r19h)	Voltage fault flag bits. Flags for each input signal when undervoltage or overvoltage threshold is exceeded.
	GPIO Data (Registers r1Ah to r1Bh)	GPIO state data. Used to read back and control the state of each GPIO.
Default and EEPROM	ADC Range Selections (Registers r0Fh to r11h)	ADC input voltage range. Selects the voltage range of the monitored inputs.
	Fault Behavior (Registers r47h to r4Ch)	Selects how the device should operate during faults. Options include latch-off or autoretry after fault. The autoretry delay is selectable (r4Fh). Use registers r48h through r4Ch to select fault conditions that trigger a critical fault event.
	GPIO Configuration (Registers r1Ch to r1Eh)	General-purpose input/output configuration registers. GPIOs are configurable as a manual-reset input, a margin disable input, a watchdog timer input and output, logic inputs/outputs, fault-dependent outputs, or as the feedback/pulldown inputs (INS_) for closed-loop tracking.
	Overvoltage and Undervoltage Thresholds (Registers r23h to r46h)	Input overvoltage and undervoltage thresholds. ADC conversion results are compared to overvoltage and undervoltage threshold values stored here. MON_ voltages exceeding threshold values trigger a fault event.
	Programmable Output Configuration (Registers r1Fh to r22h)	Programmable output configurations. Selectable output configurations include: active-low or active-high, open-drain or push-pull outputs. EN_OUT1–EN_OUT6 are configurable as charge-pump outputs, and EN_OUT1–EN_OUT4 can be configured for closed-loop tracking.
	$\overline{\text{RESET}}$ and Fault Outputs (Registers r15h to r1Bh)	$\overline{\text{RESET}}$, $\overline{\text{FAULT1}}$, and $\overline{\text{FAULT2}}$ output configuration. Programs the functionality of the $\overline{\text{RESET}}$, $\overline{\text{FAULT1}}$, and $\overline{\text{FAULT2}}$ outputs, as well as which inputs they depend on.
	Sequencing-Mode Configuration (Registers r50h to r5Bh and r5Eh to r63h)	Assign inputs and outputs for sequencing. Select sequence delays (20µs to 1.6s) with registers r50h through r54h. Use register r54h to enable/disable the reverse sequence bit for power-down operation.
	$\overline{\text{Software Enable}}$ and Margin (Register r4Dh)	Use register r4Dh to set the $\overline{\text{Software Enable}}$ bit, to select early warning thresholds and undervoltage/overvoltage, to enable/disable margining, and to enable/disable the watchdog for independent/dependent mode.
	Watchdog Functionality (Register r55h)	Configure watchdog functionality for GPIO5 and GPIO6.
EEPROM	Fault Log Results (Registers r00h to r0Eh)	ADC conversion results and failed-line flags at the time of a fault. These values are recorded by the fault event logger at the time of a critical fault.
	User EEPROM (Registers r9Ch to rFFh)	User-available EEPROM

Detailed Description

Getting Started

The MAX16047A is capable of managing up to twelve system voltages simultaneously, and the MAX16049A can manage up to eight system voltages. After boot-up, if EN is high and the Software Enable bit is set to '0,' an internal multiplexer cycles through each input. At each multiplexer stop, the 10-bit ADC converts the monitored analog voltage to a digital result and stores the result in a register. Each time the multiplexer finishes a conversion (12.45µs max), internal logic circuitry compares the conversion results to the overvoltage and undervoltage thresholds stored in memory. If a conversion violates a programmed threshold, the conversion can be configured to generate a fault. Logic outputs can be programmed to depend on many combinations of faults. Additionally, faults are programmable to trigger the nonvolatile fault logger, which writes all fault information automatically to the EEPROM and write-protects the data to prevent accidental erasure.

The MAX16047A/MAX16049A contain both I²C/SMBus-compatible and JTAG serial interfaces for accessing registers and EEPROM. Use only one interface at any given time. For more information on how to access the internal memory through these interfaces, see the *I²C/SMBus-Compatible Serial Interface* and *JTAG Serial Interface* sections. Registers are divided into three pages with access controlled by special I²C and JTAG commands.

The factory-default values at POR (power-on reset) for all RAM registers are '0's. POR occurs when V_{CC} reaches the undervoltage-lockout threshold (UVLO) of 2.85V (max). At POR, the device begins a boot-up sequence. During the boot-up sequence, all monitored inputs are masked from initiating faults and EEPROM contents are copied to the respective register locations. During boot-up, the MAX16047A/MAX16049A are not accessible through the serial interface. The boot-up sequence can take up to 1.5ms, after which the device is ready for normal operation. $\overline{RESET}$ is low during boot-up and asserts after boot-up for its programmed timeout period once all monitored channels are within their respective thresholds. During boot-up, the GPIOs and EN_OUTs are high impedance.

Accessing the EEPROM

The MAX16047A/MAX16049A memory is divided into three separate pages. The default page, selected by default at POR, contains configuration bits for all functions of the part. The extended page contains the ADC conversion results and GPIO input and output registers. Finally, the EEPROM page contains all stored configuration information as well as saved fault data and user-defined data. See the *Register Map* table for more information on the function of each register.

During the boot-up sequence, the contents of the EEPROM (r0Fh to r7Dh) are copied into the default page (r0Fh to r7Dh). Registers r00h to r0Eh of the EEPROM page contain saved fault data.

The JTAG and I²C interfaces provide access to all three pages. Each interface provides commands to select and deselect a particular page:

- 98h(I²C)/09h(JTAG)—Switches to the extended page. Switch back to the default page with 99h(I²C)/0Ah(JTAG).
- 9Ah(I²C)/0Bh(JTAG)—Switches to the EEPROM page. Switch back to the default page with 9Bh(I²C)/0Ch(JTAG).

See the *I²C/SMBus-Compatible Serial Interface* or the *JTAG Serial Interface* section.

Power

Apply 3V to 14V to V_{CC} to power the MAX16047A/MAX16049A. Bypass V_{CC} to ground with a 10µF capacitor. Two internal voltage regulators, ABP and DBP, supply power to the analog and digital circuitry within the device. Do not use ABP or DBP to power external circuitry.

ABP is a 2.85V (typ) voltage regulator that powers the internal analog circuitry. Bypass the ABP output to GND with a 1µF ceramic capacitor installed as close to the device as possible.

DBP is an internal 2.7V (typ) voltage regulator. EEPROM and digital circuitry are powered by DBP. All push-pull outputs are referenced to DBP. DBP supplies the input voltage to the internal charge pumps when the programmable outputs are configured as charge-pump outputs. Bypass the DBP output to GND with a 1µF ceramic capacitor installed as close as possible to the device.

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Table 1. EEPROM Software Enable Configurations

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
4Dh	0	**$\overline{\text{Software Enable}}$ bit** 0 = Enabled. EN must also be high to begin sequencing 1 = Disabled (factory default)
	1	**Margin bit** 1 = Margin functionality is enabled 0 = Margin disabled
	2	**Early Warning Selection bit** 0 = Early warning thresholds are undervoltage thresholds 1 = Early warning thresholds are overvoltage thresholds
	3	**Watchdog Mode Selection bit** 0 = Watchdog timer is in dependent mode 1 = Watchdog timer is in independent mode
	[7:4]	Not used

Enable

To initiate sequencing/tracking and enable monitoring, the voltage at EN must be above 0.525V and the Software Enable bit in r4Dh[0] must be set to '0.' To power down and disable monitoring, either pull EN below 0.5V or set the Software Enable bit to '1.' See Table 1 for the software enable bit configurations. Connect EN to ABP if not used.

If a fault condition occurs during the power-up cycle, the EN_OUT_ outputs are powered down immediately, independent of the state of EN. If operating in latch-on fault mode, toggle EN or toggle the Software Enable bit to clear the latch condition and restart the device once the fault condition has been removed. If EN is driven by external logic instead of from the center tap of a V_{CC}-connected resistive divider, ensure that an active-high pulse occurs on EN within 1.5ms of V_{CC} exceeding 2.85V. If the external driving logic is in the high-impedance state during power-up, this pulse can be created by connecting an external pullup resistor to EN.

Voltage Monitoring

The MAX16047A/MAX16049A feature an internal 10-bit ADC that monitors the MON_ voltage inputs. An internal multiplexer cycles through each of the twelve inputs, taking 150µs (typ) for a complete monitoring cycle. Each acquisition takes approximately 12.45µs. At each multiplexer stop, the 10-bit ADC converts the analog input to a digital result and stores the result in a register. ADC conversion results are stored in registers r00h to r17h in the extended page. Use the I^2C or JTAG serial interface to read ADC conversion results. See the *I^2C/SMBus-Compatible Serial Interface* or the *JTAG Serial Interface* section for more information on accessing the extended page.

The MAX16047A provides twelve inputs, MON1–MON12, for voltage monitoring. The MAX16049A provides eight inputs, MON1–MON8, for voltage monitoring. Each input voltage range is programmable in registers r0Fh to r11h (see Table 2). When MON_ configuration registers are set to '11,' MON_ voltages are not monitored or converted, and the multiplexer does not stop at these inputs, decreasing the total cycle time. These inputs cannot be configured to trigger fault conditions.

The three programmable thresholds for each monitored voltage include an overvoltage, an undervoltage, and an early warning threshold that can be set in r4Dh[2] to be either an undervoltage or overvoltage threshold. See the *Faults* section for more information on setting overvoltage and undervoltage thresholds. All voltage thresholds are 8 bits wide. The 8 MSBs of the 10-bit ADC conversion result are compared to these overvoltage and undervoltage thresholds.

For any undervoltage or overvoltage condition to be monitored and any faults detected, the MON_ input must be assigned to a particular sequence order. See the *Sequencing* section for more details on assigning MON_ inputs.

Table 2. Input Monitor Ranges and Enables

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
0Fh	[1:0]	**MON1 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON1 is not converted or monitored
	[3:2]	**MON2 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON2 is not converted or monitored
	[5:4]	**MON3 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON3 is not converted or monitored
	[7:6]	**MON4 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON4 is not converted or monitored
10h	[1:0]	**MON5 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON5 is not converted or monitored
	[3:2]	**MON6 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON6 is not converted or monitored
	[5:4]	**MON7 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON7 is not converted or monitored
	[7:6]	**MON8 Voltage Range Selection:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON8 is not converted or monitored

Table 2. Input Monitor Ranges and Enables (continued)

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
11h	[1:0]	**MON9 Voltage Range Selection*:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON9 is not converted or monitored
	[3:2]	**MON10 Voltage Range Selection*:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON10 is not converted or monitored
	[5:4]	**MON11 Voltage Range Selection*:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON11 is not converted or monitored
	[7:6]	**MON12 Voltage Range Selection*:** 00 = From 0 to 5.6V in 5.46mV steps 01 = From 0 to 2.8V in 2.73mV steps 10 = From 0 to 1.4V in 1.36mV steps 11 = MON12 is not converted or monitored

**MAX16047A only*

The extended memory page contains the ADC conversion result registers (see Table 3). These registers are also used internally for fault threshold comparison. Voltage-monitoring thresholds are compared with the 8 MSBs of the conversion results. Inputs that are not enabled are not converted by the ADC; they contain the last value acquired before that channel was disabled.

The ADC conversion result registers are reset to 00h at boot-up. These registers are not reset when a reboot command is executed.

Table 3. ADC Conversion Registers

EXTENDED PAGE ADDRESS	BIT RANGE	DESCRIPTION
00h	[7:0]	MON1 ADC Conversion Result (MSB)
01h	[7:6]	MON1 ADC Conversion Result (LSB)
	[5:0]	Reserved
02h	[7:0]	MON2 ADC Conversion Result (MSB)
03h	[7:6]	MON2 ADC Conversion Result (LSB)
	[5:0]	Reserved
04h	[7:0]	MON3 ADC Conversion Result (MSB)
05h	[7:6]	MON3 ADC Conversion Result (LSB)
	[5:0]	Reserved
06h	[7:0]	MON4 ADC Conversion Result (MSB)
07h	[7:6]	MON4 ADC Conversion Result (LSB)
	[5:0]	Reserved
08h	[7:0]	MON5 ADC Conversion Result (MSB)
09h	[7:6]	MON5 ADC Conversion Result (LSB)
	[5:0]	Reserved
0Ah	[7:0]	MON6 ADC Conversion Result (MSB)
0Bh	[7:6]	MON6 ADC Conversion Result (LSB)
	[5:0]	Reserved
0Ch	[7:0]	MON7 ADC Conversion Result (MSB)
0Dh	[7:6]	MON7 ADC Conversion Result (LSB)
	[5:0]	Reserved
0Eh	[7:0]	MON8 ADC Conversion Result (MSB)
0Fh	[7:6]	MON8 ADC Conversion Result (LSB)
	[5:0]	Reserved
10h	[7:0]	MON9 ADC Conversion Result (MSB)*
11h	[7:6]	MON9 ADC Conversion Result (LSB)*
	[5:0]	Reserved
12h	[7:0]	MON10 ADC Conversion Result (MSB)*
13h	[7:6]	MON10 ADC Conversion Result (LSB)*
	[5:0]	Reserved
14h	[7:0]	MON11 ADC Conversion Result (MSB)*
15h	[7:6]	MON11 ADC Conversion Result (LSB)*
	[5:0]	Reserved
16h	[7:0]	MON12 ADC Conversion Result (MSB)*
17h	[7:6]	MON12 ADC Conversion Result (LSB)*
	[5:0]	Reserved

**MAX16047A only*

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

General-Purpose Inputs/Outputs

GPIO1–GPIO6 are programmable general-purpose inputs/outputs. GPIO1–GPIO6 are configurable as a manual reset input, a margin disable input, a watchdog timer input and output, logic inputs/outputs, fault-dependent outputs, or as the feedback inputs (INS_) for closed-loop tracking. When programmed as outputs, GPIOs are open drain or push-pull. See registers r1Ch to r1Eh in Tables 4 and 5 for more detailed information on configuring GPIO1–GPIO6.

Table 4. General-Purpose IO Configuration Registers

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
1Ch	[2:0]	GPIO1 Configuration Register
	[5:3]	GPIO2 Configuration Register
	[7:6]	GPIO3 Configuration Register (LSB)
1Dh	[0]	GPIO3 Configuration Register (MSB)
	[3:1]	GPIO4 Configuration Register
	[6:4]	GPIO5 Configuration Register
	[7]	GPIO6 Configuration Register (LSB)
1Eh	[1:0]	GPIO6 Configuration Register (MSB)
	[7:2]	Reserved

Table 5. GPIO Mode Selection

CONFIGURATION BITS	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6
000	INS1	INS2	INS3	INS4	—	$\overline{\text{MARGIN}}$ input
001	Push-pull logic input/output	Push-pull logic input/output	Push-pull logic input/output	Push-pull logic input/output	Push-pull logic input/output	Push-pull logic input/output
010	Open-drain logic input/output	Open-drain logic input/output	Open-drain logic input/output	Open-drain logic input/output	Open-drain logic input/ output	Open-drain logic input/ output
011	Push-pull Any_Fault output	Push-pull Any_Fault output	Push-pull Any_Fault output	Push-pull Any_Fault output	Push-pull $\overline{\text{FAULT1}}$ output	Push-pull $\overline{\text{FAULT2}}$ output
100	Open-drain Any_Fault output	Open-drain Any_Fault output	Open-drain Any_Fault output	Open-drain Any_Fault output	Open-drain $\overline{\text{FAULT1}}$ output	Open-drain $\overline{\text{FAULT2}}$ output
101	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input
110	—	—	—	—	—	Open-drain WDO output
111	—	—	—	$\overline{\text{MR}}$ input	WDI input	Open-drain $\overline{\text{FAULTPU}}$ output

Note: *The dash "—" represents a reserved GPIO configuration. Do not set any GPIO to these values.*

Voltage Tracking Sense (INS_) Inputs

GPIO1–GPIO4 are configurable as feedback sense return inputs (INS_) for closed-loop tracking. Connect the gate of an external n-channel MOSFET to each EN_OUT_ configured for closed-loop tracking. Connect INS_ inputs to the source of the MOSFETs for tracking feedback.

Internal comparators monitor INS_ with respect to a control tracking ramp voltage for power-up/power-down and control each EN_OUT_ voltage. Under normal conditions each INS_ voltage tracks the ramp voltage until the power-good voltage threshold has been reached. The slew rate for the ramp voltage and the INS_ to MON_ power-good threshold are programmable. See the *Closed-Loop Tracking* section.

INS_ connections also act as 100Ω pulldowns for closed-loop tracking channels or for other power supplies, if INS_ are connected to the outputs of the supplies. Set the appropriate bits in r4Eh[7:4] to enable pulldown functionality. See Table 12.

General-Purpose Logic Inputs/Outputs

Configure GPIO1–GPIO6 to be used as general-purpose inputs/outputs. Write values to GPIOs through r1Ah when operating as outputs, and read values from r1Bh when operating as inputs. Register r1Bh is read-only. See Table 6 for more information on reading and writing to the GPIOs as logic inputs/outputs. Both registers r1Ah and r1Bh are located in the extended page and are therefore not loaded from EEPROM on boot-up.

Table 6. GPIO Data-In/Data-Out Data

EXTENDED PAGE ADDRESS	BIT RANGE	DESCRIPTION
1Ah	[0]	**GPIO Logic Output Data** 0 = GPIO1 is a logic-low output 1 = GPIO1 is a logic-high output
	[1]	0 = GPIO2 is a logic-low output 1 = GPIO2 is a logic-high output
	[2]	0 = GPIO3 is a logic-low output 1 = GPIO3 is a logic-high output
	[3]	0 = GPIO4 is a logic-low output 1 = GPIO4 is a logic-high output
	[4]	0 = GPIO5 is a logic-low output 1 = GPIO5 is a logic-high output
	[5]	0 = GPIO6 is a logic-low output 1 = GPIO6 is a logic-high output
	[7:6]	Not used
1Bh	[0]	**GPIO Logic Input Data** GPIO1 logic-input state
	[1]	GPIO2 logic-input state
	[2]	GPIO3 logic-input state
	[3]	GPIO4 logic-input state
	[4]	GPIO5 logic-input state
	[5]	GPIO6 logic-input state
	[7:6]	Not used

12-Channel/8-Channel EEPROM-Programmable System Managers with Nonvolatile Fault Registers

Any_Fault Outputs

GPIO1–GPIO4 are configurable as active-low push-pull or open-drain fault-dependent outputs. These outputs assert when any monitored input exceeds an overvoltage, undervoltage, or early warning threshold.

$\overline{FAULT1}$ and $\overline{FAULT2}$

GPIO5 and GPIO6 are configurable as dedicated fault outputs, $\overline{FAULT1}$ and $\overline{FAULT2}$, respectively. Fault outputs can assert on one or more overvoltage, undervoltage, or early warning conditions for selected inputs. $\overline{FAULT1}$ and $\overline{FAULT2}$ dependencies are set using registers r15h to r18h. See Table 7.

If a fault output depends on more than one MON_, the fault output will assert if one or more MON_ exceeds a programmed threshold voltage.

Table 7. $\overline{FAULT1}$ and $\overline{FAULT2}$ Output Configuration and Dependencies

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
15h	[0]	1 = $\overline{FAULT1}$ is a digital output dependent on MON1
	[1]	1 = $\overline{FAULT1}$ is a digital output dependent on MON2
	[2]	1 = $\overline{FAULT1}$ is a digital output dependent on MON3
	[3]	1 = $\overline{FAULT1}$ is a digital output dependent on MON4
	[4]	1 = $\overline{FAULT1}$ is a digital output dependent on MON5
	[5]	1 = $\overline{FAULT1}$ is a digital output dependent on MON6
	[6]	1 = $\overline{FAULT1}$ is a digital output dependent on MON7
	[7]	1 = $\overline{FAULT1}$ is a digital output dependent on MON8
16h	[0]	1 = $\overline{FAULT1}$ is a digital output dependent on MON9*
	[1]	1 = $\overline{FAULT1}$ is a digital output dependent on MON10*
	[2]	1 = $\overline{FAULT1}$ is a digital output dependent on MON11*
	[3]	1 = $\overline{FAULT1}$ is a digital output dependent on MON12*
	[4]	1 = $\overline{FAULT1}$ is a digital output that depends on the overvoltage thresholds at the input selected by r15h and r16h[3:0]
	[5]	1 = $\overline{FAULT1}$ is a digital output that depends on the undervoltage thresholds at the input selected by r15h and r16h[3:0]
	[6]	1 = $\overline{FAULT1}$ is a digital output that depends on the early warning thresholds at the input selected by r15h and r16h[3:0]
	[7]	0 = $\overline{FAULT1}$ is an active-low digital output 1 = $\overline{FAULT1}$ is an active-high digital output
17h	[0]	1 = $\overline{FAULT2}$ is a digital output dependent on MON1
	[1]	1 = $\overline{FAULT2}$ is a digital output dependent on MON2
	[2]	1 = $\overline{FAULT2}$ is a digital output dependent on MON3
	[3]	1 = $\overline{FAULT2}$ is a digital output dependent on MON4
	[4]	1 = $\overline{FAULT2}$ is a digital output dependent on MON5
	[5]	1 = $\overline{FAULT2}$ is a digital output dependent on MON6
	[6]	1 = $\overline{FAULT2}$ is a digital output dependent on MON7
	[7]	1 = $\overline{FAULT2}$ is a digital output dependent on MON8

Table 7. $\overline{\text{FAULT1}}$ and $\overline{\text{FAULT2}}$ Output Configuration and Dependencies (continued)

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
18h	[0]	1 = $\overline{\text{FAULT2}}$ is a digital output dependent on MON9*
	[1]	1 = $\overline{\text{FAULT2}}$ is a digital output dependent on MON10*
	[2]	1 = $\overline{\text{FAULT2}}$ is a digital output dependent on MON11*
	[3]	1 = $\overline{\text{FAULT2}}$ is a digital output dependent on MON12*
	[4]	1 = $\overline{\text{FAULT2}}$ is a digital output that depends on the overvoltage thresholds at the input selected by r17h and r18h[3:0]
	[5]	1 = $\overline{\text{FAULT2}}$ is a digital output that depends on the undervoltage thresholds at the input selected by r17h and 18h[3:0]
	[6]	1 = $\overline{\text{FAULT2}}$ is a digital output that depends on the early warning thresholds at the input selected by r17h and r18h[3:0]
	[7]	0 = $\overline{\text{FAULT2}}$ is an active-low digital output 1 = $\overline{\text{FAULT2}}$ is an active-high digital output

**MAX16047A only*

Fault-On Power-Up ($\overline{\text{FAULTPU}}$)

GPIO6 indicates a fault during power-up or power-down when configured as a "fault-on power-up" output. Under these conditions, all EN_OUT_ voltages are pulled low and fault data is saved to nonvolatile EEPROM. See the *Faults* section.

$\overline{\text{MARGIN}}$

GPIO6 is configurable as an active-low $\overline{\text{MARGIN}}$ input. Drive $\overline{\text{MARGIN}}$ low before varying system voltages above or below the thresholds to avoid signaling an error. Drive $\overline{\text{MARGIN}}$ high for normal operation.

When $\overline{\text{MARGIN}}$ is pulled low or r4Dh[1] is a '1,' the margin function is enabled. $\overline{\text{FAULT1}}$, $\overline{\text{FAULT2}}$, Any_Fault, and $\overline{\text{RESET}}$ are latched in their current state. Threshold violations will be ignored, and faults will not be logged.

Manual Reset ($\overline{\text{MR}}$)

GPIO4 is configurable to act as an active-low manual reset input, $\overline{\text{MR}}$. Drive $\overline{\text{MR}}$ low to assert $\overline{\text{RESET}}$. $\overline{\text{RESET}}$ remains low for the selected reset timeout period after $\overline{\text{MR}}$ transitions from low to high. See the *RESET* section for more information on selecting a reset timeout period.

Watchdog Input (WDI) and Output (WDO)

Set r1Eh[1:0] and r1Dh[7] to '110' to configure GPIO6 as WDO. Set r1Dh[6:4] to '111' to configure GPIO5 as WDI. WDO is an open-drain active-low output. See the *Watchdog Timer* section for more information about the operation of the watchdog timer.

Programmable Outputs (EN_OUT1–EN_OUT12)

The MAX16047A includes twelve programmable outputs, and the MAX16049A includes eight programmable outputs. These outputs are capable of connecting to either the enable (EN) inputs of a DC-DC or LDO power supply or to the gates of series-pass MOSFETs for closed-loop tracking mode, or for charge-pump mode. Selectable output configurations include: active-low or active-high, open-drain or push-pull. EN_OUT1–EN_OUT4 are also configurable for closed-loop tracking, and EN_OUT1–EN_OUT6 can act as charge-pump outputs with no closed-loop tracking. Use the registers r1Fh to r22h to configure outputs. See Table 8 for detailed information on configuring EN_OUT1–EN_OUT12.

Table 8. EN_OUT1–EN_OUT12 Configuration

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
1Fh	[2:0]	**EN_OUT1 Configuration:** 000 = EN_OUT1 is an open-drain active-low output 001 = EN_OUT1 is an open-drain active-high output 010 = EN_OUT1 is a push-pull active-low output 011 = EN_OUT1 is a push-pull active-high output 100 = EN_OUT1 is used in closed-loop tracking 101 = EN_OUT1 is configured with a charge-pump output (MON1 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved
	[5:3]	**EN_OUT2 Configuration:** 000 = EN_OUT2 is an open-drain active-low output 001 = EN_OUT2 is an open-drain active-high output 010 = EN_OUT2 is a push-pull active-low output 011 = EN_OUT2 is a push-pull active-high output 100 = EN_OUT2 is used in closed-loop tracking 101 = EN_OUT2 is configured with a charge-pump output (MON2 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved
	[7:6]	**EN_OUT3 Configuration (LSBs):** 000 = EN_OUT3 is an open-drain active-low output 001 = EN_OUT3 is an open-drain active-high output 010 = EN_OUT3 is a push-pull active-low output 011 = EN_OUT3 is a push-pull active-high output 100 = EN_OUT3 is used in closed-loop tracking 101 = EN_OUT3 is configured with a charge-pump output (MON3 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved

Table 8. EN_OUT1–EN_OUT12 Configuration (continued)

REGISTER/ EEPROM ADDRESS	BIT RANGE	DESCRIPTION
20h	[0]	**EN_OUT3 Configuration (MSB)**—see r1Fh[7:6]
	[3:1]	**EN_OUT4 Configuration:** 000 = EN_OUT4 is an open-drain active-low output 001 = EN_OUT4 is an open-drain active-high output 010 = EN_OUT4 is a push-pull active-low output 011 = EN_OUT4 is a push-pull active-high output 100 = EN_OUT4 is used in closed-loop tracking 101 = EN_OUT4 is configured with a charge-pump output (MON4 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved
	[6:4]	**EN_OUT5 Configuration:** 000 = EN_OUT5 is an open-drain active-low output 001 = EN_OUT5 is an open-drain active-high output 010 = EN_OUT5 is a push-pull active low output 011 = EN_OUT5 is a push-pull active-high output 100 = Reserved. EN_OUT5 is not usable for closed-loop tracking. 101 = EN_OUT5 is configured with a charge-pump output (MON5 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved
	[7]	**EN_OUT6 Configuration (LSB)**—see r21h[1:0]
21h	[1:0]	**EN_OUT6 Configuration (MSBs):** 000 = EN_OUT6 is an open-drain active-low output 001 = EN_OUT6 is an open-drain active-high output 010 = EN_OUT6 is a push-pull active-low output 011 = EN_OUT6 is a push-pull active-high output 100 = Reserved. EN_OUT6 is not useable for closed-loop tracking. 101 = EN_OUT6 is configured with a charge-pump output (MON6 + 5V) capable of driving an external n-channel MOSFET 110 = Reserved 111 = Reserved
	[3:2]	**EN_OUT7 Configuration:** 00 = EN_OUT7 is an open-drain active-low output 01 = EN_OUT7 is an open-drain active-high output 10 = EN_OUT7 is a push-pull active-low output 11 = EN_OUT7 is a push-pull active-high output
	[5:4]	**EN_OUT8 Configuration:** 00 = EN_OUT8 is an open-drain active-low output 01 = EN_OUT8 is an open-drain active-high output 10 = EN_OUT8 is a push-pull active-low output 11 = EN_OUT8 is a push-pull active-high output
	[7:6]	**EN_OUT9 Configuration*:** 00 = EN_OUT9 is an open-drain active-low output 01 = EN_OUT9 is an open-drain active-high output 10 = EN_OUT9 is a push-pull active-low output 11 = EN_OUT9 is a push-pull active-high output