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±0.3% Accurate, Quad, Power-Supply Controller with Active-Voltage Output Control and PMBus Interface

General Description

The MAX16064 is a fully integrated 4-channel digital power-supply controller and monitor IC that can be connected up to four power supplies to provide complete digital configurability. By interfacing to the power-supply reference input or feedback node, and the output enable, the MAX16064 takes control of the power supply to provide tracking, soft-start, sequencing, margining, and dynamic adjustment of the output voltage.

Power-supply sequencing can be performed autonomously or controlled over the PMBus[™] interface. Sequencing is controlled during power-down as well as power-up. Multiple MAX16064s can be combined to autonomously sequence more supplies. The sequencing order is stored in an external configuration EEPROM so sequence order changes can be reprogrammed without changing the PCB layout.

The MAX16064 features an internal temperature sensor providing an additional level of system monitoring. Other features include a reset output and an SMBus[™] alert output.

Each channel of the MAX16064 includes an accurate 12-bit analog-to-digital converter (ADC) input and a differential amplifier for accurately monitoring and reporting the voltage at the load without being influenced by any difference in ground potentials. An integrated 12-bit digital-to-analog converter (DAC) can margin power supplies and dynamically adjust the output voltage using a closed-loop control system to provide an output-voltage accuracy of $\pm 0.3\%$.

The user-programmable registers provide flexible and accurate control of time events such as delay time and transition period, monitoring for overvoltage and undervoltage, overtemperature fault and warning handling. The closed-loop operation is also programmable to make sure the MAX16064 works with any existing power supply to provide superior regulation accuracy and accurate margining.

The MAX16064 operates using a PMBus-compliant communication protocol. The device can be programmed using this protocol or with a free graphic-user interface (GUI) available from the Maxim website that significantly reduces development time. Once the configuration is complete, the results can be saved into an EEPROM or loaded into the device through PMBus at power-up. This allows remote configuration of any power supply using the MAX16064, replacing expensive recalls or field service. The MAX16064 can be programmed with up to 114 distinct addresses to support large systems. The MAX16064 is offered in a space-saving, 36-pin, lead-free, 6mm x 6mm TQFN package and is fully specified from -40°C to +85°C.

Features

- Accurate Voltage Output Control (AVOC) Controls Output Voltage with ±0.3% Accuracy
- PMBus Interface for Programming, Monitoring, Sequencing Up and Down, and Margining
- Output Voltage and Temperature Monitoring with Adjustable Monitor Rate
- Programmable Soft-Start and Soft-Stop Ramp Rates
- Power-Supply Control using REFIN or FB Terminals
- Master-Slave Clocking Option Provides Accurate Timing Reference Across Multiple Devices
- External EEPROM Interface for Autoboot on Power-Up
- ♦ 3.0V to 3.6V Operating Voltage Range
- 6mm x 6mm, 36-Pin TQFN Package

Applications

Routers Servers Storage Systems Telecom/Networking DC-DC Modules and Power Supplies

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	
MAX16064ETX+	-40°C to +85°C	36 TQFN-EP*	

+Denotes a lead(Pb)-free/RoHS-compliant package. *EP = Exposed pad.

Pin Configuration and Typical Operating Circuit appears at end of data sheet.

PMBus is a trademark of SMIF, Inc. SMBus is a trademark of Intel Corp.

_ Maxim Integrated Products 1

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

AVDD, DVDD to AGND0.3V to +4V
AVDD to DVDD0.3V to +0.3V
AGND to DGND0.3V to +0.3V
AGND1 to DGND0.3V to +0.3V
RS_+, RS to AGND0.3V to +6V
RS_C, A1/SCLE, A2/SDAE,
A3/CONTROL to AGND0.3V to (AVDD + 0.3V)
RESET, SMBALERT, ENOUT_ to AGND0.3V to +6V
SCL, SDA to DGND0.3V to +4V
DACOUT_, EN, CLKIO, REFO to AGND0.3V to (AVDD + 0.3V)
DACOUT_ Current
SDA Current1mA to +50mA

Input/Output Current (all other pins)	20mA
Continuous Power Dissipation ($T_A = +70^{\circ}C$)	
36-Pin 6mm x 6mm TQFN	
(derate 35.7mW/°C above +70°C)	2857mW
Thermal Resistance (Note 1)	
θυΑ	28°C/W
θJC	1°C/W
Operating Temperature Range	40°C to +85°C
Junction Temperature	
Storage Temperature Range	65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a fourlayer board. For detailed information on package thermal considerations, refer to <u>www.maxim-ic.com/thermal-tutorial</u>.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

 $(V_{AVDD} = V_{DVDD} = 3.0V \text{ to } 3.6V, V_{EN} = 2V, V_{RS_+} - V_{RS_-} = 2V, V_{RS_-} = 0V, T_A = T_J = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise specified.}$ Typical values are at $V_{AVDD} = V_{DVDD} = 3.3V, T_A = +25^{\circ}C.$ (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
AVDD/DVDD Operating Voltage Range			3.0		3.6	V
AVDD Undervoltage Lockout (AVDD Rising)	VUVLO		2.75	2.8	2.95	V
AVDD Undervoltage Lockout Hysteresis	VUVLO-HYS			100		mV
AVDD and DVDD Total Supply Current		$V_{\text{RS}_+} = V_{\text{RS}\} = 0V$		12	18.5	mA
OUTPUT-VOLTAGE SENSING			•			
		$T_A = +25^{\circ}C, V_{RS_+} = 1.0V, V_{RS} = 0V$	-4		+4	mV
Voltage Regulation Accuracy (2V Range)		$T_A = -40^{\circ}C$ to $+85^{\circ}C$, $V_{RS_+} = 1.0V$, $V_{RS} = 0V$	-6		+6	mV
		$T_A = +25^{\circ}C, V_{RS_+} = 2.5V, V_{RS} = 0V$	-11		+11	mV
Voltage Regulation Accuracy (5.5V Range)		$T_A = -40^{\circ}C \text{ to } +85^{\circ}C, V_{RS_+} = 2.5V, V_{RS} = 0V$	-16.5		+16.5	mV
RS_+, RS Differential Mode Range			0		5.5	V
RS to AGND Differential Voltage			-250		+250	mV
		2V range, $V_{RS_+} = -0.25V$ to +2V	-20		+20	
RS_+ Input Bias Current		5.5V range, V _{RS_+} = -0.25V to +5.5V	-20		+100	μA
RS Input Bias Current		2V or 5.5V range, V _{RS} = -0.25V to +0.25V	-20		0	μA

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{AVDD} = V_{DVDD} = 3.0V \text{ to } 3.6V, V_{EN} = 2V, V_{RS_+} - V_{RS_-} = 2V, V_{RS_-} = 0V, T_A = T_J = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise specified.}$ Typical values are at $V_{AVDD} = V_{DVDD} = 3.3V, T_A = +25^{\circ}C.$ (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
INTERNAL TEMPERATURE SEN	SOR	•	•			
Temperature Sensing Accuracy		$T_A = 0^{\circ}C \text{ to } +85^{\circ}C$		±3		°C
INTERNAL OSCILLATOR		•	•			
Frequency			7.6	8	8.4	MHz
ADC						
Resolution				12		Bits
INTERNAL REFERENCE						
Reference Voltage	V _{REF}	$T_A = +25^{\circ}C$		2.048		V
DAC						
Resolution				12		Bits
Differential Nonlinearity	DNL		-2.5		+2.5	LSB
Maximum Output-Voltage Range		No load		V _{REF} - 1 LSB		V
Capacitive Load				200		pF
Output-Voltage Slew Rate				0.35		V/µs
DAC Output Resistance				10		Ω
DAC Driving Capability		DAC output > 100mV; output error < 25mV	-1		+1	mA
DAC Output Leakage Current		DAC output switch open, VDACOUT_ = VREF or 0V	-250		+250	nA
CLKIO		•	•			
Input Logic-Low Voltage					0.8	V
Input Logic-High Voltage			2.1			V
Input Bias Current		$V_{CLKIO} = 3.6V \text{ or } 0V$	-1		+1	μA
Input Clock Duty Cycle				50		%
Output Low Voltage		CLKIO in output mode, ISINK = 4mA			0.4	V
Output High Leakage		$V_{CLKIO} = 3.6V$	-1		+1	μA
CLKIO Pullup Voltage					3.6	V
CLKIO Input Frequency Range	fext_CLK		100		1000	kHz
CLKIO Output Frequency				1		MHz
ENABLE INPUT (EN)						
EN Falling Threshold Voltage	V _{EN_TH}		1.17	1.21	1.23	V
EN Rising Threshold Voltage			1.175	1.23	1.281	V
EN Input Leakage Current			-0.25		+0.25	μA
OUTPUTS (ENOUT_, RESET, SM	BALERT)					
Output Low Voltage	VOL	I _{SINK} = 10mA			0.4	V
Culput Low Voltage	VOL	$V_{AVDD} = V_{DVDD} = 1.1V$, $I_{SINK} = 100\mu A$			0.4	V
Output Leakage		$V_{\text{ENOUT}} = 5V, 0V$	-1		+1	μA

ELECTRICAL CHARACTERISTICS (continued)

 $(V_{AVDD} = V_{DVDD} = 3.0V \text{ to } 3.6V, V_{EN} = 2V, V_{RS_+} - V_{RS_-} = 2V, V_{RS_-} = 0V, T_A = T_J = -40^{\circ}C \text{ to } +85^{\circ}C, \text{ unless otherwise specified.}$ Typical values are at $V_{AVDD} = V_{DVDD} = 3.3V$, $T_A = +25^{\circ}C.$) (Note 2)

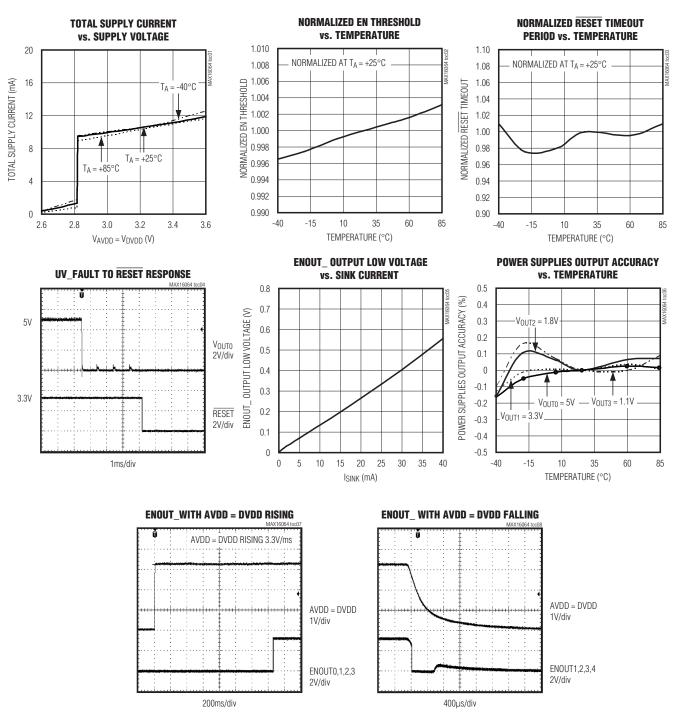
PARAMETER	SYMBOL	CONDITIONS	MIN	ТҮР	MAX	UNITS
ADDRESS PINS (A1/SCLE, A2/SI	DAE, A3/CON	ITROL)	•			•
Input Logic-Low Voltage					0.3	V
Input Logic-Low Hysteresis				50		mV
Input Logic-High Voltage			V _{AVDD} - 0.4			V
Input Logic-High Hysteresis				50		mV
Input Leakage Current			-12		+12	μA
SMBus INTERFACE (SCL, SDA)	(Note 3)		•			•
SCL, SDA Input Low Voltage	VIL	Input voltage falling			0.8	V
SCL, SDA Input High Voltage	VIH	Input voltage rising	2.1			V
SCL, SDA Input Leakage Current (Per Pin)		Device powered or unpowered, $V_{AVDD} = 0$ to 3.6V, $V_{SCL} = V_{SDA} = 0V$ or V_{AVDD}	-1		+1	μΑ
Input Capacitance	CIN			10		pF
SCL, SDA Output Low Voltage	Vol	Isink = 3mA			0.4	V
SMBUS TIMING			•			•
Serial-Clock Frequency	fSCL		10		100	kHz
Bus Free Time Between STOP and START Condition	tBUF		4.7			μs
START Condition Setup Time	tsu:sta		4.7			μs
START Condition Hold Time	^t HD:STA		4.0			μs
STOP Condition Setup Time	tsu:sto		4.0			μs
Clock Low Period	tLOW		4.7			μs
Clock High Period	thigh		4.0			μs
Data Setup Time	tsu:dat		250			ns
Output Fall Time	tOF	C _{BUS} = 10pF to 400pF			300	ns
Data Hold Time	thd:dat	From 50% SCL falling to SDA change	300			ns
Pulse Width of Spike Suppressed	tsp			30		ns
SMBus Timeout	TIMEOUT	SMBCLK time low for reset	25		55	ms
OTHER TIMING PARAMETERS			•			•
PMBus Command Response Time	^t PMB_RSP			300		μs
Fault Response Time	tFAULT_RSP			5		ms
Recovery Time After Device Reset	trst_wait	No external EEPROM		15		ms

Note 2: 100% production tested at $T_A = +25^{\circ}C$. Limits over temperature are guaranteed by design.

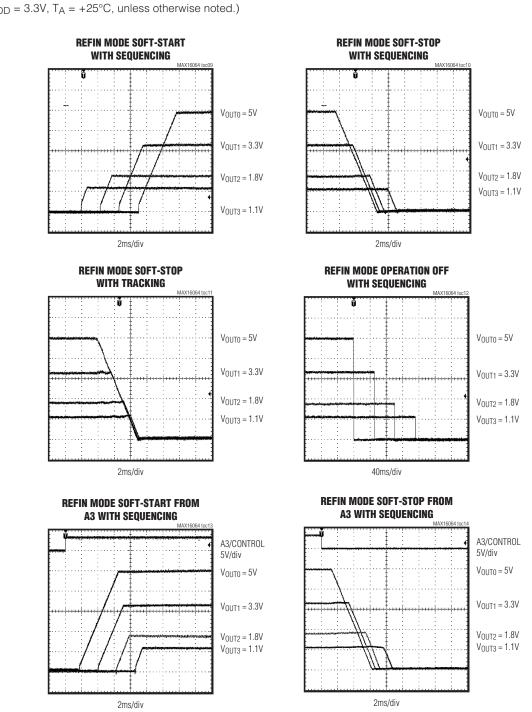
Note 3: The MAX16064 supports SCL clock stretching.

 $(V_{AVDD} = V_{DVDD} = 3.3V, T_A = +25^{\circ}C$, unless otherwise noted.)

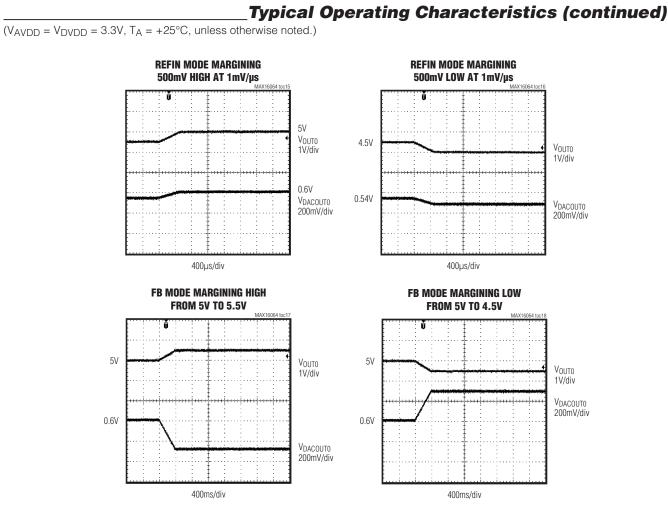
Typical Operating Characteristics



MAX16064



Typical Operating Characteristics (continued) (V_{AVDD} = V_{DVDD} = 3.3V, T_A = +25°C, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	RS2-	Differential Remote-Sense Input 2 Return of the DC-DC Output Voltage. Connect to the return terminal at the load.
2	RS2+	Differential Remote-Sense Input 2 of DC-DC Output Voltage. Connect to the load terminal where the output must be regulated.
3	RS3+	Differential Remote-Sense Input 3 of DC-DC Output Voltage. Connect to the load terminal where the output must be regulated.
4	RS3-	Differential Remote-Sense Input 3 Return of the DC-DC Output Voltage. Connect to the return terminal at the load.
5	RS3C	Filter Capacitor for V _{SENSE} Amplifier 3. Connect a 1µF capacitor from RS3C to AGND.
6	EN	Enable Input. All ENOUT_ are deasserted when the voltage on EN is below 1.2V (typ). Used to turn on/off the controlled power supplies in conjunction with the PMBus OPERATION command.
7	DACOUT1	Analog Voltage Output of Internal 12-Bit DAC 1. Connect to TRIM, REFIN, or FB of a DC-DC module or an LDO to adjust the power-supply output voltage. High impedance in shutdown.
8	AGND	Analog Ground. Connect AGND to AGND1 and to DGND externally close to the device.
9	ENOUTO	On/Off Signal Output 0. Typically used to turn on/off a power supply. Controlled by the PMBus OPERATION command or the sequencer. Can be configured as either an active-high or an active-low open-drain output. See the <i>ENOUT_ Operation</i> section.
10	ENOUT1	On/Off Signal Output 1. Typically used to turn on/off a power supply. Controlled by the PMBus OPERATION command or the sequencer. Can be configured as either an active-high or an active-low open-drain output. See the <i>ENOUT_ Operation</i> section.
11	ENOUT2	On/Off Signal Output 2. Typically used to turn on/off a power supply. Controlled by the PMBus OPERATION command or the sequencer. Can be configured as either an active-high or an active-low open-drain output. See the <i>ENOUT_ Operation</i> section.
12	ENOUT3	On/Off Signal Output 3. Typically used to turn on/off a power supply. Controlled by the PMBus OPERATION command or the sequencer. Can be configured as either an active-high or an active-low open-drain output. See the <i>ENOUT_ Operation</i> section.
13	CLKIO	Clock Input/Output. User-configurable clock input/output signal. The system controller can provide a clock input to synchronize the time bases of multiple MAX16064 devices. Alternatively, a MAX16064 can provide a 1MHz output clock to other MAX16064s for synchronization. See the <i>MFR_MODE (D1h)</i> section. When configured as an output, CLKIO is an open-drain output and a pullup resistor is required.
14	A1/SCLE	Dual-Functioned MAX16064 Slave Address Identifier (LSB) and EEPROM I ² C Clock Output. See the <i>MAX16064 Address Assignment</i> and <i>External EEPROM Interface</i> sections.
15	A2/SDAE	Dual-Functioned MAX16064 Slave Address Identifier and EEPROM I ² C Data Input/Output. See the <i>MAX16064 Address Assignment</i> and <i>External EEPROM Interface</i> sections.
16	A3/CONTROL	Dual-Functioned MAX16064 Slave Address Identifier (MSB) and Power-Supply On/Off Control Using the MFR_MODE Command. See the <i>MAX16064 Address Assignment</i> and <i>A3/CONTROL Operation</i> sections.
17	RESET	Active-Low, Open-Drain Reset Output

Pin Description (continued)

PIN	NAME	FUNCTION
18	SMBALERT	Active-Low, Open-Drain Fault-Detection Interrupt Output
19	SCL	SMBus Serial-Clock Input/Output
20	SDA	SMBus Serial-Data Input/Output
21	DGND	Digital Ground. Connect DGND to AGND and AGND1 externally close to the device.
22	DVDD	Digital Power-Supply Input. Connect a 1µF capacitor from DVDD to DGND.
23	RSVD	Reserved. Connect to DVDD externally.
24	DACOUT3	Analog Voltage Output of Internal 12-Bit DAC 3. Connect to TRIM, REFIN, or FB of a DC-DC module or an LDO to adjust the power-supply output voltage. High impedance in shutdown.
25	AGND1	Analog Ground. Connect to AGND and DGND externally close to the device.
26	AVDD	Analog Power-Supply Input. Connect a 1µF capacitor from AVDD to AGND.
27	DACOUT2	Analog Voltage Output of Internal 12-Bit DAC 2. Connect to TRIM, REFIN, or FB of a DC-DC module or an LDO to adjust the power-supply output voltage. High impedance in shutdown.
28	RS1-	Differential Remote-Sense Input 1 Return of the DC-DC Output Voltage. Connect to the return terminal at the load.
29	RS1+	Differential Remote-Sense Input 1 of DC-DC Output Voltage. Connect to the load terminal where the output must be regulated.
30	RS1C	Filter Capacitor for V _{SENSE} Amplifier 1. Connect a 1µF capacitor from RS1C to AGND.
31	REFO	Reference Output. Connect a 1µF capacitor from REFO to AGND.
32	RS0+	Differential Remote-Sense Input 0 of DC-DC Output Voltage. Connect to the load terminal where the output must be regulated.
33	RSOC	Filter Capacitor for V _{SENSE} Amplifier 0. Connect a 1µF capacitor from RS0C to AGND.
34	RS0-	Differential Remote-Sense Input 0 Return of the DC-DC Output Voltage. Connect to the return terminal at the load.
35	DACOUT0	Analog Voltage Output of Internal 12-Bit DAC 0. Connect to TRIM, REFIN, or FB of a DC-DC module or an LDO to adjust the power-supply output voltage. High impedance in shutdown.
36	RS2C	Filter Capacitor for V _{SENSE} Amplifier 2. Connect a 1µF capacitor from RS2C to AGND.
_	EP	Exposed Pad. Internally connected to AGND. Connect EP to the ground plane of the power supplies for best temperature measurement performance.

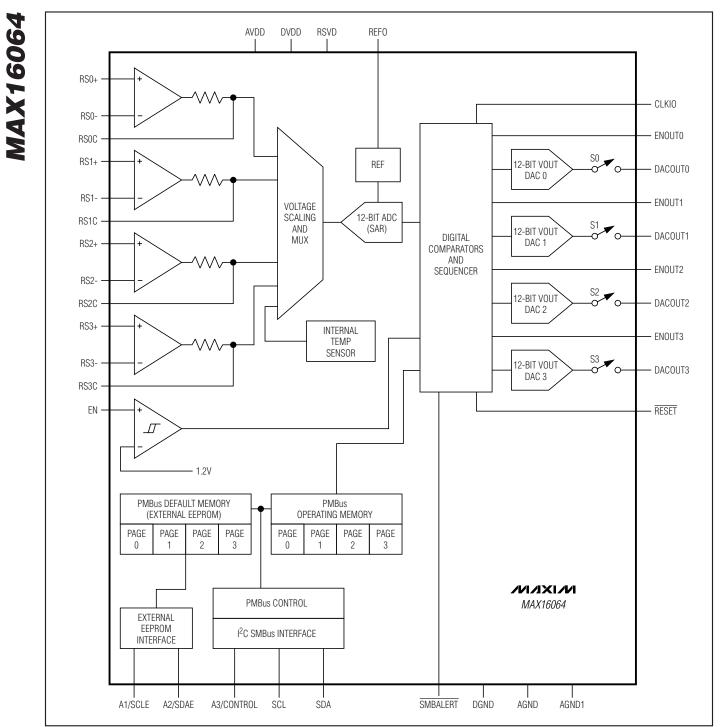


Figure 1. MAX16064 Functional Diagram

Detailed Description

The MAX16064 adds digital control functionality to four power supplies. Using a closed-loop control system, the MAX16064 can continuously adjust the power-supply output voltages to maintain $\pm 0.3\%$ output-voltage accuracy. The MAX16064 can also be programmed to sequence, track, and margin each power supply.

A PMBus-compliant interface bus provides access to configuration parameters of the MAX16064, including monitoring thresholds, sequence delays, soft-start and

soft-stop slew rates, output-voltage settings, an on-chip temperature sensor, and more.

Up to 114 MAX16064s can reside on the same PMBus bus, each controlling its own power supplies, under commands from the PMBus system controller, as shown in Figure 2. The MAX16064s can be placed close to the power supplies they control so that all sensitive analog traces are short and less susceptible to noise. The power supplies can also be placed close to the load where they provide the best transient response and lowest losses with short power plane runs.

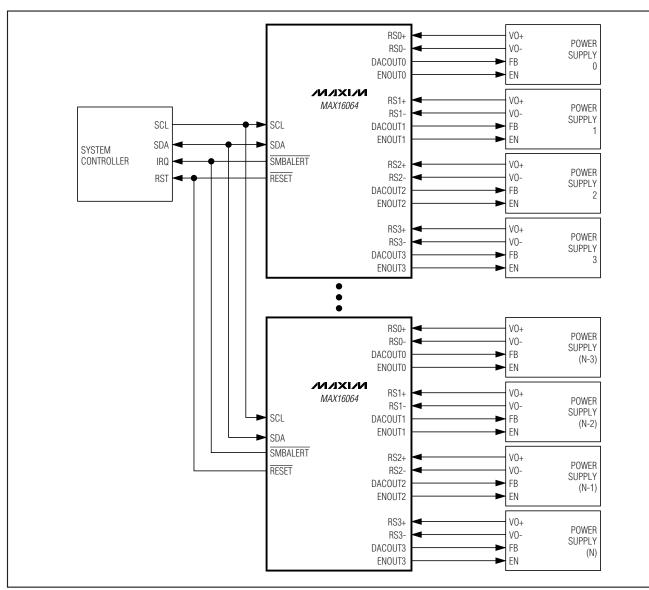


Figure 2. System Application Showing Multiple MAX16064s Controlling Power Supplies

11

MAX16064 Operating Modes

Reference Input (REFIN) Mode

Figure 3 shows how to connect a MAX16064 to the reference voltage input of a typical power supply, allowing the MAX16064 to fully control the power-supply output voltage. Connect a DACOUT_ of the MAX16064 to the REFIN input of the power supply and connect the output-voltage terminals of the power supply to the RS_+ and RS_- sense inputs of the MAX16064. The sensed voltage on RS_+ and RS_- is filtered by an internal 200Ω resistor and an external capacitor connected to RS_C, and is digitized by a 12-bit ADC that uses an accurate internal reference voltage.

Normal operation begins as follows: upon receiving an OPERATION ON command or a turn-on signal from A3/CONTROL, the MAX16064 waits the programmed tON DELAY time, then switches on the associated ENOUT_ output and ramps up the power-supply output voltage to its target VOUT COMMAND value precisely in the programmed ton RISE time. This facilitates easy implementation of tracking of multiple output rails. On reaching the target output voltage, the MAX16064 continuously monitors the power-supply output voltage obtained at the RS_+ and RS_- inputs, and regulates it to within ±0.3% by incrementing or decrementing the DACOUT_ output 1 LSB (0.5mV) at a time. The MAX16064 output-voltage correction rate is controlled by MFR_MODE.1, MFR_VLTO, and MFR_DAC_ACT_CNT, as discussed in the ADC Conversion, Monitoring, and AVOC Adjustment Rates section.

Once the requested target power-supply voltage is reached, it can be margined up or down at a slew rate programmed by the VOUT_TRANSITION_RATE parameter. To achieve this, the MAX16064 increments or decrements the DACOUT_ output in a suitable number of steps that depend on the programmed transition rate. The number of steps is calculated from the VOUT_SCALE_LOOP parameter, which must be set to the ratio of the power-supply output voltage to the power-supply reference voltage. This ratio is the same as the voltage-divider ratio implemented on the power supply from its output voltage node to the inverting input of its error amplifier. This allows the MAX16064 to correctly calculate the number of DACOUT_ steps and voltage increments/decrements per step and thus achieve the programmed rise time and transition time.

Since the reference voltage input is provided by the MAX16064, the REFIN mode provides complete control of the power supply in terms of soft-start, soft-stop, and margining transitions.

Upon receiving an OPERATION OFF command or a turn-off signal from A3/CONTROL, the MAX16064 waits the programmed tOFF_DELAY time, ramps the output voltage down to zero in the programmed tOFF_FALL time, then deasserts the ENOUT_ output. Each of the four power-supply converters has its own set of delay parameters, so sequencing is accomplished by loading different delay times for each power supply.

Feedback (FB) Mode

Some power-supply converters do not provide a reference input. In these applications, the feedback node can be used instead. Connect a DACOUT_ output of the MAX16064 to the feedback node (FB) through a resistor RFB as shown in Figure 5. In steady-state operation, the MAX16064 controls the power-supply voltage as measured between RS_+ and RS_- to $\pm 0.3\%$ accuracy by adjusting DACOUT_ 1 LSB at a time (0.5mV), up and down as required. This mode of operation is termed FB mode. Since the MAX16064 does not have control over the power-supply error-amplifier reference voltage, this mode relies on the power-supply soft-start setting to implement the required soft-start time.

Upon receiving an OPERATION ON command or a turn-on signal from A3/CONTROL, the MAX16064 waits the programmed t_{ON_DELAY} time, turns on the ENOUT_output, causing the power supply to ramp up its output voltage to its target value. The soft-start time taken by the power supply to ramp from zero to its commanded output voltage should be entered into the MAX16064 with the ton_RISE parameter.

During tON_RISE, the MAX16064 maintains DACOUT_ in a high-impedance state by keeping the S_ switches open. This allows the voltage at DACOUT_ to equal that of the FB node of the power supply. At the end of the ton RISE delay time, the internal DAC output voltage is set to match the external voltage measured on DACOUT_, and then the DACOUT_ switch S_ is closed. The voltages on either side of the resistor R_{FB} should be equal, or very close to equal. Under these conditions, little or no current flows into the FB node from DACOUT_ and no perturbations are introduced to the output voltage. From this point on, the MAX16064 adjusts the voltage at DACOUT_ to provide accurate output-voltage control. In FB mode, the user must supply ton DELAY and ton RISE. If those parameters are not set (the default values are zero), S closes prematurely and causes the supply voltage to overshoot or undershoot.

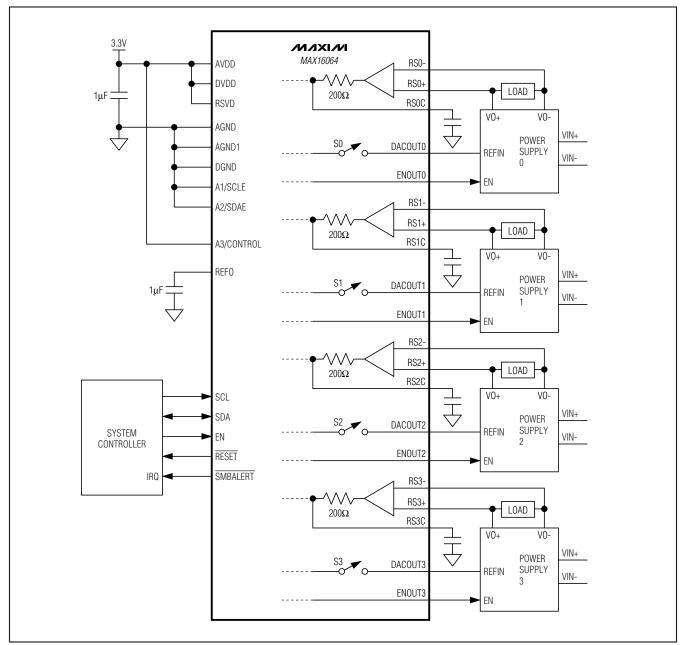


Figure 3. Typical System Application—REFIN Mode

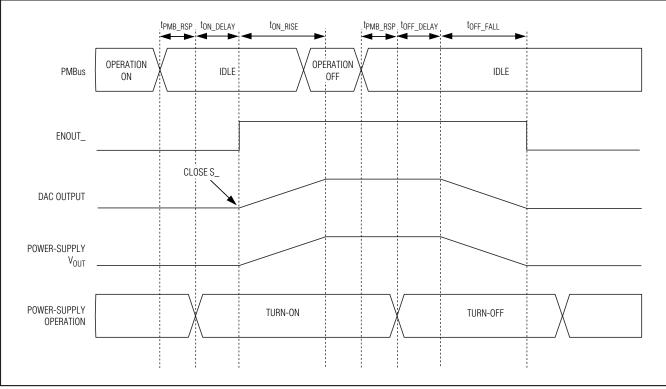


Figure 4. REFIN Mode Timing

After receiving an OPERATION OFF command or a turn-off signal from A3/CONTROL, the MAX16064 waits the programmed toFF_DELAY time, deasserts the ENOUT_ output, and turns off the power supply.

For the FB mode, use the following formula to calculate the value of $\ensuremath{\mathsf{R}}_{\ensuremath{\mathsf{FB}}}$:

$$R_{FB} = R_1 \times \frac{\Delta V_{DAC}}{\Delta V_O}$$

Where R₁ is the upper feedback divider resistor, ΔV_O is the required change in output voltage, and ΔV_{DAC} is the DACOUT_ output-voltage change that the user allows. The recommended operating range for the DACOUT_ voltage for power-supply output voltage adjustment is between 30mV and 2V. Note that ΔV_{DAC} is the difference between the steady-state power-supply FB node voltage, V_{FB}, and the voltage limits on DACOUT_. This is best illustrated with an example as follows:

Consider an application involving a power supply with $V_{FB} = 0.6V$. Let the desired margining be $\pm 10\%$ for a power-supply output voltage of 1V. For a power supply

with an upper voltage divider resistor $R_1 = 10k\Omega$, R_{FB} is calculated as follows:

$$R_{FB} = 10k\Omega \times \frac{(0.6V - 0.03V)}{0.1V} = 57k\Omega$$

This value of R_{FB} allows the MAX16064 to margin the power-supply output voltage up by 10%. It is useful to check the margin low condition by using the formula:

$$\Delta V_O = R_1 \times \frac{\Delta V_{DAC}}{R_{FB}} = 10 k\Omega \times \frac{(2.0V - 0.6V)}{57 k\Omega} = 0.245V$$

The effective margining range for the 57k Ω resistor therefore turns out to be between +10% and -24.5%.

Note that the VOUT_TRANSITION_RATE parameter has no effect on FB mode. The transition time for margining in the FB mode of operation is a function of the update rate (f_{AVOC}), see the *MFR_DAC_ACT_CNT (E0h)* section for the calculation of f_{AVOC}. R_{FB} and R₁, and t_{FB} is given by the following formula:

$$t_{FB} = \left(\frac{R_{FB} \times \Delta V_O \times 2000}{f_{AVOC} \times R_1}\right)$$

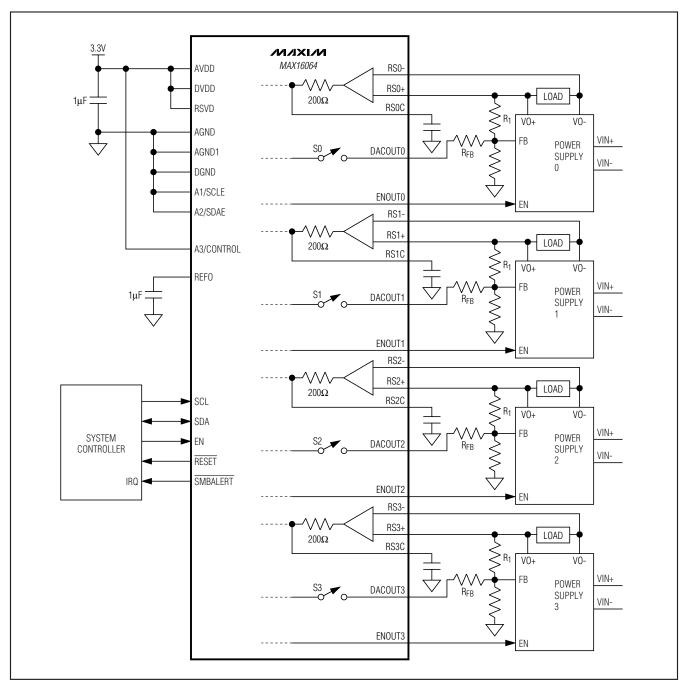


Figure 5. Typical System Application—Feedback Mode

15

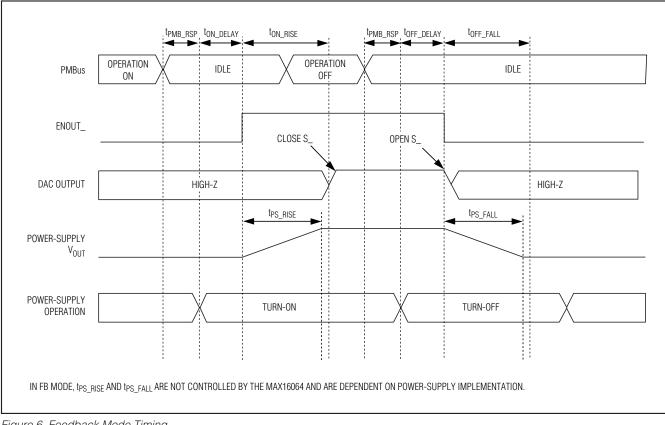


Figure 6. Feedback Mode Timing

Temperature Sensing

To obtain useful temperature readings, place the MAX16064 in close proximity to the power supplies. The on-chip temperature sensor on the MAX16064 senses the temperature of the die, which is related to the exposed pad temperature of the MAX16064 by the junction-to-case thermal resistance. The exposed pad of the MAX16064 can connect to the heat dissipating ground plane of the power supplies, and the power supplies' boards can be characterized to obtain the relationship between the power supplies' temperature and temperature as measured by the MAX16064. This information can be used to set overtemperature fault settings in the MAX16064.

ADC Conversion, Monitoring, and AVOC Adjustment Rates

Several timing parameters control the rate at which the MAX16064 monitors voltages and temperatures and the rate at which the MAX16064 adjusts the power-supply output voltages. Each of the four voltage input channels and the single temperature channel conversions are performed round-robin fashion. If the input filter is turned on by setting register MFR_MODE.1 to 0, then four conversions are performed for each channel instead of just one. A small programmable delay is inserted in between each conversion, determined by the MFR_VLTO register. This establishes the total conversion rate of the voltages and temperature. Smaller values of MFR VLTO results in a higher sampling rate, and larger values of MFR_VLTO allow for more ADC settling time.

The ADC conversion result registers are compared to the fault threshold registers at a rate that is independent of the total conversion rate. The value of register MFR_SAMPLE_RATE determines how frequently this comparison occurs. Using higher fault comparison rates increases glitch sensitivity, but slows the response time of the MAX16064 to PMBus commands. Using lower fault comparison rates makes the MAX16064 less sensitive to power-supply output voltage glitches.



Finally, the AVOC system uses a separate control loop rate that is related to the total ADC conversion rate. The value of register MFR_DAC_ACT_CNT sets the number of total ADC conversion cycles (one cycle is a complete set of ADC conversions for 4 voltages and 1 temperature) that must occur before AVOC changes the DAC output voltage. Smaller values of MFR_DAC_ACT_CNT shorten the adjustment time. Larger values of MFR_DAC_ACT_CNT adjust the output voltage at much slower rates, reducing possible negative effects on the power-supply control loop.

External EEPROM Interface

The MAX16064 can communicate with an EEPROM attached to the A1/SCLE and A2/SDAE. The MAX16064 communicates to the EEPROM with an address byte of 1010 0000 for writing and 1010 0001 for reading. For the data values of 2 bytes, the most significant byte is stored in the lower address of the EEPROM, whereas the least significant byte is stored in the higher address of the EEPROM.

Upon reset, the MAX16064 tests for the presence of a configuration EEPROM. It searches for the SIGNATURE bytes in the attached EEPROM. If the SIGNATURE bytes are present, it concludes that it has a valid configuration EEPROM and starts reading configuration information from the attached EEPROM. If the slave

address (MFR_SET_ADDRESS) is a value other than 0xFF, this overrides the slave address information previously set by the address A3:A1 pins.

Table 1b shows the contents and addresses of the configuration information expected by the MAX16064. This information is for reference only. It is recommended to use a properly configured, working MAX16064 to save its state to the EEPROM and limit direct modifications to as few fields as possible (such as the slave address).

Temperature and voltage values are stored in an internal representation, which is not the same as the format used by the corresponding PMBus commands. For details on the EEPROM internal representation, see Conversion Rules (Table 1a).

For example, to store to the EEPROM PAGE 2 VOUT_COMMAND = 3.0V, m = 19995, b = 0, R = -1. First calculate the PMBus command value, which is 5998. If the voltage range is 2V, no conversion is required. Hence write 17h to address 28 and 6Eh to address 29. If the voltage range is 5.5V, the stored EEPROM value = 5998/2.75 = 2181. So write 08h to address 28 and write 85h to address 29.

Note that the conversion is automatically handled by the MAX16064 when it stores and loads configuration information.

	READ (INTERNAL TO PMBus)	WRITE (PMBus TO INTERNAL)	
TEMPERATURE	Subtract 3010 (decimal) from the PMBus value	Add 3010 (decimal) to the PMBus value	
VOLTAGE	No conversion in 2V mode; multiply by 2.75 in 5.5V mode	No conversion in 2V mode; divide by 2.75 in 5.5V mode	

Table 1a. Conversion Rules

EEPROM ADDRESS	NAME	PAGE	PMBus COMMAND	NOTES
0	MFR_FAULT_REASON	_	0E2h	—
2	MFR_MODE		0D1h	Must also match MFR_TICK_RELOAD
4	MFR_TEMPERATURE_PEAK		0D6h	Internal representation (temperature)
6	MFR_FAULT_TEMP	_	0E4h	Internal representation (temperature)
8	MFR_VOUT_PEAK	0		
10	MFR_VOUT_PEAK	1	0D4h	Internal representation
12	MFR_VOUT_PEAK	2	0040	(voltage)
14	MFR_VOUT_PEAK	3		

Table 1b. 16-Bit Words Stored in EEPROM (continued)

EEPROM ADDRESS	NAME	PAGE	PMBus COMMAND	NOTES	
16	MFR_FAULT_VOUT	0			
18	MFR_FAULT_VOUT	1		Internal representation	
20	MFR_FAULT_VOUT	2	0E3h	(voltage)	
22	MFR_FAULT_VOUT	3			
24	VOUT_COMMAND	0			
26	VOUT_COMMAND	1		Internal representation	
28	VOUT_COMMAND	2	21h	(voltage)	
30	VOUT_COMMAND	3			
32	TON_RISE	0			
34	TON_RISE	1	0.41		
36	TON_RISE	2	61h	—	
38	TON_RISE	3			
40	TON_DELAY	0			
42	TON_DELAY	1			
44	TON_DELAY	2		—	
46	TON_DELAY	3			
48	VOUT_MARGIN_HIGH	0			
50	VOUT_MARGIN_HIGH	1		Internal representation (voltage)	
52	VOUT_MARGIN_HIGH	2	25h		
54	VOUT_MARGIN_HIGH	3			
56	VOUT_MARGIN_LOW	0			
58	VOUT_MARGIN_LOW	1		Internal representation	
60	VOUT_MARGIN_LOW	2	26h	(voltage)	
62	VOUT_MARGIN_LOW	3			
64	TOFF_FALL	0			
66	TOFF_FALL	1			
68	TOFF_FALL	2	65h	—	
70	TOFF_FALL	3			
72	OT_FAULT_LIMIT		4Fh	Internal representation	
74	MFR_SAMPLE_RATE		0D3h	_	
76–87	Reserved (set to 0)	_	_	—	
88	MFR_FAULT_RESPONSE	0			
90	MFR_FAULT_RESPONSE	1			
92	MFR_FAULT_RESPONSE	2	0D9h	-	
94	MFR_FAULT_RESPONSE	3			
96	MFR_FAULT_RETRY	0			
98	MFR_FAULT_RETRY	1			
100	MFR_FAULT_RETRY	2	0DAh	-	
102	MFR_FAULT_RETRY	3			

EEPROM ADDRESS	NAME	PAGE	PMBus COMMAND	NOTES	
104–115	MFR_DATE	_	9Dh	—	
116	MFR_STATUS_WORD	—	0D8h	Set to 0	
118	WRITE_PROTECT	_	10h	—	
120	ON_OFF_CONFIG	0		_	
122	ON_OFF_CONFIG	1	0.04		
124	ON_OFF_CONFIG	2	02h		
126	ON_OFF_CONFIG	3			
128	VOUT_SCALE_LOOP	0			
130	VOUT_SCALE_LOOP	1	0.01-		
132	VOUT_SCALE_LOOP	2	29h	_	
134	VOUT_SCALE_LOOP	3			
136	OT_WARN_LIMIT		51h	Internal representation (temperature)	
138	Reserved (set to 0)	—	—	—	
140	MFR_SET_ADDRESS	_	0DBh	Low byte: I ² C address, high byte: reserved	
142	Reserved (set to 0)	_	_	—	
144	TOFF_DELAY	0			
146	TOFF_DELAY	1		—	
148	TOFF_DELAY	2	64h		
150	TOFF_DELAY	3			
152	VOUT_TRANSITION_RATE	0		_	
154	VOUT_TRANSITION_RATE	1	071		
156	VOUT_TRANSITION_RATE	2	27h		
158	VOUT_TRANSITION_RATE	3			
160–175	Reserved (set to 0)	0	_	_	
176	MFR_MODE_OUTPUT	0			
178	MFR_MODE_OUTPUT	1		_	
180	MFR_MODE_OUTPUT	2	0DEh		
182	MFR_MODE_OUTPUT	3			
184–199	Reserved (set to 0)	_	_	_	
200	MFR_RESET_DELAY	_	0DDh	—	
202	MFR_RESET_OUTPUT	_	0E1h	_	
204	Reserved (set to 0)	_	_	—	
206	MFR_TICK_RELOAD		0D1h	—	
208	MFR_STATUS_WORD	0			
210	MFR_STATUS_WORD	1	000-		
212	MFR_STATUS_WORD	2	0D8h	Set to 0	
214	MFR_STATUS_WORD	3			

Table 1b. 16-Bit Words Stored in EEPROM (continued)



EEPROM ADDRESS	NAME	PAGE	PMBus COMMAND	NOTES
216–237	MFR_LOCATION		9Ch	—
238–255	MFR_SERIAL		9Eh	_
256–297	MFR_USER_DATA_00	_	0B0h	_
298	VOUT_OV_FAULT_LIMIT	0	40h	Internal representation (voltage)
300	VOUT_UV_FAULT_LIMIT	0	44h	Internal representation (voltage)
302	VOUT_OV_WARN_LIMIT	0	42h	Internal representation (voltage)
304	VOUT_UV_WARN_LIMIT	0	43h	Internal representation (voltage)
306	VOUT_OV_FAULT_LIMIT	1	40h	Internal representation (voltage)
308	VOUT_UV_FAULT_LIMIT	1	44h	Internal representation (voltage)
310	VOUT_OV_WARN_LIMIT	1	42h	Internal representation (voltage)
312	VOUT_UV_WARN_LIMIT	1	43h	Internal representation (voltage)
314	VOUT_OV_FAULT_LIMIT	2	40h	Internal representation (voltage)
316	VOUT_UV_FAULT_LIMIT	2	44h	Internal representation (voltage)
318	VOUT_OV_WARN_LIMIT	2	42h	Internal representation (voltage)
320	VOUT_UV_WARN_LIMIT	2	43h	Internal representation (voltage)
322	VOUT_OV_FAULT_LIMIT	3	40h	Internal representation (voltage)
324	VOUT_UV_FAULT_LIMIT	3	44h	Internal representation (voltage)
326	VOUT_OV_WARN_LIMIT	3	42h	Internal representation (voltage)
328	VOUT_UV_WARN_LIMIT	3	43h	Internal representation (voltage)
330–509	Unused (set to 0)	_	_	—
510	SIGNATURE (set to 4432h)	_	N/A	_

Table 1b. 16-Bit Words Stored in EEPROM (continued)

Figure 7 shows how the MAX16064 interfaces to an external serial EEPROM using the A1/SCLE and A2/SDAE in applications where a master controller does not exist or is not required. Using the GUI, the user can select each MAX16064 device and configure all the required output-voltage settings and sequencing/tracking information. Once the configuration is complete, the results can be saved to the external EEPROM by using the STORE_DEFAULT_ALL command and configuration restored on the MAX16064 power-on reset. The EEPROM can also be preprogrammed prior to board assembly in the manufacturing environment. A3/CONTROL can be used as a control signal to turn on/off the power supply in a similar fashion as the OPERATION command.

Use a serial EEPROM IC with a minimum of 4kb of storage to ensure proper device operation.

MAX16064 Operation

On power-up reset, the MAX16064 goes through an initialization process as shown in Figure 8.

After initialization, the MAX16064 monitors the PMBus and executes the PMBus commands accordingly. In addition, if the power supply has been commanded to turn on, the MAX16064 also monitors the power-supply output voltage and temperature at the MFR_SAMPLE_RATE. The PMBus system controller can monitor the power-supply health by issuing various inquiries and status commands to the MAX16064.

RESET Output Operation

RESET is an active-low, open-drain output that is low when the device is powering on. RESET is assigned to one of the power supplies using the MFR_RESET_OUTPUT command. When that power-supply output is at the target voltage, RESET goes high after the reset timeout period (see Figure 9). The reset timeout period (tRP) is set by the MFR_RESET_DELAY command.

The MFR_RESET_OUTPUT value defines which powersupply output affects $\overline{\text{RESET}}$. If MFR_RESET_OUTPUT is set to 0, 1, 2, or 3, then $\overline{\text{RESET}}$ goes high t_RP after that output has reached its target value. If MFR_RESET_OUT-PUT is any other value, $\overline{\text{RESET}}$ is permanently low.

If the power-supply output selected by MFR_RESET_OUTPUT is later disabled for any reason (either due to a fault condition, or an OPERATION OFF command), then RESET goes low immediately. To enable faults on any power supply to cause RESET to go low, set the MFR_MODE_OUTPUT.GLOBALFAULTS bit to a 1 for all the supplies.

RESET requires an external pullup resistor.

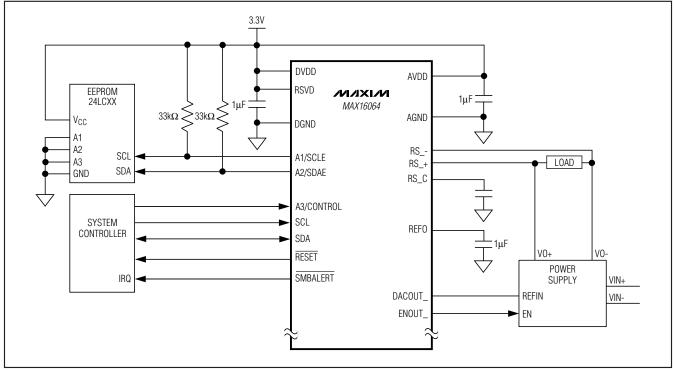


Figure 7. Typical System Application with External EEPROM

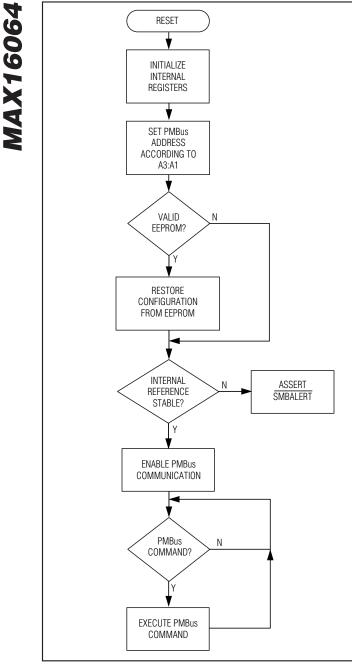


Figure 8. MAX16064 Initialization

SMBALERT Output Operation

SMBALERT is an optional interrupt signal defined in Appendix A of the SMBus specification. The MAX16064 provides an output SMBALERT as this interrupt signal. SMBALERT is an active-low, open-drain output and it asserts to signal the PMBus master if any of the voltage or temperature fault has occurred. Typically, SMBALERT is connected to all other SMBALERT opendrain signals in the system, creating a wired-OR function with all SMBALERT outputs. When the master is interrupted by its SMBALERT input, it stops or finishes the current bus transfer and places an alert response address (ARA) on the bus. The slave that pulled the SMBALERT signal low acknowledges the ARA and places its own address on the bus, identifying itself to the master as the slave that caused the interrupt.

SMBALERT deasserts when the MAX16064 responds to the ARA. SMBALERT deasserts when all the fault conditions are removed. SMBALERT is also cleared by the CLEAR_FAULTS command.

ENOUT_ Operation

When power is applied, all ENOUT_ are held low. Upon receiving a command to turn on the power supply, ENOUT_ goes high. The polarity can be changed by the ENOUT_POL bit of the MFR_MODE_OUTPUT command. Setting the bit to a 1 makes the ENOUT_ active low. If the bit in the external EEPROM is set to 1, upon power-up, the ENOUT_ is held low until the bit is copied from the EEPROM to the on-chip register at which time the ENOUT_ goes high. Upon receiving a command to turn on the power supply, ENOUT_ goes low. It takes 1.60ms (typ) to copy the configuration bits from the EEPROM to the on-chip registers.

Table 2. ENOUT_ Active State

ENOUT_ DEFAULT STARTUP STATE	MFR_MODE_OUTPUT. ENOUT_POL	ENOUT_ ACTIVE STATE
Low	0	Active high
Low	1	Active low

EN Operation

The MAX16064 includes an enable input (EN) that controls all ENOUT_ signals in conjunction with the MFR_MODE command. Unless MFR_MODE.IGNORE_EN is set, a below-threshold level on EN prevents any ENOUT_ from turning on. Additionally, if the voltage at EN falls below the 1.2V (typ) threshold during OPERATION ON, the MAX16064 follows the fault action in MFR_FAULT_RESPONSE.EN. Figure 9 shows a typical sequencing with MFR_MODE.IGNORE_EN = 0.



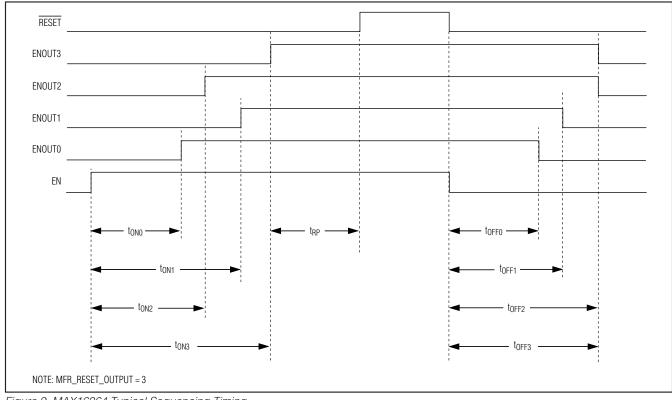


Figure 9. MAX16064 Typical Sequencing Timing

MAX16064 Address Assignment

The MAX16064 picks a slave address in one of the two ways described below:

1) Hardwired by A3:A2:A1.

2) Restored from EEPROM at power-on.

Address assignment order is shown in Figure 10.

The MAX16064 reads A3:A2:A1 address pins upon device reset and determines its address according to Table 3.

Table 3. MAX16064 A3:A1 Slave Address Assignment

A3/CONTROL	A2/SDAE	A1/SCLE	ADDRESS (BITS 7–1)
L	L	L	40h
L	L	Z	01h*
L	Z	L	02h
L	Z	Z	03h
Z	L	L	04h
Z	L	Z	05h
Z	Z	L	06h
Z	Z	Z	07h
L	L	Н	09h
L	Z	Н	OBh
Z	L	Н	0Dh

A3/CONTROL	A2/SDAE	A1/SCLE	ADDRESS (BITS 7–1)
Z	Z	Н	0Fh
L	Н	L	12h
L	Н	Z	13h
Z	Н	L	16h
Z	Н	Z	17h
L	Н	Н	1Bh
Z	Н	Н	1Fh
Н	L	L	24h
Н	L	Z	25h
Н	Z	L	26h
Н	Z	Z	27h
Н	L	Н	2Dh
Н	Z	Н	2Fh
Н	Н	L	36h
Н	Н	Z	37h
Н	Н	Н	3Fh

Table 3. MAX16064 A3:A1 Slave Address Assignment (continued)

*The shaded addresses are not available if external EEPROM is attached.

The hardwired address pins give $3^3 = 27$ address options. For example, to configure the MAX16064 to have a slave address of 010 0101 (25h), set A3:A2:A1 = H:L:Z. The MAX16064 also responds to the broadcast address (00h).

If an EEPROM with valid SIGNATURE bytes is attached to the MAX16064, the MAX16064 tries to restore its slave address from the EEPROM. This overrides the address set by the address pins. This gives a total of 128 possible slave addresses. Note that there are 14 reserved addresses that are restricted by the PMBus specification and may not be used in PMBus systems. If the address bit 7 from the EEPROM is set to 1, this is an invalid address and the MAX16064 continues using the address set by the address pins. When an EEPROM is attached to A2/SDAE and A1/SCLE, these pins assume either a logic-high or a logic-low level, therefore, the resulting number of possible addresses set by the A3:A2:A1 pins in this scenario is $2^3 = 8$.

In addition, for the MAX16064 with an EEPROM attached, the system controller can change the MAX16064 slave address by sending the new address with the MFR_SET_ADDRESS command. However, the new address is not immediately effective. The new address must be stored to the EEPROM first using the STORE_DEFAULT_ALL command. Then, the

MAX16064 power must be cycled to start the address assignment procedure and recalls the new address from the EEPROM.

A3/CONTROL Operation

/N/XI/N

The A3/CONTROL input is utilized in combination with the A2 and A1 inputs to set the PMBus address when power is applied to the device. After the PMBus address detection, the A3/CONTROL input functions as the PMBus CONTROL input.

The ON_OFF_CONFIG command determines whether the A3/CONTROL input affects the on/off behavior of the power supply. When A3/CONTROL is enabled by the ON OFF CONFIG command, a transition of A3/CON-TROL from low to high turns the power supply on, as if the MAX16064 has received an OPERATION ON command. A transition of A3/CONTROL from high to low initiates a soft-off to the power supply, as if the MAX16064 has received an OPERATION OFF command (soft-off, with sequencing). The MAX16064 still responds to the PMBus OPERATION command while A3/CONTROL is enabled. To detect the A3/CONTROL input, the A3/CONTROL signal pulse width has to satisfy the tA3 LOW and tA3 HIGH requirements to be detected. See the ON_OFF_CONFIG (02h) section and Table 6 for more information.

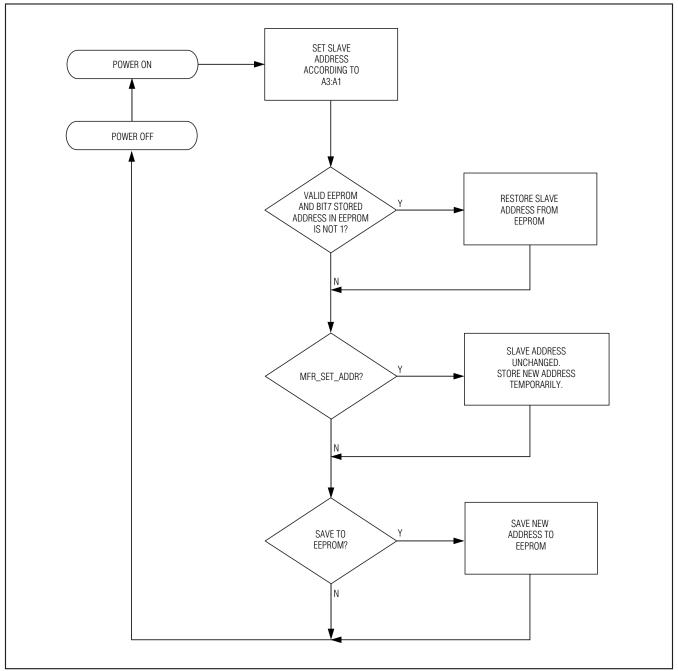


Figure 10. MAX16064 Address Assignment