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MAX16065/MAX16066

12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

General Description

The MAX16065/MAX16066 flash-configurable system managers monitor and sequence multiple system voltages. The MAX16065/MAX16066 can also accurately monitor ($\pm 2.5\%$) one current channel using a dedicated high-side current-sense amplifier. The MAX16065 manages up to twelve system voltages simultaneously, and the MAX16066 manages up to eight supply voltages. These devices integrate a selectable differential or single-ended analog-to-digital converter (ADC) and configurable outputs for sequencing power supplies. Device configuration information, including overvoltage and undervoltage limits, timing settings, and the sequencing order is stored in nonvolatile flash memory. During a fault condition, fault flags and channel voltages can be automatically stored in the nonvolatile flash memory for later read-back.

The internal 1% accurate 10-bit ADC measures each input and compares the result to one overvoltage, one undervoltage, and one early warning limit that can be configured as either undervoltage or overvoltage. A fault signal asserts when a monitored voltage falls outside the set limits. Up to three independent fault output signals are configurable to assert under various fault conditions.

Because the MAX16065/MAX16066 support a power-supply voltage of up to 14V, they can be powered directly from the 12V intermediate bus in many systems.

The integrated sequencer provides precise control over the power-up and power-down order of up to twelve (MAX16065) or up to eight (MAX16066) power supplies. Eight outputs (EN_OUT1–EN_OUT8) are configurable with charge-pump outputs to directly drive external n-channel MOSFETs.

The MAX16065/MAX16066 include eight/six programmable general-purpose inputs/outputs (GPIO_s). GPIO_s are flash configurable as dedicated fault outputs, as a watchdog input or output, or as a manual reset.

The MAX16065/MAX16066 feature nonvolatile fault memory for recording information during system shutdown events. The fault logger records a failure in the internal flash and sets a lock bit protecting the stored fault data from accidental erasure. An SMBus or a JTAG serial interface configures the MAX16065/MAX16066. The MAX16065 is available in a 48-pin, 7mm x 7mm, TQFN package, and the MAX16066 is available in a 40-pin, 6mm x 6mm, TQFN package. Both devices are fully specified from -40°C to $+85^{\circ}\text{C}$.

Features

- ◆ Operate from 2.8V to 14V
- ◆ $\pm 2.5\%$ Current-Monitoring Accuracy
- ◆ 1% Accurate 10-Bit ADC Monitors 12/8 Voltage Inputs
- ◆ Single-Ended or Differential ADC for System Voltage/Current Monitoring
- ◆ Integrated High-Side Current-Sense Amplifier
- ◆ 12/8 Monitored Inputs with Overvoltage/Undervoltage/Early Warning Limit
- ◆ Nonvolatile Fault Event Logger
- ◆ Power-Up and Power-Down Sequencing Capability
- ◆ Independent Secondary Sequence Block
- ◆ 12/8 Outputs for Sequencing/Power-Good Indicators
- ◆ Two Programmable Fault Outputs and One Reset Output
- ◆ Eight General-Purpose Inputs/Outputs Configurable as:
 - Dedicated Fault Outputs
 - Watchdog Timer Function
 - Manual Reset
 - Margin Enable
- ◆ SMBus (with Timeout) or JTAG Interface
- ◆ Flash Configurable Time Delays and Thresholds
- ◆ -40°C to $+85^{\circ}\text{C}$ Operating Temperature Range

Applications

Networking Equipment
 Telecom Equipment (Base Stations, Access)
 Storage/Raid Systems
 Servers

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16065ETM+	-40°C to $+85^{\circ}\text{C}$	48 TQFN-EP*
MAX16066ETL+	-40°C to $+85^{\circ}\text{C}$	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Typical Operating Circuits appear at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

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ABSOLUTE MAXIMUM RATINGS

V_{CC}, CSP, CSM to GND.....-0.3V to +15V
 CSP to CSM.....-0.7V to +0.7V
 MON_, GPIO_, SCL, SDA, A0, RESET, EN_OUT9–EN_OUT12 to GND (programmed as open-drain outputs).....-0.3V to +6V
 EN, TCK, TMS, TDI to GND-0.3V to +4V
 DBP, ABP to GND.....-0.3V to the lower of +4V or (V_{CC} + 0.3V)
 EN_OUT1–EN_OUT8 to GND (programmed as open-drain outputs)-0.3V to +15V
 TDO, EN_OUT_, GPIO_, RESET (programmed as push-pull outputs)..... -0.3V to (V_{DBP} + 0.3V)

Input/Output Current20mA
 Continuous Power Dissipation (T_A = +70°C)
 40-Pin TQFN (derate 26.3mW/°C above +70°C).....2105mW
 48-Pin TQFN (derate 27.8mW/°C above +70°C).....2222mW
 Operating Temperature Range.....-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range.....-65°C to +150°C
 Lead Temperature (soldering, 10s)+300°C
 Soldering Temperature (reflow)+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.)
 (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V _{CC}	Reset output asserted low	1.2			V
		(Note 2)	2.8		14	
Undervoltage Lockout (Rising)	V _{UVLO}	Minimum voltage on V _{CC} to ensure the device is flash configurable			2.7	V
Undervoltage Lockout Hysteresis	V _{UVLO_HYS}			100		mV
Minimum Flash Operating Voltage	V _{flash}	Minimum voltage on V _{CC} to ensure flash erase and write operations		2.7		V
Supply Current	I _{CC}	No load on output pins		4.5	7	mA
		During flash writing cycle		10	14	
ABP Regulator Voltage	V _{ABP}	C _{ABP} = 1μF, no load, V _{CC} = 5V	2.85	3	3.15	V
DBP Regulator Voltage	V _{DBP}	C _{DBP} = 1μF, no load, V _{CC} = 5V	2.8	3	3.1	V
Boot Time	t _{BOOT}	V _{CC} > V _{UVLO}		200	350	μs
Flash Writing Time		8-byte word		122		ms
Internal Timing Accuracy		(Note 3)	-8		+8	%
EN Input Voltage	V _{TH_EN_R}	EN voltage rising		1.41		V
	V _{TH_EN_F}	EN voltage falling	1.365	1.39	1.415	
EN Input Current	I _{EN}		-0.5		+0.5	μA
MON_ Input Voltage Range			0		5.5	V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
ADC DC ACCURACY							
Resolution					10	Bits	
Gain Error	ADCGAIN	T _A = +25°C			0.35	%	
		T _A = -40°C to +85°C			0.70		
Offset Error	ADCOFF				1	LSB	
Integral Nonlinearity	ADCINL				1	LSB	
Differential Nonlinearity	ADCDNL				1	LSB	
ADC Total Monitoring Cycle Time	t _{CYCLE}	No MON_ fault detected		40	50	μs	
ADC IN_ Ranges		1 LSB = 5.43mV		5.56		V	
		1 LSB = 2.72mV		2.78			
		1 LSB = 1.36mV		1.39			
CURRENT SENSE							
CSP Input-Voltage Range	V _{CSP}		3		14	V	
Input Bias Current	I _{CSP}			14	25	μA	
	I _{CSM}	V _{CSP} = V _{CSM}		3	5		
CSP Total Unadjusted Error	CSPERR	(Note 4)			2	%FSR	
Overcurrent Differential Threshold	OV _{CTH}	V _{CSP} - V _{CSM}	Gain = 48	21.5	25	30.5	mV
			Gain = 24	46	51	56	
			Gain = 12	94	101	108	
			Gain = 6	190	202	210	
V _{SENSE} Fault Threshold Hysteresis	OV _{CHYS}			0.5		%OV _{CTH}	
Secondary Overcurrent Threshold Timeout	OV _{CDEL}	r73h[6:5] = '00'		0		ms	
		r73h[6:5] = '01'	3	4	5		
		r73h[6:5] = '10'	12	16	20		
		r73h[6:5] = '11'	50	64	60		
V _{SENSE} Ranges			Gain = 6		232	mV	
			Gain = 12		116		
			Gain = 24		58		
			Gain = 48		29		
ADC Current Measurement Accuracy			V _{SENSE} = 150mV (gain = 6 only)	-2.5	±0.2	+2.5	%
			V _{SENSE} = 50mV, gain = 12	-4	±0.2	+4	
			V _{SENSE} = 25mV, gain = 24		±0.5		
			V _{SENSE} = 10mV, gain = 48		±1		
Gain Accuracy		V _{SENSE} = 20mV to 100mV, V _{CSP} = 5V, gain = 6	-1.5		+1.5	%	
Common-Mode Rejection Ratio	CMRR _{SNS}	V _{CSP} > 4V		80		dB	
Power-Supply Rejection Ratio	PSRR _{SNS}			80		dB	

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS (EN_OUT_, RESET, GPIO_)						
Output-Voltage Low	V _{OL}	I _{SINK} = 2mA			0.4	V
		I _{SINK} = 10mA, GPIO_ only			0.7	
		V _{CC} = 1.2V, I _{SINK} = 100μA (RESET only)			0.3	
Maximum Output Sink Current		Total current into EN_OUT_, RESET, GPIO_, V _{CC} = 3.3V			30	mA
Output-Voltage High (Push-Pull)		I _{SOURCE} = 100μA	2.4			V
Output Leakage (Open Drain)					1	μA
		V _{EN_OUT1} - V _{EN_OUT8} = 13.2V			5	
OUT_ Overdrive (Charge Pump) (EN_OUT1-EN_OUT8 Only)		I _{GATE_} = 1μA	10	11	13	V
OUT_ Pullup Current (Charge Pump)	I _{CH_UP}	During power up, V _{GATE} = 1V	2.5	4		μA
SMBus INTERFACE						
Logic-Input Low Voltage	V _{IL}	Input voltage falling			0.8	V
Logic-Input High Voltage	V _{IH}	Input voltage rising	2.0			V
Input Leakage Current		I _N = GND or V _{CC}	-1		+1	μA
Output Voltage Low (SDA/SCL)	V _{OL}	I _{SINK} = 3mA			0.4	V
Input Capacitance	C _{IN}			5		pF
SMBus Timeout	t _{TIMEOUT}	SCL time low for reset	25		35	ms
INPUTS (A0, GPIO_)						
Input Logic-Low	V _{IL}				0.8	V
Input Logic-High	V _{IH}		2.0			V
WDI Pulse Width	t _{WDI}		100			ns
MR Pulse Width	t _{MR}		1			μs
MR to RESET Delay				0.5		μs
MR Glitch Rejection				100		ns
SMBus TIMING						
Serial Clock Frequency	f _{SCL}				400	kHz
Bus Free Time Between STOP and START Condition	t _{BUF}		1.3			μs
START Condition Setup Time	t _{SU:STA}		0.6			μs
START Condition Hold Time	t _{HD:STA}		0.6			μs
STOP Condition Setup Time	t _{SU:STO}		0.6			μs
Clock Low Period	t _{LOW}		1.3			μs
Clock High Period	t _{HIGH}		0.6			μs
Data Setup Time	t _{SU:DAT}		100			ns

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Fall Time	t _{OF}	CBUS = 10pF to 400pF			250	ns
Data Hold Time	t _{HD:DAT}	From 50% SCL falling to SDA change	0.3		0.9	μs
Pulse Width of Spike Suppressed	t _{SP}			30		ns
JTAG INTERFACE						
TDI, TMS, TCK Logic-Low Input Voltage	V _{IL}	Input voltage falling			0.8	V
TDI, TMS, TCK Logic-High Input Voltage	V _{IH}	Input voltage rising	2			V
TDO Logic-Output Low Voltage	V _{OL}	I _{SINK} = 3mA			0.4	V
TDO Logic-Output High Voltage	V _{OH}	I _{SOURCE} = 200μA	2.4			V
TDI, TMS Pullup Resistors	R _{PU}	Pullup to DBP	40	50	60	kΩ
I/O Capacitance	C _{I/O}			5		pF
TCK Clock Period	t ₁				1000	ns
TCK High/Low Time	t _{2, t3}		50	500		ns
TCK to TMS, TDI Setup Time	t ₄		15			ns
TCK to TMS, TDI Hold Time	t ₅		10			ns
TCK to TDO Delay	t ₆				500	ns
TCK to TDO High-Z Delay	t ₇				500	ns

Note 1: Specifications are guaranteed for the stated global conditions, unless otherwise noted. 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.

Note 2: For V_{CC} of 3.6V or lower, connect V_{CC}, DBP, and ABP together. For higher supply applications, connect only V_{CC} to the supply rail.

Note 3: Applies to RESET, fault, autoretry, sequence delays, and watchdog timeout.

Note 4: Total unadjusted error is a combination of gain, offset, and quantization error.

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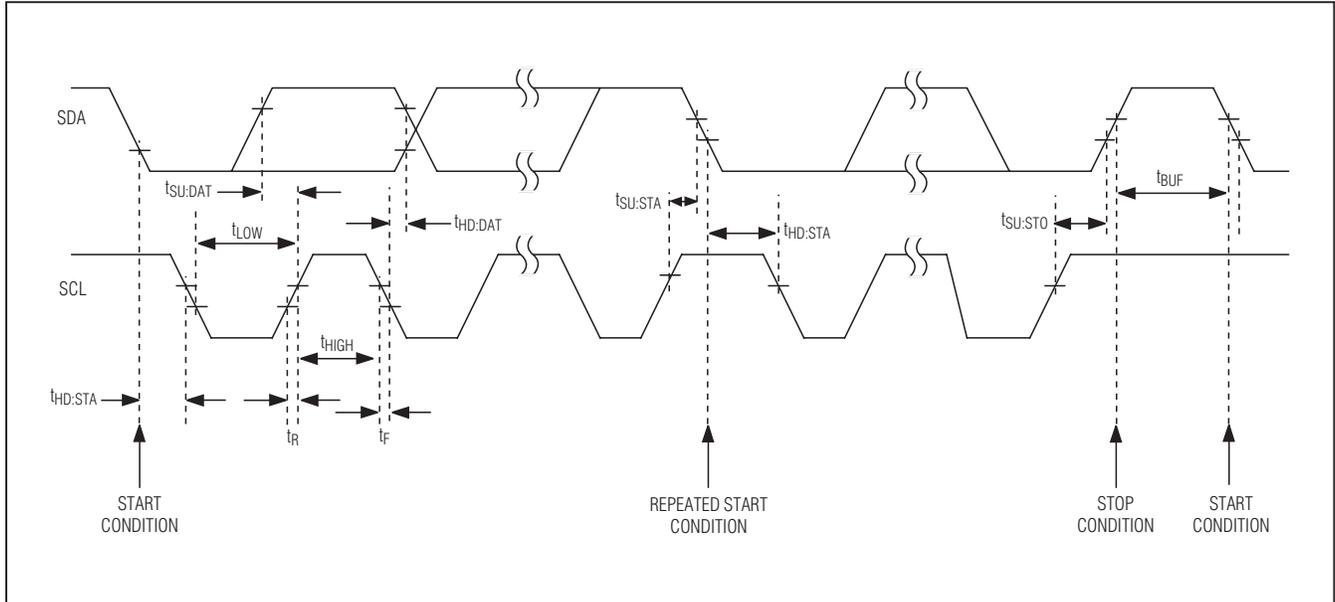


Figure 1. SMBus Timing Diagram

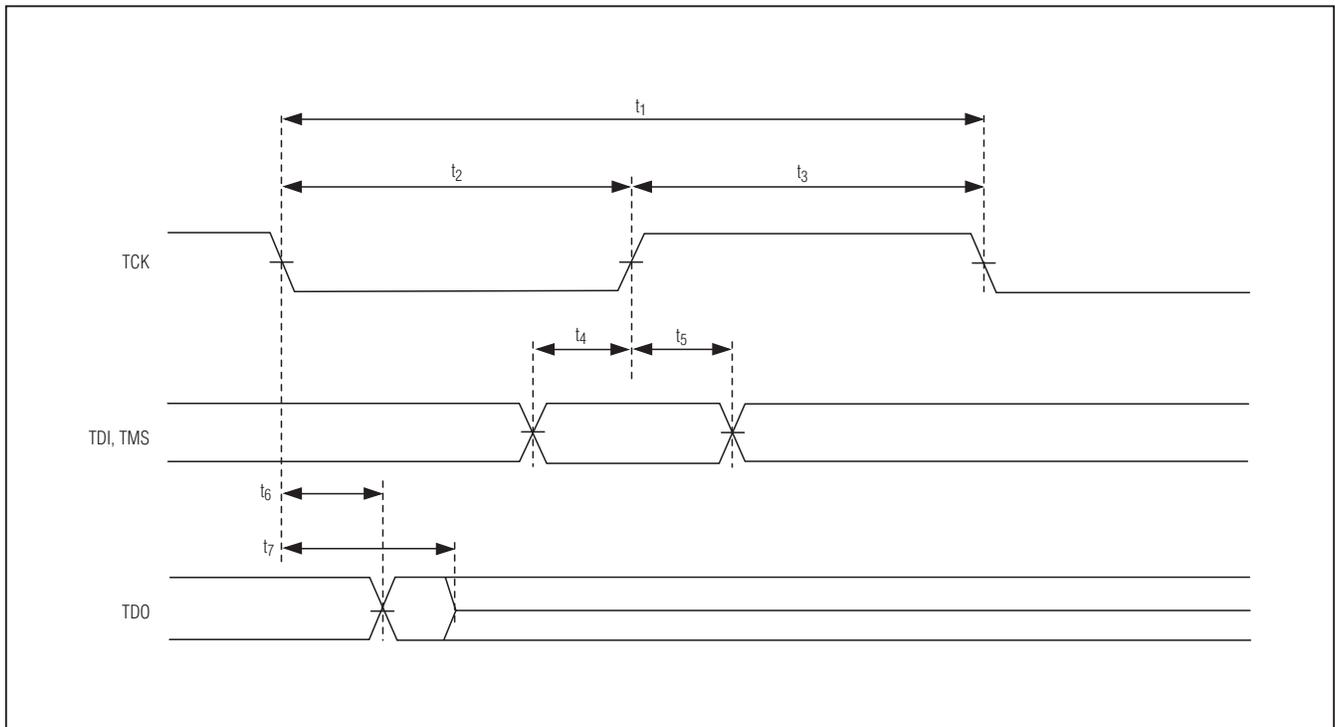


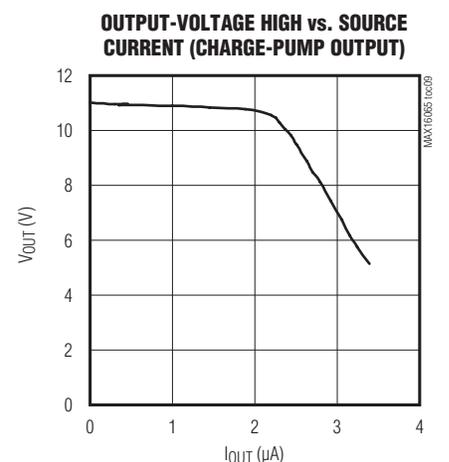
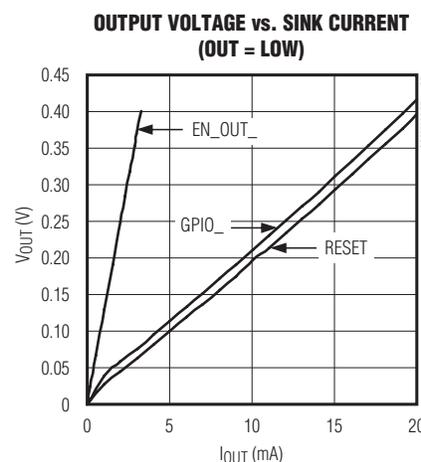
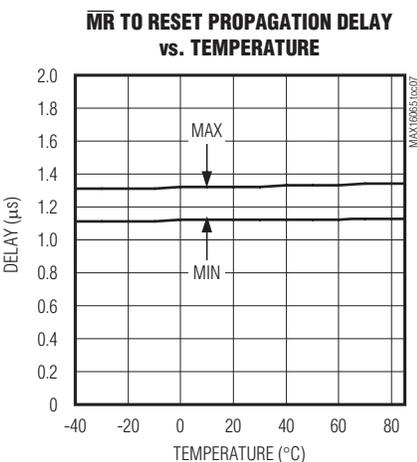
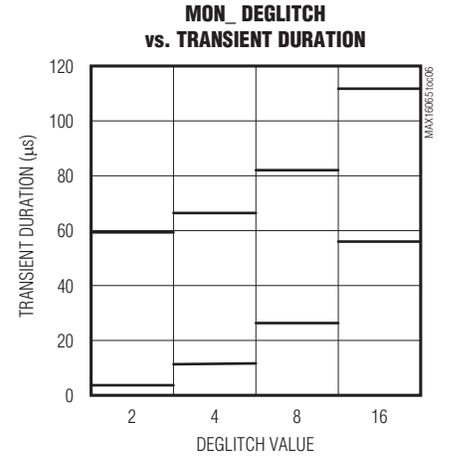
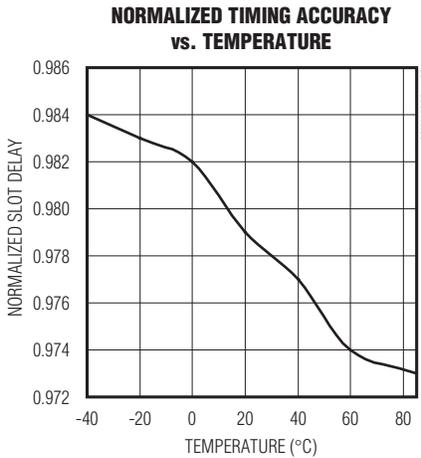
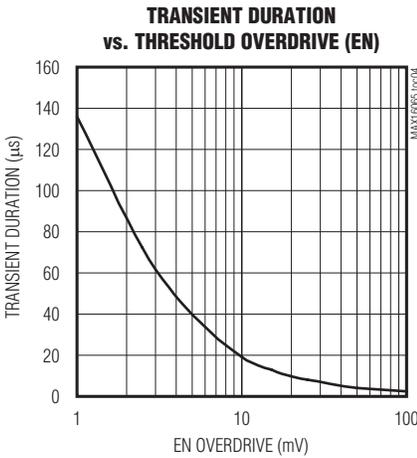
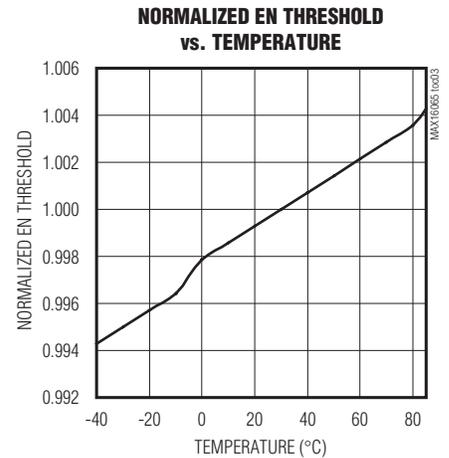
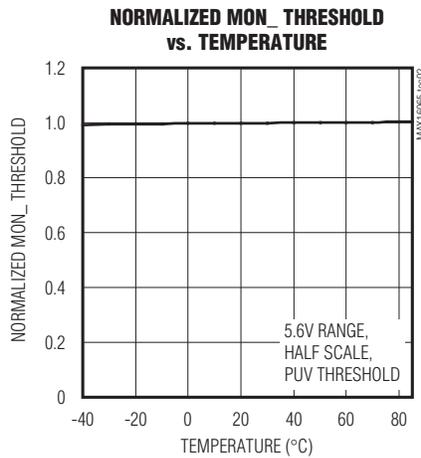
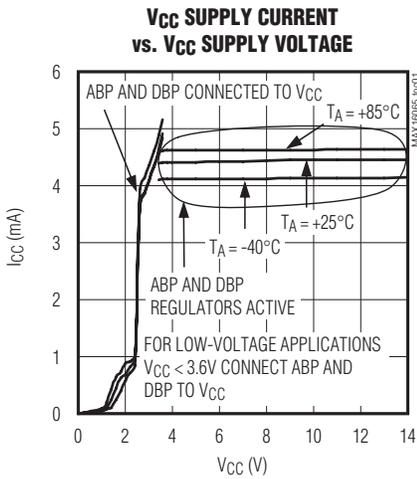
Figure 2. JTAG Timing Diagram

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Typical Operating Characteristics

(Typical values are at $V_{CC} = 3.3V$, $T_A = +25^\circ C$, unless otherwise noted.)



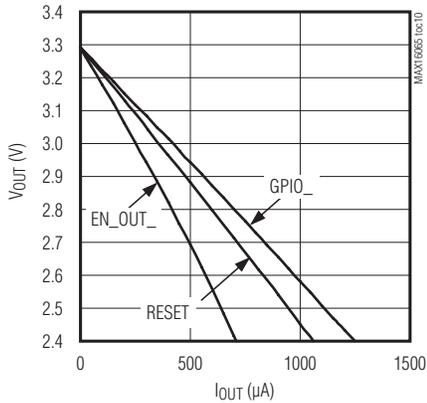
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12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

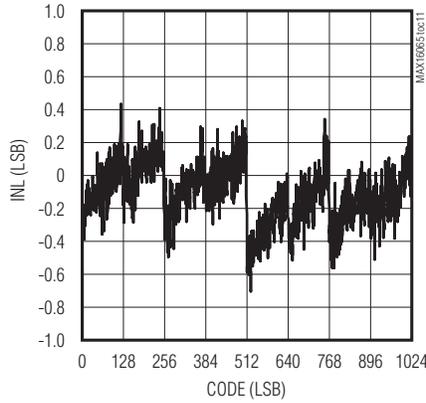
Typical Operating Characteristics (continued)

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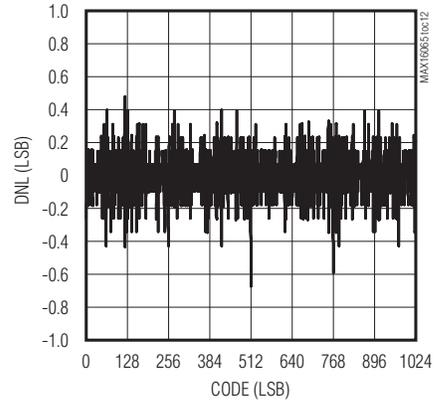
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (PUSH-PULL OUTPUT)



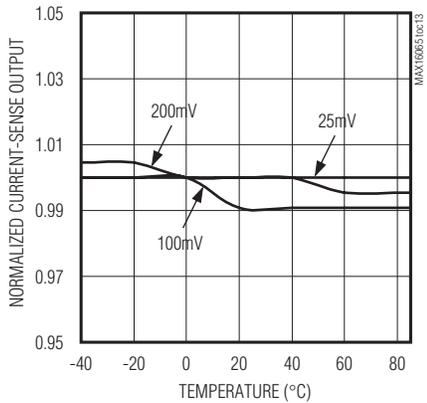
INTEGRAL NONLINEARITY vs. CODE



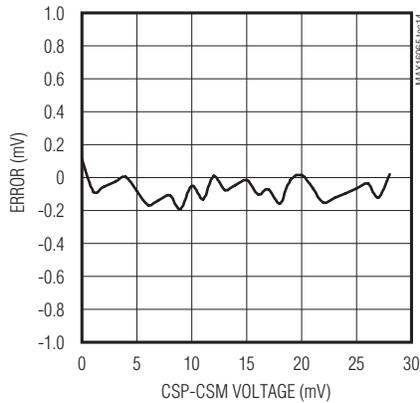
DIFFERENTIAL NONLINEARITY vs. CODE



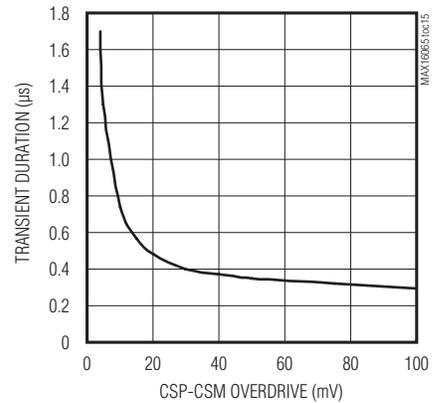
NORMALIZED CURRENT-SENSE ACCURACY vs. TEMPERATURE



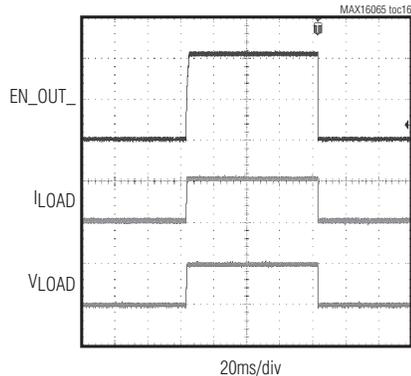
CURRENT-SENSE ACCURACY vs. CSP-CSM VOLTAGE



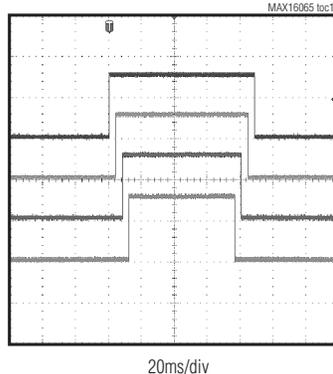
CURRENT-SENSE TRANSIENT DURATION vs. CSP-CSM OVERDRIVE



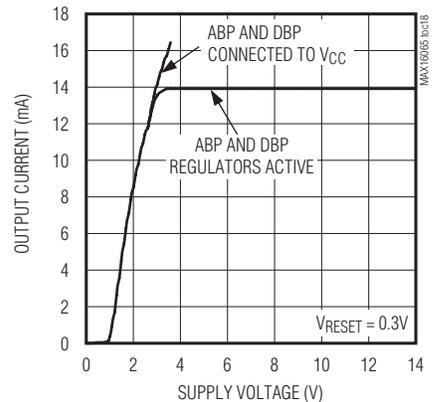
FET TURN-ON WITH CHARGE PUMP



SEQUENCING MODE



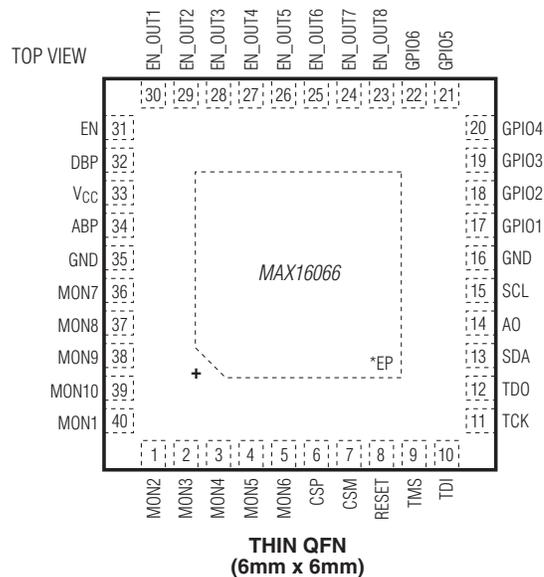
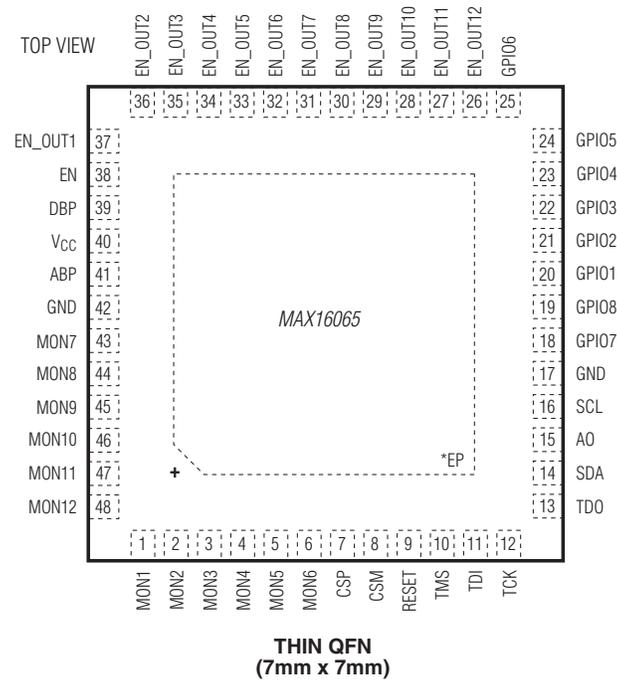
RESET OUTPUT CURRENT vs. SUPPLY VOLTAGE



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Pin Configurations



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12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

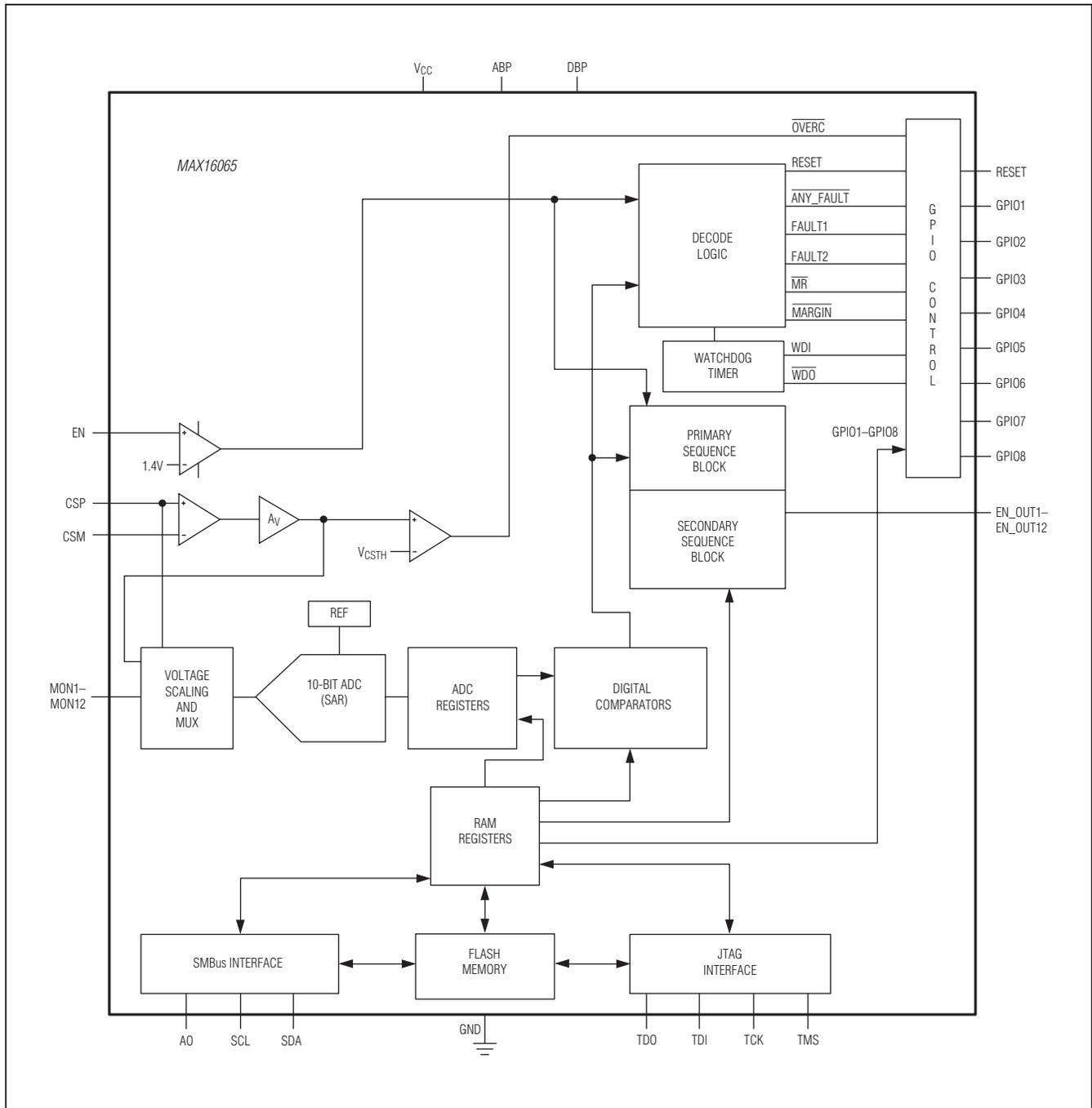
Pin Description

PIN		NAME	FUNCTION
MAX16065	MAX16066		
1–6, 43–46	40, 1–5, 36–39	MON1–MON10	Monitor Voltage Inputs. Set monitor voltage range through configuration registers. Measured value written to ADC register can be read back through the SMBus or JTAG interface.
47, 48	—	MON11, MON12	Monitor Voltage Inputs. Set monitor voltage range through configuration registers. Measured value written to ADC register can be read back through the SMBus or JTAG interface.
7	6	CSP	Current-Sense Amplifier Positive Input. Connect CSP to the source side of the external sense resistor.
8	7	CSM	Current-Sense Amplifier Negative Input. Connect CSM to the load side of the external sense resistor.
9	8	RESET	Configurable Reset Output
10	9	TMS	JTAG Test Mode Select
11	10	TDI	JTAG Test Data Input
12	11	TCK	JTAG Test Clock
13	12	TDO	JTAG Test Data Output
14	13	SDA	SMBus Serial-Data Open-Drain Input/Output
15	14	A0	Four-State SMBus Address. Address sampled upon POR.
16	15	SCL	SMBus Serial-Clock Input
17, 42	16, 35	GND	Ground
20–25	17–22	GPIO1–GPIO6	General-Purpose Input/Outputs. GPIO_s can be configured to act as a TTL input, a push-pull, open-drain, or high-impedance output or a pulldown circuit during a fault event.
18, 19	—	GPIO7, GPIO8	General-Purpose Input/Outputs. GPIO_s can be configured to act as a TTL input, a push-pull, open-drain, or high-impedance output or a pulldown circuit during a fault event or reverse sequencing.
26–29	—	EN_OUT12–EN_OUT9	Outputs. Set EN_OUT_ with active-high/active-low logic and with push-pull or open-drain configuration. EN_OUT_ can be asserted by a combination of IN_ voltages configurable through the flash.
30–37	23–30	EN_OUT8–EN_OUT1	Outputs. Set EN_OUT_ with active-high/active-low logic and with push-pull or open-drain configuration. EN_OUT_ can be asserted by a combination of IN_ voltages configurable through the flash. EN_OUT1–EN_OUT8 can be configured with a charge-pump output (+10V above GND) that can drive an external n-channel MOSFET.
38	31	EN	Analog Enable Input. All outputs deassert when VEN is below the enable threshold.
39	32	DBP	Digital Bypass. All push-pull outputs are referenced to DBP. Bypass DBP with a 1µF capacitor to GND.
40	33	VCC	Device Power Supply. Connect VCC to a voltage from 2.8V to 14V. Bypass VCC with a 10µF capacitor to GND.
41	34	ABP	Analog Bypass. Bypass ABP with a 1µF ceramic capacitor to GND.
—	—	EP	Exposed Pad. Internally connected to GND. Connect to ground, but do not use as the main ground connection.

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Functional Diagram



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12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

Detailed Description

The MAX16065 manages up to twelve system power supplies and the MAX16066 can manage up to eight system power supplies. After boot-up, if EN is high and the software enable bit is set to '1,' a power-up sequence begins based on the configuration stored in flash and the EN_OUT_s are controlled accordingly. When the power-up sequence is successfully completed, the monitoring phase begins. An internal multiplexer cycles through each MON_ input. At each multiplexer stop, the 10-bit ADC converts the monitored analog voltage to a digital result and stores the result in a register. Each time a conversion cycle (50µs, max) completes, internal logic circuitry compares the conversion results to the over-voltage and undervoltage thresholds stored in memory. When a result violates a programmed threshold, the conversion can be configured to generate a fault. GPIO_ can be programmed to assert on combinations of faults. Additionally, faults can be configured to shut off the system and trigger the nonvolatile fault logger, which writes all fault information automatically to the flash and write-protects the data to prevent accidental erasure.

The MAX16065/MAX16066 contain both SMBus and JTAG serial interfaces for accessing registers and flash. Use only one interface at any given time. For more information on how to access the internal memory through these interfaces, see the *SMBus-Compatible Interface* and *JTAG Serial Interface* sections. The memory map is divided into three pages with access controlled by special SMBus and JTAG commands.

The factory-default values at POR (power-on reset) for all RAM registers are '0's. POR occurs when VCC reaches the undervoltage-lockout threshold (UVLO) of 2.8V (max). At POR, the device begins a boot-up sequence. During the boot-up sequence, all monitored inputs are masked from initiating faults and flash contents are copied to the respective register locations. During boot-up, the MAX16065/MAX16066 are not accessible through the serial interface. The boot-up sequence takes up to 350µs, after which the device is ready for normal operation. RESET is asserted low up to the boot-up phase and remains asserted for its programmed timeout period once sequencing is completed and all monitored channels are within their respective thresholds. Up to the boot-up phase, the GPIO_s and EN_OUT_s are high impedance.

Power

Apply 2.8V to 14V to VCC to power the MAX16065/MAX16066. Bypass VCC to ground with a 10µF capacitor. Two internal voltage regulators, ABP and DBP, supply power to the analog and digital circuitry within the device. For operation at 3.6V or lower, disable the regulators by connecting ABP and DBP to VCC.

ABP is a 3.0V (typ) voltage regulator that powers the internal analog circuitry. Bypass ABP to GND with a 1µF ceramic capacitor installed as close to the device as possible.

DBP is an internal 3.0V (typ) voltage regulator. DBP powers flash and digital circuitry. All push-pull outputs refer to DBP. DBP supplies the input voltage to the internal charge pump when the programmable outputs are configured as charge-pump outputs. Bypass the DBP output to GND with a 1µF ceramic capacitor installed as close as possible to the device.

Do not power external circuitry from ABP or DBP.

Sequencing

To sequence a system of power supplies safely, the output voltage of a power supply must be good before the next power supply may turn on. Connect EN_OUT_ outputs to the enable input of an external power supply and connect MON_ inputs to the output of the power supply for voltage monitoring. More than one MON_ can be used if the power supply has multiple outputs.

Sequence Order

The MAX16065/MAX16066 provide a system of ordered slots to sequence multiple power supplies. To determine the sequence order, assign each EN_OUT_ to a slot ranging from Slot 1 to Slot 12. EN_OUT_(s) assigned to Slot 1 are turned on first, followed by outputs assigned to Slot 2, and so on through Slot 12. Multiple EN_OUT_s assigned to the same slot turn on at the same time.

Each slot includes a built-in configurable sequence delay (registers r77h to r7Dh) ranging from 20µs to 1.6s. During a reverse sequence, slots are turned off in reverse order starting from Slot 12. The MAX16065/MAX16066 can be configured to power-down in simultaneous mode or in reverse sequence mode as set in r75h[0]. See Tables 5 and 6 for the EN_OUT_ slot assignment bits, and Tables 3 and 4 for the sequence delays.

During power-up or power-down sequencing, the current sequencer state can be found in r21h[4:0].

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Table 1. Current Sequencer Slot

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
21h	[4:0]	Current Sequencer State: 00000 = Slot 0 00001 = Slot 1 00010 = Slot 2 00011 = Slot 3 00100 = Slot 4 00101 = Slot 5 00110 = Slot 6 00111 = Slot 7 01000 = Slot 8 01001 = Slot 9 01010 = Slot 10 01011 = Slot 11 01100 = Slot 12 01101 = Secondary sequence monitoring mode 01110 = Primary sequence fault 01111 = Primary sequence monitoring mode 10000 = Secondary sequence fault 10001 to 11111 = Reserved
	[7:5]	Reserved

Multiple Sequencing Groups

The MAX16065/MAX16066 sequencing slots can be split into two groups: the primary sequence and the secondary sequence. The last slot of the primary sequence is selected using register bits r7Dh[7:4]. The secondary sequence begins at the slot after the one specified in register bits r7Dh[7:4]. The primary sequence is controlled by the EN input and the software enable bit in r73h[0]. Outputs assigned to slots in the primary sequence turn on, and monitoring begins for inputs assigned to these slots. RESET deasserts after the primary sequence and timeout period completes.

To initiate secondary sequencing and monitoring, set the software enable r73h[1] bit to 1. Additionally, if GPIO₁ is configured as EN2 then both the software enable 2 and EN2 must be high. Outputs assigned to slots in the secondary sequence turn on, and monitoring begins for inputs assigned to these slots. If a GPIO₁ is configured as the RESET2 output, it deasserts after the secondary sequence and timeout period completes.

If a critical fault occurs in the primary sequence group, both sequence groups automatically shut down. If a critical fault occurs in the secondary sequence group, then just the outputs assigned to slots in the secondary sequence turn off. The failing slot in secondary sequence is stored in r1Dh.

Multiple sequencing groups can be used to conserve power by powering down secondary systems when not in use.

Enable and Enable2

To initiate sequencing/tracking and enable monitoring, the voltage at EN must be above 1.4V and the software enable bit in r73h[0] must be set to '1.' To power down and disable monitoring, either pull EN below 1.35V or set the Software Enable bit to '0.' See Table 2 for the software enable bit configurations. Connect EN to ABP if not used.

If a fault condition occurs during the power-up cycle, the EN_OUT₁ outputs are powered down immediately, regardless of the state of EN. In the monitoring state, if EN falls below the threshold, the sequencing state machine begins the power-down sequence. If EN rises above the threshold during the power-down sequence, the sequence state machine continues the power-down sequence until all the channels are powered off and then the device immediately begins the power-up sequence. When in the monitoring state, a register bit, ENRESET, is set to a '1' when EN falls below the undervoltage threshold. This register bit latches and must be cleared through software. This bit indicates if RESET asserted low due to EN going under the threshold. The POR state of ENRESET is '0'. The bit is only set on a falling edge

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of the EN comparator output or the software enable bit. If operating in latch-on fault mode, toggle EN or toggle the Software Enable bit to clear the latch condition and restart the device once the fault condition has been removed.

To initiate secondary sequencing and monitoring set the software enable r73h[1] bit to 1. Additionally, if GPIO_ is configured as EN2 then both the software enable 2 bit and EN2 must be high. To power-down and disable monitoring, either drive EN2 low or set the Software Enable2 bit to '0.' See Table 2 for the software enable bit configurations.

When a fault condition occurs during the power-up cycle, the EN_OUT_ outputs are powered down immediately, independent of the state of EN2. Drive EN2 low to begin the secondary power-down sequence. When EN2 is

driven high during the power-down sequence, the sequence state machine continues the power-down sequence until the secondary channels are powered off and then the device immediately begins the power-up sequence.

Monitoring Inputs While Sequencing

An enabled MON_ input can be assigned to a slot ranging from Slot 1 to Slot 12. EN_OUT_s are always asserted at the beginning of a slot. The supply voltages connected to the MON_ inputs must exceed the undervoltage threshold before the programmed timeout period expires otherwise a fault condition will occur. The undervoltage threshold checking cannot be disabled during power-up and power-down. See Tables 5 and 6 for the MON_ slot assignment bits. The programmed

Table 2. Software Enable Configurations

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
73h	273h	[0]	Software enable 1 (primary sequence)
		[1]	Software enable 2 (secondary sequence)
		[2]	1 = Margin mode enabled
		[3]	Early warning threshold select 0 = Early warning is undervoltage 1 = Early warning is overvoltage
		[4]	Independent watchdog mode enable 1 = Watchdog timer is independent of sequencer 0 = Watchdog timer boots after sequence completes

Table 3. Slot Delay Register

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
77h	277h	[3:0]	Sequence Slot 0 Delay
		[7:4]	Sequence Slot 1 Delay
78h	278h	[3:0]	Sequence Slot 2 Delay
		[7:4]	Sequence Slot 3 Delay
79h	279h	[3:0]	Sequence Slot 4 Delay
		[7:4]	Sequence Slot 5 Delay
7Ah	27Ah	[3:0]	Sequence Slot 6 Delay
		[7:4]	Sequence Slot 7 Delay
7Bh	27Bh	[3:0]	Sequence Slot 8 Delay
		[7:4]	Sequence Slot 9 Delay
7Ch	27Ch	[3:0]	Sequence Slot 10 Delay
		[7:4]	Sequence Slot 11 Delay
7Dh	27Dh	[3:0]	Sequence Slot 12 Delay
		[7:4]	Grouped Sequence Split Location, Final Slot of Primary Sequence

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Table 4. Power-Up/Power-Down Slot Delays

CODE	VALUE
0000	25µs
0001	500µs
0010	1ms
0011	2ms
0100	3ms
0101	4ms
0110	6ms
0111	8ms
1000	10ms
1001	12ms
1010	25ms
1011	100ms
1100	200ms
1101	400ms
1110	800ms
1111	1.6s

sequence delay is then counted before moving to the next slot.

Slot 0 does not monitor any MON_ input and does not control any EN_OUT_. Slot 0 waits for the Software Enable bit r73h[0] to be a logic-high and for the voltage on EN to rise above 1.4V before initiating the power-up sequence and counting its own sequence delay.

Any MON_ input that suffers a fault that occurs during power-up sequencing causes all the EN_OUT_s to turn off and the sequencer to shut down regardless of the state of the critical fault enables (see the *Faults* section for more information). If a MON_ input is less critical to system operation, it can be configured as “monitoring only” (see Table 6) for either the primary or secondary sequence. Monitoring for MON_ inputs assigned as “monitoring only” begins after sequencing is complete for that group, and can trigger a critical fault only if specifically configured to do so using the critical fault enables.

Power-Up

On power-up, when EN is high and the Software Enable bit is 1, the MAX16065/MAX16066 begin sequencing with Slot 0. After the sequencing delay for Slot 0 expires, the sequencer advances to Slot 1, and all EN_OUT_s assigned to the slot assert. All MON_ inputs assigned to Slot 1 are monitored and when the voltage rises above the UV fault threshold, the sequence delay counter is started.

When the tFAULT counter expires before all MON_ inputs assigned to the slot are above the fault UV threshold, a fault asserts. EN_OUT_ outputs are disabled and the MAX16065/MAX16066 return to the power-off state. When the sequence delay expires, the MAX16065/MAX16066 proceed to the next slot.

After the voltages on all MON_ inputs assigned to the last slot exceed the UV fault threshold and the slot delay expires, the MAX16065/MAX16066 start the reset timeout counter. After the reset timeout, RESET deasserts. r75h[4:1] sets the tFAULT delay. See Table 7 for details.

Power-Down

Power-down starts when EN is pulled low or the Software Enable bit is set to '0.' Power down EN_OUT_s simultaneously or in reverse-sequence mode by setting the Reverse Sequence bit (r75h[0]) appropriately.

Reverse-Sequence Mode

When the MAX16065/MAX16066 are fully powered up (including secondary sequence group, if enabled) and EN or the Software Enable bit is set to '0', the EN_OUT_s assigned to Slot 12 deassert, the MAX16065/MAX16066 wait for the Slot 12 sequence delay and then proceed to the previous slot (Slot 11), and so on until the EN_OUT_s assigned to Slot 1 turn off. When simultaneous power-down is selected (r75h[0] set to '0'), all EN_OUT_s turn off at the same time.

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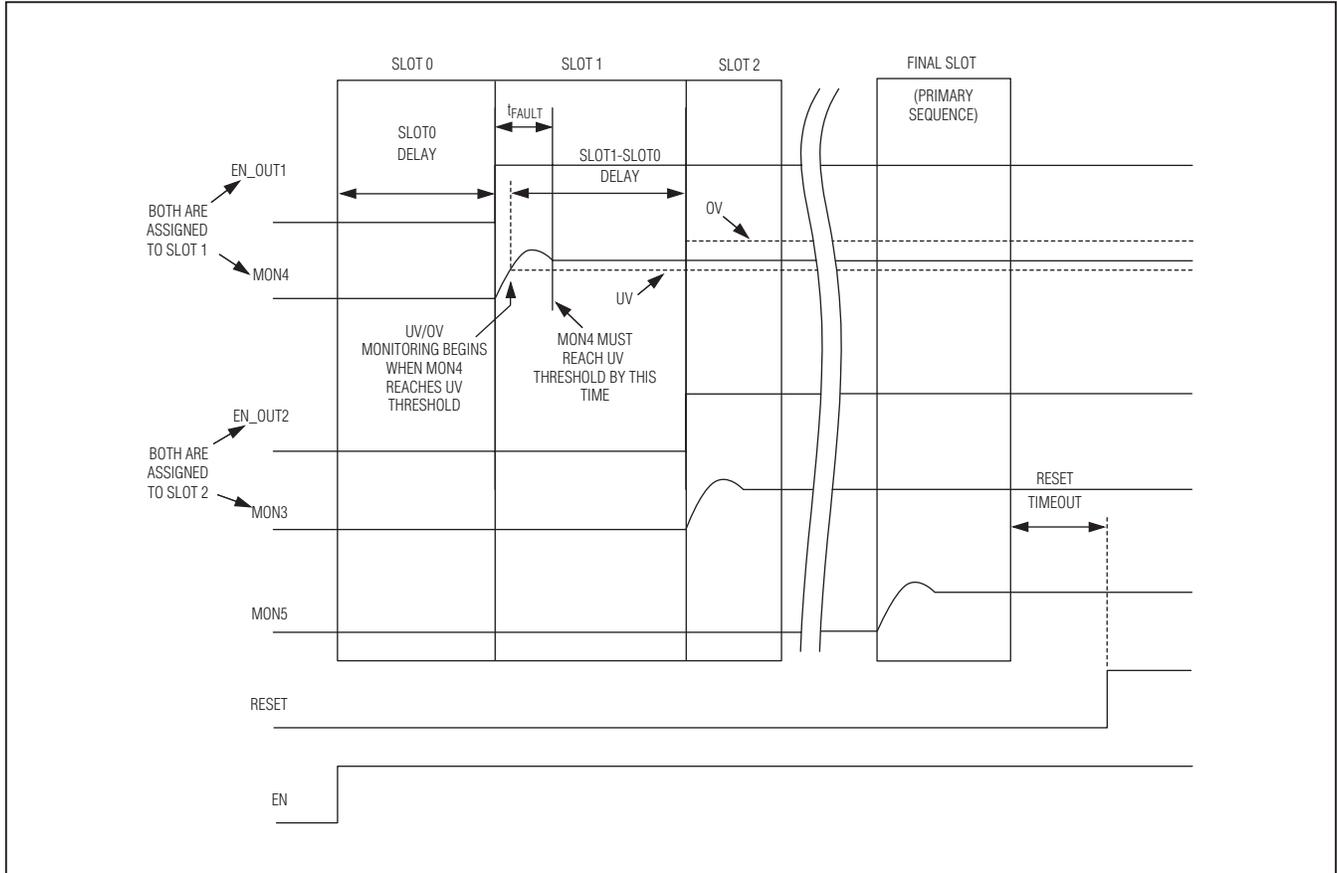


Figure 3. Delay and Reset Timing

Table 5. MON_ and EN_OUT_ Assignment Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
7Eh	27Eh	[3:0]	MON1
		[7:4]	MON2
7Fh	27Fh	[3:0]	MON3
		[7:4]	MON4
80h	280h	[3:0]	MON5
		[7:4]	MON6
81h	281h	[3:0]	MON7
		[7:4]	MON8
82h	282h	[3:0]	MON9
		[7:4]	MON10
83h	283h	[3:0]	MON11
		[7:4]	MON12

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Table 5. MON_ and EN_OUT_ Assignment Registers (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
84h	284h	[3:0]	EN_OUT1
		[7:4]	EN_OUT2
85h	285h	[3:0]	EN_OUT3
		[7:4]	EN_OUT4
86h	286h	[3:0]	EN_OUT5
		[7:4]	EN_OUT6
87h	287h	[3:0]	EN_OUT7
		[7:4]	EN_OUT8
88h	288h	[3:0]	EN_OUT9
		[7:4]	EN_OUT10
89h	289h	[3:0]	EN_OUT11
		[7:4]	EN_OUT12

Table 6. MON_ and EN_OUT_ Slot Assignment Codes

SLOT ASSIGNMENT		
CODE	MON_ DESCRIPTION	EN_OUT_ DESCRIPTION
0000	Not assigned	Not assigned
0001	Slot 1	Slot 1
0010	Slot 2	Slot 2
0011	Slot 3	Slot 3
0100	Slot 4	Slot 4
0101	Slot 5	Slot 5
0110	Slot 6	Slot 6
0111	Slot 7	Slot 7
1000	Slot 8	Slot 8
1001	Slot 9	Slot 9
1010	Slot 10	Slot 10
1011	Slot 11	Slot 11
1100	Slot 12	Slot 12
1101	Monitoring only, secondary sequence	General-purpose input (EN_OUT9–EN_OUT12 only)
1110	Monitoring only, primary sequence	General-purpose output (EN_OUT9–EN_OUT12 only)
1111	Not assigned	Not assigned

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Table 7. t_{FAULT} Delay Settings

CODE	DELAY
0000	120µs
0001	150µs
0010	250µs
0011	380µs
0100	600µs
0101	1ms
0110	1.5ms
0111	2.5ms
1000	4ms
1001	6ms
1010	10ms
1011	15ms
1100	25ms
1101	40ms
1110	60ms
1111	100ms

When the secondary sequence group is already powered down and EN or the Software Enable bit is set to '0', the reverse power-down sequence is similar to above, but starts from the last slot assigned to the primary sequence r7Dh[7:4]. After the last assigned slot is powered down the previous slot will power down and so on until Slot 0 is powered down.

To power down the secondary sequence group, drive EN2 low or set r75h[1] to '0'. The secondary reverse power-down sequence will start at Slot 12 and end at the primary sequence monitoring mode state at which point only the slots assigned to the primary sequence are active.

Voltage/Current Monitoring

The MAX16065/MAX16066 feature an internal 10-bit ADC that monitors the MON_ voltage inputs. An internal multiplexer cycles through each of the enabled inputs, taking less than 40µs for a complete monitoring cycle. Each acquisition takes approximately 3.2µs. At each multiplexer stop, the 10-bit ADC converts the analog input to a digital result and stores the result in a register. ADC conversion results are stored in registers r00h to r1Ah (see Table 10). Use the SMBus or JTAG serial interface to read ADC conversion results.

The MAX16065 provides twelve inputs, MON1–MON12, for voltage monitoring. The MAX16066 provides eight inputs, MON1–MON8, for voltage monitoring. Each input

voltage range is programmable in registers r43h to r45h (see Table 9). When MON_ configuration registers are set to '11,' MON_ voltages are not monitored, and the multiplexer does not stop at these inputs, decreasing the total cycle time. These inputs cannot be configured to trigger fault conditions.

The three programmable thresholds for each monitored voltage include an overvoltage, an undervoltage, and a secondary warning threshold that can be set in r73h[3] to be either an undervoltage or overvoltage threshold. See the *Faults* section for more information on setting overvoltage and undervoltage thresholds. All voltage thresholds are 8 bits wide. The 8 MSBs of the 10-bit ADC conversion result are compared to these overvoltage and undervoltage thresholds.

For any undervoltage or overvoltage condition to be monitored and any faults detected, the MON_ input must be assigned to a sequence order or set to monitoring mode as described in the *Sequencing* section.

Inputs that are not enabled are not converted by the ADC; they contain the last value acquired before that channel was disabled.

The ADC conversion result registers are reset to 00h at boot-up. These registers are not reset when a reboot command is executed.

Configure the MAX16065/MAX16066 for differential mode in r46h (Table 9). The possible differential

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pairs are MON1/MON2, MON3/MON4, MON5/MON6, MON7/MON8 with the first input always being at a higher voltage than the second. Use differential voltage sensing to eliminate voltage offsets or measure supply current. See Figure 4. In differential mode, the odd-numbered MON_ input measures the absolute voltage with respect to GND while the result of the even input is the difference between the odd and even inputs. See Figure 4 for the typical differential measurement circuit.

Internal Current-Sense Amplifier

The current-sense inputs, CSP/CSM, and a current-sense amplifier facilitate power monitoring (see Figure 5). The voltage on CSP relative to GND is also monitored by the ADC when the current-sense amplifier is enabled with r47h[0]. The conversion results are located in registers r19h and r1Ah (see Table 10). There are two selectable voltage ranges for CSP set by r47h[1], see Table 8. Although the voltage can be monitored over SMBus or JTAG, this voltage has no threshold comparators and cannot trigger any faults. Regarding the current-sense amplifier, there are four selectable ranges and the ADC output for a current-sense conversion is:

$$X_{ADC} = (V_{SENSE} \times A_v) / 1.4V \times (2^8 - 1)$$

where X_{ADC} is the 8-bit decimal ADC result in register r18h, V_{SENSE} is $V_{CSP} - V_{CSM}$, and A_v is the current-sense voltage gain set by r47h[3:2].

In addition, there are two programmable current-sense trip thresholds: primary overcurrent and secondary overcurrent. For fast fault detection, the primary overcurrent threshold is implemented with an analog comparator connected to the internal \overline{OVERC} signal. The \overline{OVERC} signal can be output on one of the GPIO_s. See the *General-Purpose Inputs/Outputs* section for configuring the GPIO_ to output the \overline{OVERC} signal. The primary threshold is set by:

$$I_{TH} = V_{CSTH} / R_{SENSE}$$

where I_{TH} is the current threshold to be set, V_{CSTH} is the threshold set by r47h[3:2], and R_{SENSE} is the value of the sense resistor. See Table 8 for a description of r47h. \overline{OVERC} depends only on the primary overcurrent threshold. The secondary overcurrent threshold is implemented through ADC conversions and digital comparison set by r6Ch. The secondary overcurrent threshold includes programmable time delay options located in r73h[6:5]. Primary and secondary current-sense faults are enabled/disabled through r47h[0].

General-Purpose Inputs/Outputs

GPIO1–GPIO8 are programmable general-purpose inputs/outputs. GPIO1–GPIO8 are configurable as a manual reset input, a watchdog timer input and output, logic inputs/outputs, fault-dependent outputs. When programmed as outputs, GPIO_s are open drain or push-pull. See Tables 12 and 13 for more detailed information on configuring GPIO1–GPIO8.

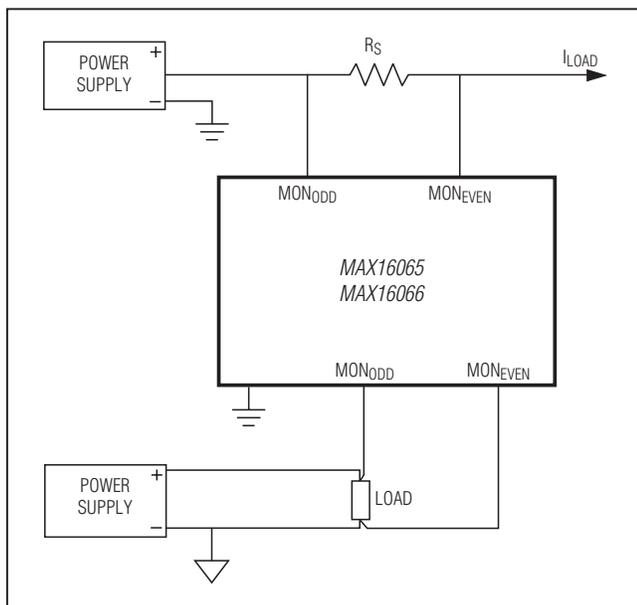


Figure 4. Differential Measurement Connections

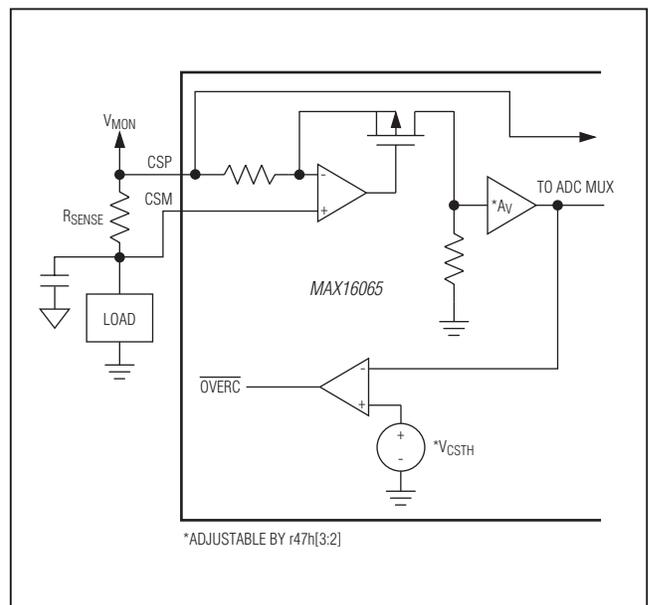


Figure 5. Current-Sense Amplifier

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Table 8. Overcurrent Primary Threshold and Current-Sense Control

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
47h	247h	[0]	1 = Current sense is enabled 0 = Current sense is disabled
		[1]	1 = CSP full-scale range is 14V 0 = CSP full-scale range is 7V
		[3:2]	Overcurrent Primary Threshold and Current-Sense Gain Setting: 00 = 200mV threshold, $A_V = 6V/V$ 01 = 100mV threshold, $A_V = 12V/V$ 10 = 50mV threshold, $A_V = 24V/V$ 11 = 25mV threshold, $A_V = 48V/V$
73h	273h	[6:5]	Overcurrent Secondary Threshold Deglitch: 00 = No delay 01 = 4ms 10 = 15ms 11 = 60ms

Table 9. ADC Configuration Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
43h	243h	[1:0]	ADC1 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	ADC2 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[5:4]	ADC3 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:6]	ADC4 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted

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Table 9. ADC Configuration Registers (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
44h	244h	[1:0]	ADC5 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	ADC6 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[5:4]	ADC7 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:6]	ADC8 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
45h	245h	[1:0]	ADC9 Full-Scale Range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	ADC10 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[5:4]	ADC11 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:6]	ADC12 Full-Scale Range: 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted

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Table 9. ADC Configuration Registers (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
46h	246h	[0]	Differential Conversion ADC1–ADC2: 0 = Disabled 1 = Enabled
		[1]	Differential Conversion ADC3–ADC4: 0 = Disabled 1 = Enabled
		[2]	Differential Conversion ADC5–ADC6: 0 = Disabled 1 = Enabled
		[3]	Differential Conversion ADC7–ADC8: 0 = Disabled 1 = Enabled

Table 10. ADC Conversion Results (Read Only)

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
00h	[7:0]	ADC1 result (MSB) bits 9–2
01h	[7:6]	ADC1 result (LSB) bits 1–0
02h	[7:0]	ADC2 result (MSB) bits 9–2
03h	[7:6]	ADC2 result (LSB) bits 1–0
04h	[7:0]	ADC3 result (MSB) bits 9–2
05h	[7:6]	ADC3 result (LSB) bits 1–0
06h	[7:0]	ADC4 result (MSB) bits 9–2
07h	[7:6]	ADC4 result (LSB) bits 1–0
08h	[7:0]	ADC5 result (MSB) bits 9–2
09h	[7:6]	ADC5 result (LSB) bits 1–0
0Ah	[7:0]	ADC6 result (MSB) bits 9–2
0Bh	[7:6]	ADC6 result (LSB) bits 1–0
0Ch	[7:0]	ADC7 result (MSB) bits 9–2
0Dh	[7:6]	ADC7 result (LSB) bits 1–0
0Eh	[7:0]	ADC8 result (MSB) bits 9–2
0Fh	[7:6]	ADC8 result (LSB) bits 1–0
10h	[7:0]	ADC9 result (MSB) bits 9–2
11h	[7:6]	ADC9 result (LSB) bits 1–0
12h	[7:0]	ADC10 result (MSB) bits 9–2
13h	[7:6]	ADC10 result (LSB) bits 1–0
14h	[7:0]	ADC11 result (MSB) bits 9–2
15h	[7:6]	ADC11 result (LSB) bits 1–0
16h	[7:0]	ADC12 result (MSB) bits 9–2
17h	[7:6]	ADC12 result (LSB) bits 1–0
18h	[7:0]	Current-sense ADC result
19h	[7:0]	CSP ADC output (MSB) bits 9–2
1Ah	[7:6]	CSP ADC output (LSB) bits 1–0

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When GPIO1–GPIO8 are configured as general-purpose inputs/outputs, read values from the GPIO_ ports through r1Eh and write values to GPIO_s through r3Eh. Note that r3Eh has a corresponding flash register, which programs the default state of a general-purpose output. See Table 11 for more information on reading and writing to the GPIO_.

Fault1 and Fault2

GPIO1–GPIO8 are configurable as dedicated fault outputs, Fault1 or Fault2. Fault outputs can assert on one or more overvoltage, undervoltage, or early warning conditions for selected inputs, as well as the secondary overcurrent comparator. Fault1 and Fault2 dependencies are set using registers r36h to r3Ah. See Table 14. When a fault output depends on more than one MON_, the fault output asserts when one or more MON_ exceeds a programmed threshold voltage. These fault outputs act independently of the critical fault system, described in the *Critical Faults* section.

Table 11. GPIO_ State Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
1Eh	—	[0]	GPIO1 input state
		[1]	GPIO2 input state
		[2]	GPIO3 input state
		[3]	GPIO4 input state
		[4]	GPIO5 input state
		[5]	GPIO6 input state
		[6]	GPIO7 input state
		[7]	GPIO8 input state
3Eh	23Eh	[0]	GPIO1 output state
		[1]	GPIO2 output state
		[2]	GPIO3 output state
		[3]	GPIO4 output state
		[4]	GPIO5 output state
		[5]	GPIO6 output state
		[6]	GPIO7 output state
		[7]	GPIO8 output state

Table 12. GPIO_ Configuration Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
3Fh	23Fh	[2:0]	GPIO1 configuration
		[5:3]	GPIO2 configuration
		[7:6]	GPIO3 configuration (LSB)
40h	240h	[0]	GPIO3 configuration (MSB)
		[3:1]	GPIO4 configuration
		[6:4]	GPIO5 configuration
		[7]	GPIO6 configuration (LSB)
41h	241h	[1:0]	GPIO6 configuration (MSB)
		[4:2]	GPIO7 configuration
		[7:5]	GPIO8 configuration

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Table 12. GPIO_ Configuration Registers (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
42h	242h	[0]	Output Configuration for GPIO1: 0 = Push-pull 1 = Open drain
		[1]	Output Configuration for GPIO2: 0 = Push-pull 1 = Open drain
		[2]	Output Configuration for GPIO3: 0 = Push-pull 1 = Open drain
		[3]	Output Configuration for GPIO4: 0 = Push-pull 1 = Open drain
		[4]	Output Configuration for GPIO5: 0 = Push-pull 1 = Open drain
		[5]	Output Configuration for GPIO6: 0 = Push-pull 1 = Open drain
		[6]	Output Configuration for GPIO7: 0 = Push-pull 1 = Open drain
		[7]	Output Configuration for GPIO8: 0 = Push-pull 1 = Open drain

Table 13. GPIO_ Function Configuration Bits

	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7	GPIO8
000	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input
001	Logic output	Logic output	Logic output	Logic output	Logic output	Logic output	Logic output	Logic output
010	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output
011	Fault1 output	Fault1 output	$\overline{\text{FAULTPU}}$ output	Fault1 output	Fault1 output	Fault1 output	Fault1 output	$\overline{\text{FAULTPU}}$ output
100	$\overline{\text{ANY_FAULT}}$ output	RESET2 output	$\overline{\text{ANY_FAULT}}$ output	$\overline{\text{ANY_FAULT}}$ output	$\overline{\text{ANY_FAULT}}$ output	RESET2 output	$\overline{\text{ANY_FAULT}}$ output	RESET2 output
101	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output
110	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output
111	WDI input	—	—	$\overline{\text{EXTFAULT}}$ input/output	EN2 input	$\overline{\text{MARGIN}}$ input	EN2 input	$\overline{\text{EXTFAULT}}$ input/output

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ANY_FAULT

GPIO1, GPIO3, GPIO4, GPIO5, and GPIO7 are configurable to assert low during any fault condition. This includes power-up, power-down fault conditions as well as conditions where Fault1 or Fault2 assert.

Second Enable (EN2)

GPIO5 and GPIO7 are configurable as the enable input for the secondary sequence. See the *Multiple Sequencing Groups* section for more details.

Table 14. Fault1 and Fault2 Dependencies

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
36h	236h	0	1 = Fault1 depends on MON1
		1	1 = Fault1 depends on MON2
		2	1 = Fault1 depends on MON3
		3	1 = Fault1 depends on MON4
		4	1 = Fault1 depends on MON5
		5	1 = Fault1 depends on MON6
		6	1 = Fault1 depends on MON7
		7	1 = Fault1 depends on MON8
37h	237h	0	1 = Fault1 depends on MON9
		1	1 = Fault1 depends on MON10
		2	1 = Fault1 depends on MON11
		3	1 = Fault1 depends on MON12
		4	1 = Fault1 depends on the overvoltage thresholds of the inputs selected by r36h and r37h[3:0]
		5	1 = Fault1 depends on the undervoltage thresholds of the inputs selected by r36h and r37h[3:0]
		6	1 = Fault1 depends on the early warning thresholds of the inputs selected by r36h and r37h[3:0]
		7	0 = Fault1 is an active-low digital output 1 = Fault1 is an active-high digital output
38h	238h	[0]	1 = Fault2 depends on MON1
		[1]	1 = Fault2 depends on MON2
		[2]	1 = Fault2 depends on MON3
		[3]	1 = Fault2 depends on MON4
		[4]	1 = Fault2 depends on MON5
		[5]	1 = Fault2 depends on MON6
		[6]	1 = Fault2 depends on MON7
		[7]	1 = Fault2 depends on MON8