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19-5028; Rev 2; 6/10

MAXIM

6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

General Description

The MAX16067 flash-configurable system manager monitors and sequences multiple system voltages. The MAX16067 manages up to six system voltages simultaneously. The MAX16067 integrates an analog-to-digital converter (ADC) and configurable outputs for sequencing power supplies. Device configuration information, including overvoltage and undervoltage limits, time delay settings, and the sequencing order is stored in nonvolatile flash memory. During a fault condition, fault flags and channel voltages can be automatically stored in the nonvolatile flash memory for later readback.

The internal 1% accurate, 10-bit ADC measures each input and compares the result to one overvoltage and one undervoltage limit. A fault signal asserts when a monitored voltage falls outside the set limits.

The MAX16067 supports a power-supply voltage of up to 14V and can be powered directly from the 12V intermediate bus in many systems.

The integrated sequencer provides precise control over the power-up and power-down order of up to six power supplies. Three outputs (EN_OUT1 to EN_OUT3) are configurable with charge-pump outputs to directly drive external n-channel MOSFETs.

The MAX16067 includes six programmable general-purpose inputs/outputs (GPIOs). GPIOs are flash configurable as a fault output, as a watchdog input or output, or as a manual reset.

The MAX16067 features nonvolatile fault memory for recording information during system shutdown events. The fault logger records a failure in the internal flash and sets a lock bit protecting the stored fault data from accidental erasure.

An SMBus™ or a JTAG serial interface configures the MAX16067. The MAX16067 is available in a 32-pin, 5mm x 5mm, TQFN package and is fully specified over the -40°C to +85°C extended temperature range.

Features

- **Operates from 2.8V to 14V**
- **1% Accurate, 10-Bit ADC Monitors 6 Voltage Inputs**
- **Analog EN Monitoring Input**
- **6 Monitored Inputs with Overvoltage and Undervoltage Limits**
- **Nonvolatile Fault Event Logger**
- **Power-Up and Power-Down Sequencing Capability**
- **6 Outputs for Sequencing/Power-Good Indicators**
- **3 Configurable Charge-Pump Outputs**
- **Six General-Purpose Inputs/Outputs Configurable as:**
  - **Dedicated Fault Output**
  - **Watchdog Timer Function**
  - **Manual Reset**
  - **SMBus Alert**
  - **Fault Propagation Input/Output**
- **SMBus and JTAG Interface**
- **Supports Cascading with MAX16065/MAX16066**
- **Flash-Configurable Time Delays and Thresholds**
- **-40°C to +85°C Extended Operating Temperature Range**

Applications

Networking Equipment

Telecom Equipment (Base Stations, Access)

Storage/RAID Systems

Servers

Typical Operating Circuit appears at end of data sheet.

Ordering Information/Selector Guide

PART	PIN-PACKAGE	VOLTAGE-DETECTOR INPUTS	GENERAL-PURPOSE INPUTS/OUTPUTS	SEQUENCING OUTPUTS
MAX16067ETJ+	32 TQFN-EP*	6	6	6

Note: *This device is specified over the -40°C to +85°C extended temperature range.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

SMBus is a trademark of Intel Corp.

6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +15V
MON_, SCL, SDA, A0 to GND .....-0.3V to +6V
EN, TCK, TMS, TDI to GND .....-0.3V to +4V
TDO to GND .....-0.3V to (V_{DBP} + 0.3V)
EN_OUT1, EN_OUT2, EN_OUT3
(configured as open-drain) to GND .....-0.3V to +15V
EN_OUT1, EN_OUT2, EN_OUT3
(configured as charge pump) to GND .....-0.3V to +15V
EN_OUT4, EN_OUT5, EN_OUT6, RESET, GPIO_
(configured as open-drain) to GND.....-0.3V to +6V
EN_OUT_, RESET, GPIO_ (configured as push-pull)
to GND .....-0.3V to (V_{DBP} + 0.3V)
DBP, ABP to GND .....-0.3V to minimum of (4V and (V_{CC} + 0.3V))
Continuous Current (all other pins).....±20mA
Continuous Current (GND, pin 5).....±30mA
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C)..... 2759mW*
Thermal Resistance (Note 1)
θ_{JA}.....29°C/W
θ_{JC} .....2°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

*As per JEDEC 51 Standard, Multilayer Board (PCB).

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.8V to 14V, T_A = T_J = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	RESET output asserted low	1.2			V
			2.8		14	
Undervoltage Lockout	V_{UVLO}	Minimum voltage on V_{CC} to ensure the device is flash configurable			2.7	V
Undervoltage Lockout Hysteresis	$UVLO_{HYS}$			55		mV
Minimum Flash Operating Voltage	V_{FLASH}	Minimum voltage on V_{CC} to ensure flash erase and write operations	2.7			V
Supply Current	I_{CC1}	No load on any output		2.8	4	mA
	I_{CC2}	No load on any output, during flash writing cycle		7.7	14	
		V_{CC} = V_{ABP} = V_{DBP} = 3.6V (Note 3)			5	
DBP Regulator Voltage	V_{DBP}	V_{CC} = 5V, C_{DBP} = 1µF, no load	2.8	3	3.2	V
ABP Regulator Voltage	V_{ABP}	V_{CC} = 5V, C_{ABP} = 1µF, no load	2.85	3	3.15	V
Boot Time	t_{BOOT}	V_{CC} > V_{UVLO}		100	200	µs
Flash Writing Time		8-byte word		122		ms
Internal Timing Accuracy		(Note 4)	-10		+10	%
ADC						
Resolution				10		Bits
Gain Error	ADC_{GAIN}	T_A = +25°C			0.35	%
		T_A = -40°C to +85°C			0.75	
Offset Error	ADC_{OFF}				1.50	LSB
Integral Nonlinearity	ADC_{INL}				1	LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = T_J = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Nonlinearity	ADC_{DNL}				1	LSB
ADC Total Monitoring Cycle Time	t_{CYCLE}	Monitoring all 6 inputs, no MON_ fault detected		24	30	µs
ADC MON_ Ranges	ADC_{RNG}	MON_ range set to '00'		5.552		V
		MON_ range set to '01'		2.776		
		MON_ range set to '10'		1.388		
ADC LSB Step Size	ADC_{LSB}	MON_ range set to '00'		5.42		mV
		MON_ range set to '01'		2.71		
		MON_ range set to '10'		1.35		
ADC Input Leakage Current					1	µA
ENABLE INPUT (EN)						
EN Input-Voltage Threshold	$V_{TH\_EN\_R}$	EN voltage rising		1.24		V
	$V_{TH\_EN\_F}$	EN voltage falling	1.195	1.215	1.235	
EN Input Current	I_{EN}		-0.5		+0.5	µA
EN Input-Voltage Range			0		3.6	V
OUTPUTS (EN_OUT_, RESET, GPIO_)						
Output Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
		I_{SINK} = 10mA, GPIO_ only			0.7	
		V_{CC} = 1.2V, I_{SINK} = 100µA (RESET only)			0.3	
Maximum Output Sink Current		Total current into EN_OUT_, RESET, GPIO_, V_{CC} = 3.3V			30	mA
Output-Voltage High (Push-Pull)	V_{OH}	I_{SOURCE} =100µA	2.4			V
Output-Voltage High (EN_OUT1, EN_OUT2, EN_OUT3 Configured as Charge Pumps)	V_{OH_CP}	$I_{EN\_OUT\_}$= 1µA	11	11.7	13	V
EN_OUT_ Pullup Current (Charge Pump)	I_{CH_UP}	$V_{EN\_OUT\_}$ = 1V	5.4	7.9		µA
Output Leakage Current (Open Drain)	I_{OUT_LKG}				1	µA
		EN_OUT1, EN_OUT2, EN_OUT3 > 11.8V			5	
INPUTS (A0, GPIO_)						
Input Logic-Low	V_{IL}				0.8	V
Input Logic-High	V_{IH}		2.0			V
WDI Pulse Width	t_{WDI}		100			ns
$\overline{MR}$ Pulse Width	$t_{\overline{MR}}$		2			µs
SMBus INTERFACE						
Logic-Input Low Voltage	V_{IL}	Input voltage falling			0.8	V
Logic-Input High Voltage	V_{IH}	Input voltage rising	2.0			V
Input Leakage Current		V_{CC} shorted to GND, $V_{MON\_}$ = 0 or 6V	-1		+1	µA
Output Sink Current	V_{OL}	I_{SINK} = 3mA			0.4	V
Input Capacitance	C_{IN}			5		pF

6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = T_J = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SMBus TIMING							
Serial-Clock Frequency	f_{SCL}					400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}			1.3			µs
START Condition Setup Time	$t_{SU:STA}$			0.6			µs
START Condition Hold Time	$t_{HD:STA}$			0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$			0.6			µs
Clock Low Period	t_{LOW}			1.3			µs
Clock High Period	t_{HIGH}			0.6			µs
Data Setup Time	$t_{SU:DAT}$			100			ns
Output Fall Time	t_{OF}	10pF ≤ C_{BUS} ≤ 400pF				250	ns
Data Hold Time	$t_{HD:DAT}$	From 50% SCL falling to SDA change	Receive	0.15			µs
			Transmit	0.3		0.9	
Pulse Width of Spike Suppressed	t_{SP}				250		ns
SMBus Timeout	$t_{TIMEOUT}$	SMBCLK time low for reset		22		35	ms
JTAG INTERFACE							
TDI, TMS, TCK Logic-Low Input Voltage	V_{IL}	Input voltage falling				0.8	V
TDI, TMS, TCK Logic-High Input Voltage	V_{IH}	Input voltage rising		2.0			V
TDO Logic-Output Low Voltage	V_{OL_TDO}	I_{SINK} = 3mA				0.4	V
TDO Logic-Output High Voltage	V_{OH_TDO}	I_{SOURCE} = 200µA		2.4			V
TDI, TMS Pullup Resistors	R_{JPU}	Pullup to DBP		30	50	65	kΩ
I/O Capacitance	$C_{I/O}$				5		pF
TCK Clock Period	t_1					1000	ns
TCK High/Low Time	t_2, t_3			50	500		ns
TCK to TMS, TDI Setup Time	t_4			15			ns
TCK to TMS, TDI Hold Time	t_5			15			ns
TCK to TDO Delay	t_6					500	ns
TCK to TDO High-Z Delay	t_7					500	ns

Note 2: Specifications are guaranteed for the stated global conditions, unless otherwise noted. 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.

Note 3: For V_{CC} of 3.6V or lower, connect V_{CC}, DBP, and ABP together. For higher supply applications, connect only V_{CC} to the supply rail.

Note 4: Applies to RESET (except for reset timeout period of 25µs), fault, autoretry, sequence delays, and watchdog timeout.

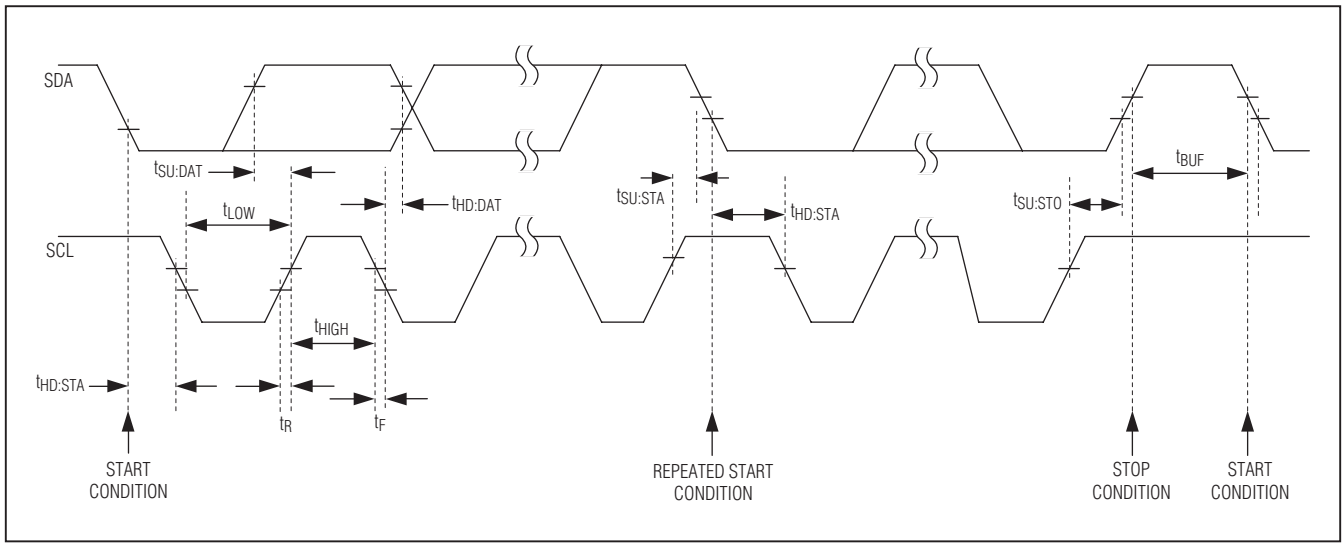


Figure 1. SMBus Timing Diagram

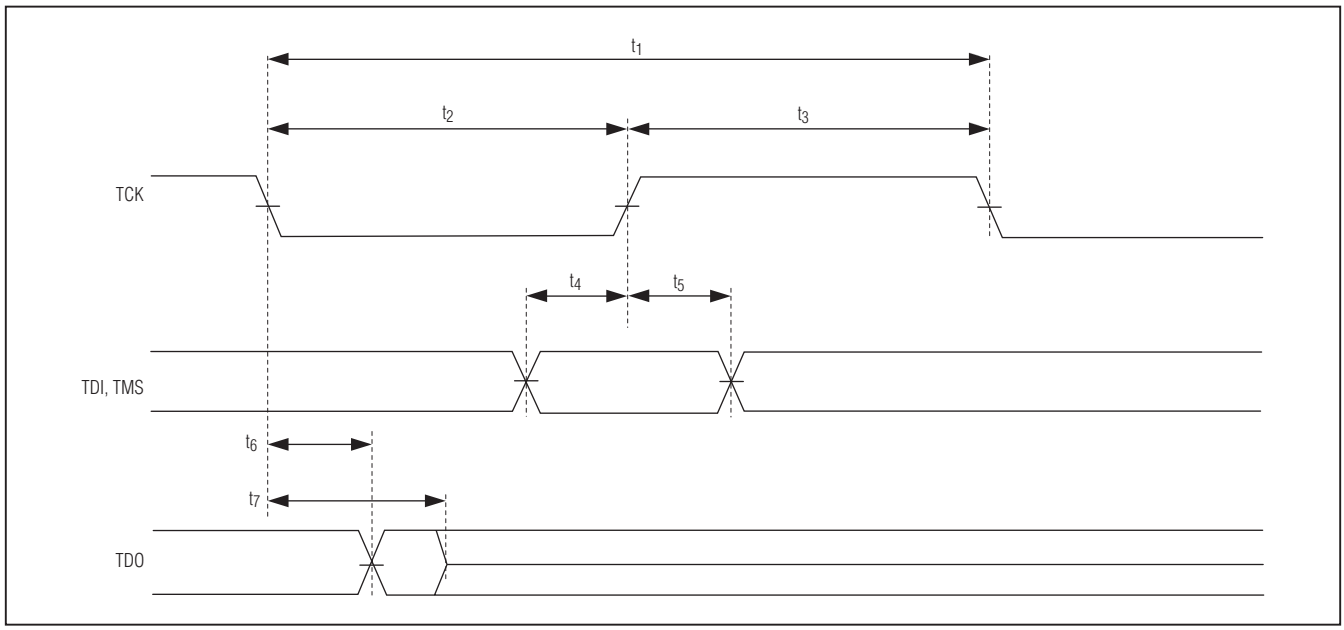


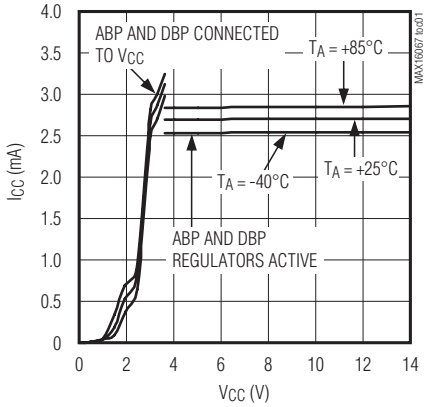
Figure 2. JTAG Timing Diagram

6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

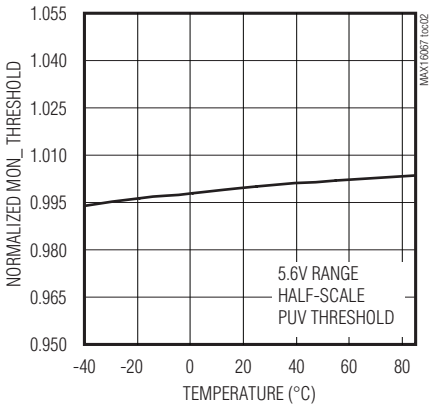
Typical Operating Characteristics

(Typical values are at V_{CC} = 3.3V, T_A = +25°C.)

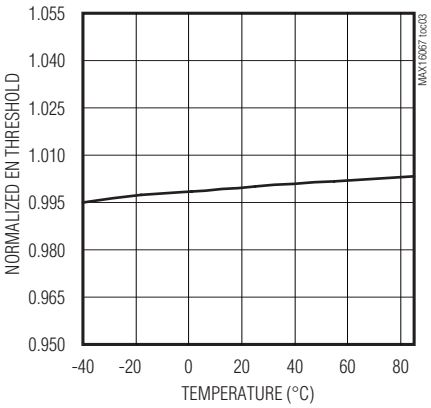
V_{CC} SUPPLY CURRENT vs. V_{CC} SUPPLY VOLTAGE



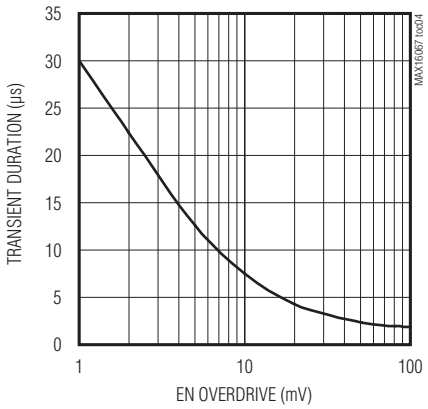
NORMALIZED MON_THRESHOLD vs. TEMPERATURE



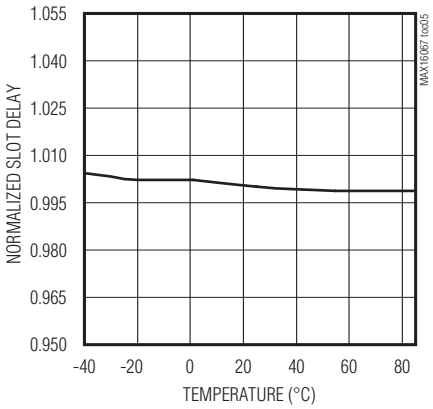
NORMALIZED EN THRESHOLD vs. TEMPERATURE



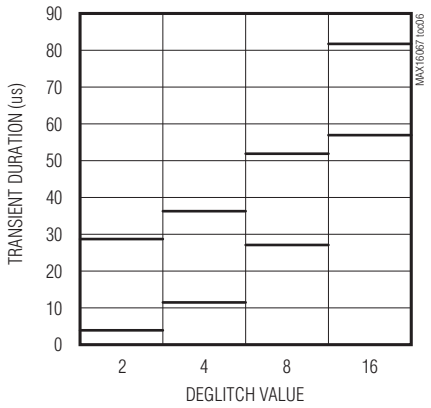
TRANSIENT DURATION vs. THRESHOLD OVERDRIVE (EN)



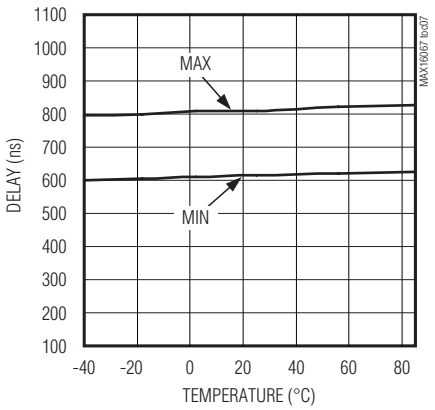
NORMALIZED TIMING ACCURACY vs. TEMPERATURE



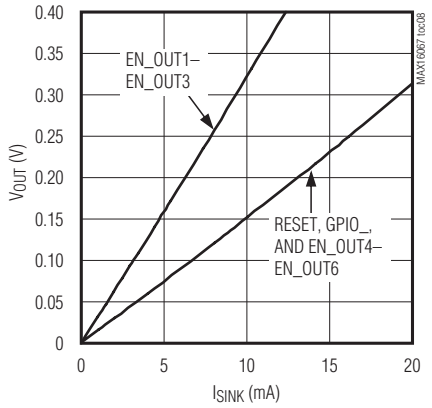
TRANSIENT DURATION vs. MON_ DEGLITCH



$\overline{MR}$ TO RESET PROPAGATION DELAY vs. TEMPERATURE



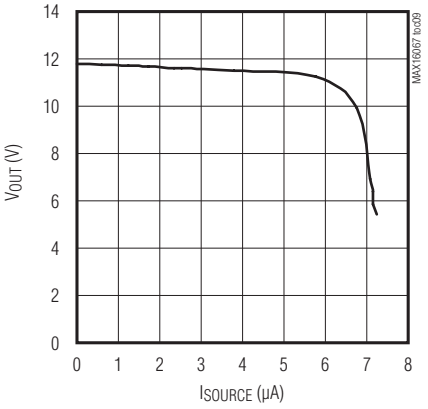
OUTPUT VOLTAGE vs. SINK CURRENT (OUT = LOW)



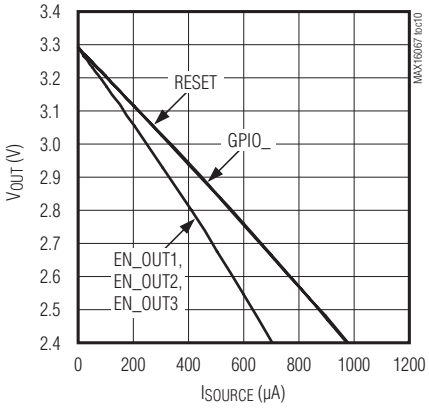
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = 3.3V, T_A = +25°C.)

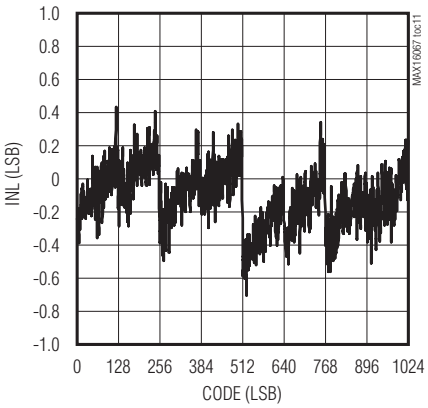
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (CHARGE-PUMP OUTPUT)



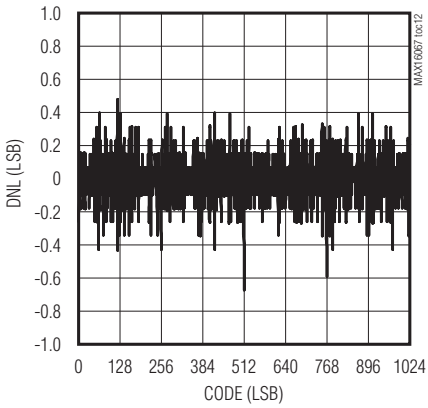
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (PUSH-PULL OUTPUT)



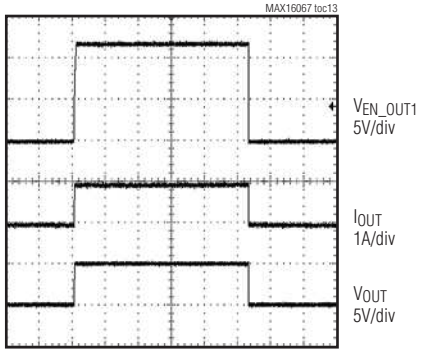
INTEGRAL NONLINEARITY vs. CODE



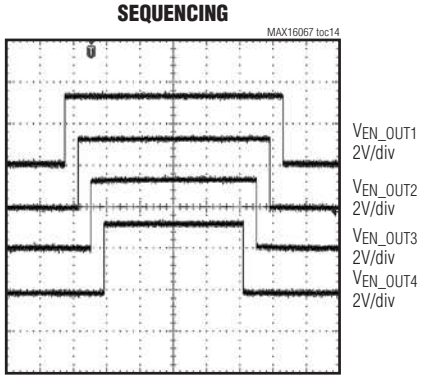
DIFFERENTIAL NONLINEARITY vs. CODE



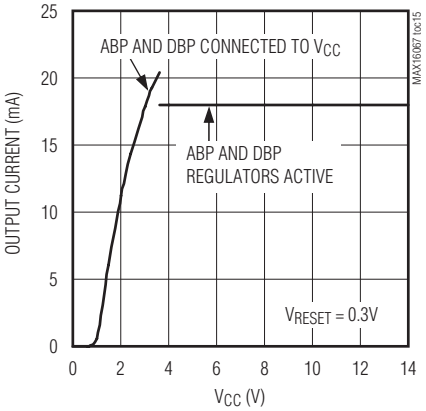
FET TURN_ON WITH CHARGE PUMP



SEQUENCING

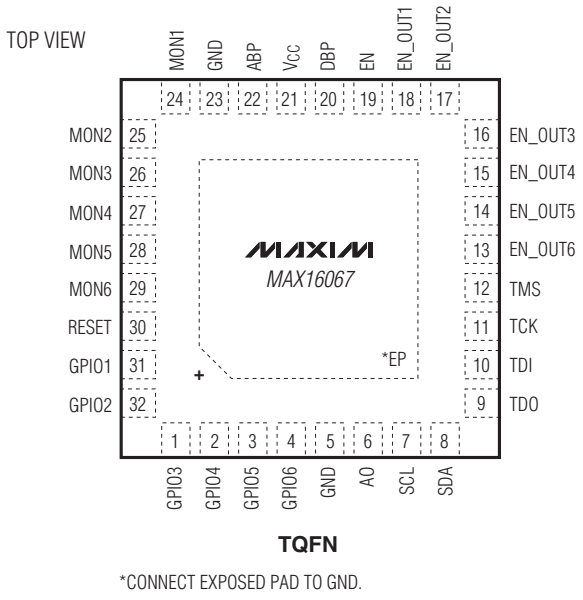


RESET OUTPUT CURRENT vs. V_{CC} SUPPLY VOLTAGE



6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

Pin Configuration



TQFN

*CONNECT EXPOSED PAD TO GND.

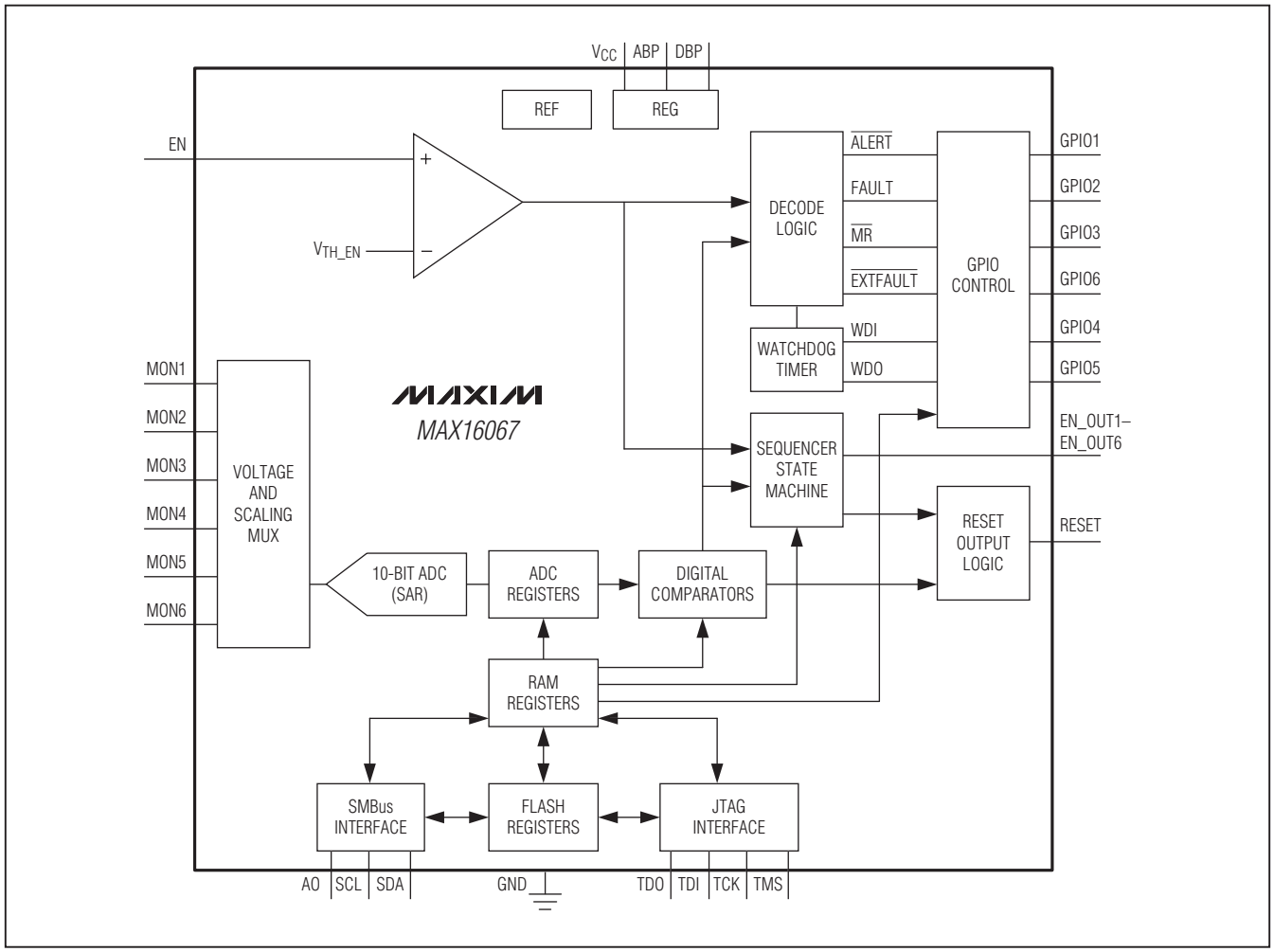
Pin Description

PIN	NAME	FUNCTION
1–4, 31, 32	GPIO3–GPIO6, GPIO1, GPIO2	General-Purpose Inputs/Outputs. Each GPIO_ can be configured to act as an input, a push-pull output, an open-drain output, or a special function.
5, 23	GND	Ground. Connect all GNDs together.
6	A0	Four-State SMBus Address. Address is sampled upon POR.
7	SCL	SMBus Serial-Clock Input
8	SDA	SMBus Serial-Data Open-Drain Input/Output
9	TDO	JTAG Test Data Output
10	TDI	JTAG Test Data Input
11	TCK	JTAG Test Clock
12	TMS	JTAG Test Mode Select
13–18	EN_OUT6–EN_OUT1	Outputs. Set EN_OUT_ with an active-high/active-low logic and with push-pull or open-drain configuration. EN_OUT_ can be asserted by a combination of MON_ voltages configurable through the flash. EN_OUT1–EN_OUT3 can be configured with a charge-pump output (+12V above GND) that can drive an external n-channel MOSFET. All EN_OUT_ can be configured as GPIOs.
19	EN	Analog Enable Input. All outputs deassert when V_{EN} is below the enable threshold.

Pin Description (continued)

PIN	NAME	FUNCTION
20	DBP	Digital Bypass. All push-pull outputs are referenced to DBP. Bypass DBP with a 1µF capacitor to GND.
21	VCC	Power-Supply Input. Bypass VCC to GND with a 10µF ceramic capacitor.
22	ABP	Analog Bypass. Bypass ABP to GND with a 1µF ceramic capacitor.
24–29	MON1–MON6	Monitor Voltage Inputs. Set the monitor voltage range through the configuration registers. Measured values are written to the ADC registers and can be read back through the SMBus or JTAG interface.
30	RESET	Configurable Reset Output
—	EP	Exposed Pad. Internally connected to GND. Connect to ground, but do not use EP as the main ground connection.

Functional Diagram



6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

Detailed Description

The MAX16067 manages up to six system power supplies. After boot-up, if EN is high and the software-enable bit is set to '1,' a power-up sequence begins based on the configuration stored in flash and the EN_OUT_s are controlled accordingly. When the power-up sequence is successfully completed, the monitoring phase begins. An internal multiplexer cycles through each MON_ input. At each multiplexer stop, the 10-bit ADC converts the monitored analog voltage to a digital result and stores the result in a register. Each time a conversion cycle (5µs, max) completes, internal logic circuitry compares the conversion results to the overvoltage and undervoltage thresholds stored in memory. When a result violates a programmed threshold, the conversion can be configured to generate a fault. GPIO_ can be programmed to assert on combinations of faults. Additionally, faults can be configured to shut off the system and trigger the nonvolatile fault logger, which writes all fault information automatically to the flash and write-protects the data to prevent accidental erasure.

The MAX16067 contains both SMBus and JTAG serial interfaces for accessing registers and flash. Use only one interface at any given time. For more information on how to access the internal memory through these interfaces, see the *SMBus-Compatible Serial Interface* and *JTAG Serial Interface* sections. The memory map is divided into three pages with access controlled by special SMBus and JTAG commands.

The factory-default values at POR (power-on reset) for all RAM registers are '0's. POR occurs when V_{CC} reaches the undervoltage-lockout threshold (UVLO) of 2.7V (max). At POR, the device begins a boot-up sequence. During the boot-up sequence, all monitored inputs are masked from initiating faults and flash contents are copied to the respective register locations. During boot-up, the MAX16067 is not accessible through the serial interface. The boot-up sequence takes up to 150µs, after which the device is ready for normal operation. RESET is asserted low up to the boot-up phase after which it assumes its programmed active state. RESET remains active for its programmed timeout period once sequencing is completed and all monitored channels are within their respective thresholds. Up to the boot-up phase, the GPIO_s and EN_OUT_s are high impedance.

Power

Apply 2.8V to 14V to V_{CC} to power the MAX16067. Bypass V_{CC} to ground with a 10µF capacitor. Two internal voltage regulators, ABP and DBP, supply power to the analog and digital circuitry within the device. For operation at 3.6V or lower, disable the regulators by connecting ABP and DBP to V_{CC}.

ABP is a 3.0V (typ) voltage regulator that powers the internal analog circuitry. Bypass ABP to GND with a 1µF ceramic capacitor installed as close as possible to the device.

DBP is an internal 3.0V (typ) voltage regulator. DBP powers flash and digital circuitry. All push-pull outputs refer to DBP. DBP supplies the input voltage to the internal charge pump when the programmable outputs are configured as charge-pump outputs. Bypass the DBP output to GND with a 1µF ceramic capacitor installed as close as possible to the device.

Do not power external circuitry from ABP or DBP.

Sequencing

To sequence a system of power supplies safely, the output voltage of a power supply must be good before the next power supply may turn on. Connect EN_OUT_ outputs to the enable input of the external power supplies and connect MON_ inputs to the output of the power supplies for voltage monitoring. More than one MON_ can be used if the power supply has multiple outputs.

Sequence Order

The MAX16067 provides a system of ordered slots to sequence multiple power supplies. To determine the sequence order, assign each EN_OUT_ to a slot ranging from Slot 1 to Slot 6 (Table 6b). EN_OUT_(s) assigned to Slot 1 are turned on first, followed by outputs assigned to Slot 2 through Slot 6. Multiple EN_OUT_s assigned to the same slot turn on at the same time.

Each slot includes a built-in configurable sequence delay (registers r77h to r7Dh) ranging from 80µs to 5.079s. During a reverse sequence, slots are turned off in reverse order starting from Slot 6. The MAX16067 can be configured to power down in simultaneous mode or in reverse-sequence mode as set in r75h[0]. Set r75h[0] to '1' for reverse sequence power-down.

See Tables 5 and 6 for the MON_ and EN_OUT_ slot assignment bits, and Tables 2 and 3 for the sequence delays.

During power-up or power-down sequencing, the current sequencer state can be found in r21h[3:0].

Table 1. Current Sequencer Slot

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
21h	[3:0]	Current-sequencer state 0000 = Slot0 0001 = Slot1 0010 = Slot2 0011 = Slot3 0100 = Slot4 0101 = Slot5 0110 = Slot6 0111 = Power-on mode 1000 = Fault state 1001 to 1111 = Unused
	[7:4]	Reserved

A sequencing delay occurs between each slot and is configured in registers 77h–7Dh as shown in Table 2. Each sequencing delay is stored as an 8-bit value and is calculated as follows:

$$t_{SEQ} = \left(5 \times 10^{-6}\right) \times 2^{a} \times (16 + b)$$

where t_{SEQ} is in seconds, a is the decimal value of the 4 MSBs and b is the decimal value of the 4 LSBs. See Table 3 for example calculations.

Enable Input (EN)

To initiate sequencing and enable monitoring, the voltage at EN must be above 1.24V (typ) and the software enable bit in r73h[0] must be set to '1.' To power down and disable monitoring, either pull EN below 1.215V (typ) or set the software enable bit to '0.' See Table 4 for the software enable bit configurations. Connect EN to ABP if not used.

If a fault condition occurs during the power-up cycle, the EN_OUT_ outputs are powered down immediately, regardless of the state of EN. In the monitoring state, if EN falls below the threshold, the sequencing state machine begins the power-down sequence. If EN rises above the threshold during the power-down sequence, the sequence state machine continues the power-down sequence until all the channels are powered off and then the device immediately begins the power-up sequence. When in the monitoring state, and when EN falls below the undervoltage threshold, a register bit, ENRESET (r20h[2]), is set to a '1.' This register bit latches and must be cleared through software. This bit indicates if RESET is asserted low due to EN going under the threshold. The POR state of ENRESET is '0'. The bit is only set on a falling edge of the EN comparator output or the software enable bit. If operating in latch-on fault mode, toggle EN or toggle the software enable bit to clear the latch condition and restart the device once the fault condition has been removed.

Table 2. Slot Delay Register

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
77h	277h	[7:0]	Sequence slot 0 to slot 1 delay
78h	278h	[7:0]	Sequence slot 1 to slot 2 delay
79h	279h	[7:0]	Sequence slot 2 to slot 3 delay
7Ah	27Ah	[7:0]	Sequence slot 3 to slot 4 delay
7Bh	27Bh	[7:0]	Sequence slot 4 to slot 5 delay
7Ch	27Ch	[7:0]	Sequence slot 5 to slot 6 delay
7Dh	27Dh	[7:0]	Sequence slot 6 to power-on state delay

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Table 3. Power-Up/Power-Down Slot Delays

Code	Value
0000 0000	$t_{SEQ} = \left(5 \times 10^{-6}\right) \times 2^{a} \times (16 + b) = \left(5 \times 10^{-6}\right) \times 2^{0} \times (16 + 0) = 80\mu s$
• • •	• • •
1111 1111	$t_{SEQ} = \left(5 \times 10^{-6}\right) \times 2^{a} \times (16 + b) = \left(5 \times 10^{-6}\right) \times 2^{15} \times (16 + 15) = 5.079s$

Table 4. Software Enable Configurations

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
73h	273h	[0]	Software enable 1 = Sequencing enabled 0 = Power-down
		[1]	Reserved
		[2]	1 = Margin mode enabled
		[3]	Reserved
		[4]	Independent watchdog mode enable 1 = Watchdog timer is independent of sequencer 0 = Watchdog timer boots after sequence completes

Monitoring Inputs While Sequencing

An enabled MON_ input can be assigned to a slot ranging from Slot 1 to Slot 6. EN_OUT_s are always asserted at the beginning of a slot. The supply voltages connected to the MON_ inputs must exceed the undervoltage threshold before the programmed fault timeout period expires, otherwise, a fault condition occurs. Once a MON_ input crosses the undervoltage threshold, the monitoring for overvoltage begins. The undervoltage and overvoltage threshold checking cannot be disabled during power-up and power-down. See Tables 5 and 6 for the MON_ slot assignment bits. The programmed sequence delay is then counted before moving to the next slot.

Slot 0 does not monitor any MON_ input and does not control any EN_OUT_. Slot 0 waits for the software enable bit r73h[0] to be a logic-high and for the voltage on EN to rise above 1.24V (typ) before initiating the power-up sequence and counting its own sequence delay.

Any MON_ input that suffers a fault during power-up sequencing causes all the EN_OUT_s to turn off and the sequencer to shut down regardless of the state of the critical fault enables (see the *Faults* section). If a MON_ input is less critical to system operation, it can be configured as “monitoring only” (see Table 6a) for sequencing. Monitoring for MON_ inputs assigned as “monitoring only” begins after sequencing is complete, and can trigger a critical fault only if specifically configured to do so using the critical fault enables.

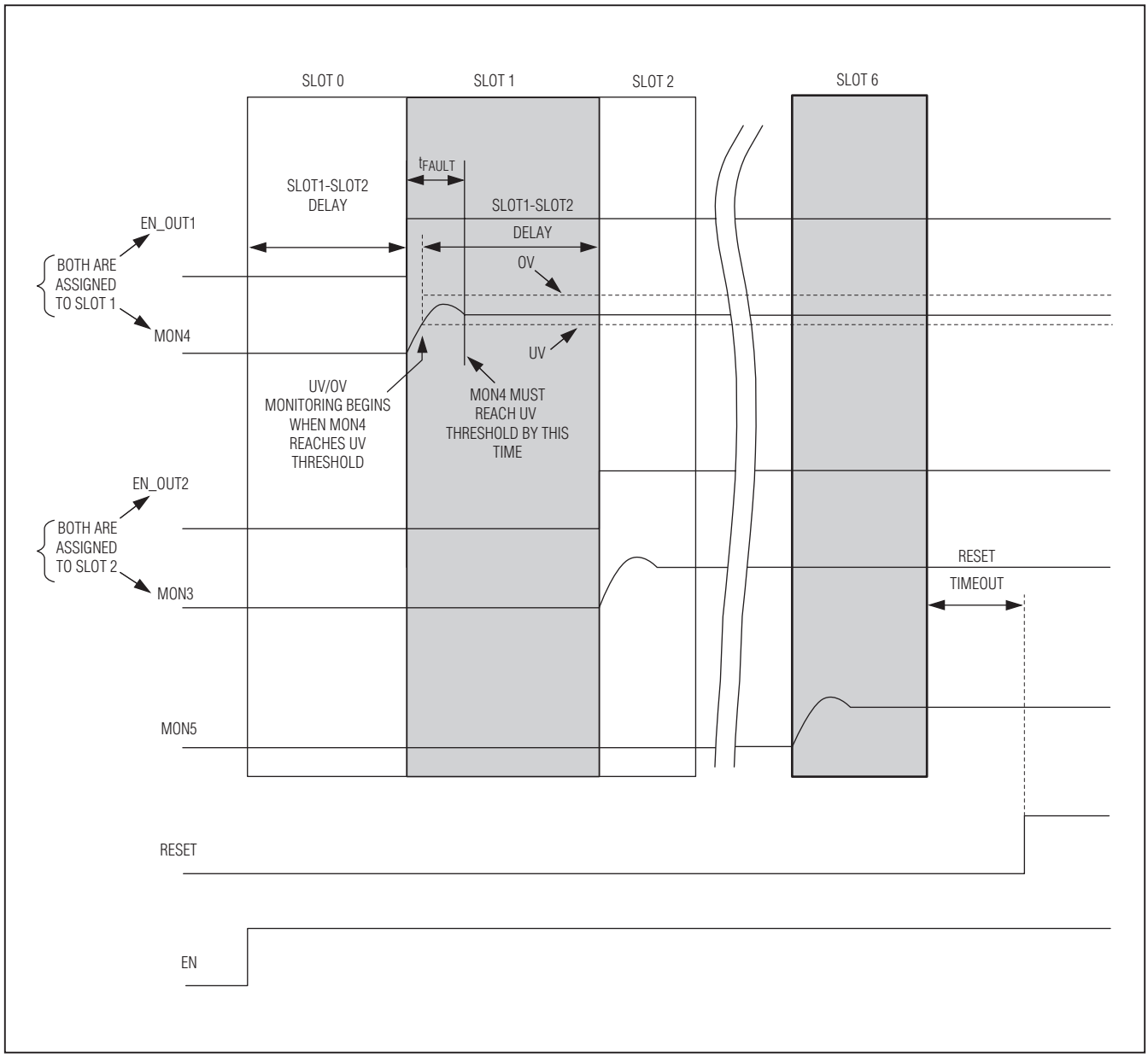

Figure 3. Delay and Reset Timing

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Table 5. MON_ and EN_OUT_ Assignment Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
7Eh	27Eh	[2:0]	MON1
		[3]	Not used
		[6:4]	MON2
		[7]	Not used
7Fh	27Fh	[2:0]	MON3
		[3]	Not used
		[6:4]	MON4
		[7]	Not used
80h	280h	[2:0]	MON5
		[3]	Not used
		[6:4]	MON6
		[7]	Not used
81h–83h	281h–283h	—	Not used
84h	284h	[3:0]	EN_OUT1
		[7:4]	EN_OUT2
85h	285h	[3:0]	EN_OUT3
		[7:4]	EN_OUT4
86h	286h	[3:0]	EN_OUT5
		[7:4]	EN_OUT6

Table 6a. MON_ Slot Assignment Codes

SLOT ASSIGNMENT	
CODE	MON_ DESCRIPTION
000	Not assigned
001	Slot 1
010	Slot 2
011	Slot 3
100	Slot 4
101	Slot 5
110	Slot 6
111	Monitoring-only state

Table 6b. EN_OUT_ Slot Assignment Codes

SLOT ASSIGNMENT	
CODE	EN_OUT_ DESCRIPTION
0000	Not assigned
0001	Slot 1
0010	Slot 2
0011	Slot 3
0100	Slot 4
0101	Slot 5
0110	Slot 6
1101	General-purpose input
1110	General-purpose output
—	All other unspecified codes are not assigned.

Power-Up

On power-up, when EN is high and the software enable bit is '1', the MAX16067 begins sequencing with Slot 0. After the sequencing delay for Slot 0 expires, the sequencer advances to Slot 1, and all EN_OUT_s assigned to the slot assert. All MON_ inputs assigned to Slot 1 are monitored and when the voltage rises above the undervoltage (UV) fault threshold, the sequence delay counter is started. When the sequence delay expires, the MAX16067 proceeds to the next slot.

When the t_{FAULT} counter expires before all MON_ inputs assigned to the slot are above the fault UV threshold, a fault asserts. EN_OUT_ outputs are disabled and the MAX16067 returns to the fault state. Register r75h[4:1] sets the t_{FAULT} delay. See Table 7 for details.

After the voltages on all MON_ inputs assigned to the last slot exceed the UV fault threshold and the slot delay expires, the MAX16067 starts the reset timeout counter. After the reset timeout, RESET deasserts. See Table 22 for more information on setting the reset timeout.

Power-Down

Power-down starts when EN is pulled low or the software enable bit is set to '0.' Power down EN_OUT_s simultaneously or in reverse sequence mode by setting the reverse sequence bit (r75h[0]) appropriately. Set r75h[0] to '1' to power down in reverse sequence.

Reverse Sequence Mode

When the MAX16067 is fully powered up and EN is pulled low or the software enable bit is set to '0', the EN_OUT_s assigned to Slot 6 deassert, the MAX16067 waits for the Slot 6 sequence delay and then proceeds to the previous slot (Slot 5), and so on until the EN_OUT_s assigned to Slot 1 turn off. When simultaneous power-down is selected (r75h[0] is set to '0'), all EN_OUT_s turn off at the same time.

Voltage Monitoring

The MAX16067 features an internal 10-bit ADC that monitors the MON_ voltage inputs. An internal multiplexer cycles through each of the enabled inputs, taking less than 24µs for a complete monitoring cycle. Each acquisition takes approximately 4µs. At each multiplexer stop, the 10-bit ADC converts the analog input to a digital result and stores the result in a register. ADC conversion results are stored in registers r00h–r0Bh (see Table 9). Use the SMBus or JTAG serial interface to read ADC conversion results.

The MAX16067 provides six inputs, MON1–MON6, for voltage monitoring. Each input-voltage range is programmable in registers r43h–r44h (see Table 8). When MON_ configuration registers are set to '11,' MON_ voltages are not monitored and the multiplexer does not stop at these inputs, decreasing the total cycle time. These inputs cannot be configured to trigger fault conditions.

Table 7. t_{FAULT} Delay Settings

r75h[4:1]	FAULT DELAY
0000	120µs
0001	150µs
0010	250µs
0011	380µs
0100	600µs
0101	1ms
0110	1.5ms
0111	2.5ms
1000	4ms
1001	6ms
1010	10ms
1011	15ms
1100	25ms
1101	40ms
1110	60ms
1111	100ms

The two programmable thresholds for each monitored voltage include an overvoltage and an undervoltage threshold. See the *Faults* section for more information on setting overvoltage and undervoltage thresholds. All voltage thresholds are 8 bits wide. The 8 MSBs of the 10-bit ADC conversion result are compared to these overvoltage and undervoltage thresholds.

For any undervoltage or overvoltage condition to be monitored and any faults detected, the MON_ input must be assigned to a sequence order or set to monitoring mode as described in the *Sequencing* section. Inputs that are not enabled are not converted by the ADC; they contain the last value acquired before that channel was disabled. The ADC conversion result registers are reset to 00h at boot-up. These registers are not reset when a reboot command is executed.

To temporarily disable voltage monitoring during voltage margining conditions, set r73h[2] to '1' to enable margining mode functionality. Faults, except for faults triggered by $\overline{\text{EXTFAULT}}$ pulled low externally, are not recorded when the device is in margining mode but the ADC continues to run and conversion results continue to be available. Set r73h[2] back to '0' for normal functionality.

Table 8. ADC Configuration Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
43h	243h	[1:0]	MON1 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	MON2 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[5:4]	MON3 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:6]	MON4 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
44h	244h	[1:0]	MON5 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	MON6 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:4]	Not used

Table 9. ADC Conversion Results (Read Only)

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
00h	[7:0]	MON1 result (MSB)
01h	[7:6]	MON1 result (LSB)
02h	[7:0]	MON2 result (MSB)
03h	[7:6]	MON2 result (LSB)
04h	[7:0]	MON3 result (MSB)
05h	[7:6]	MON3 result (LSB)
06h	[7:0]	MON4 result (MSB)
07h	[7:6]	MON4 result (LSB)
08h	[7:0]	MON5 result (MSB)
09h	[7:6]	MON5 result (LSB)
0Ah	[7:0]	MON6 result (MSB)
0Bh	[7:6]	MON6 result (LSB)

General-Purpose Inputs/Outputs

GPIO1–GPIO6 are programmable general-purpose inputs/outputs. GPIO1–GPIO6 are configurable as a manual reset input, a watchdog timer input and output, logic inputs/outputs, and fault-dependent outputs. When programmed as outputs, GPIOs are open-drain or push-pull. See Tables 10 and 11 for more detailed information on configuring GPIO1–GPIO6.

When GPIO1–GPIO6 are configured as general-purpose inputs/outputs, read values from the GPIO ports through r1Eh and write values to GPIOs through r3Eh. Note that r3Eh has a corresponding flash register, which programs the default state of a general purpose output. See Table 12 for more information on reading and writing to the GPIO.

Table 10. GPIO_ Configuration Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
3Fh	23Fh	[1:0]	GPIO1 configuration
		[3:2]	GPIO2 configuration
		[5:4]	GPIO3 configuration
		[7:6]	GPIO4 configuration
40h	240h	[1:0]	GPIO5 configuration
		[3:2]	GPIO6 configuration
		[4]	ARAEN bit
		[7:5]	Not used

Table 11. GPIO_ Function Configuration Bits

	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6
00	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input
01	Logic output (push-pull)	Logic output (push-pull)	Logic output (push-pull)	Logic output (push-pull)	Logic output (push-pull)	Logic output (push-pull)
10	Logic output (open drain)	Logic output (open drain)	Logic output (open drain)	Logic output (open drain)	Logic output (open drain)	Logic output (open drain)
11	$\overline{\text{ALERT}}$ (open drain)	FAULT (open drain)	$\overline{\text{MR}}$ input	WDI	$\overline{\text{WDO}}$ (open drain)	$\overline{\text{EXTFAULT}}$ (open drain)

Table 12. GPIO_ State Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
1Eh	—	[0]	GPIO1 input state
		[1]	GPIO2 input state
		[2]	GPIO3 input state
		[3]	GPIO4 input state
		[4]	GPIO5 input state
		[5]	GPIO6 input state
		[7:6]	Not used
3Eh	23Eh	[0]	GPIO1 output state
		[1]	GPIO2 output state
		[2]	GPIO3 output state
		[3]	GPIO4 output state
		[4]	GPIO5 output state
		[5]	GPIO6 output state
		[7:6]	Not used

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ALERT

GPIO1 is configurable as the SMBus alert signal, ALERT. ALERT asserts when any fault condition occurs. When the SMBus host sends the ARA (Alert Response Address), the MAX16067 responds with its slave address and deasserts ALERT. ALERT is an open-drain output.

Set the ARAEN bit in r40h[4] to '1' to disable the ARA feature. Under these conditions, the device does not respond to an ARA on the SMBus line.

FAULT

GPIO2 is configurable as a dedicated fault output, FAULT. FAULT asserts when an overvoltage or undervoltage condition occurs on the selected inputs. FAULT dependencies are set using registers r36h and r37h (see Table 13). When FAULT depends on more than one MON_, the fault output asserts when one or more MON_ exceeds a programmed threshold voltage. FAULT acts independently of the critical fault system, described in the *Critical Faults* section. Use r37h[7] to set the polarity of FAULT.

Manual Reset (MR)

GPIO3 is configurable to act as an active-low manual reset input, MR. Drive MR low to assert RESET. RESET remains asserted for the selected reset timeout period after MR transitions from low to high. When connecting MR to a pushbutton, use a pullup resistor. See the *Reset Output* section for more information on selecting a reset timeout period.

Watchdog Input (WDI) and Output (WDO)

GPIO4 and GPIO5 are configurable as the watchdog timer input (WDI) and output, WDO, respectively. See Table 23 for configuration details. WDO is an open-drain, active-low output. See the *Watchdog Timer* section for more information about the operation of the watchdog timer.

External Fault (EXTFAULT)

GPIO6 is configurable as the external fault input/output, EXTFAULT. EXTFAULT asserts if any monitored voltage exceeds an overvoltage or undervoltage threshold. EXTFAULT also asserts if a power-up or power-down sequencing fault occurs. This signal can be used to cascade multiple MAX16067s.

Pull EXTFAULT low externally to force the sequencer to enter a fault state. Under these conditions, all outputs deassert.

Two configuration bits determine the behavior of the MAX16067 when EXTFAULT is pulled low by an external device. Register bit r72h[5], if set to a '1', causes the sequencer state machine to enter the fault state, deasserting all the outputs when EXTFAULT is pulled low. When this happens, the flag bit r1Ch[6] is set to indicate the cause of the fault. If register bit r6Dh[2] is set in addition to r72h[5], EXTFAULT going low triggers a nonvolatile fault log operation.

Table 13. FAULT Dependencies

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
36h	236h	[0]	FAULT depends on MON1 undervoltage threshold
		[1]	FAULT depends on MON2 undervoltage threshold
		[2]	FAULT depends on MON3 undervoltage threshold
		[3]	FAULT depends on MON4 undervoltage threshold
		[4]	FAULT depends on MON5 undervoltage threshold
		[5]	FAULT depends on MON6 undervoltage threshold
		[7:6]	Not used
37h	237h	[0]	FAULT depends on MON1 overvoltage threshold
		[1]	FAULT depends on MON2 overvoltage threshold
		[2]	FAULT depends on MON3 overvoltage threshold
		[3]	FAULT depends on MON4 overvoltage threshold
		[4]	FAULT depends on MON5 overvoltage threshold
		[5]	FAULT depends on MON6 overvoltage threshold
		[6]	Not used
		[7]	0 = FAULT is an active-low digital output 1 = FAULT is an active-high digital output

Faults

The MAX16067 monitors the input (MON_) channels and compares the results with an overvoltage threshold and an undervoltage threshold. Based on these conditions, the MAX16067 asserts various fault outputs and save specific information about the channel conditions and voltages into the nonvolatile flash. Once a critical fault event occurs, the failing channel condition, ADC conversions at the time of the fault, or both can be saved by configuring the event logger. The event logger records a single failure in the internal flash and sets a lock bit which protects the stored fault data from accidental erasure on a subsequent power-up.

The MAX16067 is capable of measuring overvoltage and undervoltage fault events. Fault conditions are detected at the end of each ADC conversion. An overvoltage event occurs when the voltage at a monitored input exceeds the overvoltage threshold for that input. An undervoltage event occurs when the voltage at a monitored input falls below the undervoltage threshold. Fault thresholds are set in registers r49h–r59h as shown in Table 14. Disabled inputs are not monitored for fault conditions and are skipped over by the input multiplexer. Only the upper 8 bits of a conversion result are compared with the programmed fault thresholds.

Table 14. Fault Threshold Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
48h	248h	[7:0]	Not used
49h	249h	[7:0]	MON1 overvoltage threshold
4Ah	24Ah	[7:0]	MON1 undervoltage threshold
4Bh	24Bh	[7:0]	Not used
4Ch	24Ch	[7:0]	MON2 overvoltage threshold
4Dh	24Dh	[7:0]	MON2 undervoltage threshold
4Eh	24Eh	[7:0]	Not used
4Fh	24Fh	[7:0]	MON3 overvoltage threshold
50h	250h	[7:0]	MON3 undervoltage threshold
51h	251h	[7:0]	Not used
52h	252h	[7:0]	MON4 overvoltage threshold
53h	253h	[7:0]	MON4 undervoltage threshold
54h	254h	[7:0]	Not used
55h	255h	[7:0]	MON5 overvoltage threshold
56h	256h	[7:0]	MON5 undervoltage threshold
57h	257h	[7:0]	Not used
58h	258h	[7:0]	MON6 overvoltage threshold
59h	259h	[7:0]	MON6 undervoltage threshold

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Deglitch

Fault conditions are detected at the end of each conversion. When the voltage on an input falls outside a monitored threshold for one acquisition, the input multiplexer remains on that channel and performs several successive conversions. To trigger a fault, the input must stay outside the threshold for a certain number of acquisitions as determined by the deglitch setting in r74h[6:5] (see Table 15).

Fault Flags

Fault flags indicate the fault status of a particular input. The fault flag of any monitored input in the device can be read at any time from registers r1Bh and r1Ch, as shown in Table 16. Clear a fault flag by writing a '1' to the appropriate bit in the flag register. Unlike the fault signals sent to the fault outputs, these bits are masked by the critical fault enable bits (see Table 17). The fault flag is only set when the matching enable bit in the critical fault enable register is also set.

If GPIO6 is configured as the $\overline{\text{EXTFAULT}}$ input/output and $\overline{\text{EXTFAULT}}$ is pulled low by an external circuit, bit r1Ch[6] is set.

The SMB Alert ($\overline{\text{ALERT}}$) bit is set if the MAX16067 has asserted the SMBus Alert output. Clear by writing a '1'. See the *SMBALERT ($\overline{\text{ALERT}}$)* section for more details.

Table 15. Deglitch Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
74h	274h	[6:5]	Voltage comparator deglitch configuration 00 = 2 cycles 01 = 4 cycles 10 = 8 cycles 11 = 16 cycles

Table 16. Fault Flags

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
1Bh	[0]	MON1 undervoltage threshold
	[1]	MON2 undervoltage threshold
	[2]	MON3 undervoltage threshold
	[3]	MON4 undervoltage threshold
	[4]	MON5 undervoltage threshold
	[5]	MON6 undervoltage threshold
	[7:6]	Reserved
1Ch	[0]	MON1 overvoltage threshold
	[1]	MON2 overvoltage threshold
	[2]	MON3 overvoltage threshold
	[3]	MON4 overvoltage threshold
	[4]	MON5 overvoltage threshold
	[5]	MON6 overvoltage threshold
	[6]	External fault ($\overline{\text{EXTFAULT}}$)
	[7]	SMB alert

Critical Faults

During normal operation, a fault condition can be configured to shut down all the EN_OUT_s and store fault information in the flash memory by setting the appropriate critical fault enable bits. During power-up and power-down, all sequenced MON inputs are considered critical. Faults during power-up and power-down always cause the EN_OUT_s to turn off and can store fault information in the flash memory, depending on the contents of r6Dh[1:0]. Set the appropriate critical fault enable bits in registers r6Eh–r72h (see Table 17) for a fault condition to trigger a critical fault.

Logged fault information is stored in flash registers r200h–r208h (see Table 18). After fault information is logged, the flash is locked and must be unlocked to enable a new fault log to be stored. Write a '0' to r8Ch[1] to unlock the configuration flash. Fault information can be configured to store ADC conversion results and/or fault flags in registers. Select the critical fault configuration in r6Dh[1:0]. Set r6Dh[1:0] to '11' to turn off the fault logger. All stored ADC results are 8 bits wide (MSBs of the conversion).

Power-Up/Power-Down Faults

All EN_OUT_s deassert when an overvoltage or undervoltage fault is detected during power-up/power-down and the MAX16067 enters to the fault state. Fault information can be stored to flash depending on r6D[1:0] (see Table 17).

Table 17. Critical Fault Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
6Dh	26Dh	[1:0]	Fault Information to Log 00 = Save failed line flags and ADC values in flash 01 = Save only failed line flags in flash 10 = Save only ADC values in flash 11 = Do not save anything
		[2]	1 = Fault log triggered when $\overline{\text{EXTFAULT}}$ is pulled low externally
		[7:3]	Not used
6Eh	26Eh	[0]	1 = Fault log triggered when MON1 is below its undervoltage threshold
		[1]	1 = Fault log triggered when MON2 is below its undervoltage threshold
		[2]	1 = Fault log triggered when MON3 is below its undervoltage threshold
		[3]	1 = Fault log triggered when MON4 is below its undervoltage threshold
		[4]	1 = Fault log triggered when MON5 is below its undervoltage threshold
		[5]	1 = Fault log triggered when MON6 is below its undervoltage threshold
		[7:6]	Not used
6Fh	26Fh	[3:0]	Not used
		[4]	1 = Fault log triggered when MON1 is above its overvoltage threshold
		[5]	1 = Fault log triggered when MON2 is above its overvoltage threshold
		[6]	1 = Fault log triggered when MON3 is above its overvoltage threshold
		[7]	1 = Fault log triggered when MON4 is above its overvoltage threshold
70h	270h	[0]	1 = Fault log triggered when MON5 is above its overvoltage threshold
		[1]	1 = Fault log triggered when MON6 is above its overvoltage threshold
		[7:2]	Not used
71h	271h	[7:0]	Not used
72h	272h	[4:0]	Not used
		[5]	1 = $\overline{\text{EXTFAULT}}$ pulled low externally causes sequencer to enter fault state, turning off all EN_OUT_s 0 = $\overline{\text{EXTFAULT}}$ pulled low externally does not cause sequencer to enter fault state
		[7:6]	Not used

6-Channel, Flash-Configurable System Manager with Nonvolatile Fault Registers

Table 18. Nonvolatile Fault Log Registers

FLASH ADDRESS	BIT RANGE	DESCRIPTION
200h	[3:0]	Sequencer state where the fault has happened (see Table 1 for state codes). Fault has happened during power-up if bit [3] = 0 and during power-down if [3] = 1. Bits [2:0] indicate the slot number.
	[7:4]	Not used
201h	[0]	Fault log triggered on MON1 falling below its undervoltage threshold
	[1]	Fault log triggered on MON2 falling below its undervoltage threshold
	[2]	Fault log triggered on MON3 falling below its undervoltage threshold
	[3]	Fault log triggered on MON4 falling below its undervoltage threshold
	[4]	Fault log triggered on MON5 falling below its undervoltage threshold
	[5]	Fault log triggered on MON6 falling below its undervoltage threshold
	[7:6]	Not used
202h	[0]	Fault log triggered on MON1 exceeding its overvoltage threshold
	[1]	Fault log triggered on MON2 exceeding its overvoltage threshold
	[2]	Fault log triggered on MON3 exceeding its overvoltage threshold
	[3]	Fault log triggered on MON4 exceeding its overvoltage threshold
	[4]	Fault log triggered on MON5 exceeding its overvoltage threshold
	[5]	Fault log triggered on MON6 exceeding its overvoltage threshold
	[6]	Fault log triggered on $\overline{\text{EXTFAULT}}$
	[7]	Not used
203h	[7:0]	MON1 ADC output (8 MSBs)
204h	[7:0]	MON2 ADC output (8 MSBs)
205h	[7:0]	MON3 ADC output (8 MSBs)
206h	[7:0]	MON4 ADC output (8 MSBs)
207h	[7:0]	MON5 ADC output (8 MSBs)
208h	[7:0]	MON6 ADC output (8 MSBs)

Autoretry/Latch Mode

The MAX16067 can be configured for one of two fault management methods: autoretry or latch-on-fault. Set r74h[4:3] to '00' to select the latch-on-fault mode. In this configuration, EN_OUT_s deassert after a critical fault event. The device does not reinitiate the power-up sequence until EN is toggled or the software enable bit is toggled. See the *Enable Input (EN)* section for more information on setting the software enable bit.

Set r74h[4:3] to a value other than '00' to select autoretry mode (see Table 19). In this configuration, the device shuts down after a critical fault event then restarts following a configurable delay. Use r74h[2:0] to select an autoretry delay from 20ms to 1.6s. See Table 19 for more information on setting the autoretry delay.

When fault information is stored in flash (see the *Critical Faults* section) and autoretry mode is selected, set an autoretry delay greater than the time required for the storing operation. When fault information is stored in flash and latch-on-fault mode is chosen, toggle EN or reset the software enable bit only after the completion of the storing operation. When saving information about the failed lines only, ensure a delay of at least 12ms before the restart procedure. Otherwise, ensure a minimum 153ms timeout, to ensure that ADC conversions are completed and values are stored correctly in flash.

Table 19. Autoretry Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
74h	274h	[2:0]	Retry Delay 000 = 20ms 001 = 40ms 010 = 80ms 011 = 150ms 100 = 280ms 101 = 540ms 110 = 1s 111 = 2s
		[4:3]	Autoretry/Latch Mode 00 = Latch 01 = Reserved 10 = Reserved 11 = Always retry

Programmable Outputs (EN_OUT1–EN_OUT6)

The MAX16067 includes six programmable outputs. These outputs are capable of connecting to either the enable (EN) inputs of a DC-DC or LDO power supply, or to drive the gate of an n-channel MOSFET in charge-pump mode. Selectable output configurations include: active-low or active-high, open-drain or push-pull. EN_OUT1–EN_OUT3 can act as charge-pump outputs, EN_OUT1–EN_OUT6 can be configured as general-purpose inputs or general-purpose outputs. Use the registers r30h–r33h to configure outputs. See Table 20 for detailed information on configuring EN_OUT1–EN_OUT6.

In charge-pump configuration: EN_OUT1, EN_OUT2, and EN_OUT3 act as high-voltage charge-pump outputs to drive up to three external n-channel MOSFETs. During sequencing, an EN_OUT_ output is configured as a charge-pump output 11V above GND. See the *Sequencing* section for more detailed information on power-supply sequencing.

In open-drain output configuration: Connect an external pullup resistor from the output to an external voltage up to 5.5V (EN_OUT4, EN_OUT5, EN_OUT6) or 14V (EN_OUT1, EN_OUT2, EN_OUT3) when configured as an open-drain output. Choose the pullup resistor depending on the number of devices connected to the open-drain output and the allowable current consumption. The open-drain output configuration allows wired-OR connection.

In push-pull configuration: The MAX16067's programmable outputs are referenced to V_{DBP}.

Table 20. EN_OUT1–EN_OUT6 Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
30h	230h	[1:0]	EN_OUT1 Configuration 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[3:2]	EN_OUT2 Configuration 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[5:4]	EN_OUT3 Configuration 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[7:6]	EN_OUT4 Configuration 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
31h	231h	[1:0]	EN_OUT5 Configuration 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[3:2]	EN_OUT6 Configuration 00 = Active-low, open drain 01 = Active-high, open drain 10 = Active-low, push-pull 11 = Active-high, push-pull
		[7:4]	Not used
33h	233h	[0]	EN_OUT1 Charge-Pump Output Configuration 0 = Charge-pump output disabled 1 = Charge-pump output enabled (active-high)
		[1]	EN_OUT2 Charge-Pump Output Configuration 0 = Charge-pump output disabled 1 = Charge-pump output enabled (active-high)
		[2]	EN_OUT3 Charge-Pump Output Configuration 0 = Charge-pump output disabled 1 = Charge-pump output enabled (active-high)
		[7:3]	Not used

EN_OUT_s as GPIO

EN_OUT1–EN_OUT6 can be configured as general-purpose inputs by setting the sequencing slot assignments in r84h–r86h to '1101' or as general-purpose outputs by setting the slot assignments to '1110'. See Tables 5 and 6. If an EN_OUT_ is configured as a general-purpose input, the state of the GPIO can be read from r1Fh (see Table 21). If an EN_OUT_ is configured as a general-purpose output, it is controlled by r34h.

EN_OUT_ State During Power-Up

When V_{CC} is ramped from 0V to the operating supply voltage, the EN_OUT_ output is high impedance until V_{CC} reaches UVLO and then EN_OUT_ goes into the configured deasserted state. See Figures 4 and 5. Configure RESET as an active-low push-pull or open-drain output pulled up to V_{CC} through a 10kΩ resistor for Figures 4 and 5.

Table 21. EN_OUT_ GPIO State Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
1Fh	—	[0]	EN_OUT1 input state
		[1]	EN_OUT2 input state
		[2]	EN_OUT3 input state
		[3]	EN_OUT4 input state
		[4]	EN_OUT5 input state
		[5]	EN_OUT6 input state
		[7:6]	Not used
34h	234h	[0]	1 = Assert EN_OUT1
		[1]	1 = Assert EN_OUT2
		[2]	1 = Assert EN_OUT3
		[3]	1 = Assert EN_OUT4
		[4]	1 = Assert EN_OUT5
		[5]	1 = Assert EN_OUT6
		[7:6]	Not used

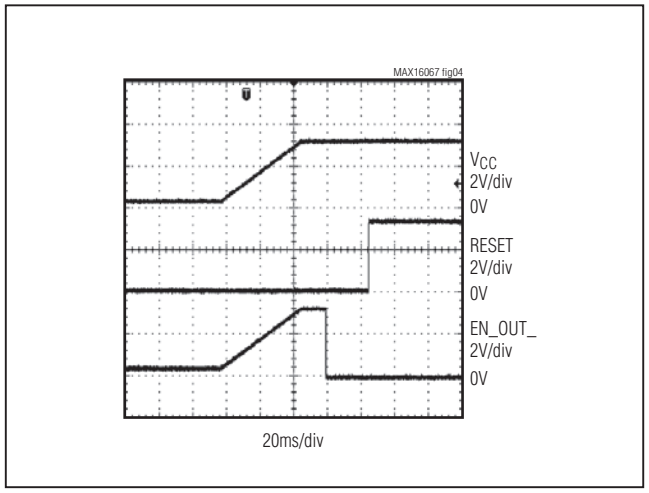

Figure 4. RESET and EN_OUT_ During Power-Up, EN_OUT_ is in Open-Drain Active-Low Configuration

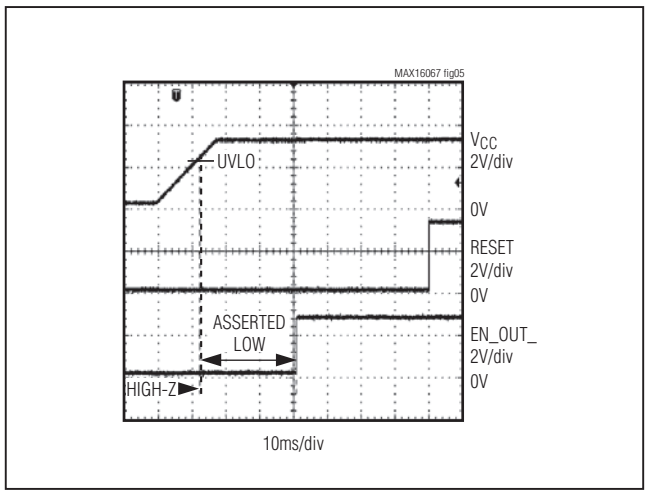

Figure 5. RESET and EN_OUT_ During Power-Up, EN_OUT_ is in Push-Pull Active-High Configuration