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MAX16070/MAX16071

12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

General Description

The MAX16070/MAX16071 flash-configurable system monitors supervise multiple system voltages. The MAX16070/MAX16071 can also accurately monitor (±2.5%) one current channel using a dedicated high-side current-sense amplifier. The MAX16070 monitors up to twelve system voltages simultaneously, and the MAX16071 monitors up to eight supply voltages. These devices integrate a selectable differential or single-ended analog-to-digital converter (ADC). Device configuration information, including overvoltage and undervoltage limits and timing settings are stored in nonvolatile flash memory. During a fault condition, fault flags and channel voltages can be automatically stored in the nonvolatile flash memory for later read-back.

The internal 1% accurate 10-bit ADC measures each input and compares the result to one overvoltage, one undervoltage, and one early warning limit that can be configured as either undervoltage or overvoltage. A fault signal asserts when a monitored voltage falls outside the set limits. Up to three independent fault output signals are configurable to assert under various fault conditions.

Because the MAX16070/MAX16071 support a power-supply voltage of up to 14V, they can be powered directly from the 12V intermediate bus in many systems.

The MAX16070/MAX16071 include eight/six programmable general-purpose inputs/outputs (GPIOs). GPIOs are flash configurable as dedicated fault outputs, as a watchdog input or output, or as a manual reset.

The MAX16070/MAX16071 feature nonvolatile fault memory for recording information during system shutdown events. The fault logger records a failure in the internal flash and sets a lock bit protecting the stored fault data from accidental erasure. An SMBus or a JTAG serial interface configures the MAX16070/MAX16071. The MAX16070/MAX16071 are available in a 40-pin, 6mm x 6mm, TQFN package. Both devices are fully specified from -40°C to +85°C.

Applications

Networking Equipment

Telecom Equipment (Base Stations, Access)

Storage/RAID Systems

Servers

Features

- **Operate from 2.8V to 14V**
- **±2.5% Current-Monitoring Accuracy**
- **1% Accurate 10-Bit ADC Monitors 12/8 Voltage Inputs**
- **Single-Ended or Differential ADC for System Voltage/Current Monitoring**
- **Integrated High-Side, Current-Sense Amplifier**
- **12/8 Monitored Inputs with Overvoltage/Undervoltage/Early Warning Limit**
- **Nonvolatile Fault Event Logger**
- **Two Programmable Fault Outputs and One Reset Output**
- **Eight General-Purpose Inputs/Outputs Configurable as:**
  - **Dedicated Fault Outputs**
  - **Watchdog Timer Function**
  - **Manual Reset**
  - **Margin Enable**
- **SMBus (with Timeout) or JTAG Interface**
- **Flash Configurable Time Delays and Thresholds**
- **-40°C to +85°C Operating Temperature Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX16070ETL+	-40°C to +85°C	40 TQFN-EP*
MAX16071ETL+	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration and Typical Operating Circuits appear at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-5003; Rev 4; 11/14

ABSOLUTE MAXIMUM RATINGS

V_{CC}, CSP, CSM to GND.....-0.3V to +15V
CSP to CSM.....-0.7V to +0.7V
MON_, GPIO_, SCL, SDA, A0, RESET to GND
(programmed as open-drain outputs).....-0.3V to +6V
EN, TCK, TMS, TDI to GND .....-0.3V to +4V
DBP, ABP to GND .....-0.3V to the lower of +4V or (V_{CC} + 0.3V)
TDO, GPIO_, RESET
(programmed as push-pull outputs) .... -0.3V to (V_{DBP} + 0.3V)
Input/Output Current 20mA
Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 26.3mW/°C above +70°C).....2105mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V_{CC}	Reset output asserted low	1.2			V
		(Note 2)	2.8		14	
Undervoltage Lockout (Rising)	V_{UVLO}	Minimum voltage on V_{CC} to ensure the device is flash configurable			2.7	V
Undervoltage Lockout Hysteresis	V_{UVLO_HYS}			100		mV
Minimum Flash Operating Voltage	V_{flash}	Minimum voltage on V_{CC} to ensure flash erase and write operations	2.7			V
Supply Current	I_{CC}	No load on output pins		4.5	7	mA
		During flash writing cycle		10	14	
ABP Regulator Voltage	V_{ABP}	C_{ABP} = 1µF, no load, V_{CC} = 5V	2.85	3	3.15	V
DBP Regulator Voltage	V_{DBP}	C_{DBP} = 1µF, no load, V_{CC} = 5V	2.8	3	3.1	V
Boot Time	t_{BOOT}	V_{CC} > V_{UVLO}		200	350	µs
Flash Writing Time		8-byte word		122		ms
Internal Timing Accuracy		(Note 3)	-8		+8	%
EN Input Voltage	$V_{TH\_EN\_R}$	EN voltage rising		1.41		V
	$V_{TH\_EN\_F}$	EN voltage falling	1.365	1.39	1.415	
EN Input Current	I_{EN}		-0.5		+0.5	µA
Input Voltage Range			0		5.5	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC DC ACCURACY							
Resolution						10	Bits
Gain Error	ADC_{GAIN}	T_A = +25°C				0.35	%
		T_A = -40°C to +85°C				0.70	
Offset Error	ADC_{OFF}					1	LSB
Integral Nonlinearity	ADC_{INL}					1	LSB
Differential Nonlinearity	ADC_{DNL}					1	LSB
ADC Total Monitoring Cycle Time	t_{CYCLE}	No MON_ fault detected			40	50	µs
ADC IN_ Ranges		1 LSB = 5.43mV			5.56		V
		1 LSB = 2.72mV			2.78		
		1 LSB = 1.36mV			1.39		
CURRENT SENSE							
CSP Input-Voltage Range	V_{CSP}			3		14	V
Input Bias Current	I_{CSP}				14	25	µA
	I_{CSM}	V_{CSP} = V_{CSM}			3	5	
CSP Total Unadjusted Error	CSP_{ERR}	(Note 4)				2	%FSR
Overcurrent Differential Threshold	OVC_{TH}	V_{CSP} - V_{CSM}	Gain = 48	21.5	25	30.5	mV
			Gain = 24	46	51	56	
			Gain = 12	94	101	108	
			Gain = 6	190	202	210	
V_{SENSE} Fault Threshold Hysteresis	OVC_{HYS}				0.5		$\%OVC_{TH}$
Secondary Overcurrent Threshold Timeout	OVC_{DEL}	r73h[6:5] = '00'			0		ms
		r73h[6:5] = '01'		3	4	5	
		r73h[6:5] = '10'		12	16	20	
		r73h[6:5] = '11'		50	64	60	
V_{SENSE} Ranges		Gain = 6			232		mV
		Gain = 12			116		
		Gain = 24			58		
		Gain = 48			29		
ADC Current Measurement Accuracy		V_{SENSE} = 150mV (gain = 6 only)		-2.5	±0.2	+2.5	%
		V_{SENSE} = 50mV, gain = 12		-4	±0.2	+4	
		V_{SENSE} = 25mV, gain = 24			±0.5		
		V_{SENSE} = 10mV, gain = 48			±1		
Gain Accuracy		V_{SENSE} = 20mV to 100mV, V_{CSP} = 5V, gain = 6		-1.5		+1.5	%
Common-Mode Rejection Ratio	$CMRR_{SNS}$	V_{CSP} > 4V			80		dB
Power-Supply Rejection Ratio	$PSRR_{SNS}$				80		dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUTS (RESET, GPIO_)						
Output-Voltage Low	V_{OL}	I_{SINK} = 2mA			0.4	V
		I_{SINK} = 10mA, GPIO_ only			0.7	
		V_{CC} = 1.2V, I_{SINK} = 100µA (RESET only)			0.3	
Maximum Output Sink Current		Total current into RESET, GPIO_, V_{CC} = 3.3V			30	mA
Output-Voltage High (Push-Pull)		I_{SOURCE} = 100µA	2.4			V
Output Leakage (Open Drain)					1	µA
SMBus INTERFACE						
Logic-Input Low Voltage	V_{IL}	Input voltage falling			0.8	V
Logic-Input High Voltage	V_{IH}	Input voltage rising	2.0			V
Input Leakage Current		IN = GND or V_{CC}	-1		+1	µA
Output Sink Current	V_{OL}	I_{SINK} = 3mA			0.4	V
Input Capacitance	C_{IN}			5		pF
SMBus Timeout	$t_{TIMEOUT}$	SCL time low for reset	25		35	ms
INPUTS (A0, GPIO_)						
Input Logic-Low	V_{IL}				0.8	V
Input Logic-High	V_{IH}		2.0			V
WDI Pulse Width	t_{WDI}		100			ns
$\overline{MR}$ Pulse Width	t_{MR}		1			µs
$\overline{MR}$ to RESET Delay				0.5		µs
$\overline{MR}$ Glitch Rejection				100		ns
SMBus TIMING						
Serial Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		1.3			µs
START Condition Setup Time	$t_{SU:STA}$		0.6			µs
START Condition Hold Time	$t_{HD:STA}$		0.6			µs
STOP Condition Setup Time	$t_{SU:STO}$		0.6			µs
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 2.8V to 14V, T_A = -40°C to +85°C, unless otherwise specified. Typical values are at V_{ABP} = V_{DBP} = V_{CC} = 3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Fall Time	t_{OF}	C_{BUS} = 10pF to 400pF			250	ns
Data Hold Time	$t_{HD:DAT}$	From 50% SCL falling to SDA change	0.3		0.9	µs
Pulse Width of Spike Suppressed	t_{SP}			30		ns
JTAG INTERFACE						
TDI, TMS, TCK Logic-Low Input Voltage	V_{IL}	Input voltage falling			0.8	V
TDI, TMS, TCK Logic-High Input Voltage	V_{IH}	Input voltage rising	2			V
TDO Logic-Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
TDO Logic-Output High Voltage	V_{OH}	I_{SOURCE} = 200µA	2.4			V
TDI, TMS Pullup Resistors	R_{PU}	Pullup to DBP	40	50	60	kΩ
I/O Capacitance	$C_{I/O}$			5		pF
TCK Clock Period	t_1				1000	ns
TCK High/Low Time	t_2, t_3		50	500		ns
TCK to TMS, TDI Setup Time	t_4		15			ns
TCK to TMS, TDI Hold Time	t_5		10			ns
TCK to TDO Delay	t_6				500	ns
TCK to TDO High-Z Delay	t_7				500	ns

Note 1: Specifications are guaranteed for the stated global conditions, unless otherwise noted. 100% production tested at T_A = +25°C and T_A = +85°C. Specifications at T_A = -40°C are guaranteed by design.

Note 2: For 3.3V V_{CC} applications, connect V_{CC}, DBP, and ABP together. For higher supply applications, connect V_{CC} only to the supply rail.

Note 3: Applies to RESET, fault, autoretry, sequence delays, and watchdog timeout.

Note 4: Total unadjusted error is a combination of gain, offset, and quantization error.

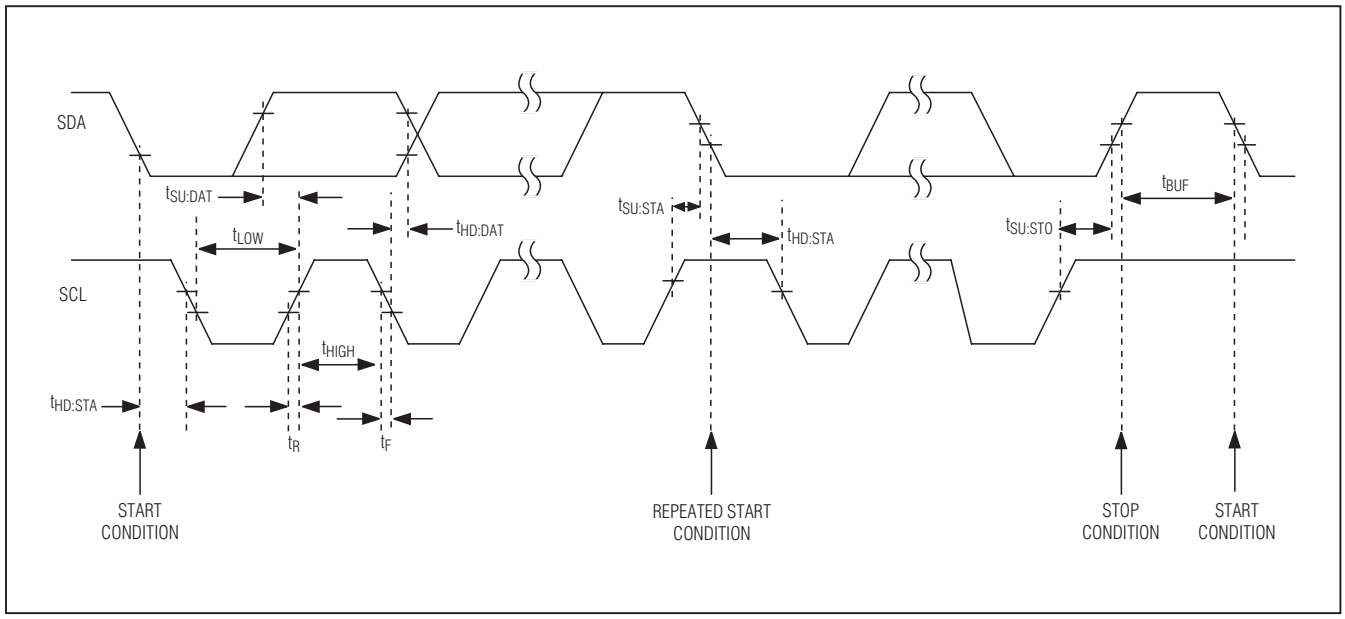


Figure 1. SMBus Timing Diagram

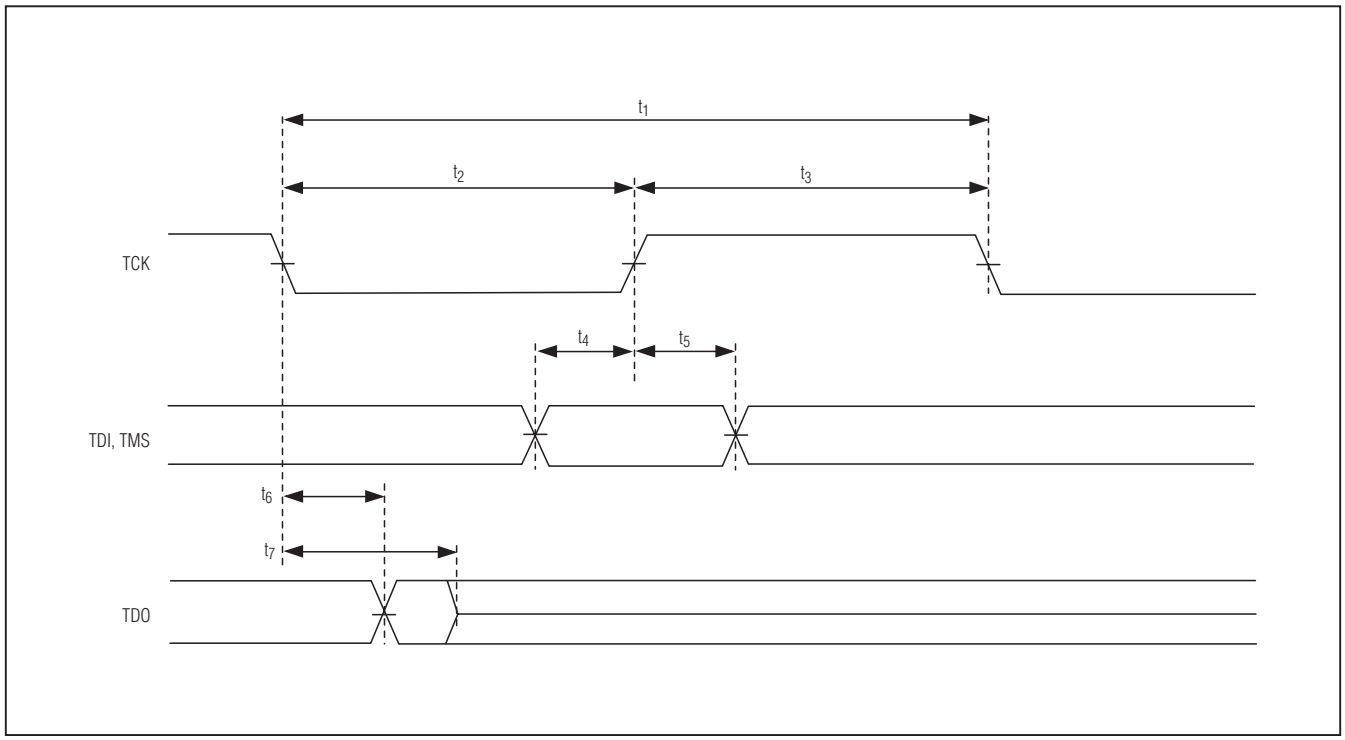


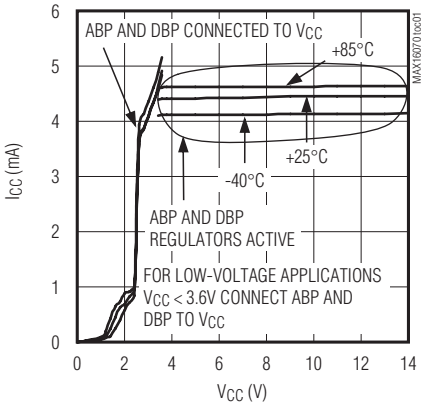
Figure 2. JTAG Timing Diagram

12-Channel/8-Channel, Flash-Configurable System Managers with Nonvolatile Fault Registers

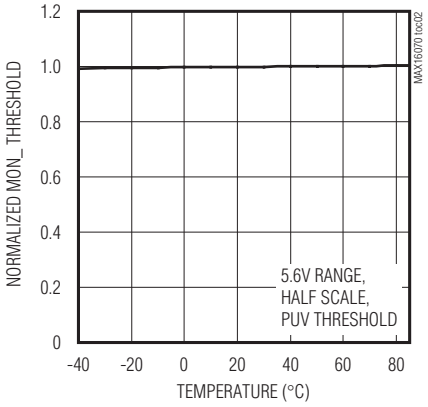
Typical Operating Characteristics

(Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

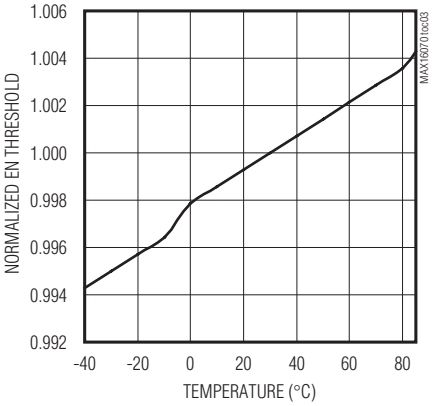
VCC SUPPLY CURRENT vs. VCC SUPPLY VOLTAGE



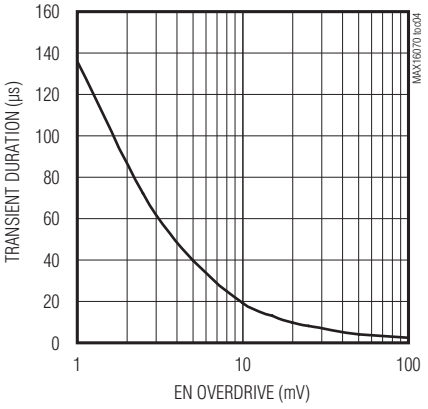
NORMALIZED MON_ THRESHOLD vs. TEMPERATURE



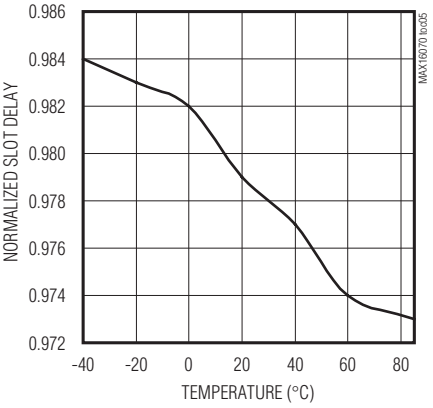
NORMALIZED EN THRESHOLD vs. TEMPERATURE



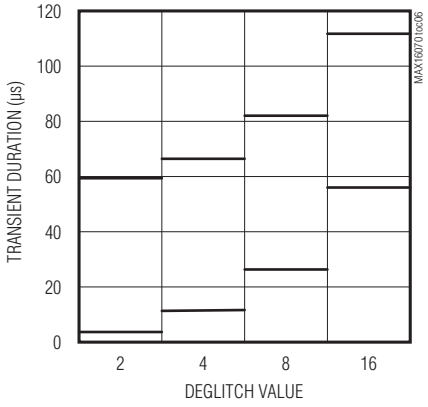
TRANSIENT DURATION vs. THRESHOLD OVERDRIVE (EN)



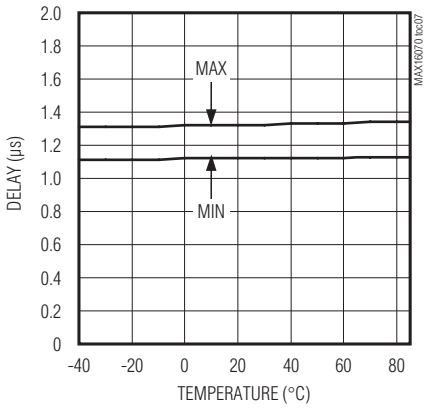
NORMALIZED TIMING ACCURACY vs. TEMPERATURE



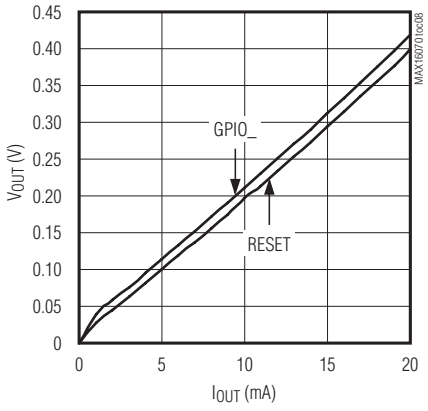
MON_ DEGLITCH vs. TRANSIENT DURATION



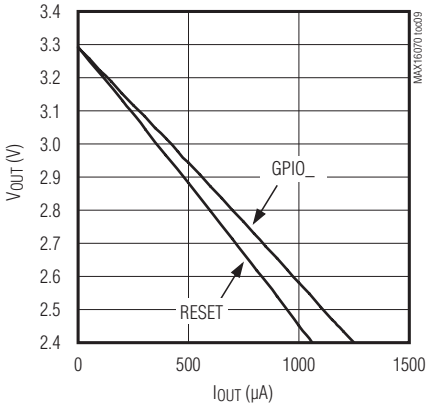
MR TO RESET PROPAGATION DELAY vs. TEMPERATURE



OUTPUT VOLTAGE vs. SINK CURRENT (OUT = LOW)



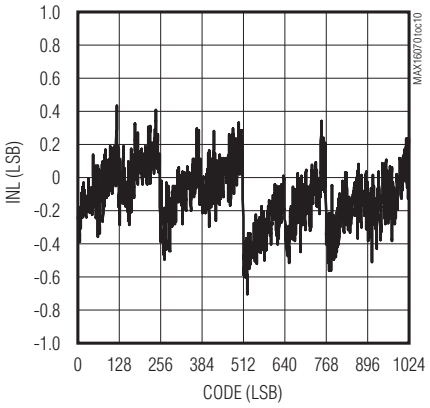
OUTPUT-VOLTAGE HIGH vs. SOURCE CURRENT (PUSH-PULL OUTPUT)



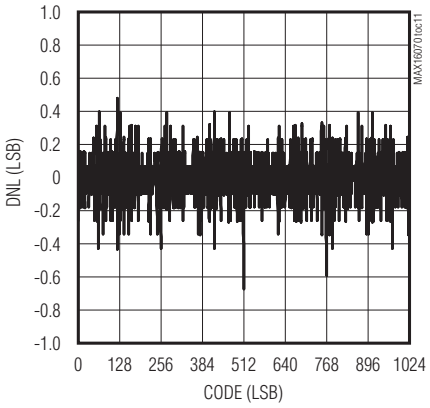
Typical Operating Characteristics (continued)

(Typical values are at V_{CC} = 3.3V, T_A = +25°C, unless otherwise noted.)

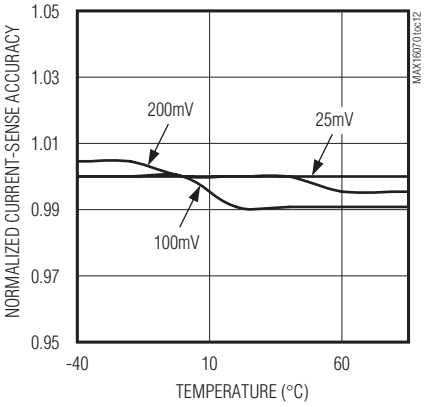
INTEGRAL NONLINEARITY vs. CODE



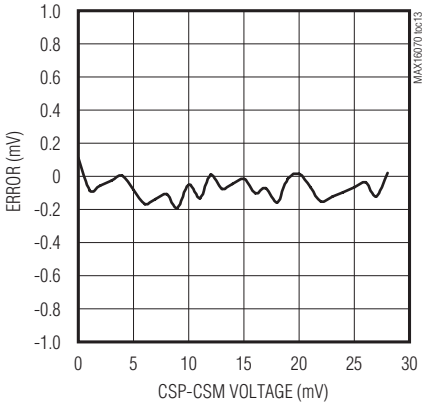
DIFFERENTIAL NONLINEARITY vs. CODE



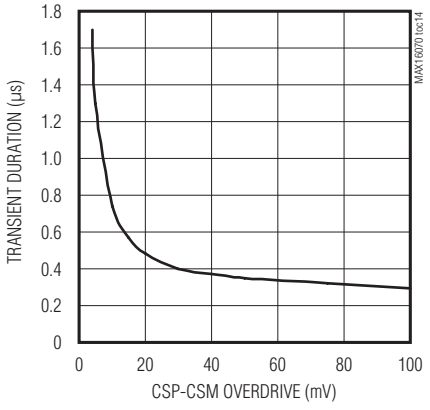
NORMALIZED CURRENT-SENSE ACCURACY vs. TEMPERATURE



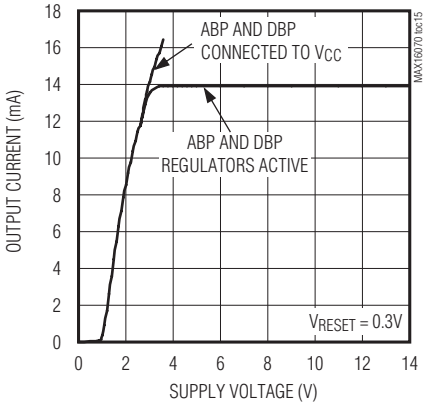
CURRENT-SENSE ACCURACY vs. CSP-CSM VOLTAGE



CURRENT-SENSE TRANSIENT DURATION vs. CSP-CSM OVERDRIVE



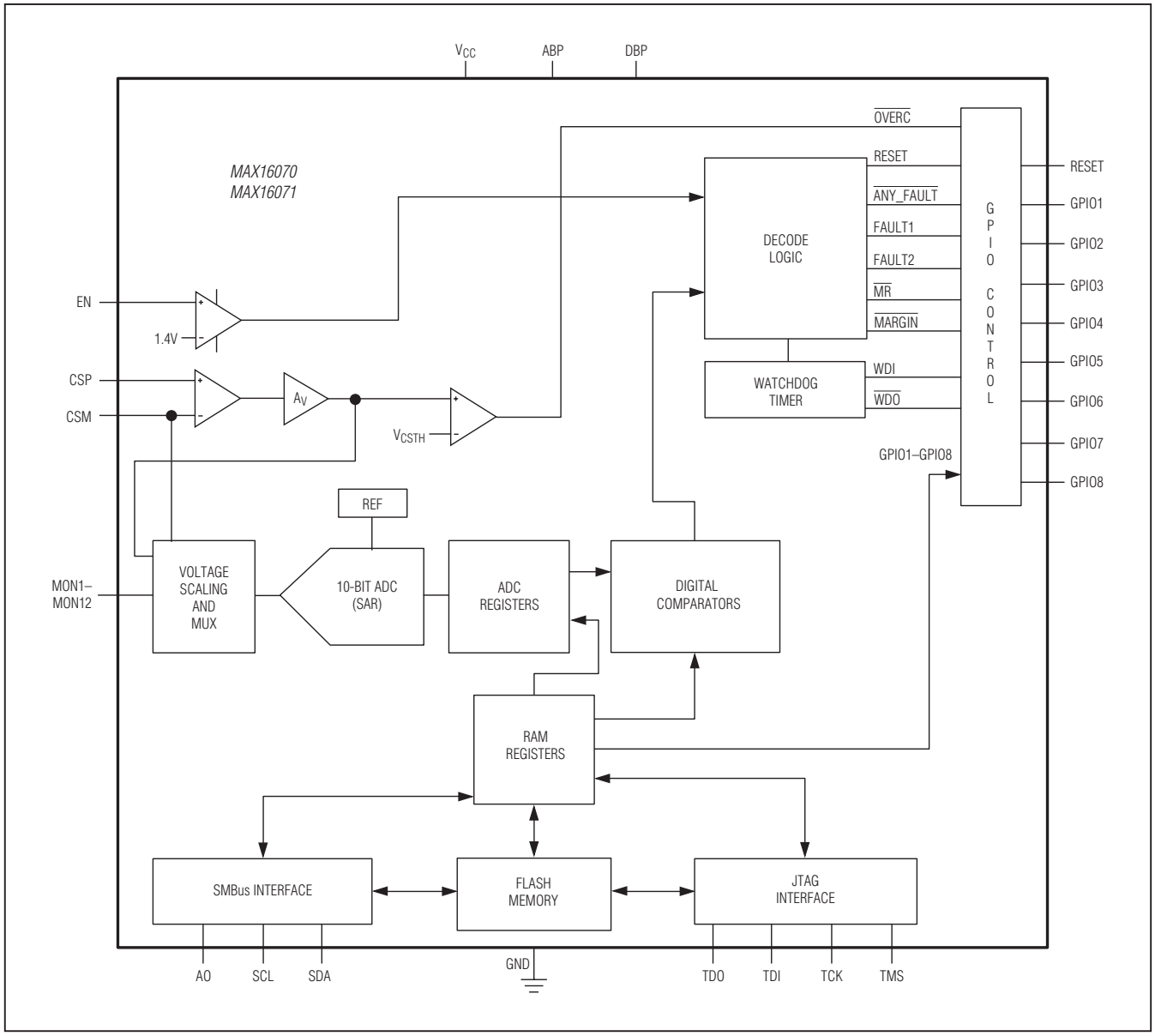
RESET OUTPUT CURRENT vs. SUPPLY VOLTAGE



Pin Description

PIN		NAME	FUNCTION
MAX16070	MAX16071		
1–5, 34, 35, 40	1–5, 36, 37, 40	MON2–MON6, MON7, MON8, MON1	Monitor Voltage Input 1–Monitor Voltage Input 8. Set monitor voltage range through configuration registers. Measured value written to the ADC register can be read back through the SMBus or JTAG interface.
6	6	CSP	Current-Sense Amplifier Positive Input. Connect CSP to the source side of the external sense resistor.
7	7	CSM	Current-Sense Amplifier Negative Input. Connect CSM to the load side of the external sense resistor.
8	8	RESET	Configurable Reset Output
9	9	TMS	JTAG Test Mode Select
10	10	TDI	JTAG Test Data Input
11	11	TCK	JTAG Test Clock
12	12	TDO	JTAG Test Data Output
13	13	SDA	SMBus Serial-Data Open-Drain Input/Output
14	14	A0	Four-State SMBus Address. Address sampled upon POR.
15	15	SCL	SMBus Serial Clock Input
16, 33	16, 35	GND	Ground
17, 18	—	GPIO7, GPIO8	General-Purpose Input/Output 7 and General-Purpose Input/Output 8. GPIO_s can be configured to act as a TTL input, a push-pull, open-drain, or high-impedance output or a pulldown circuit during a fault event or reverse sequencing.
19–24	17–22	GPIO1–GPIO6	General-Purpose Input/Output 1–General-Purpose Input/Output 6. GPIO_s can be configured to act as a TTL input, a push-pull, open-drain, or high-impedance output or a pulldown circuit during a fault event.
25, 26, 27, 29	23–28, 30, 38, 39	N.C.	No Connection. Not internally connected.
28	29	EN	Analog Enable Input. All outputs deassert when V_{EN} is below the enable threshold.
30	31, 32	DBP	Digital Bypass. All push-pull outputs are referenced to DBP. Bypass DBP with a 1µF capacitor to GND.
31	33	V_{CC}	Device Power Supply. Connect V_{CC} to a voltage from 2.8V to 14V. Bypass V_{CC} with a 10µF capacitor to GND.
32	34	ABP	Analog Bypass. Bypass ABP with a 1µF ceramic capacitor to GND.
36–39	—	MON9–MON12	Monitor Voltage Input 9–Monitor Voltage Input 12. Set monitor voltage range through configuration registers. Measured value written to the ADC register can be read back through the SMBus or JTAG interface.
—	—	EP	Exposed Pad. Internally connected to GND. Connect to ground, but do not use as the main ground connection.

Functional Diagram



Detailed Description

The MAX16070 monitors up to twelve system power supplies and the MAX16071 can monitor up to eight system power supplies. After boot-up, if EN is high and the software enable bit is set to '1,' monitoring begins based on the configuration stored in flash. An internal multiplexer cycles through each MON_ input. At each multiplexer stop, the 10-bit ADC converts the monitored analog voltage to a digital result and stores the result in a register. Each time a conversion cycle (50µs, max) completes, internal logic circuitry compares the conversion results to the overvoltage and undervoltage thresholds stored in memory. When a result violates a programmed threshold, the conversion can be configured to generate a fault. GPIO_ can be programmed to assert on combinations of faults. Additionally, faults can be configured to shut off the system and trigger the nonvolatile fault logger, which writes all fault information automatically to the flash and write-protects the data to prevent accidental erasure.

The MAX16070/MAX16071 contain both SMBus and JTAG serial interfaces for accessing registers and flash. Use only one interface at any given time. For more information on how to access the internal memory through these interfaces, see the *SMBus-Compatible Interface* and *JTAG Serial Interface* sections. The memory map is divided into three pages with access controlled by special SMBus and JTAG commands.

The factory-default values at POR (power-on reset) for all RAM registers are '0's. POR occurs when V_{CC} reaches the undervoltage-lockout threshold (UVLO) of 2.8V (max). At POR, the device begins a boot-up sequence. During the boot-up sequence, all monitored inputs are masked from initiating faults and flash contents are copied to the respective register locations. During boot-up, the MAX16070/MAX16071 are not accessible through the serial interface. The boot-up sequence takes up to 150µs, after which the device is ready for normal operation. RESET is asserted low up to the boot-up phase and remains asserted for its programmed timeout period once sequencing is completed and all monitored channels are within their respective thresholds. Up to the boot-up phase, the GPIO_s are high impedance.

Power

Apply 2.8V to 14V to V_{CC} to power the MAX16070/MAX16071. Bypass V_{CC} to ground with a 10µF capacitor. Two internal voltage regulators, ABP and DBP, supply power to the analog and digital circuitry within the device. For operation at 3.6V or lower, disable the regulators by connecting ABP and DBP to V_{CC}.

ABP is a 3.0V (typ) voltage regulator that powers the internal analog circuitry. Bypass ABP to GND with a 1µF ceramic capacitor installed as close to the device as possible.

DBP is an internal 3.0V (typ) voltage regulator. DBP powers flash and digital circuitry. All push-pull outputs refer to DBP. Bypass the DBP output to GND with a 1µF ceramic capacitor installed as close as possible to the device.

Do not power external circuitry from ABP or DBP.

Enable

To enable monitoring, the voltage at EN must be above 1.4V and the software enable bit in r73h[0] must be set to '1.' To power down and disable monitoring, either pull EN below 1.35V or set the Software Enable bit to '0.' See Table 1 for the software enable bit configurations. Connect EN to ABP if not used.

Table 1. Software Enable Configurations

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
73h	273h	[0]	Software enable
		[1]	Reserved
		[2]	1 = Margin mode enabled
		[3]	Early warning threshold select 0 = Early warning is undervoltage 1 = Early warning is overvoltage
		[4]	Independent watchdog mode enable 1 = Watchdog timer is independent of sequencer 0 = Watchdog timer boots after sequence completes

When in the monitoring state, a register bit, ENRESET, is set to a '1' when EN falls below the undervoltage threshold. This register bit latches and must be cleared through software. This bit indicates if RESET asserted low due to EN going under the threshold. The POR state of ENRESET is '0'. The bit is only set on a falling edge of the EN comparator output or the software enable bit.

Voltage/Current Monitoring

The MAX16070/MAX16071 feature an internal 10-bit ADC that monitors the MON_ voltage inputs. An internal multiplexer cycles through each of the enabled inputs, taking less than 40µs for a complete monitoring cycle. Each acquisition takes approximately 3.2µs. At each multiplexer stop, the 10-bit ADC converts the analog input to a digital result and stores the result in a register. ADC conversion results are stored in registers r00h to r1Ah (see Table 6). Use the SMBus or JTAG serial interface to read ADC conversion results.

The MAX16070 provides twelve inputs, MON1 to MON12, for voltage monitoring. The MAX16071 provides eight inputs, MON1 to MON8, for voltage monitoring. Each input voltage range is programmable in registers r43h to r45h (see Table 5). When MON_ configuration registers are set to '11,' MON_ voltages are not monitored, and the multiplexer does not stop at these inputs, decreasing the total cycle time. These inputs cannot be configured to trigger fault conditions.

The three programmable thresholds for each monitored voltage include an overvoltage, an undervoltage, and a secondary warning threshold that can be set in r73h[3] to be either an undervoltage or overvoltage threshold. See the *Faults* section for more information on setting overvoltage and undervoltage thresholds. All voltage thresholds are 8 bits wide. The 8 MSBs of the 10-bit ADC conversion result are compared to these overvoltage and undervoltage thresholds.

Inputs that are not enabled are not converted by the ADC; they contain the last value acquired before that channel was disabled.

The ADC conversion result registers are reset to 00h at boot-up. These registers are not reset when a reboot command is executed.

Configure the MAX16070/MAX16071 for differential mode in r46h (Table 5). The possible differential pairs are MON1/MON2, MON3/MON4, MON5/MON6, MON7/MON8, MON9/MON10, MON11/MON12 with the first input always being at a higher voltage than the second. Use differential voltage sensing to eliminate voltage offsets or measure supply current. See Figure 3. In differential mode, the odd-numbered MON_ input measures the absolute voltage with respect to GND while the result of the even input is the difference between the odd and even inputs. See Figure 3 for the typical differential measurement circuit.

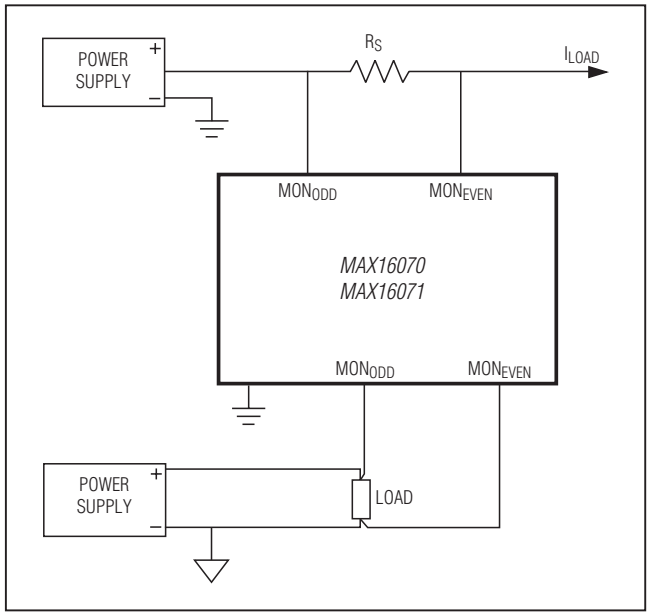


Figure 3. Differential Measurement Connections

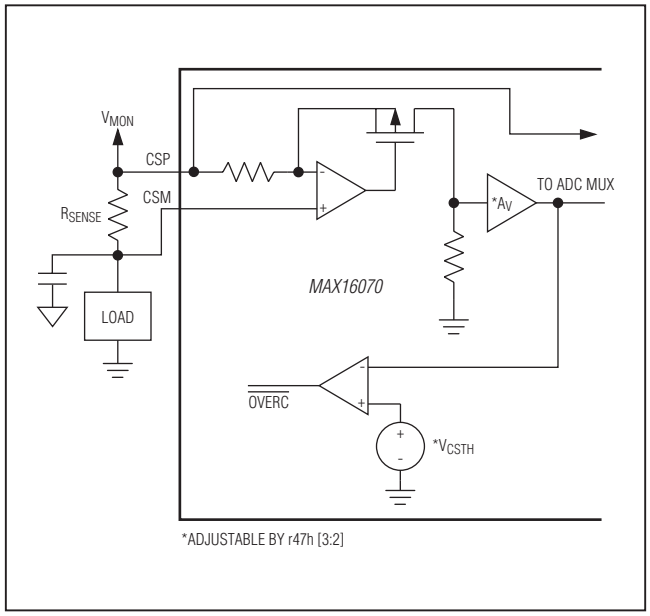


Figure 4. Current-Sense Amplifier

Boot-Up Delay

Once EN is above its threshold and the software-enable bit is set, a boot-up delay occurs before monitoring begins. This delay is configured in register r77h[3:0] as shown in Tables 2 and 3.

Internal Current-Sense Amplifier

The current-sense inputs, CSP/CSM, and a current-sense amplifier facilitate power monitoring (see Figure 4). The voltage on CSP relative to GND is also monitored by the ADC when the current-sense amplifier is enabled with r47h[0]. The conversion results are located in registers r19h and r1Ah (see Table 6). There are two selectable voltage ranges for CSP set by r47h[1], see Table 4. Although the voltage can be monitored over SMBus or JTAG, this voltage has no threshold comparators and cannot trigger any faults. Regarding the current-sense amplifier, there are four selectable ranges and the ADC output for a current-sense conversion is:

$$X_{ADC} = (V_{SENSE} \times A_V)/1.4V \times (2^8 - 1)$$

where X_{ADC} is the 8-bit decimal ADC result in register r18h, V_{SENSE} is V_{CSP} - V_{CSM}, and A_V is the current-sense voltage gain set by r47h[3:2].

In addition, there are two programmable current-sense trip thresholds: primary overcurrent and secondary overcurrent. For fast fault detection, the primary overcurrent threshold is implemented with an analog comparator connected to the internal $\overline{OVERC}$ signal. The $\overline{OVERC}$ signal can be output on one of the GPIO_s. See the *General-Purpose Inputs/Outputs* section for configuring the GPIO_ to output the $\overline{OVERC}$ signal. The primary threshold is set by:

$$I_{TH} = V_{CSTH}/R_{SENSE}$$

where I_{TH} is the current threshold to be set, V_{CSTH} is the threshold set by r47h[3:2], and R_{SENSE} is the value of the sense resistor. See Table 4 for a description of r47h. $\overline{OVERC}$ depends only on the primary overcurrent threshold. The secondary overcurrent threshold is implemented through ADC conversions and digital comparison set by r6Ch. The secondary overcurrent threshold includes programmable time delay options located in r73h[6:5]. Primary and secondary current-sense faults are enabled/disabled through r47h[0].

Table 2. Boot-Up Delay Register

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
77h	277h	[3:0]	Boot-up delay
		[7:0]	Reserved

Table 3. Boot-Up Delay Values

CODE	VALUE
0000	25µs
0001	500µs
0010	1ms
0011	2ms
0100	3ms
0101	4ms
0110	6ms
0111	8ms
1000	10ms
1001	12ms
1010	25ms
1011	100ms
1100	200ms
1101	400ms
1110	800ms
1111	1.6s

Table 4. Overcurrent Primary Threshold and Current-Sense Control

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
47h	247h	[0]	1 = Current sense is enabled 0 = Current sense is disabled
		[1]	1 = CSP full-scale range is 14V 0 = CSP full-scale range is 7V
		[3:2]	Overcurrent primary threshold and current-sense gain setting 00 = 200mV threshold, A_V = 6V/V 01 = 100mV threshold, A_V = 12V/V 10 = 50mV threshold, A_V = 24V/V 11 = 25mV threshold, A_V = 48V/V
73h	273h	[6:5]	Overcurrent secondary threshold deglitch 00 = No delay 01 = 14ms 10 = 15ms 11 = 60ms

Table 5. ADC Configuration Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
43h	243h	[1:0]	ADC1 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	ADC2 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[5:4]	ADC3 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:6]	ADC4 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted

Table 5. ADC Configuration Registers (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
44h	244h	[1:0]	ADC5 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	ADC6 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[5:4]	ADC7 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:6]	ADC8 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
45h	245h	[1:0]	ADC9 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[3:2]	ADC10 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[5:4]	ADC11 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted
		[7:6]	ADC12 full-scale range 00 = 5.6V 01 = 2.8V 10 = 1.4V 11 = Channel not converted

Table 5. ADC Configuration Registers (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
46h	246h	[0]	Differential conversion ADC1, ADC2 0 = Disabled 1 = Enabled
		[1]	Differential conversion ADC3, ADC4 0 = Disabled 1 = Enabled
		[2]	Differential conversion ADC5, ADC6 0 = Disabled 1 = Enabled
		[3]	Differential conversion ADC7, ADC8 0 = Disabled 1 = Enabled
		[4]	Differential conversion ADC9, ADC10 0 = Disabled 1 = Enabled
		[5]	Differential conversion ADC11, ADC12 0 = Disabled 1 = Enabled

Table 6. ADC Conversion Results (Read Only)

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
00h	[7:0]	ADC1 result (MSB) bits 9–2
01h	[7:6]	ADC1 result (LSB) bits 1, 0
02h	[7:0]	ADC2 result (MSB) bits 9–2
03h	[7:6]	ADC2 result (LSB) bits 1, 0
04h	[7:0]	ADC3 result (MSB) bits 9–2
05h	[7:6]	ADC3 result (LSB) bits 1, 0
06h	[7:0]	ADC4 result (MSB) bits 9–2
07h	[7:6]	ADC4 result (LSB) bits 1, 0
08h	[7:0]	ADC5 result (MSB) bits 9–2
09h	[7:6]	ADC5 result (LSB) bits 1, 0
0Ah	[7:0]	ADC6 result (MSB) bits 9–2
0Bh	[7:6]	ADC6 result (LSB) bits 1, 0
0Ch	[7:0]	ADC7 result (MSB) bits 9–2
0Dh	[7:6]	ADC7 result (LSB) bits 1, 0
0Eh	[7:0]	ADC8 result (MSB) bits 9–2
0Fh	[7:6]	ADC8 result (LSB) bits 1, 0
10h	[7:0]	ADC9 result (MSB) bits 9–2
11h	[7:6]	ADC9 result (LSB) bits 1, 0
12h	[7:0]	ADC10 result (MSB) bits 9–2
13h	[7:6]	ADC10 result (LSB) bits 1, 0
14h	[7:0]	ADC11 result (MSB) bits 9–2
15h	[7:6]	ADC11 result (LSB) bits 1, 0
16h	[7:0]	ADC12 result (MSB) bits 9–2
17h	[7:6]	ADC12 result (LSB) bits 1, 0
18h	[7:0]	Current-sense ADC result
19h	[7:0]	CSP ADC output (MSB) bits 9–2
1Ah	[7:6]	CSP ADC output (LSB) bits 1, 0

General-Purpose Inputs/Outputs

GPIO1 to GPIO8 are programmable general-purpose inputs/outputs. GPIO1–GPIO8 are configurable as a manual reset input, a watchdog timer input and output, logic inputs/outputs, fault-dependent outputs. When programmed as outputs, GPIO_s are open drain or push-pull. See Tables 8 and 9 for more detailed information on configuring GPIO1 to GPIO8.

When GPIO1 to GPIO8 are configured as general-purpose inputs/outputs, read values from the GPIO_ ports through r1Eh and write values to GPIO_s through r3Eh. Note that r3Eh has a corresponding flash register, which programs the default state of a general-purpose output. See Table 7 for more information on reading and writing to the GPIO_.

Table 7. GPIO_ State Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
1Eh	—	[0]	GPIO1 input state
		[1]	GPIO2 input state
		[2]	GPIO3 input state
		[3]	GPIO4 input state
		[4]	GPIO5 input state
		[5]	GPIO6 input state
		[6]	GPIO7 input state
		[7]	GPIO8 input state
3Eh	23Eh	[0]	GPIO1 output state
		[1]	GPIO2 output state
		[2]	GPIO3 output state
		[3]	GPIO4 output state
		[4]	GPIO5 output state
		[5]	GPIO6 output state
		[6]	GPIO7 output state
		[7]	GPIO8 output state

Table 8. GPIO_ Configuration Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
3Fh	23Fh	[2:0]	GPIO1 configuration
		[5:3]	GPIO2 configuration
		[7:6]	GPIO3 configuration (LSB)
40h	240h	[0]	GPIO3 configuration (MSB)
		[3:1]	GPIO4 configuration
		[6:4]	GPIO5 configuration
		[7]	GPIO6 configuration (LSB)
41h	241h	[1:0]	GPIO6 configuration (MSB)
		[4:2]	GPIO7 configuration
		[7:5]	GPIO8 configuration

Table 8. GPIO_ Configuration Registers (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
42h	242h	[0]	Output configuration for GPIO1 0 = Push-pull 1 = Open drain
		[1]	Output configuration for GPIO2 0 = Push-pull 1 = Open drain
		[2]	Output configuration for GPIO3 0 = Push-pull 1 = Open drain
		[3]	Output configuration for GPIO4 0 = Push-pull 1 = Open drain
		[4]	Output configuration for GPIO5 0 = Push-pull 1 = Open drain
		[5]	Output configuration for GPIO6 0 = Push-pull 1 = Open drain
		[6]	Output configuration for GPIO7 0 = Push-pull 1 = Open drain
		[7]	Output configuration for GPIO8 0 = Push-pull 1 = Open drain

Table 9. GPIO_ Function Configuration Bits

CODE	GPIO1	GPIO2	GPIO3	GPIO4	GPIO5	GPIO6	GPIO7	GPIO8
000	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input	Logic input
001	Logic output	Logic output	Logic output	Logic output	Logic output	Logic output	Logic output	Logic output
010	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output	Fault2 output
011	Fault1 output	Fault1 output	—	Fault1 output	Fault1 output	Fault1 output	Fault1 output	—
100	$\overline{\text{ANY\_FAULT}}$ output	—	$\overline{\text{ANY\_FAULT}}$ output	$\overline{\text{ANY\_FAULT}}$ output	$\overline{\text{ANY\_FAULT}}$ output	—	$\overline{\text{ANY\_FAULT}}$ output	—
101	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output	$\overline{\text{OVERC}}$ output
110	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output	$\overline{\text{MR}}$ input	$\overline{\text{WDO}}$ output
111	WDI input	—	—	$\overline{\text{EXTFAULT}}$ input/output	—	$\overline{\text{MARGIN}}$ input	—	$\overline{\text{EXTFAULT}}$ input/output

Fault1 and Fault2

GPIO1 to GPIO8 are configurable as dedicated fault outputs, Fault1 or Fault2. Fault outputs can assert on one or more overvoltage, undervoltage, or early warning conditions for selected inputs, as well as the secondary overcurrent comparator. Fault1 and Fault2 dependencies are set using registers r36h to r3Ah. See Table 10. When a fault output depends on more than one MON_, the fault output asserts when one or more MON_ exceeds a programmed threshold voltage. These fault outputs act independently of the critical fault system, described in the *Critical Faults* section.

Table 10. Fault1 and Fault2 Dependencies

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
36h	236h	0	1 = Fault1 depends on MON1
		1	1 = Fault1 depends on MON2
		2	1 = Fault1 depends on MON3
		3	1 = Fault1 depends on MON4
		4	1 = Fault1 depends on MON5
		5	1 = Fault1 depends on MON6
		6	1 = Fault1 depends on MON7
		7	1 = Fault1 depends on MON8
37h	237h	0	1 = Fault1 depends on MON9
		1	1 = Fault1 depends on MON10
		2	1 = Fault1 depends on MON11
		3	1 = Fault1 depends on MON12
		4	1 = Fault1 depends on the overvoltage thresholds of the inputs selected by r36h and r37h[3:0]
		5	1 = Fault1 depends on the undervoltage thresholds of the inputs selected by r36h and r37h[3:0]
		6	1 = Fault1 depends on the early warning thresholds of the inputs selected by r36h and r37h[3:0]
		7	0 = Fault1 is an active-low digital output 1 = Fault1 is an active-high digital output
38h	238h	[0]	1 = Fault2 depends on MON1
		[1]	1 = Fault2 depends on MON2
		[2]	1 = Fault2 depends on MON3
		[3]	1 = Fault2 depends on MON4
		[4]	1 = Fault2 depends on MON5
		[5]	1 = Fault2 depends on MON6
		[6]	1 = Fault2 depends on MON7
		[7]	1 = Fault2 depends on MON8

Table 10. Fault1 and Fault2 Dependencies (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
39h	239h	[0]	1 = Fault2 depends on MON9
		[1]	1 = Fault2 depends on MON10
		[2]	1 = Fault2 depends on MON11
		[3]	1 = Fault2 depends on MON12
		[4]	1 = Fault2 depends on the overvoltage thresholds of the inputs selected by r38h and r39h[3:0]
		[5]	1 = Fault2 depends on the undervoltage thresholds of the inputs selected by r38h and r39h[3:0]
		[6]	1 = Fault2 depends on the early warning thresholds of the inputs selected by r38h and r39h[3:0]
		[7]	0 = Fault2 is an active-low digital output 1 = Fault2 is an active-high digital output
3Ah	23Ah	[0]	1 = Fault1 depends on secondary overcurrent comparator
		[1]	1 = Fault2 depends on secondary overcurrent comparator
		[7:2]	Reserved

ANY_FAULT

GPIO1, GPIO3, GPIO4, GPIO5, and GPIO7 are configurable to assert low during any fault condition.

Overcurrent Comparator ($\overline{OVERC}$)

GPIO1 to GPIO8 are configurable to assert low when the voltage across CSP and CSM exceed the primary overcurrent threshold. See the *Internal Current-Sense Amplifier* section for more details.

Manual Reset ($\overline{MR}$)

GPIO1, GPIO3, GPIO5, and GPIO7 are configurable to act as an active-low manual reset input, $\overline{MR}$. Drive $\overline{MR}$ low to assert RESET. RESET remains asserted for the selected reset timeout period after $\overline{MR}$ transitions from low to high.

Watchdog Input (WDI) and Output ($\overline{WDO}$)

GPIO2, GPIO4, GPIO6, and GPIO8 are configurable as the watchdog timer output, $\overline{WDO}$. GPIO1 is configurable as WDI. See Table 17 for configuration details. $\overline{WDO}$ is an active-low output. See the *Watchdog Timer* section for more information about the operation of the watchdog timer.

External Fault ($\overline{EXTFAULT}$)

GPIO4 and GPIO8 are configurable as the external fault input/output. When configured as push-pull, $\overline{EXTFAULT}$ signals that a critical fault has occurred on one or more monitored voltages or current. When configured as open-drain, $\overline{EXTFAULT}$ can be asserted low by an external circuit to trigger a critical fault. This signal can be used to cascade multiple MAX16070/MAX16071s.

One configuration bit determines the behavior of the MAX16070/MAX16071 when $\overline{EXTFAULT}$ is pulled low by some other device. If register bit r6Dh[2] is set, $\overline{EXTFAULT}$ going low triggers a nonvolatile fault log operation.

Faults

The MAX16070/MAX16071 monitor the input (MON_) channels and compare the results with an overvoltage threshold, an undervoltage threshold, and a selectable overvoltage or undervoltage early warning threshold. Based on these conditions, the MAX16070/MAX16071 assert various fault outputs and save specific information about the channel conditions and voltages into the nonvolatile flash. Once a critical fault event occurs, the failing channel condition, ADC conversions at the time of the fault, or both can be saved by configuring the event logger. The event logger records a single failure in the internal flash and sets a lock bit that protects the stored fault data from accidental erasure on a subsequent power-up.

An overvoltage event occurs when the voltage at a monitored input exceeds the overvoltage threshold for that input. An undervoltage event occurs when the voltage at a monitored input falls below the undervoltage threshold. Fault thresholds are set in registers r48h to r6Ch as shown in Table 11. Disabled inputs are not monitored for fault conditions and are skipped over by the input multiplexer. Only the upper 8 bits of a conversion result are compared with the programmed fault thresholds.

Table 11. Fault Threshold Registers

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
48h	248h	[7:0]	MON1 secondary threshold
49h	249h	[7:0]	MON1 overvoltage threshold
4Ah	24Ah	[7:0]	MON1 undervoltage threshold
4Bh	24Bh	[7:0]	MON2 secondary threshold
4Ch	24Ch	[7:0]	MON2 overvoltage threshold
4Dh	24Dh	[7:0]	MON2 undervoltage threshold
4Eh	24Eh	[7:0]	MON3 secondary threshold
4Fh	24Fh	[7:0]	MON3 overvoltage threshold
50h	250h	[7:0]	MON3 undervoltage threshold
51h	251h	[7:0]	MON4 secondary threshold
52h	252h	[7:0]	MON4 overvoltage threshold
53h	253h	[7:0]	MON4 undervoltage threshold
54h	254h	[7:0]	MON5 secondary threshold
55h	255h	[7:0]	MON5 overvoltage threshold
56h	256h	[7:0]	MON5 undervoltage threshold
57h	257h	[7:0]	MON6 secondary threshold
58h	258h	[7:0]	MON6 overvoltage threshold
59h	259h	[7:0]	MON6 undervoltage threshold
5Ah	25Ah	[7:0]	MON7 secondary threshold
5Bh	25Bh	[7:0]	MON7 overvoltage threshold
5Ch	25Ch	[7:0]	MON7 undervoltage threshold
5Dh	25Dh	[7:0]	MON8 secondary threshold
5Eh	25Eh	[7:0]	MON8 overvoltage threshold
5Fh	25Fh	[7:0]	MON8 undervoltage threshold
60h	260h	[7:0]	MON9 secondary threshold
61h	261h	[7:0]	MON9 overvoltage threshold
62h	262h	[7:0]	MON9 undervoltage threshold
63h	263h	[7:0]	MON10 secondary threshold
64h	264h	[7:0]	MON10 overvoltage threshold
65h	265h	[7:0]	MON10 undervoltage threshold
66h	266h	[7:0]	MON11 secondary threshold
67h	267h	[7:0]	MON11 overvoltage threshold
68h	268h	[7:0]	MON11 undervoltage threshold
69h	269h	[7:0]	MON12 secondary threshold
6Ah	26Ah	[7:0]	MON12 overvoltage threshold
6Bh	26Bh	[7:0]	MON12 undervoltage threshold
6Ch	26Ch	[7:0]	Secondary overcurrent threshold

The general-purpose inputs/outputs (GPIO1 to GPIO8) can be configured as $\overline{\text{ANY\_FAULT}}$ outputs or dedicated Fault1 and Fault2 outputs to indicate fault conditions. These fault outputs are not masked by the critical fault enable bits shown in Table 14. See the *General-Purpose Inputs/Outputs* section for more information on configuring GPIO_s as fault outputs.

Deglitch

Fault conditions are detected at the end of each conversion. When the voltage on an input falls outside a monitored threshold for one acquisition, the input multiplexer remains on that channel and performs several successive conversions. To trigger a fault, the input must stay outside the threshold for a certain number of acquisitions as determined by the deglitch setting in r73h[6:5] and r74h[6:5] (see Table 12).

Fault Flags

Fault flags indicate the fault status of a particular input. The fault flag of any monitored input in the device can be read at any time from registers r1Bh and r1Ch, as shown in Table 13. Clear a fault flag by writing a '1' to the appropriate bit in the flag register. Unlike the fault signals sent to the fault outputs, these bits are masked by the Critical Fault Enable bits (see Table 14). The fault flag is only set when the matching enable bit in the critical fault enable register is also set.

Table 12. Deglitch Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
73h	273h	[6:5]	Overcurrent comparator deglitch time 00 = No deglitch 01 = 4ms 10 = 15ms 11 = 60ms
74h	274h	[6:5]	Voltage comparator deglitch configuration 00 = 2 cycles 01 = 4 cycles 10 = 8 cycles 11 = 16 cycles

Table 13. Fault Flags

REGISTER ADDRESS	BIT RANGE	DESCRIPTION
1Bh	[0]	MON1
	[1]	MON2
	[2]	MON3
	[3]	MON4
	[4]	MON5
	[5]	MON6
	[6]	MON7
	[7]	MON8
1Ch	[0]	MON9
	[1]	MON10
	[2]	MON11
	[3]	MON12
	[4]	Overcurrent
	[5]	External fault ($\overline{\text{EXTFAULT}}$)
	[6]	SMB alert

Table 14. Critical Fault Configuration

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
6Dh	26Dh	[1:0]	Fault information to log 00 = Save failed line flags and ADC values in flash 01 = Save only failed line flags in flash 10 = Save only ADC values in flash 11 = Do not save anything
		[2]	1 = Fault log triggered when $\overline{\text{EXTFAULT}}$ is pulled low externally
		[7:3]	Not used
6Eh	26Eh	[0]	1 = Fault log triggered when MON1 is below its undervoltage threshold
		[1]	1 = Fault log triggered when MON2 is below its undervoltage threshold
		[2]	1 = Fault log triggered when MON3 is below its undervoltage threshold
		[3]	1 = Fault log triggered when MON4 is below its undervoltage threshold
		[4]	1 = Fault log triggered when MON5 is below its undervoltage threshold
		[5]	1 = Fault log triggered when MON6 is below its undervoltage threshold
		[6]	1 = Fault log triggered when MON7 is below its undervoltage threshold
		[7]	1 = Fault log triggered when MON8 is below its undervoltage threshold
6Fh	26Fh	[0]	1 = Fault log triggered when MON9 is below its undervoltage threshold
		[1]	1 = Fault log triggered when MON10 is below its undervoltage threshold
		[2]	1 = Fault log triggered when MON11 is below its undervoltage threshold
		[3]	1 = Fault log triggered when MON12 is below its undervoltage threshold
		[4]	1 = Fault log triggered when MON1 is above its overvoltage threshold
		[5]	1 = Fault log triggered when MON2 is above its overvoltage threshold
		[6]	1 = Fault log triggered when MON3 is above its overvoltage threshold
		[7]	1 = Fault log triggered when MON4 is above its overvoltage threshold
70h	270h	[0]	1 = Fault log triggered when MON5 is above its overvoltage threshold
		[1]	1 = Fault log triggered when MON6 is above its overvoltage threshold
		[2]	1 = Fault log triggered when MON7 is above its overvoltage threshold
		[3]	1 = Fault log triggered when MON8 is above its overvoltage threshold
		[4]	1 = Fault log triggered when MON9 is above its overvoltage threshold
		[5]	1 = Fault log triggered when MON10 is above its overvoltage threshold
		[6]	1 = Fault log triggered when MON11 is above its overvoltage threshold
		[7]	1 = Fault log triggered when MON12 is above its overvoltage threshold
71h	271h	[0]	1 = Fault log triggered when MON1 is above/below the early threshold warning
		[1]	1 = Fault log triggered when MON2 is above/below the early threshold warning
		[2]	1 = Fault log triggered when MON3 is above/below the early threshold warning
		[3]	1 = Fault log triggered when MON4 is above/below the early threshold warning
		[4]	1 = Fault log triggered when MON5 is above/below the early threshold warning
		[5]	1 = Fault log triggered when MON6 is above/below the early threshold warning
		[6]	1 = Fault log triggered when MON7 is above/below the early threshold warning
		[7]	1 = Fault log triggered when MON8 is above/below the early threshold warning

Table 14. Critical Fault Configuration (continued)

REGISTER ADDRESS	FLASH ADDRESS	BIT RANGE	DESCRIPTION
72h	272h	[0]	1 = Fault log triggered when MON9 is above/below the early threshold warning
		[1]	1 = Fault log triggered when MON10 is above/below the early threshold warning
		[2]	1 = Fault log triggered when MON11 is above/below the early threshold warning
		[3]	1 = Fault log triggered when MON12 is above/below the early threshold warning
		[4]	1 = Fault log triggered when overcurrent early threshold is exceeded
		[5]	Reserved, must be set to '1'
		[7:6]	Reserved

If a GPIO_ is configured as an open-drain $\overline{\text{EXTFAULT}}$ input/output, and $\overline{\text{EXTFAULT}}$ is pulled low by an external circuit, bit r1Ch[5] is set.

The SMB Alert bit is set if the MAX16070/MAX16071 have asserted the SMBus Alert output. Clear by writing a '1'. See *SMBALERT* section for more details.

Critical Faults

During normal operation, a fault condition can be configured to store fault information in the flash memory by setting the appropriate critical fault enable bits. Set the appropriate critical fault enable bits in registers r6Eh to r72h (see Table 14) for a fault condition to trigger a critical fault.

Logged fault information is stored in flash registers r200h to r20Fh (see Table 15). After fault information is logged, the flash is locked and must be unlocked to enable a new fault log to be stored. Write a '0' to r8Ch[1] to unlock the fault flash. Fault information can be configured to store ADC conversion results and/or fault flags in registers. Select the critical fault configuration in r6Dh[1:0]. Set r6Dh[1:0] to '11' to turn off the fault logger. All stored ADC results are 8 bits wide.

Table 15. Nonvolatile Fault Log Registers

FLASH ADDRESS	BIT RANGE	DESCRIPTION
200h	—	Reserved
201h	[0]	Fault log triggered on MON1
	[1]	Fault log triggered on MON2
	[2]	Fault log triggered on MON3
	[3]	Fault log triggered on MON4
	[4]	Fault log triggered on MON5
	[5]	Fault log triggered on MON6
	[6]	Fault log triggered on MON7
	[7]	Fault log triggered on MON8
202h	[0]	Fault log triggered on MON9
	[1]	Fault log triggered on MON10
	[2]	Fault log triggered on MON11
	[3]	Fault log triggered on MON12
	[4]	Fault log triggered on overcurrent
	[5]	Fault log triggered on $\overline{\text{EXTFAULT}}$
	[7:6]	Not used