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19-1566; Rev 2; 1/01

MAXIM

Advanced Chemistry-Independent, Level 2 Battery Chargers with Input Current Limiting

General Description

The MAX1645 are high-efficiency battery chargers capable of charging batteries of any chemistry type. It uses the Intel System Management Bus (SMBus™) to control voltage and current charge outputs.

When charging lithium-ion (Li+) batteries, the MAX1645 automatically transition from regulating current to regulating voltage. The MAX1645 can also limit line input current so as not to exceed a predetermined current drawn from the DC source. A 175s charge safety timer prevents "runaway charging" should the MAX1645 stop receiving charging voltage/ current commands.

The MAX1645 employs a next-generation synchronous buck control circuity that lowers the minimum input-to-output voltage drop by allowing the duty cycle to exceed 99%. The MAX1645 can easily charge one to four series Li+ cells.

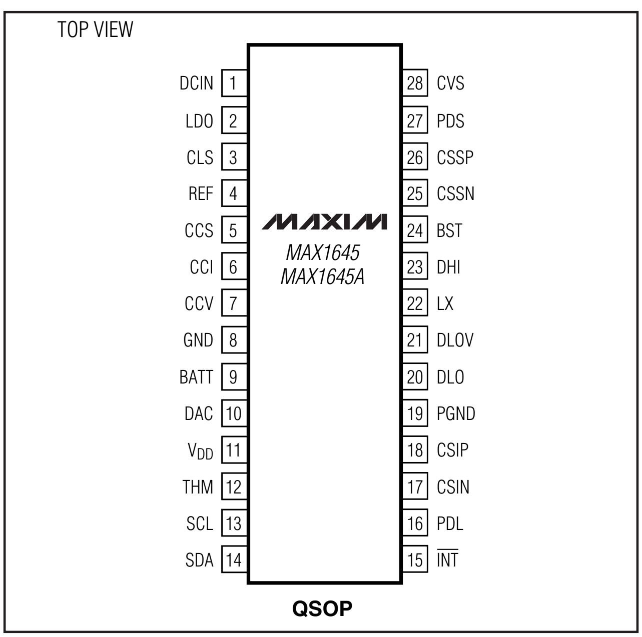
Applications

Notebook Computers
Point-of-Sale Terminals
Personal Digital Assistants

Features

- ♦ **Input Current Limiting**
- ♦ **175s Charge Safety Timeout**
- ♦ **128mA Wake-Up Charge**
- ♦ **Charges Any Chemistry Battery: Li+, NiCd, NiMH, Lead Acid, etc.**
- ♦ **Intel SMBus 2-Wire Serial Interface**
- ♦ **Compliant with Level 2 Smart Battery Charger Spec Rev. 1.0**
- ♦ **+8V to +28V Input Voltage Range**
- ♦ **Up to 18.4V Battery Voltage**
- ♦ **11-Bit Battery Voltage Setting**
- ♦ **±0.8% Output Voltage Accuracy with Internal Reference**
- ♦ **3A max Battery Charge Current**
- ♦ **6-Bit Charge Current Setting**
- ♦ **99.99% max Duty Cycle for Low-Dropout Operation**
- ♦ **Load/Source Switchover Drivers**
- ♦ **>97% Efficiency**

Pin Configuration



Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX1645EEI	-40°C to +85°C	28 QSOP
MAX1645AEEI	-40°C to +85°C	28 QSOP

Typical Operating Circuit appears at end of data sheet.

SMBus is a trademark of Intel Corp.

Advanced Chemistry-Independent, Level 2 Battery Chargers with Input Current Limiting

ABSOLUTE MAXIMUM RATINGS

DCIN, CVS, CSSP, CSSN, LX to GND....................-0.3V to +30V
CSSP to CSSN, CSIP to CSIN ....-0.3V to +0.3V
PDS, PDL to GND ....-0.3V to (V_{CSSP} + 0.3V)
BST to LX..-0.3V to +6V
DHI to LX ....-0.3V to (V_{BST} + 0.3V)
CSIP, CSIN, BATT to GND ....-0.3V to +22V
LDO to GND ....-0.3V to (lower of 6V or V_{DCIN} + 0.3V)
DLO to GND ....-0.3V to (V_{DLOV} + 0.3V)
REF, DAC, CCV, CCI, CCS, CLS to GND.....-0.3V to (V_{LDO} + 0.3V)
V_{DD}, SCL, SDA, INT, DLOV to GND.........................-0.3V to +6V
THM to GND ....-0.3V to (V_{DD} + 0.3V)
PGND to GND ....-0.3V to +0.3V
LDO Continuous Current..50mA
Continuous Power Dissipation (T_A = +70°C)
28-Pin QSOP (derate 10.8mW/°C above +70°C).........860mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature...-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{DD} = +3.3V, V_{BATT} = +16.8V, V_{DCIN} = +18V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL SPECIFICATIONS							
DCIN Typical Operating Range	V_{DCIN}			8		28	V
DCIN Supply Current	I_{DCIN}	8V < V_{DCIN} < 28V			1.7	6	mA
DCIN Supply Current Charging Inhibited		8V < V_{DCIN} < 28V			0.7	2	mA
DCIN Undervoltage Threshold		When AC_PRESENT switches	DCIN rising		7.5	7.85	V
			DCIN falling	7	7.4		
LDO Output Voltage	V_{LDO}	8V < V_{DCIN} < 28V, 0 < I_{LDO} < 15mA		5.15	5.4	5.65	V
V_{DD} Input Voltage Range (Note 1)		8V < V_{DCIN} < 28V		2.8		5.65	V
V_{DD} Undervoltage Threshold		When the SMB responds to commands	V_{DD} rising		2.55	2.8	V
			V_{DD} falling	2.1	2.5		
V_{DD} Quiescent Current	I_{DD}	0 < V_{DCIN} < 6V, V_{DD} = 5V, V_{SCL} = 5V, V_{SDA} = 5V			80	150	µA
REF Output Voltage	V_{REF}	0 < I_{REF} < 200µA		4.066	4.096	4.126	V
BATT Undervoltage Threshold (Note 2)		When I_{CHARGE} drops to 128mA		2.4		2.8	V
PDS Charging Source Switch Turn-Off Threshold	$V_{PDS-OFF}$	V_{CVS} referred to V_{BATT}, V_{CVS} falling		50	100	150	mV
PDS Charging Source Switch Threshold Hysteresis	$V_{PDS-HYS}$	V_{CVS} referred to V_{BATT}		100	200	300	mV
PDS Output Low Voltage, PDS Below CSSP		I_{PDS} = 0		8	10	12	V
PDS Turn-On Current		PDS = CSSP		100	150	300	µA
PDS Turn-Off Current		V_{PDS} = V_{CSSP} - 2V, V_{DCIN} = 16V		10	50		mA
PDL Load Switch Turn-Off Threshold	$V_{PDL-OFF}$	V_{CVS} referred to V_{BATT}, V_{CVS} rising		-150	-100	-50	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DD} = +3.3V, V_{BATT} = +16.8V, V_{DCIN} = +18V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PDL Load Switch Threshold Hysteresis	$V_{PDL-HYS}$	V_{CVS} referred to V_{BATT}		100	200	300	mV
PDL Turn-Off Current		V_{CSSN} - V_{PDL} = 1V		6	12		mA
PDL Turn-On Resistance		PDL to GND		50	100	150	kΩ
CVS Input Bias Current		V_{CVS} = 28V			6	20	µA
BATT Full-Charge Voltage	V0	ChargingVoltage() = 0x41A0		16.666	16.8	16.934	V
		ChargingVoltage() = 0x3130		12.492	12.592	12.692	
		ChargingVoltage() = 0x20D0		8.333	8.4	8.467	
		ChargingVoltage() = 0x1060		4.150	4.192	4.234	
BATT Charge Current (Note 3)	I0	R_{CS} = 50mΩ	ChargingCurrent() = 0x0BC0	2.798	3.008	3.218	A
			ChargingCurrent() = 0x0080	61.6	128	194.4	mA
DCIN Source Current Limit (Note 3)		R_{CSS} = 40mΩ	V_{CLS} = 4.096V	4.714	5.12	5.526	A
			V_{CLS} = 2.048V	2.282	2.56	2.838	
BATT Undervoltage Charge Current		MAX1645	V_{BATT} = 1V, R_{CSI} = 50mΩ	20	128	200	mA
		MAX1645A	V_{BATT} = 1V, R_{CSI} = 50mΩ	61.6	128	194.4	
BATT/CSIP/CSIN Input Voltage Range				0		20	V
Total BATT Input Bias Current		Total of I_{BATT}, I_{CSIP}, and I_{CSIN}; V_{BATT} = 0 to 20V		-700		700	µA
Total BATT Quiescent Current		Total of I_{BATT}, I_{CSIP}, and I_{CSIN}; V_{BATT} = 0 to 20V, charge inhibited		-100		100	µA
Total BATT Standby Current		Total of I_{BATT}, I_{CSIP}, and I_{CSIN}; V_{BATT} = 0 to 20V, V_{DCIN} = 0		-5		5	µA
CSSP Input Bias Current		V_{CSSP} = V_{CSSN} = V_{DCIN} = 0 to 28V		-100	540	1000	µA
CSSN Input Bias Current		V_{CSSP} = C_{CSSN} = V_{DCIN} = 0 to 28V		-100	35	100	mA
CSSP/CSSN Quiescent Current		V_{CSSP} = V_{CSSN} = 28V, V_{DCIN} = 0		-1		1	µA
Battery Voltage-Error Amp DC Gain		From BATT to CCV		200	500		V/V
CLS Input Bias Current		V_{CLS} = V_{REF}/2 to V_{REF}		-1	0.05	1	µA
Battery Voltage-Error Amp Transconductance		From BATT to CCV, ChargingVoltage() = 0x41A0, V_{BATT} = 16.8V		0.111	0.222	0.444	µA/mV
Battery Current-Error Amp Transconductance		From CSIP/SCIN to CCI, ChargingCurrent() = 0x0BC0, V_{CSIP} - V_{CSIN} = 150.4mV		0.5	1	2	µA/mV
Input Current-Error Amp Transconductance		From CSSP/CSSN to CCS, V_{CLS} = 2.048V, V_{CSSP} - V_{CSSN} = 102.4mV		0.5	1	2	µA/mV
CCV/CCI/CCS Clamp Voltage (Note 4)		V_{CCV} = V_{CCI} = V_{CCS} = 0.25V to 2V		150	300	600	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DD} = +3.3V, V_{BATT} = +16.8V, V_{DCIN} = +18V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC-TO-DC CONVERTER SPECIFICATIONS						
Minimum Off-Time	t_{OFF}		1	1.25	1.5	µs
Maximum On-Time	t_{ON}		5	10	15	ms
Maximum Duty Cycle			99	99.99		%
LX Input Bias Current		V_{DCIN} = 28V, V_{BATT} = V_{LX} = 20V		200	500	µA
LX Input Quiescent Current		V_{DCIN} = 0, V_{BATT} = V_{LX} = 20V			1	µA
BST Supply Current		DHI high		6	15	µA
DLOV Supply Current		V_{DLOV} = V_{LDO}, DLO low		5	10	µA
Inductor Peak Current Limit		R_{CSI} = 50mΩ	5.0	6.0	7.0	A
DHI Output Resistance		DHI high or low, V_{BST} - V_{LX} = 4.5V		6	14	Ω
DLO Output Resistance		DLO high or low, V_{DLOV} = 4.5V		6	14	Ω
THERMISTOR COMPARATOR SPECIFICATIONS						
THM Input Bias Current		V_{THM} = 4% of V_{DD} to 96% of V_{DD}, V_{DD} = 2.8V to 5.65V	-1		1	µA
Thermistor Overrange Threshold		V_{DD} = 2.8V to 5.65V, V_{THM} falling	89.5	91	92.5	% of V_{DD}
Thermistor Cold Threshold		V_{DD} = 2.8V to 5.65V, V_{THM} falling	74	75.5	77	% of V_{DD}
Thermistor Hot Threshold		V_{DD} = 2.8V to 5.65V, V_{THM} falling	22	23.5	25	% of V_{DD}
Thermistor Underrange Threshold		V_{DD} = 2.8V to 5.65V, V_{THM} falling	6	7.5	9	% of V_{DD}
Thermistor Comparator Threshold Hysteresis		All 4 comparators, V_{DD} = 2.8V to 5.65V		1		% of V_{DD}
SMB INTERFACE LEVEL SPECIFICATIONS (V_{DD} = 2.8V to 5.65V)						
SDA/SCL Input Low Voltage					0.6	V
SDA/SCL Input High Voltage			1.4			V
SDA/SCL Input Hysteresis				220		mV
SDA/SCL Input Bias Current			-1		1	µA
SDA Output Low Sink Current		V_{SDA} = 0.4V	6			mA
$\overline{INT}$ Output High Leakage		$V_{\overline{INT}}$ = 5.65V			1	µA
$\overline{INT}$ Output Low Voltage		$I_{\overline{INT}}$ = 1mA		25	200	mV
SMB INTERFACE TIMING SPECIFICATIONS (V_{DD} = 2.8V to 5.65V, Figures 4 and 5)						
SCL High Period	t_{HIGH}		4			µs
SCL Low Period	t_{LOW}		4.7			µs
Start Condition Setup Time from SCL	$t_{SU:STA}$		4.7			µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		4			µs
SDA Setup Time from SCL	$t_{SU:DAT}$		250			ns
SDA Hold Time from SCL	$t_{HD:DAT}$		0			ns

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DD} = +3.3V, V_{BATT} = +16.8V, V_{DCIN} = +18V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SDA Output Data Valid from SCL	t_{DV}				1	µs
Maximum Charge Period Without a ChargingVoltage() or Charging Current() Loaded	t_{WDT}		140	175	210	s

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{DD} = +3.3V, V_{BATT} = +16.8V, V_{DCIN} = +18V, **T_A = -40°C to +85°C**, unless otherwise noted. Guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
GENERAL SPECIFICATIONS						
DCIN Typical Operating Range	V_{DCIN}			8	28	V
DCIN Supply Current	I_{DCIN}	8V < V_{DCIN} < 28V			6	mA
DCIN Supply Current Charging Inhibited		8V < V_{DCIN} < 28V			2	mA
DCIN Undervoltage Threshold		When AC_PRESENT switches	DCIN rising		7.85	V
			DCIN falling	7		
LDO Output Voltage	V_{LDO}	8V < V_{DCIN} < 28V, 0 < I_{LDO} < 15mA		5.15	5.65	V
V_{DD} Input Voltage Range (Note 1)		8V < V_{DCIN} < 28V		2.8	5.65	V
V_{DD} Undervoltage Threshold		When the SMB responds to commands	V_{DD} rising		2.8	V
			V_{DD} falling	2.1		
V_{DD} Quiescent Current	I_{DD}	0 < V_{DCIN} < 6V, V_{DD} = 5V, V_{SCL} = 5V, V_{SDA} = 5V			150	µA
REF Output Voltage	V_{REF}	0 < I_{REF} < 200µA		4.035	4.157	V
BATT Undervoltage Threshold (Note 2)		When I_{CHARGE} drops to 128mA		2.4	2.8	V
PDS Charging Source Switch Turn-Off Threshold	$V_{PDS-OFF}$	V_{CVS} referred to V_{BATT}, V_{CVS} falling		50	150	mV
PDS Charging Source Switch Threshold Hysteresis	$V_{PDS-HYS}$	V_{CVS} referred to V_{BATT}		100	300	mV
PDS Output Low Voltage, PDS Below CSSP		I_{PDS} = 0		8	12	V
PDS Turn-On Current		PDS = CSSP		100	300	µA
PDS Turn-Off Current		V_{PDS} = V_{CSSP} - 2V, V_{DCIN} = 16V		10		mA
PDL Load Switch Turn-Off Threshold	$V_{PDL-OFF}$	V_{CVS} referred to V_{BATT}, V_{CVS} rising		-150	-50	mV
PDL Load Switch Threshold Hysteresis	$V_{PDL-HYS}$	V_{CVS} referred to V_{BATT}		100	300	mV
PDL Turn-Off Current		V_{CSSN} - V_{PDL} = 1V		6		mA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DD} = +3.3V, V_{BATT} = +16.8V, V_{DCIN} = +18V, **T_A = -40°C to +85°C**, unless otherwise noted. Guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PDL Turn-On Resistance		PDL to GND		50	150	kΩ
CVS Input Bias Current		V_{CVS} = 28V			20	µA
ERROR AMPLIFIER SPECIFICATIONS						
BATT Full-Charge Voltage	V0	ChargingVoltage() = 0x41A0		16.532	17.068	V
		ChargingVoltage() = 0x3130		12.391	12.793	
		ChargingVoltage() = 0x20D0		8.266	8.534	
		ChargingVoltage() = 0x1060		4.124	4.260	
BATT Charge Current (Note 3)	I0	R_{CSI} = 50mΩ	ChargingCurrent() = 0x0BC0	2.608	3.408	A
			ChargingCurrent() = 0x0080	15.2	240.8	mA
DCIN Source Current Limit (Note 3)		R_{CSS} = 40mΩ	V_{CLS} = 4.096V	4.358	5.882	A
			V_{CLS} = 2.048V	2.054	3.006	
BATT Undervoltage Charge Current		V_{BATT} = 1V, R_{CSI} = 50mΩ		20	200	mA
BATT/CSIP/CSIN Input Voltage Range				0	20	V
Total BATT Input Bias Current		Total of I_{BATT}, I_{CSIP}, and I_{CSIN}; V_{BATT} = 0 to 20V		-700	700	µA
Total BATT Quiescent Current		Total of I_{BATT}, I_{CSIP}, and I_{CSIN}; V_{BATT} = 0 to 20V, charge inhibited		-100	100	µA
Total BATT Standby Current		Total of I_{BATT}, I_{CSIP}, and I_{CSIN}; V_{BATT} = 0 to 20V, V_{DCIN} = 0		-5	5	µA
CSSP/Input Bias Current		V_{CSSP} = V_{CSSN} = V_{DCIN} = 28V		-100	1000	µA
CSSN Input Bias Current		V_{CSSP} = V_{CSSN} = V_{DCIN} = 28V		-100	100	µA
CSSP/CSSN Quiescent Current		V_{CSSP} = V_{CSSN} = 28V, V_{DCIN} = 0		-1	1	µA
Battery Voltage-Error Amp DC Gain		From BATT to CCV		200		V/V
CLS Input Bias Current		V_{CLS} = V_{REF}/2 to V_{REF}		-1	1	µA
Battery Voltage-Error Amp Transconductance		From BATT to CCV, ChargingVoltage() = 0x41A0, V_{BATT} = 16.8V		0.111	0.444	µA/mV
Battery Current-Error Amp Transconductance		From CSIP/CSIN to CCI, ChargingCurrent() = 0x0BC0, V_{CSIP} -V_{CSIN} = 150.4mV		0.5	2	µA/mV
Input Current-Error Amp Transconductance		From CSSP/CSSN to CCS, V_{CLS} = 2.048V, V_{CSSP} - V_{CSSN} = 102.4mV		0.5	2	µA/mV
CCV/CCI/CCS Clamp Voltage (Note 4)		V_{CCV} = V_{CCI} = V_{CCS} = 0.25V to 2V		150	600	mV
DC-TO-DC CONVERTER SPECIFICATIONS						
Minimum Off-Time	t_{OFF}			1	1.5	µs
Maximum On-Time	t_{ON}			5	15	ms
Maximum Duty Cycle				99		%

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DD} = +3.3V, V_{BATT} = +16.8V, V_{DCIN} = +18V, **T_A = -40°C to +85°C**, unless otherwise noted. Guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
LX Input Bias Current		V_{DCIN} = 28V, V_{BATT} = V_{LX} = 20V		500	µA
LX Input Quiescent Current		V_{DCIN} = 0, V_{BATT} = V_{LX} = 20V		1	µA
BST Supply Current		DHI high		15	µA
DLOV Supply Current		V_{DLOV} = V_{LDO}, DLO low		10	µA
Inductor Peak Current Limit		R_{CSI} = 50mΩ	5.0	7.0	A
DHI Output Resistance		DHI high or low, V_{BST} - V_{LX} = 4.5V		14	Ω
DLO Output Resistance		DLO high or low, V_{DLOV} = 4.5V		14	Ω
THERMISTOR COMPARATOR SPECIFICATIONS					
THM Input Bias Current		V_{THM} = 4% of V_{DD} to 96% of V_{DD}, V_{DD} = 2.8V to 5.65V	-1	1	µA
Thermistor Overrange Threshold		V_{DD} = 2.8V to 5.65V, V_{THM} falling	89.5	92.5	% of V_{DD}
Thermistor Cold Threshold		V_{DD} = 2.8V to 5.65V, V_{THM} falling	74	77	% of V_{DD}
Thermistor Hot Threshold		V_{DD} = 2.8V to 5.65V, V_{THM} falling	22	25	% of V_{DD}
Thermistor Underrange Threshold		V_{DD} = 2.8V to 5.65V, V_{THM} falling	6	9	% of V_{DD}
SMB INTERFACE LEVEL SPECIFICATIONS (V_{DD} = 2.8V to 5.65V)					
SDA/SCL Input Low Voltage				0.6	V
SDA/SCL Input High Voltage			1.4		V
SDA/SCL Input Bias Current			-1	1	µA
SDA Output Low Sink Current		V_{SDA} = 0.4V	6		mA
$\overline{INT}$ Output High Leakage		$V_{\overline{INT}}$ = 5.65V		1	µA
$\overline{INT}$ Output Low Voltage		$I_{\overline{INT}}$ = 1mA		200	mV
SMB INTERFACE TIMING SPECIFICATIONS (V_{DD} = 2.8V to 5.65V, Figures 4 and 5)					
SCL High Period	t_{HIGH}		4		µs
SCL Low Period	t_{LOW}		4.7		µs
Start Condition Setup Time from SCL	$t_{SU:STA}$		4.7		µs
Start Condition Hold Time from SCL	$t_{HD:STA}$		4		µs
SDA Setup Time from SCL	$t_{SU:DAT}$		250		ns
SDA Hold Time from SCL	$t_{HD:DAT}$		0		ns

Advanced Chemistry-Independent, Level 2 Battery Chargers with Input Current Limiting

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{DD} = +3.3V, V_{BATT} = +16.8V, V_{DCIN} = +18V, **T_A = -40°C to +85°C**, unless otherwise noted. Guaranteed by design.)

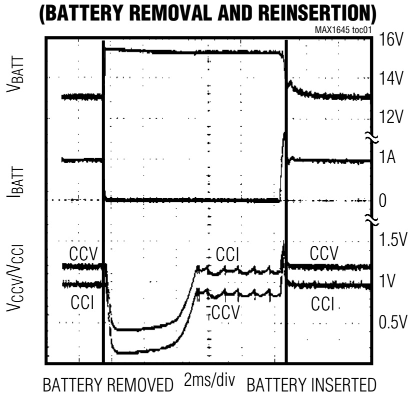
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
SDA Output Data Valid from SCL	t_{DV}			1	µs
Maximum Charge Period Without a ChargingVoltage() or Charging Current() loaded	t_{WDT}		140	210	s

Note 1: Guaranteed by meeting the SMB timing specs.
Note 2: The charger reverts to a trickle-charge mode of I_{CHARGE} = 128mA below this threshold.
Note 3: Does not include current-sense resistor tolerance.
Note 4: Voltage difference between CCV, and CCI or CCS when one of these three pins is held low and the others try to pull high.

Typical Operating Characteristics

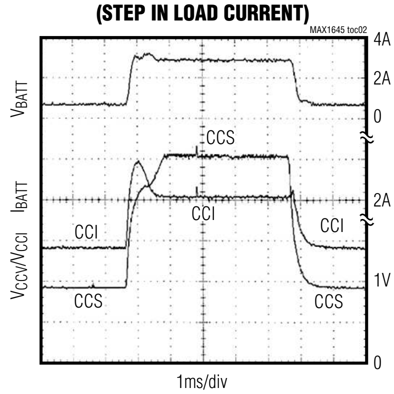
(Circuit of Figure 1, V_{DCIN} = 20V, T_A = +25°C, unless otherwise noted.)

LOAD-TRANSIENT RESPONSE (BATTERY REMOVAL AND REINSERTION)



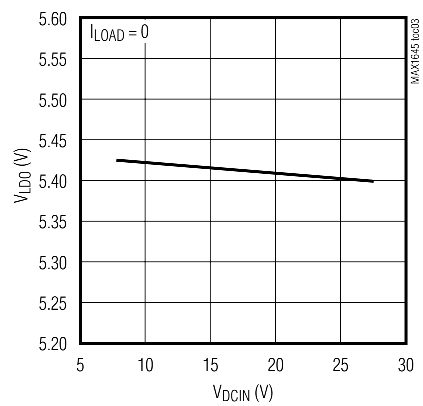
ChargingVoltage() = 15000mV
ChargingCurrent() = 1000mA

LOAD-TRANSIENT RESPONSE (STEP IN LOAD CURRENT)

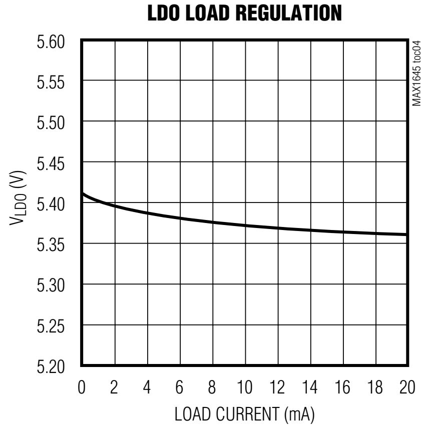


ChargingCurrent() = 3008mA
V_{BATT} = 16V
LOAD STEP: 0A TO 2A
I_{SOURCE} LIMIT = 2.5A

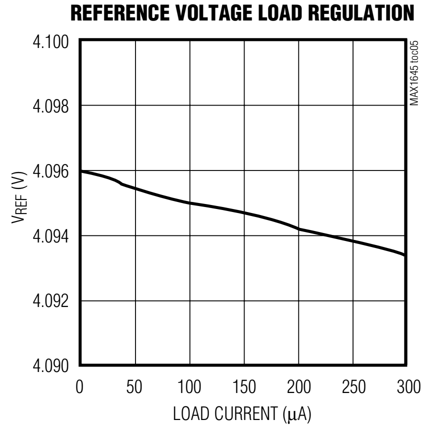
LDO LINE REGULATION



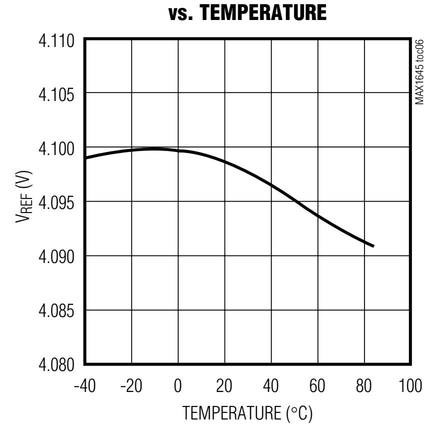
LDO LOAD REGULATION



REFERENCE VOLTAGE LOAD REGULATION



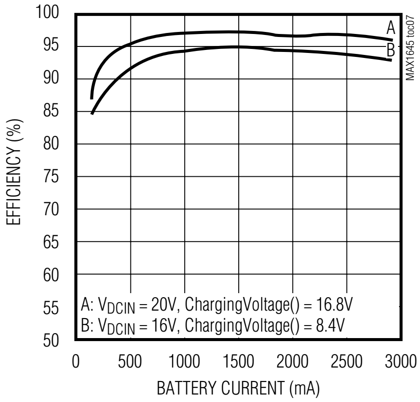
REFERENCE VOLTAGE vs. TEMPERATURE



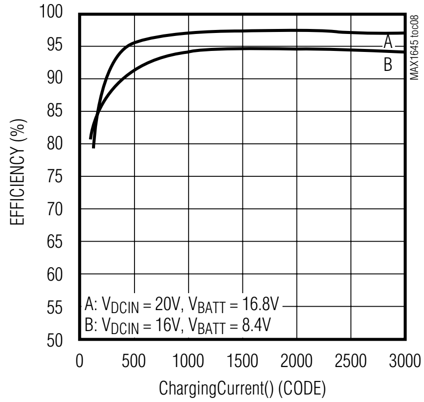
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{DCIN} = 20V, T_A = +25°C, unless otherwise noted.)

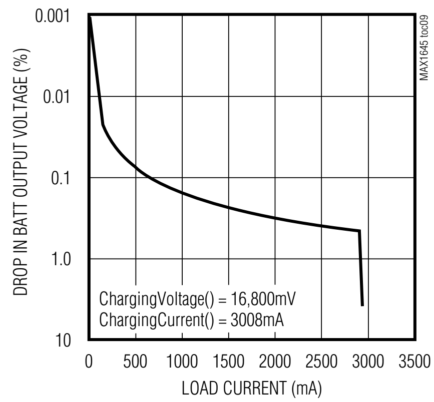
EFFICIENCY vs. BATTERY CURRENT (VOLTAGE-CONTROL LOOP)



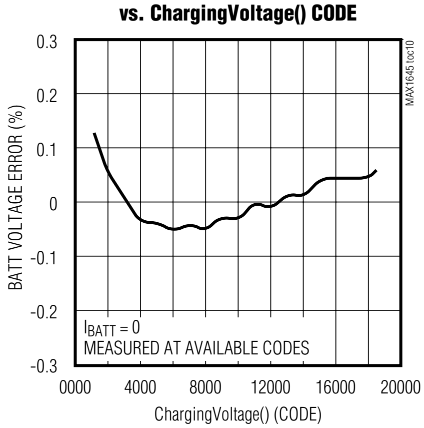
EFFICIENCY vs. BATTERY CURRENT (CURRENT-CONTROL LOOP)



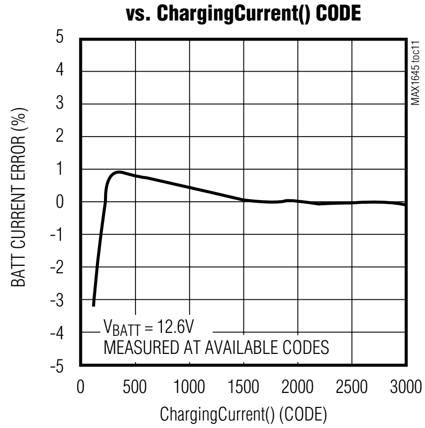
OUTPUT VI CHARACTERISTICS



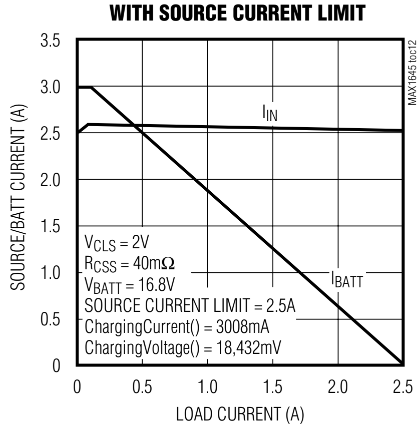
BATT VOLTAGE ERROR vs. ChargingVoltage() CODE



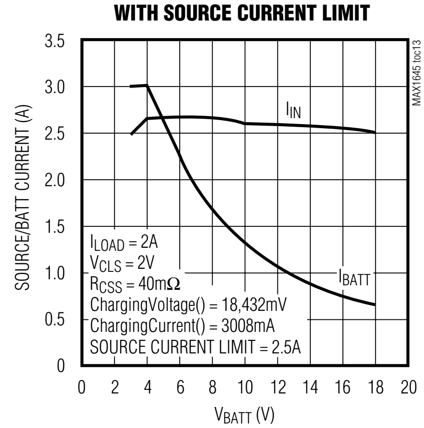
CURRENT-SETTING ERROR vs. ChargingCurrent() CODE



SOURCE/BATT CURRENT vs. LOAD CURRENT WITH SOURCE CURRENT LIMIT



SOURCE/BATT CURRENT vs. V_{BATT} WITH SOURCE CURRENT LIMIT



Advanced Chemistry-Independent, Level 2 Battery Chargers with Input Current Limiting

Pin Description

PIN	NAME	FUNCTION
1	DCIN	DC Supply Voltage Input
2	LDO	5.4V Linear-Regulator Voltage Output. Bypass with a 1µF capacitor to GND.
3	CLS	Source Current Limit Input
4	REF	4.096V Reference Voltage Output
5	CCS	Charging Source Compensation Capacitor Connection. Connect a 0.01µF capacitor from CCS to GND.
6	CCI	Battery Current-Loop Compensation Capacitor Connection. Connect a 0.01µF capacitor from CCI to GND.
7	CCV	Battery Voltage-Loop Compensation Capacitor Connection. Connect a 10kΩ resistor in series with a 0.01µF capacitor to GND.
8	GND	Ground
9	BATT	Battery Voltage Output
10	DAC	DAC Voltage Output
11	V_{DD}	Logic Circuitry Supply Voltage Input (2.8V to 5.65V)
12	THM	Thermistor Voltage Input
13	SCL	SMB Clock Input
14	SDA	SMB Data Input/Output. Open-drain output. Needs external pull-up.
15	$\overline{INT}$	Interrupt Output. Open-drain output. Needs external pull-up.
16	PDL	PMOS Load Switch Driver Output
17	CSIN	Battery Current-Sense Negative Input
18	CSIP	Battery Current-Sense Positive Input
19	PGND	Power Ground
20	DLO	Low-Side NMOS Driver Output
21	DLOV	Low-Side NMOS Driver Supply Voltage. Bypass with 0.1µF capacitor to GND.
22	LX	Inductor Voltage Sense Input
23	DHI	High-Side NMOS Driver Output
24	BST	High-Side Driver Bootstrap Voltage Input. Bypass with 0.1µF capacitor to LX.
25	CSSN	Charging Source Current-Sense Negative Input
26	CSSP	Charging Source Current-Sense Positive Input
27	PDS	Charging Source PMOS Switch Driver Output
28	CVS	Charging Source Voltage Input

Detailed Description

The MAX1645/MAX1645A consist of current-sense amplifiers, an SMBus interface, transconductance amplifiers, reference circuitry, and a DC–DC converter (Figure 2). The DC–DC converter generates the control signals for the external MOSFETs to maintain the voltage and the current set by the SMBus interface. The MAX1645/MAX1645A feature a voltage-regulation loop and two current-regulation loops. The loops operate independently of each other. The voltage-regulation loop monitors BATT to ensure that its voltage never exceeds the voltage set point (V0). The battery current-regulation loop monitors current delivered to BATT to ensure that it never exceeds the current-limit set point (I0). The battery current-regulation loop is in control as long as BATT voltage is below V0. When BATT voltage reaches V0, the current loop no longer regulates. A third loop reduces the battery-charging current when the sum of the system (the main load) and the battery charger input current exceeds the charging source current limit.

Setting Output Voltage

The MAX1645/MAX1645A voltage DACs have a 16mV LSB and an 18.432V full scale. The SMBus specification allows for a 16-bit ChargingVoltage() command that translates to a 1mV LSB and a 65.535V full-scale voltage; therefore, the ChargingVoltage() value corresponds to the output voltage in millivolts. The MAX1645/MAX1645A ignore the first four LSBs and use the next 11 LSBs to control the voltage DAC. All codes greater than or equal to 0b0100 1000 0000 0000 (18432mV) result in a voltage overrange, limiting the charger voltage to 18.432V. All codes below 0b0000 0100 0000 0000 (1024mV) terminate charging.

Setting Output Current

The MAX1645/MAX1645A current DACs have a 64mA LSB and a 3.008A full scale. The SMBus specification allows for a 16-bit ChargingCurrent() command that translates to a 1mA LSB and a 65.535A full-scale current; the ChargingCurrent() value corresponds to the charging voltage in milliamps. The MAX1645/MAX1645A drop the first six LSBs and use the next six LSBs to control the current DAC. All codes above 0b00 1011 1100 0000 (3008mA) result in a current overrange, limiting the charger current to 3.008A. All codes below 0b0000 0000 1000 0000 (128mA) turn the charging current off. A 50mΩ sense resistor (R2 in Figure 1) is required to achieve the correct CODE/current scaling.

Input Current Limiting

The MAX1645/MAX1645A limit the current drawn by the charger when the load current becomes high. The devices limit the charging current so the AC adapter voltage is not loaded down. An internal amplifier, CSS, compares the voltage between CSSP and CSSN to the voltage at CLS/20. V_{CLS} is set by a resistor-divider between REF and GND.

The input source current is the sum of the device current, the charge input current, and the load current. The device current is minimal (6mA max) in comparison to the charge and load currents. The charger input current is generated by the DC-DC converter; therefore, the actual source current required is determined as follows:

$$I_{SOURCE} = I_{LOAD} + [(I_{CHARGE} \cdot V_{BATT}) / (V_{IN} \cdot \eta)]$$

where η is the efficiency of the DC-DC converter (typically 85% to 95%).

V_{CLS} determines the threshold voltage of the CSS comparator. R3 and R4 (Figure 1) set the voltage at CLS. Sense resistor R1 sets the maximum allowable source current. Calculate the maximum current as follows:

$$I_{MAX} = V_{CLS} / (20 \cdot R_1)$$

(Limit V_{CSSP} - V_{CSSN} to between 102.4mV and 204.8mV.)

The configuration in Figure 1 provides an input current limit of:

$$I_{MAX} = (2.048V / 20) / 0.04\Omega = 2.56A$$

LDO Regulator

An integrated LDO regulator provides a +5.4V supply derived from DCIN, which can deliver up to 15mA of current. The LDO sets the gate-drive level of the NMOS switches in the DC-DC converter. The drivers are actually powered by DLOV and BST, which must be connected to LDO through a lowpass filter and a diode as shown in Figure 1. See also the *MOSFET Drivers* section. The LDO also supplies the 4.096V reference and most of the control circuitry. Bypass LDO with a 1µF capacitor.

V_{DD} Supply

This input provides power to the SMBus interface and the thermistor comparators. Typically connect V_{DD} to LDO or, to keep the SMBus interface of the MAX1645/MAX1645A active while the supply to DCIN is removed, connect an external supply to V_{DD}.

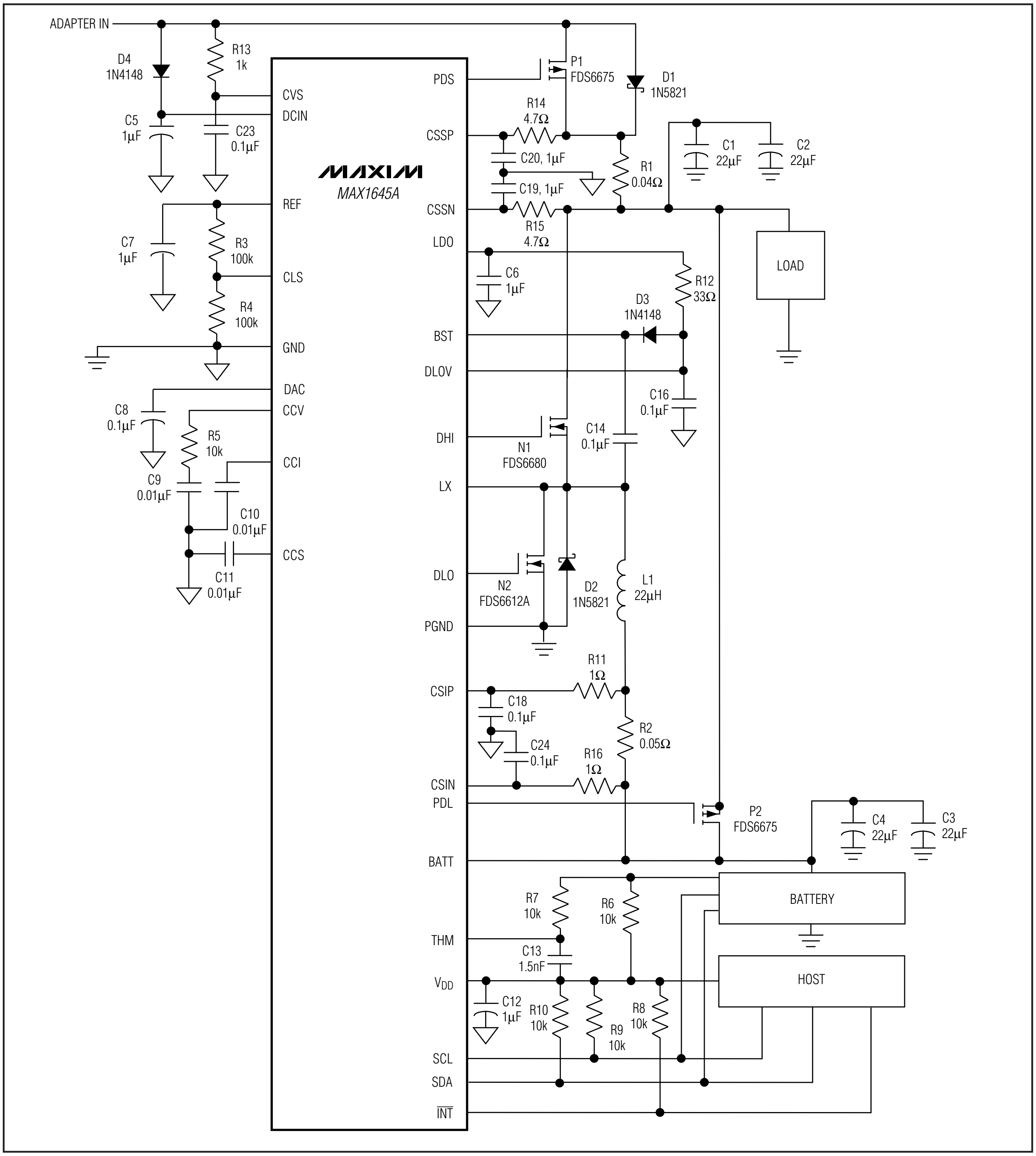


Figure 1. Typical Application Circuit

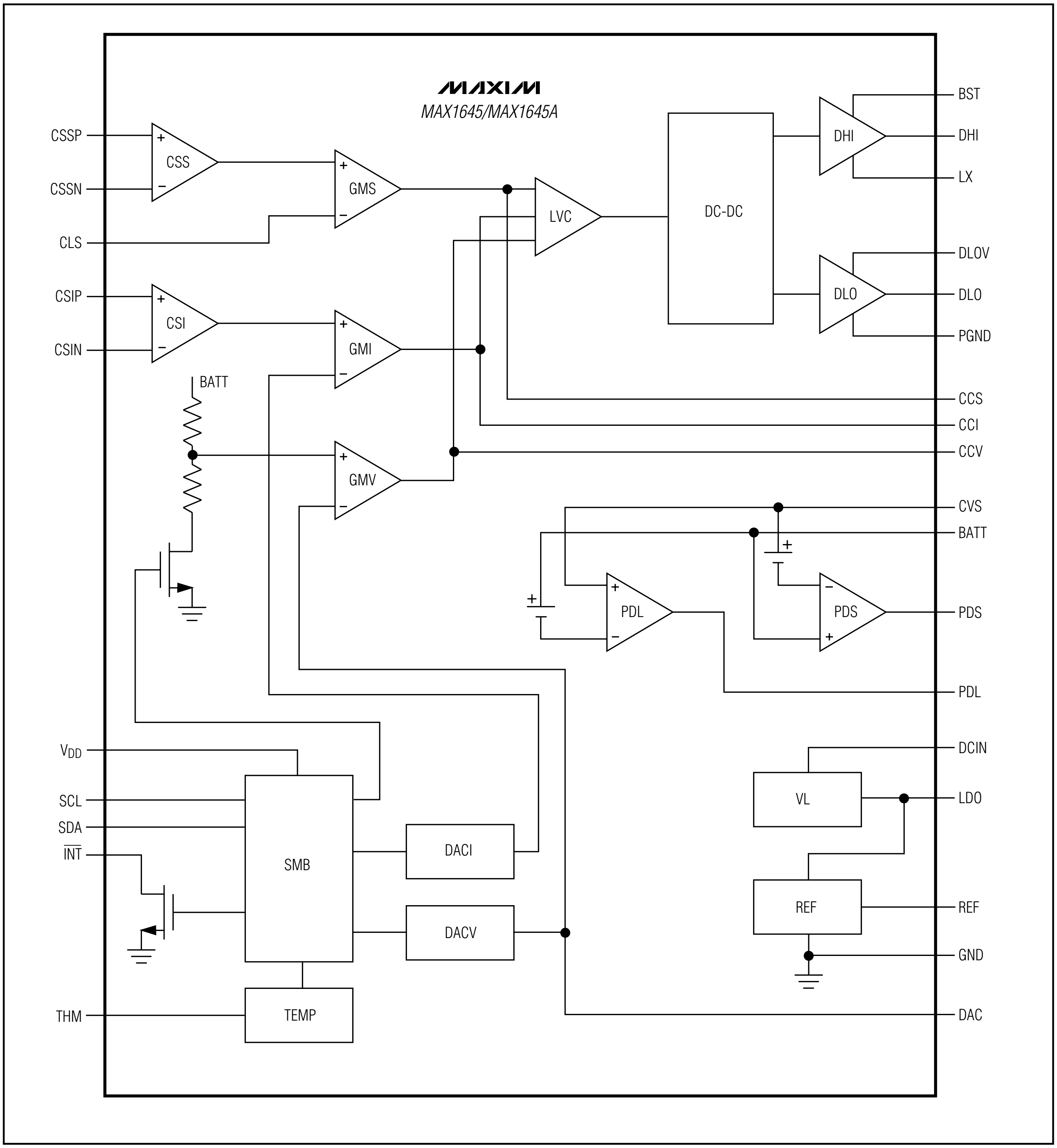


Figure 2. Functional Diagram

Operating Conditions

The MAX1645/MAX1645A change their operation depending on the voltages at DCIN, BATT, V_{DD}, and THM. Several important operating states follow:

- **AC Present.** When DCIN is > 7.5V, the battery is considered to be in an AC Present state. In this condition, both the LDO and REF will function properly and battery charging is allowed. When AC is present, the AC_PRESENT bit (bit 15) in the ChargerStatus() register is set to "1."
- **Power Fail.** When DCIN is < BATT + 0.3V, the part is in the Power Fail state, since the charger doesn't have enough input voltage to charge the battery. In Power Fail, the PDS input PMOS switch is turned off and the POWER_FAIL bit (bit 13) in the ChargerStatus() register is set to "1."
- **Battery Present.** When THM is < 91% of V_{DD}, the battery is considered to be present. The MAX1645/MAX1645A use the THM pin to detect when a battery is connected to the charger. When the battery is present, the BATTERY_PRESENT bit (bit 14) in the ChargerStatus() register is set to "1" and charging can proceed. When the battery is not present, all of the registers are reset. With no battery present, the charger will perform a "Float" charge to minimize contact arcing on battery connection. "Float" charge will still try to regulate the BATT pin voltage at 18.32V with 128mA of current compliance.
- **Battery Undervoltage.** When BATT < 2.5V, the battery is in an undervoltage state. This causes the charger to reduce its current compliance to 128mA. The content of the ChargingCurrent() register is unaffected and, when the BATT voltage exceeds 2.7V, normal charging resumes. ChargingVoltage() is unaffected and can be set as low as 1.024V.
- **V_{DD} Undervoltage.** When V_{DD} < 2.5V, the V_{DD} supply is in an undervoltage state, and the SMBus interface will not respond to commands. Coming out of the undervoltage condition, the part will be in its Power-On Reset state. No charging will occur when V_{DD} is under voltage.

SMBus Interface

The MAX1645/MAX1645A receive control inputs from the SMBus interface. The serial interface complies with the SMBus specification (refer to the System Management Bus Specification from Intel Corporation). Charger functionality complies with the Intel/Duracell Smart Charger Specification for a Level 2 charger.

The MAX1645/MAX1645A use the SMBus Read-Word and Write-Word protocols to communicate with the battery being charged, as well as with any host system that monitors the battery-to-charger communications as a Level 2 SMBus charger. The MAX1645/MAX1645A are SMBus slave devices and do not initiate communication on the bus. They receive commands and respond to queries for status information. Figure 3 shows examples of the SMBus Write-Word and Read-Word protocols, and Figures 4 and 5 show the SMBus serial-interface timing.

Each communication with these parts begins with the MASTER issuing a START condition that is defined as a falling edge on SDA with SCL high and ends with a STOP condition defined as a rising edge on SDA with SCL high. Between the START and STOP conditions, the device address, the command byte, and the data bytes are sent. The MAX1645/MAX1645As' device address is 0x12 and supports the charger commands as described in Tables 1–6.

Battery Charger Commands

ChargerSpecInfo()

The ChargerSpecInfo() command uses the Read-Word protocol (Figure 3b). The command code for ChargerSpecInfo() is 0x11 (0b00010001). Table 1 lists the functions of the data bits (D0–D15). Bit 0 refers to the D0 bit in the Read-Word protocol. The MAX1645/MAX1645A comply with level 2 Smart Battery Charger Specification Revision 1.0; therefore, the ChargerSpecInfo() command returns 0x01.

ChargerMode()

The ChargerMode() command uses the Write-Word protocol (Figure 3a). The command code for ChargerMode() is 0x12 (0b00010010). Table 2 lists the functions of the data bits (D0–D15). Bit 0 refers to the D0 bit in the Write-Word protocol.

To charge a battery that has a thermistor impedance in the HOT range (i.e., THERMISTOR_HOT = 1 and THERMISTOR_UR = 0), the host must use the ChargerMode() command to clear HOT_STOP after the battery is inserted. The HOT_STOP bit returns to its default power-up condition ("1") whenever the battery is removed.

ChargerStatus()

The ChargerStatus() command uses the Read-Word protocol (Figure 3b). The command code for ChargerStatus() is 0x13 (0b00010011). Table 3 describes the functions of the data bits (D0–D15). Bit 0 refers to the D0 bit in the Read-Word protocol.

The ChargerStatus() command returns information about thermistor impedance and the MAX1645/MAX1645A's internal state. The latched bits, THERMISTOR_HOT and ALARM_INHIBITED, are cleared whenever BATTERY_PRESENT = 0 or ChargerMode() is written with POR_RESET = 1. The ALARM_INHIBITED status bit can also be cleared by writing a new charging current OR charging voltage.

a) Write-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	ACK	P
	7 bits	1b	1b	8 bits	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0	MSB LSB	0	MSB LSB	0	
	Preset to 0b0001001			ChargerMode() = 0x12 ChargingCurrent() = 0x14 ChargerVoltage() = 0x15 AlarmWarning() = 0x16		D7 D0		D15 D8		

b) Read-Word Format

S	SLAVE ADDRESS	W	ACK	COMMAND BYTE	ACK	S	SLAVE ADDRESS	R	ACK	LOW DATA BYTE	ACK	HIGH DATA BYTE	NACK	P
	7 bits	1b	1b	8 bits	1b		7 bits	1b	1b	8 bits	1b	8 bits	1b	
	MSB LSB	0	0	MSB LSB	0		MSB LSB	1	0	MSB LSB	0	MSB LSB	1	
	Preset to 0b0001001			ChargerSpecInfo() = 0x11 ChargerStatus() = 0x13			Preset to 0b0001001			D7 D0		D15 D8		

Legend:
S = Start Condition or Repeated Start Condition
ACK = Acknowledge (logic low)
W = Write Bit (logic low)
P = Stop Condition
NACK = NOT Acknowledge (logic high)
R = Read Bit (logic high)

MASTER TO SLAVE (unshaded)
SLAVE TO MASTER (shaded: ACK fields in a) and b); LOW DATA BYTE and HIGH DATA BYTE in b))

Figure 3. SMBus a) Write-Word and b) Read-Word Protocols

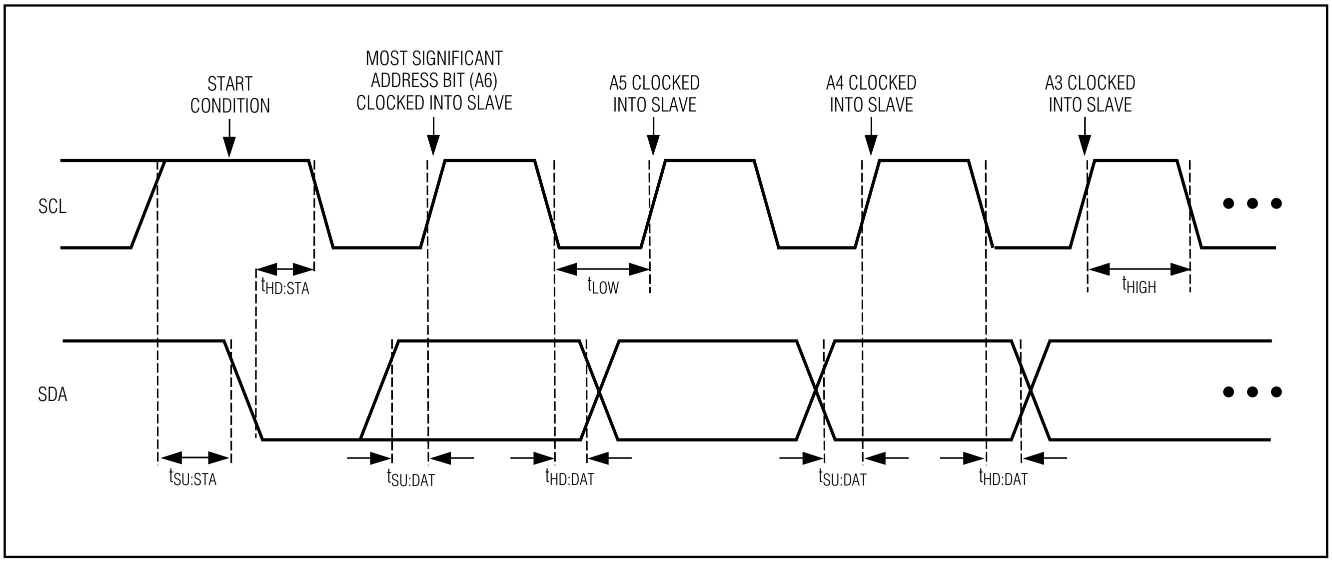


Figure 4. SMBus Serial Interface Timing—Address

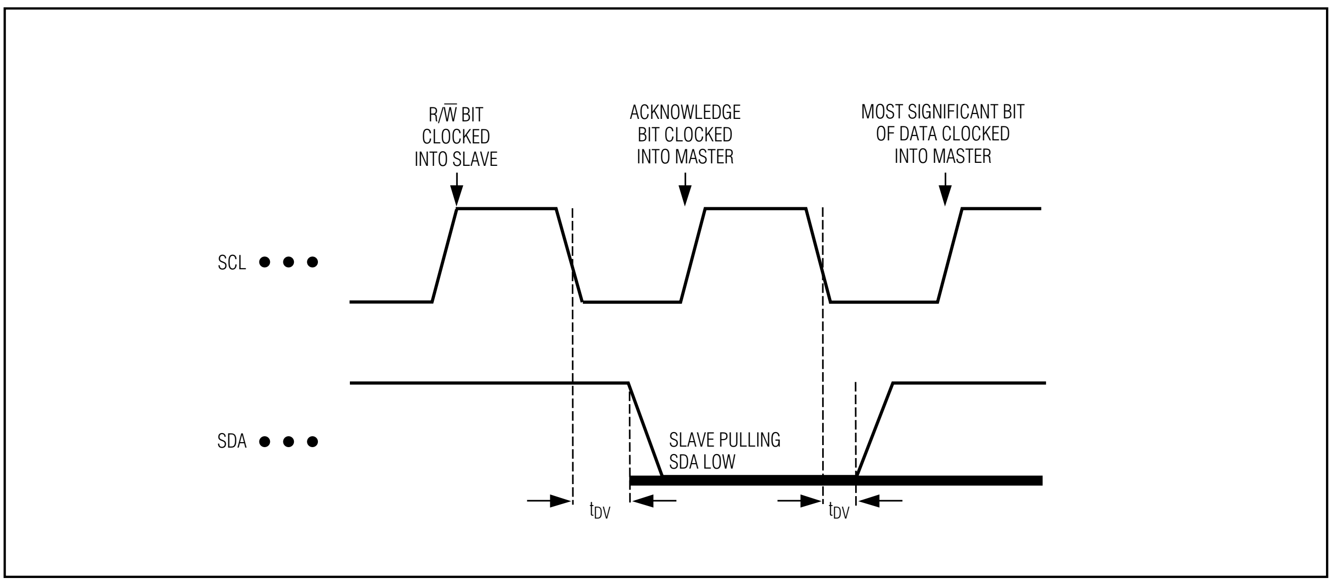


Figure 5. SMBus Serial Interface Timing—Acknowledgment

Table 1. ChargerSpecInfo()

BIT	NAME	DESCRIPTION
0	CHARGER_SPEC	Returns a “1” for Version 1.0
1	CHARGER_SPEC	Returns a “0” for Version 1.0
2	CHARGER_SPEC	Returns a “0” for Version 1.0
3	CHARGER_SPEC	Returns a “0” for Version 1.0
4	SELECTOR_SUPPORT	Returns a “0,” indicating no smart battery selector functionality
5	Reserved	Returns a “0”
6	Reserved	Returns a “0”
7	Reserved	Returns a “0”
8	Reserved	Returns a “0”
9	Reserved	Returns a “0”
10	Reserved	Returns a “0”
11	Reserved	Returns a “0”
12	Reserved	Returns a “0”
13	Reserved	Returns a “0”
14	Reserved	Returns a “0”
15	Reserved	Returns a “0”

Command: 0x11

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Table 2. ChargerMode()

BIT	NAME	DESCRIPTION
0	INHIBIT_CHARGE	0* = Allow normal operation; clear the CHG_INHIBITED flip-flop. 1 = Turn off the charger; set the CHG_INHIBITED flip-flop. The CHG_INHIBITED flip-flop is not affected by any other commands.
1	ENABLE_POLLING	Not implemented
2	POR_RESET	0 = No change. 1 = Change the ChargingVoltage() to 0xFFFF and the ChargingCurrent() to 0x00C0; clear the THERMISTOR_HOT and ALARM_INHIBITED flip-flops.
3	RESET_TO_ZERO	Not implemented
4	AC_PRESENT_MASK	0* = Interrupt on either edge of the AC_PRESENT status bit. 1 = Do not interrupt because of an AC_PRESENT bit change.
5	BATTERY_PRESENT_ MASK	0* = Interrupt on either edge of the BATTERY_PRESENT status bit. 1 = Do not interrupt because of a BATTERY_PRESENT bit change.
6	POWER_FAIL_MASK	0* = Interrupt on either edge of the POWER_FAIL status bit. 1 = Do not interrupt because of a POWER_FAIL bit change.
7		Not implemented
8		Not implemented
9		Not implemented
10	HOT_STOP	0 = The THERMISTOR_HOT status bit does not turn off the charger. 1* = The THERMISTOR_HOT status bit does turn off the charger. THERMISTOR_HOT is reset by either POR_RESET or BATTERY_PRESENT = 0 status bit.
11		Not implemented
12		Not implemented
13		Not implemented
14		Not implemented
15		Not implemented

Command: 0x12

**State at chip initial power-on (i.e., V_{DD} from 0 to +3.3V)*

Table 3. ChargerStatus()

BIT	NAME	FUNCTION
0	CHARGE_INHIBITED	0* = Ready to charge Smart Battery. 1 = Charger is inhibited, I(chg) = 0mA. This status bit returns the value of the CHG_INHIBITED flip-flop.
1	MASTER_MODE	Always returns “0”
2	VOLTAGE_NOT_REG	0 = Battery voltage is limited at the set point. 1 = Battery voltage is less than the set point.
3	CURRENT_NOT_REG	0 = Battery current is limited at the set point. 1 = Battery current is less than the set point.
4	LEVEL_2	Always returns a “1”
5	LEVEL_3	Always returns a “0”
6	CURRENT_OR	0* = The ChargingCurrent() value is valid for the MAX1645. 1 = The ChargingCurrent() value exceeds the MAX1645 output range, i.e., programmed ChargingCurrent() exceeds 3008mA.
7	VOLTAGE_OR	0 = The ChargingVoltage() value is valid for the MAX1645. 1* = The ChargingVoltage() value exceeds the MAX1645 output range, i.e., programmed ChargingVoltage() exceeds 1843mV.
8	THERMISTOR_OR	0 = THM is < 91% of the reference voltage. 1 = THM is > 91% of the reference voltage.
9	THERMISTOR_COLD	0 = THM is < 75.5% of the reference voltage. 1 = THM is > 75.5% of the reference voltage.
10	THERMISTOR_HOT	0 = THM has not dropped to < 23.5% of the reference voltage. 1 = THM has dropped to < 23.5% of the reference voltage. THERMISTOR_HOT flip-flop cleared by BATTERY_PRESENT = 0 or writing a “1” into the POR_RESET bit in the ChargerMode() command.
11	THERMISTOR_UR	0 = THM is > 7.5% of the reference voltage. 1 = THM is < 7.5% of the reference voltage.
12	ALARM_INHIBITED	Returns the state of the ALARM_INHIBITED flip-flop. This flip-flop is set by either a watchdog timeout or by writing an AlarmWarning() command with bits 11, 12, 13, 14, or 15 set. This flip-flop is cleared by BATTERY_PRESENT = 0, writing a “1” into the POR_RESET bit in the ChargerMode() command, or by receiving successive ChargingVoltage() and ChargingCurrent() commands. POR: 0.
13	POWER_FAIL	0 = The charging source voltage CVS is above the BATT voltage. 1 = The charging source voltage CVS is below the BATT voltage.
14	BATTERY_PRESENT	0 = No battery is present (based on THM input). 1 = Battery is present (based on THM input).
15	AC_PRESENT	0 = DCIN is below the 7.5V undervoltage threshold. 1 = DCIN is above the 7.5V undervoltage threshold.

Command: 0x13

**State at chip initial power-on.*

Table 4. ChargerCurrent()

BIT	NAME	FUNCTION
0		Not used. Normally a 1mA weight.
1		Not used. Normally a 2mA weight.
2		Not used. Normally a 4mA weight.
3		Not used. Normally an 8mA weight.
4		Not used. Normally a 16mA weight.
5		Not used. Normally a 32mA weight.
6	Charge Current, DACI 0	0 = Adds 0mA of charger-current compliance. 1 = Adds 64mA of charger-current compliance, 128mA min.
7	Charge Current, DACI 1	0 = Adds 0mA of charger-current compliance. 1 = Adds 128mA of charger-current compliance.
8	Charge Current, DACI 2	0 = Adds 0mA of charger-current compliance. 1 = Adds 256mA of charger-current compliance.
9	Charge Current, DACI 3	0 = Adds 0mA of charger-current compliance. 1 = Adds 512mA of charger-current compliance.
10	Charge Current, DACI 4	0 = Adds 0mA of charger-current compliance. 1 = Adds 1024mA of charger-current compliance.
11	Charge Current, DACI 5	0 = Adds 0mA of charger-current compliance. 1 = Adds 2048mA of charger-current compliance, 3008mA max.
12–15		0 = Adds 0mA of charger current compliance. 1 = Sets charger compliance into overrange, 3008mA.

Command: 0x14

Table 5. ChargingVoltage()

PIN	BIT NAME	FUNCTION
0		Not used. Normally a 1mV weight.
1		Not used. Normally a 2mV weight.
2		Not used. Normally a 4mV weight.
3		Not used. Normally an 8mV weight.
4	Charge Voltage, DACV 0	0 = Adds 0mV of charger-voltage compliance. 1 = Adds 16mV of charger-voltage compliance, 1.024V min.
5	Charge Voltage, DACV 1	0 = Adds 0mV of charger-voltage compliance. 1 = Adds 32mV of charger-voltage compliance, 1.024V min.
6	Charge Voltage, DACV 2	0 = Adds 0mV of charger-voltage compliance. 1 = Adds 64mV of charger-voltage compliance, 1.024V min.
7	Charge Voltage, DACV 3	0 = Adds 0mV of charger-voltage compliance. 1 = Adds 128mV of charger-voltage compliance, 1.024V min.
8	Charge Voltage, DACV 4	0 = Adds 0mV of charger-voltage compliance. 1 = Adds 256mV of charger-voltage compliance, 1.024V min.
9	Charge Voltage, DACV 5	0 = Adds 0mV of charger-voltage compliance. 1 = Adds 512mV of charger-voltage compliance, 1.024V min.
10	Charge Voltage, DACV 6	0 = Adds 0mA of charger-voltage compliance. 1 = Adds 1024mV of charger-voltage compliance.
11	Charge Voltage, DACV 7	0 = Adds 0mV of charger-voltage compliance. 1 = Adds 2048mV of charger-voltage compliance.
12	Charge Voltage, DACV 8	0 = Adds 0mV of charger-voltage compliance. 1 = Adds 4096mV of charger-voltage compliance.
13	Charge Voltage, DACV 9	0 = Adds 0mV of charger-voltage compliance. 1 = Adds 8192mV of charger-voltage compliance.
14	Charge Voltage, DACV 10	0 = Adds 0mV of charger-voltage compliance. 1 = Adds 16384mV of charger-voltage compliance, 18432mV max.
15	Charge Voltage, Overrange	0 = Adds 0mV of charger-voltage compliance. 1 = Sets charger compliance into overrange, 18432mV.

Command: 0x15

Table 6. AlarmWarning()

BIT	BIT NAME	DESCRIPTION
0	Error Code	Not used
1	Error Code	Not used
2	Error Code	Not used
3	Error Code	Not used
4	FULLY_DISCHARGED	Not used
5	FULLY_CHARGED	Not used
6	DISCHARGING	Not used
7	INITIALIZING	Not used
8	REMAINING_TIME_ ALARM	Not used
9	REMAINING_CAPACITY_ ALARM	Not used
10	Reserved	Not used
11	TERMINATE_ DISCHARGE_ALARM	0 = Charge normally 1 = Terminate charging
12	OVER_TEMP_ALARM	0 = Charge normally 1 = Terminate charging
13	OTHER_ALARM	0 = Charge normally 1 = Terminate charging
14	TERMINATE_CHARGE_ ALARM	0 = Charge normally 1 = Terminate charging
15	OVER_CHARGE_ALARM	0 = Charge normally 1 = Terminate charging

Command: 0x16

ChargingCurrent() (POR: 0x0080)

The ChargingCurrent() command uses the Write-Word protocol (Figure 3a). The command code for ChargingCurrent() is 0x14 (0b00010100). The 16-bit binary number formed by D15–D0 represents the current-limit set point (I0) in milliamps. However, since the MAX1645/MAX1645A have 64mA resolution in setting I0, the D0–D5 bits are ignored as shown in Table 4. Figure 6 shows the mapping between I0 (the current-regulation-loop set point) and the ChargingCurrent() code. All codes above 0b00 1011 1100 0000 (3008mA) result in a current overrange, limiting the charger current to 3.008A. All codes below 0b0000 0000 1000 0000 (128mA) turn the charging current off. A 50mΩ sense resistor (R2 in Figure 1) is required to achieve the correct CODE/current scaling.

The power-on reset value for the ChargingCurrent() register is 0x0080; thus, the first time a MAX1645/MAX1645A is powered on, the BATT current regulates to 128mA. Any time the battery is removed, the ChargingCurrent() register returns to its power-on reset state.

ChargingVoltage() (POR: 0x4800)

The ChargingVoltage() command uses the Write-Word protocol (Figure 3a). The command code for ChargingVoltage() is 0x15 (0b00010101). The 16-bit binary number formed by D15–D0 represents the voltage set point (V0) in millivolts; however, since the MAX1645/MAX1645A have 16mV resolution in setting V0, the D0, D1, D2, and D3 bits are ignored as shown in Table 5.

The ChargingVoltage command is used to set the battery charging voltage compliance from 1.024V to 18.432V. All codes greater than or equal to 0b0100 1000 0000 0000 (18432mV) result in a voltage overrange, limiting the charger voltage to 18.432V. All codes below 0b0000 0100 0000 0000 (1024mV) terminate charge. Figure 7 shows the mapping between V0 (the voltage-regulation-loop set point) and the ChargingVoltage() code.

The power-on reset value for the ChargingVoltage() register is 0x4880; thus, the first time a MAX1645/MAX1645A are powered on, the BATT voltage regulates to 18.432V. Any time the battery is removed, the ChargingVoltage() register returns to its power-on reset state. The voltage at DAC corresponds to the set compliance voltage divided by 4.5.

AlarmWarning() (POR: Not Alarm)

The AlarmWarning() command uses the Write-Word protocol (Figure 3a). The command code for AlarmWarning() is 0x16 (0b00010110). AlarmWarning() sets the ALARM_INHIBITED status bit in the MAX1645/MAX1645A if D15, D14, D13, D12, or D11 of the Write-Word protocol data equals 1. Table 6 summarizes the Alarm-Warning() command's function. The ALARM_INHIBITED status bit remains set until the battery is removed, a ChargerMode() command is written with the POR_RESET bit set, or new ChargingCurrent() AND ChargingVoltage() values are written. As long as ALARM_INHIBITED = 1, the MAX1645/MAX1645A switching regulators remain off.

Interrupts and Alert Response Address

The MAX1645/MAX1645A request an interrupt by pulling the $\overline{INT}$ pin low. An interrupt is normally requested when there is a change in the state of the ChargerStatus() bits POWER_FAIL (bit 13), BATTERY_PRESENT (bit 14), or AC_PRESENT (bit 15). Therefore, the $\overline{INT}$ pin will pull low whenever the AC adapter is connected or disconnected, the battery is inserted or removed, or the charger goes in or out of dropout. The interrupts from each of the ChargerStatus() bits can be masked by an associated ChargerMode() bit POWER_FAIL_MASK (bit 6), BATTERY_PRESENT_MASK (bit 5), or AC_PRESENT_MASK (bit 4).

All interrupts are cleared by sending any command to the MAX1645/MAX1645A, or by sending a command to the AlertResponse() address, 0x19, using a modified Receive Byte protocol. In this protocol, all devices that set an interrupt will try to respond by transmitting their address, and the device with the highest priority, or most leading 0's, will be recognized and cleared. The process will be repeated until all devices requesting interrupts are addressed and cleared. The MAX1645/

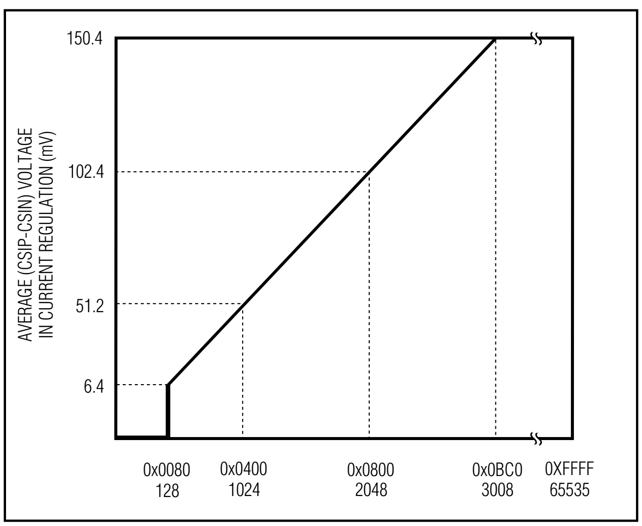

Figure 6. Average Voltage Between CSIP and CSIN vs. Charging Current() Code

Advanced Chemistry-Independent, Level 2 Battery Chargers with Input Current Limiting

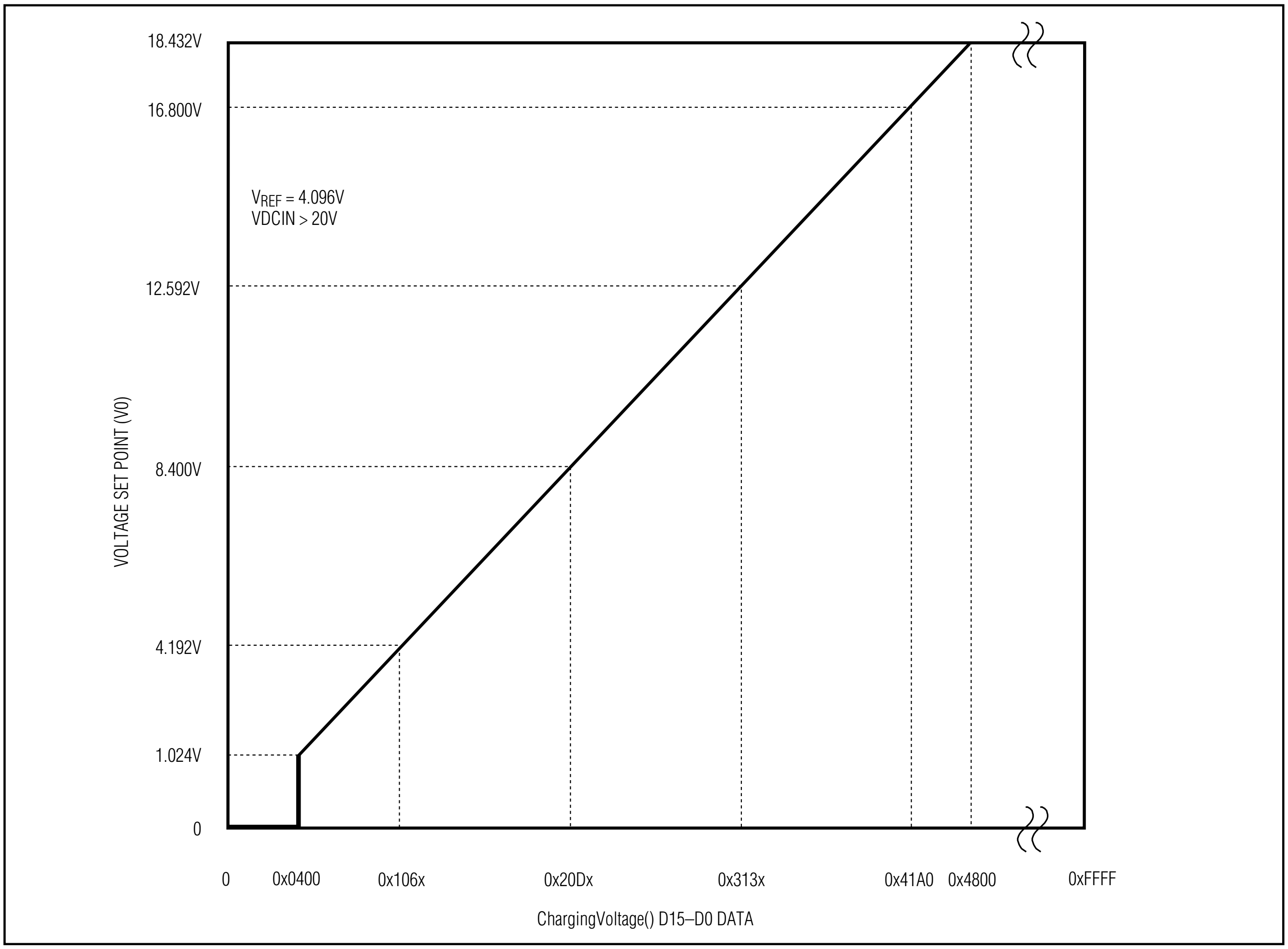

Figure 7. ChargingVoltage() Code to Voltage Mapping

MAX1645A respond to the AlertResponse() address with 0x13, which is their address and a trailing "1."

Charger Timeout

The MAX1645/MAX1645A include a timer that terminates charge if the charger has not received a ChargingVoltage() or ChargingCurrent() command in 175sec. During charging, the timer is reset each time a ChargingVoltage() or ChargingCurrent() command is received; this ensures that the charging cycle is not terminated.

If timeout occurs, charging will terminate and both ChargingVoltage() and ChargingCurrent() commands are required to restart charging. A power-on reset will also restart charging at 128mA.

DC-to-DC Converter

The MAX1645/MAX1645A employ a buck regulator with a boot-strapped NMOS high-side switch and a low-side NMOS synchronous rectifier.

DC-DC Controller

The control scheme is a constant off-time, variable frequency, cycle-by-cycle current mode. The off-time is constant for a given BATT voltage; it varies with V_{BATT} to keep the ripple current constant. During low-dropout operation, a maximum on-time of 10ms allows the controller to achieve >99% duty cycle with continuous conduction. Figure 8 shows the controller functional diagram.

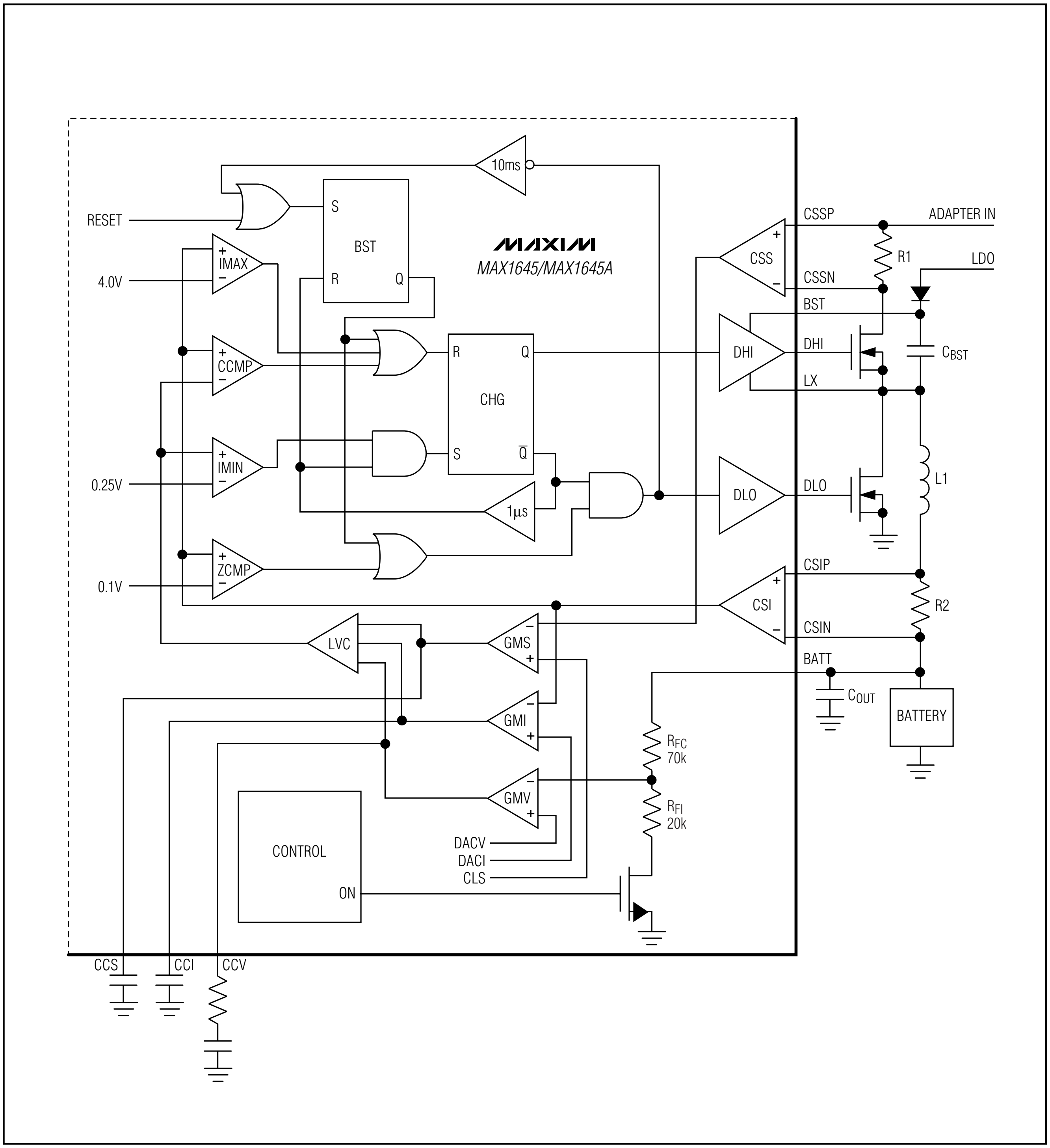

Figure 8. DC-to-DC Converter Functional Diagram