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# Complete DDR2 and DDR3 Memory Power-Management Solution

MAX17000

## General Description

The MAX17000 pulse-width modulation (PWM) controller provides a complete power solution for notebook DDR, DDR2, and DDR3 memory. It comprises a step-down controller, a source/sink LDO regulator, and a reference buffer to generate the required VDDQ, VTT, and VTTR rails.

The VDDQ rail is supplied by a step-down converter using Maxim's proprietary Quick-PWM™ controller. The high-efficiency, constant-on-time PWM controller handles wide input/output voltage ratios (low duty-cycle applications) with ease and provides 100ns response to load transients while maintaining a relatively constant switching frequency. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes. The controller senses the current to achieve an accurate valley current-limit protection. It is also built in with overvoltage, undervoltage, and thermal protections. The MAX17000 can be set to run in three different modes: power-efficient SKIP mode, low-noise forced-PWM mode, and standby mode to support memory in notebook computer standby operation. The switching frequency is programmable from 200kHz to 600kHz to allow small components and high efficiency. The VDDQ output voltage can be set to a preset 1.8V or 1.5V, or be adjusted from 1.0V to 2.5V by an external resistor-divider. This output has 1% accuracy over line-and-load operating range.

The MAX17000 includes a  $\pm 2A$  source/sink LDO regulator for the memory termination VTT rail. This VTT regulator has a  $\pm 5mV$  deadband that either sources or sinks, ideal for the fast-changing load burst present in memory termination applications. This feature also reduces output capacitance requirements.

The VTTR reference buffer sources and sinks  $\pm 3mA$ , providing the reference voltage needed by the memory controller and devices on the memory bus.

The MAX17000 is available in a 24-pin, 4mm x 4mm, TQFN package.

## Applications

Notebook Computers  
DDR, DDR2, and DDR3 Memory Supplies  
SSTL Memory Supplies

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

## Features

- ◆ **SMPS Regulator (VDDQ)**  
Quick-PWM with 100ns Load-Step Response  
Output Voltages—Preset 1.8V, 1.5V, or Adjustable 1.0V to 2.5V  
1%  $V_{OUT}$  Accuracy Over Line and Load  
26V Maximum Input Voltage Rating  
Accurate Valley Current-Limit Protection  
200kHz to 600kHz Switching Frequency
- ◆ **Source/Sink Linear Regulator (VTT)**  
 $\pm 2A$  Peak Source/Sink  
Low-Output Capacitance Requirement  
Output Voltages—Preset VDDQ/2 or REFIN  
Adjustable from 0.5V to 1.5V
- ◆ **Low Quiescent Current Standby State**
- ◆ **Soft-Start/Soft-Shutdown**
- ◆ **SMPS Power-Good Window Comparator**
- ◆ **VTT Power-Good Window Comparator**
- ◆ **Selectable Overvoltage Protection**
- ◆ **Undervoltage/Thermal Protections**
- ◆  **$\pm 3mA$  Reference Buffer (VTTR)**

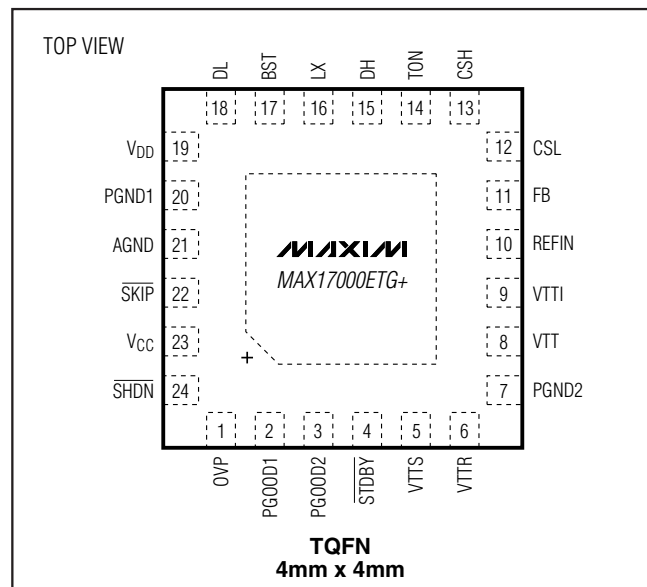
## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17000ETG+	-40°C to +85°C	24 TQFN-EP*

+ Denotes a lead(Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

## Pin Configuration





# Complete DDR2 and DDR3 Memory Power-Management Solution

## ABSOLUTE MAXIMUM RATINGS

TON to PGND1	-0.3V to +28V
VDD to PGND1	-0.3V to +6V
VCC to VDD	-0.3V to +0.3V
OVP to AGND	-0.3V to +6V
SHDN, STDBY, SKIP to AGND	-0.3V to +6V
REFIN, FB, PGOOD1, PGOOD2 to AGND	-0.3V to (VCC + 0.3V)
CSH, CSL to AGND	-0.3V to (VCC + 0.3V)
DL to PGND1	-0.3V to (VDD + 0.3V)
BST to PGND1	-1V to +34V
BST to LX	-0.3V to +6V
DH to LX	-0.3V to (VBST + 0.3V)
BST to VDD	-0.3V to +26V

VTTI to PGND2	-0.3V to +6V
VTT to PGND2	-0.3V to (VTTI + 0.3V)
VTTs to AGND	-0.3V to (VCC + 0.3V)
VTR to AGND	-0.3V to (VCSL + 0.3V)
PGND1, PGND2 to AGND	-0.3V to +0.3V
Continuous Power Dissipation (TA = +70°C) 24-Pin, 4mm x 4mm TQFN-EP (derated 27.8mW/°C above +70°C)	2222mW
Operating Temperature Range	-40°C to +85°C
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(VIN = 12V, VCC = VDD = VSHDN = VREFIN = 5V, VCSL = 1.8V, STDBY = SKIP = AGND, TA = 0°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>PWM CONTROLLER</b>							
Input Voltage Range	VIN		3		26	V	
	VCC, VDD		4.5		5.5		
Output Voltage Accuracy	VCSL	VIN = 4.5V to 26V, SKIP = VCC	FB = AGND	1.485	1.500	1.515	V
			FB = VCC	1.782	1.800	1.818	
			FB = Adj	0.99	1.000	1.01	
Output Voltage Range	VCSL		1		2.7	V	
Load Regulation Error		VCSH - VCSL = 0 to 18mV, SKIP = VCC		0.1		%	
Line Regulation Error		VDD = 4.5V to 5.5V, VIN = 4.5V to 26V		0.25		%	
Soft-Start Ramp Time	tsSTART	Rising edge of SHDN		1.4	2.1	ms	
Soft-Stop Ramp Time	tsSTOP	Falling edge of SHDN		2.8		ms	
Soft-Stop Threshold				25		mV	
On-Time Accuracy (Note 2)	tON	VIN = 12V, VCSL = 1.2V	RTON = 96.75k→ (600kHz), 167ns nominal	-15		+15	%
			RTON = 200k→(300kHz), 333ns nominal	-10		+10	
			RTON = 303.25k→ (200kHz), 500ns nominal	-15		+15	

# Complete DDR2 and DDR3 Memory Power-Management Solution

MAX17000

## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = 12V$ ,  $V_{CC} = V_{DD} = V_{SHDN} = V_{REFIN} = 5V$ ,  $V_{CSL} = 1.8V$ ,  $\overline{STDBY} = \overline{SKIP} = AGND$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 2)		250	350	ns
Quiescent Supply Current ( $V_{DD}$ )	$I_{DD}$	FB forced above 1.0V, $\overline{STDBY} = AGND$ or $V_{CC}$ , $T_A = +25^{\circ}C$		0.01	1.00	$\mu A$
Quiescent Supply Current ( $V_{CC}$ )	$I_{CC}$	FB forced above 1.0V (SMPS, VTT, and VTTR blocks); $\overline{STDBY} = V_{CC}$		2	4	mA
		FB forced above 1.0V (ultra-skip and VTTR blocks); $\overline{STDBY} = AGND$		275	475	$\mu A$
Shutdown Supply Current ( $V_{DD} + V_{CC}$ )	$I_{CC} + I_{DD}$	$\overline{SHDN} = AGND$ , $T_A = +25^{\circ}C$		0.01	5	$\mu A$
TON Pin Shutdown Current	$I_{TON}$	$\overline{SHDN} = AGND$ , $V_{IN} = 26V$ , $V_{DD} = 0$ or $5V$ , $T_A = +25^{\circ}C$		0.01	1.00	$\mu A$
<b>LINEAR REGULATOR (VTT)</b>						
VTTI Input Voltage Range	$V_{TTI}$		1.0		2.8	V
VTTI Supply Current	$I_{VTTI}$	$V_{VTTI} = 2.5V$ , $V_{REFIN} = 1.4V$		10	50	$\mu A$
VTTI Shutdown Current		$\overline{SHDN} = AGND$ , $T_A = +25^{\circ}C$			10	$\mu A$
REFIN Input Bias Current		$V_{VTTI} = 2.5V$ , $V_{REFIN} = 1.4V$	-50		+50	nA
REFIN Range	$V_{REFIN}$		0.5		1.5	V
REFIN Disable Threshold			$V_{CC} - 0.3$			V
VTT Internal MOSFET		High-side on-resistance (source, $I_{VTT} = 0.1A$ )		0.12	0.25	$\Omega$
		Low-side on-resistance (sink, $I_{VTT} = 0.1A$ )		0.18	0.36	
VTT Output-Accuracy Source Load		$(V_{REFIN} - 5mV)$ or $(V_{CSL}/2 - 5mV)$ to $V_{TTS}$ , $V_{TT} = V_{TTS}$	$V_{REFIN} = 1V$ , $I_{VTT} = +50\mu A$	-5	+5	mV
			$V_{REFIN} = 0.5V$ to $1.5V$ , $I_{VTT} = +300mA$		-5	
VTT Output-Accuracy Sink Load		$(V_{REFIN} + 5mV)$ or $(V_{CSL}/2 + 5mV)$ to $V_{TTS}$ , $V_{TT} = V_{TTS}$	$V_{REFIN} = 1V$ , $I_{VTT} = -50\mu A$	-5	+5	mV
			$V_{REFIN} = 0.5V$ to $1.5V$ , $I_{VTT} = -300mA$		+5	
VTT Load Regulation		$-50\mu A$ to $-1A \leq I_{VTT} \leq +50\mu A$ to $+1A$		13	17	mV/A
VTT Line Regulation		$1.0V \leq V_{TTI} \leq 2.8V$ , $I_{VTT} = \pm 100mA$		1		mV
VTT Current Limit		Source	2		4	A
		Sink	-4		-2	
VTT Current-Limit Soft-Start Time		With respect to internal VTT_EN signal		160		$\mu s$
VTT Discharge MOSFET		OVP = $V_{CC}$		16		$\Omega$
VTTI Input Current		$T_A = +25^{\circ}C$		0.1	1.0	$\mu A$

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = 12V$ ,  $V_{CC} = V_{DD} = V_{SHDN} = V_{REFIN} = 5V$ ,  $V_{CSL} = 1.8V$ ,  $\overline{STDBY} = \overline{SKIP} = AGND$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>REFERENCE BUFFER (VTTR)</b>						
VTTR Output Accuracy (Adj)		REFIN to VTTR	$I_{VTT} = \pm 1mA$	-10	+10	mV
			$I_{VTT} = \pm 3mA$	-20	+20	
VTTR Output Accuracy (Preset)		$V_{CSL}/2$ to VTTR	$I_{VTT} = \pm 1mA$	-10	+10	mV
			$I_{VTT} = \pm 3mA$	-20	+20	
VTTR Maximum Recommended Current		Source/sink		5		mA
<b>FAULT DETECTION (SMPS)</b>						
SMPS OVP and PGOOD1 Upper Trip Threshold			12	15	18	%
SMPS OVP and PGOOD1 Upper Trip Threshold Fault-Propagation Delay	$t_{OVP}$	FB forced 25mV above trip threshold		10		$\mu s$
SMPS Output Undervoltage Fault-Propagation Delay	$t_{UVP}$			200		$\mu s$
SMPS PGOOD1 Lower Trip Threshold		Measured at FB, hysteresis = 25mV	-12	-15	-18	%
PGOOD1 Lower Trip Threshold Propagation Delay	$t_{PGOOD1}$	FB forced 50mV below PGOOD1 trip threshold		10		$\mu s$
PGOOD1 Output Low Voltage		$I_{SINK} = 3mA$			0.4	V
PGOOD1 Leakage Current	$I_{PGOOD1}$	FB = 1V (PGOOD1 high impedance), PGOOD1 forced to 5V, $T_A = +25^{\circ}C$			1	$\mu A$
TON POR Threshold	$V_{POR(IN)}$	Rising edge, PWM disabled below this level; hysteresis = 200mV		3.0		V
<b>FAULT DETECTION (VTT)</b>						
PGOOD2 Upper Trip Threshold		Hysteresis = 25mV	8	10	13	%
PGOOD2 Lower Trip Threshold		Hysteresis = 25mV	-13	-10	-8	%
PGOOD2 Propagation Delay	$t_{PGOOD2}$	VTTs forced 50mV beyond PGOOD2 trip threshold		10		$\mu s$
PGOOD2 Fault Latch Delay		VTTs forced 50mV beyond PGOOD2 trip threshold		5		ms
PGOOD2 Output Low Voltage		$I_{SINK} = 3mA$			0.4	V
PGOOD2 Leakage Current	$I_{PGOOD2}$	VTTs = $V_{REFIN}$ (PGOOD2 high impedance), PGOOD2 forced to 5V, $T_A = +25^{\circ}C$			1	$\mu A$
<b>FAULT DETECTION</b>						
Thermal-Shutdown Threshold	$T_{SHDN}$	Hysteresis = 15 $^{\circ}C$		160		$^{\circ}C$
$V_{CC}$ Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, IC disabled below this level; hysteresis = 200mV	3.8	4.1	4.4	V
CSL Discharge MOSFET		OVP = $V_{CC}$		16		$\rightarrow$

# Complete DDR2 and DDR3 Memory Power-Management Solution

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = 12V$ ,  $V_{CC} = V_{DD} = V_{SHDN} = V_{REFIN} = 5V$ ,  $V_{CSL} = 1.8V$ ,  $\overline{STDBY} = \overline{SKIP} = AGND$ ,  $T_A = 0^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = +25^{\circ}C$ .) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CURRENT LIMIT</b>						
Valley Current-Limit Threshold	$V_{LIMIT}$	$V_{CSH} - V_{CSL}$	17	20	25	mV
Current-Limit Threshold (Negative)	$V_{NEG}$	$V_{CSH} - V_{CSL}$ , $\overline{SKIP} = V_{CC}$		-23		mV
Current-Limit Threshold (Zero Crossing)	$V_{ZX}$	$V_{CSH} - V_{CSL}$		1		mV
<b>SMPS GATE DRIVERS</b>						
DH Gate Driver On-Resistance	$R_{DH}$	BST - LX forced to 5V		1.5	5.0	$\Omega$
DL Gate Driver On-Resistance	$R_{DL}$	DL high		1.5	5.0	$\Omega$
		DL low		0.6	3.0	
DH Gate Driver Source/Sink Current	$I_{DH}$	DH forced to 2.5V, BST - LX forced to 5V		1		A
DL Gate Driver Source/Sink Current	$I_{DL(SRC)}$	DL forced to 2.5V		1		A
	$I_{DL(SNK)}$	DL forced to 2.5V		3		
Dead Time	$t_{DEAD}$	DL rising, $T_A = +25^{\circ}C$	10	25		ns
		DL falling, $T_A = +25^{\circ}C$	15	35		
Internal BST Switch On-Resistance	$R_{BST}$	$I_{BST} = 10mA$ , $V_{DD} = 5V$ internal design target		4.5		$\Omega$
LX, BST Leakage Current		$V_{BST} = V_{LX} = 26V$ , $\overline{SHDN} = AGND$ , $T_A = +25^{\circ}C$		0.001	20	$\mu A$
<b>INPUTS AND OUTPUTS</b>						
Logic Input Threshold		$\overline{SHDN}$ , $\overline{STDBY}$ , $\overline{SKIP}$ , OVP, rising edge hysteresis = 300mV/600mV (min/max)	1.30	1.65	2.00	V
Logic Input Current		$\overline{SKIP} = AGND$ or $V_{CC}$ ,	-1		+1	$\mu A$
Input Leakage Current		$V_{CSH} = 0V$ or $V_{CC}$ , $T_A = +25^{\circ}C$	-1		+1	$\mu A$
Input Bias Current		$V_{CSL} = 0V$ or $V_{CC}$		55	100	$\mu A$

# Complete DDR2 and DDR3 Memory Power-Management Solution

## ELECTRICAL CHARACTERISTICS

( $V_{IN} = 12V$ ,  $V_{CC} = V_{DD} = V_{SHDN} = V_{REFIN} = 5V$ ,  $V_{CSL} = 1.8V$ ,  $\overline{STDBY} = \overline{SKIP} = AGND$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.)  
(Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	
<b>PWM CONTROLLER</b>						
Input Voltage Range	$V_{IN}$		3	26	V	
	$V_{CC}, V_{DD}$		4.5	5.5		
Output Voltage Accuracy	$V_{CSL}$	$V_{IN} = 4.5V$ to $26V$ , $\overline{SKIP} = V_{CC}$	FB = AGND	1.485	1.520	V
			FB = $V_{CC}$	1.782	1.820	
			FB = Adj	0.990	1.020	
On-Time Accuracy (Note 2)	$t_{ON}$	$V_{IN} = 12V$ , $V_{CSL} = 1.2V$	$R_{TON} = 96.75k \rightarrow$ (600kHz), 167ns nominal	-15	+15	%
			$R_{TON} = 200k \rightarrow$ (300kHz), 333ns nominal	-10	+10	
			$R_{TON} = 303.25k \rightarrow$ (200kHz), 500ns nominal	-15	+15	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 2)		350	ns	
Quiescent Supply Current ( $V_{CC}$ )	$I_{CC}$	FB forced above 1.0V (PWM, VTT, and VTTR blocks); $\overline{STDBY} = V_{CC}$		4	mA	
		FB forced above 1.0V (ultra-skip and VTTR blocks); $\overline{STDBY} = AGND$		475	$\mu A$	
<b>LINEAR REGULATOR (VTT)</b>						
VTTI Input Voltage Range	$V_{VTTI}$		1.0	2.8	V	
VTTI Supply Current	$I_{VTTI}$	$V_{VTTI} = 2.5V$ , $V_{REFIN} = 1.4V$		50	$\mu A$	
REFIN Range	$V_{REFIN}$		0.5	1.5	V	
REFIN Disable Threshold			$V_{CC} - 0.3$		V	
VTT Internal MOSFET		High-side on-resistance (source, $I_{VTT} = 0.1A$ )		0.25	$\rightarrow$	
		Low-side on-resistance (sink, $I_{VTT} = 0.1A$ )		0.36		
VTT Load Regulation		$-50\mu A$ to $-1A \leq I_{VTT} \leq +50\mu A$ to $+1A$		17	mV/A	

# Complete DDR2 and DDR3 Memory Power-Management Solution

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = 12V$ ,  $V_{CC} = V_{DD} = V_{SHDN} = V_{REFIN} = 5V$ ,  $V_{CSL} = 1.8V$ ,  $\overline{STDBY} = \overline{SKIP} = AGND$ ,  $T_A = -40^{\circ}C$  to  $+85^{\circ}C$ , unless otherwise noted.)  
(Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	
<b>REFERENCE BUFFER (VTTR)</b>						
VTTR Output Accuracy (Adj)		REFIN to VTTR	$I_{VT} = \pm 1mA$	-10	+10	mV
			$I_{VT} = \pm 3mA$	-20	+20	
VTTR Output Accuracy (Preset)		$V_{CSL}/2$ to VTTR	$I_{VT} = \pm 1mA$	-10	+10	mV
			$I_{VT} = \pm 3mA$	-20	+20	
<b>FAULT DETECTION (SMPS)</b>						
PGOOD1 Output Low Voltage		$I_{SINK} = 3mA$		0.4	V	
<b>FAULT DETECTION (VTT)</b>						
PGOOD2 Output Low Voltage		$I_{SINK} = 3mA$		0.4	V	
<b>FAULT DETECTION</b>						
$V_{CC}$ Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, IC disabled below this level; hysteresis = 200mV	4.0	4.4	V	
<b>CURRENT LIMIT</b>						
Valley Current-Limit Threshold	$V_{LIMIT}$	$V_{CSH} - V_{CSL}$	15	25	mV	
<b>SMPS GATE DRIVERS</b>						
DH Gate Driver On-Resistance	$R_{DH}$	BST - LX forced to 5V		5	→	
DL Gate Driver On-Resistance	$R_{DL}$	DL high		5	→	
		DL low		3		
Dead Time	$t_{DEAD}$	DL rising	10		ns	
		DL falling	15			
<b>INPUTS AND OUTPUTS</b>						
Logic Input Threshold		$\overline{SHDN}$ , $\overline{STDBY}$ , $\overline{SKIP}$ , OVP, rising edge hysteresis = 300mV/600mV (min/max)	1.3	2	V	

**Note 1:** Limits are 100% production tested at  $T_A = +25^{\circ}C$ . Maximum and minimum limits over temperature are guaranteed by design and characterization.

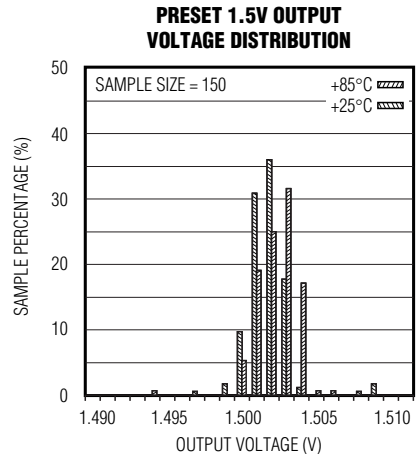
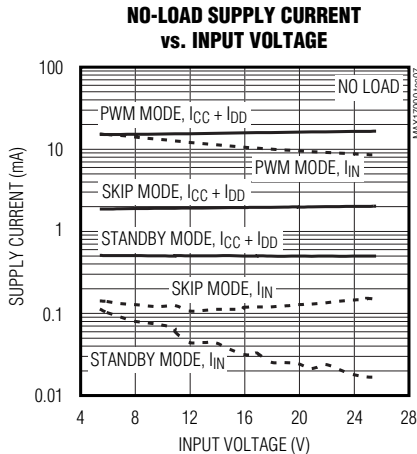
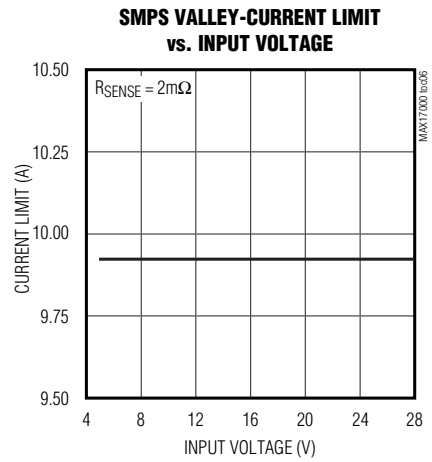
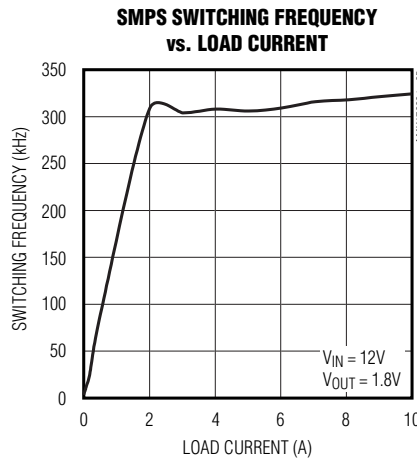
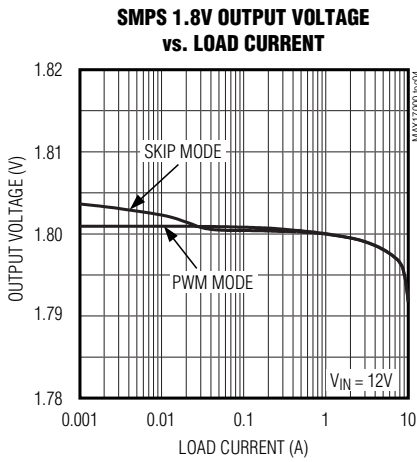
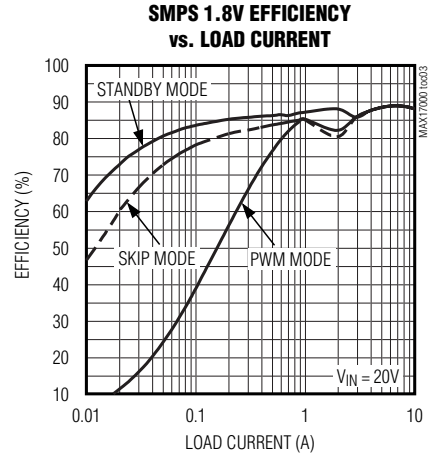
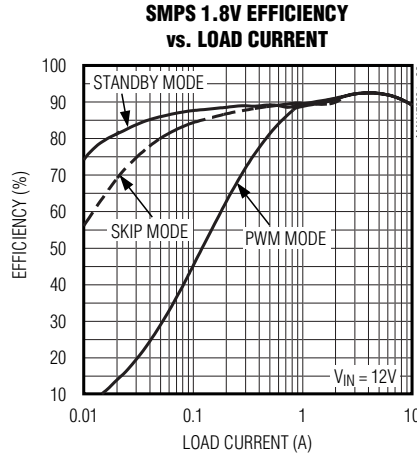
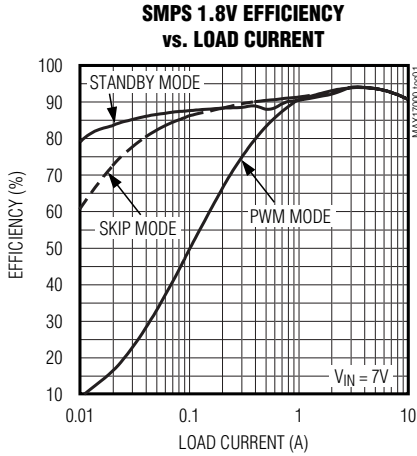
**Note 2:** On-time and off-time specifications are measured from 50% point at the DH pin with LX = GND,  $V_{BST} = 5V$ , and a 250pF capacitor connected from DH to LX. Actual in-circuit times might differ due to MOSFET switching speeds.



# Complete DDR2 and DDR3 Memory Power-Management Solution

## Typical Operating Characteristics

(MAX17000 Circuit of Figure 1,  $V_{IN} = 12V$ ,  $V_{DD} = V_{CC} = 5V$ ,  $\overline{SKIP} = GND$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)



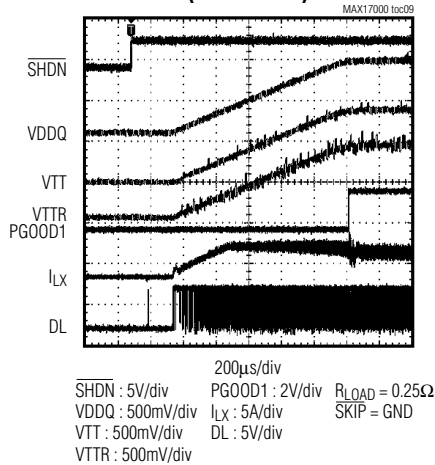
# Complete DDR2 and DDR3 Memory Power-Management Solution

MAX17000

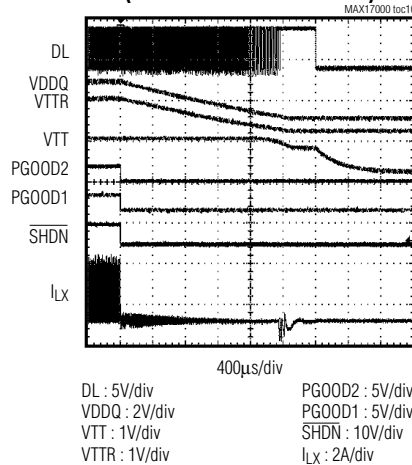
## Typical Operating Characteristics (continued)

(MAX17000 Circuit of Figure 1,  $V_{IN} = 12V$ ,  $V_{DD} = V_{CC} = 5V$ ,  $\overline{SKIP} = GND$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

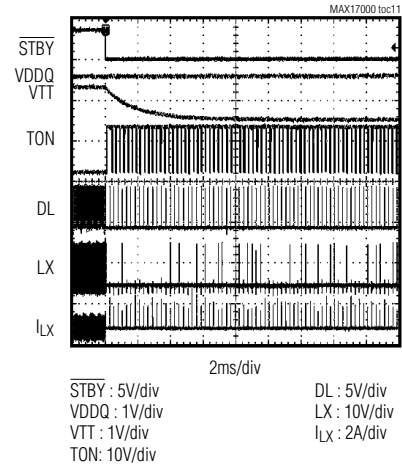
**STARTUP WAVEFORM  
(HEAVY LOAD)**



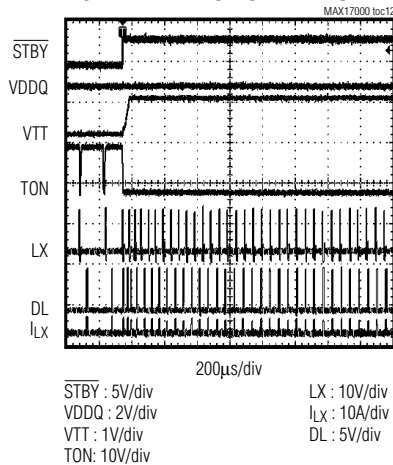
**SHUTDOWN WAVEFORM  
(DISCHARGE MODE ENABLED)**



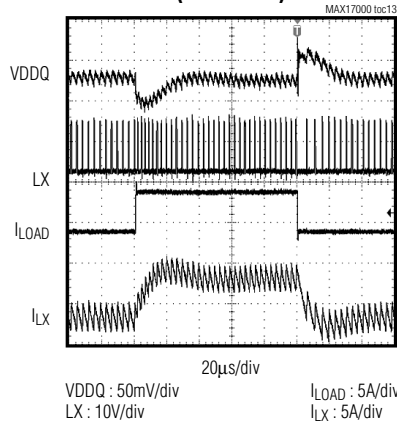
**STANDBY TRANSITION WAVEFORM**



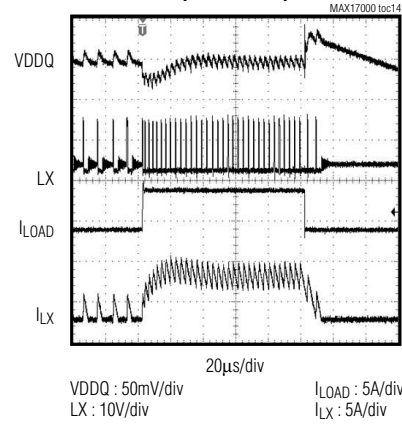
**STANDBY TRANSITION WAVEFORM**



**SMPS LOAD-TRANSIENT RESPONSE  
(SKIP MODE)**



**SMPS LOAD-TRANSIENT RESPONSE  
(SKIP MODE)**

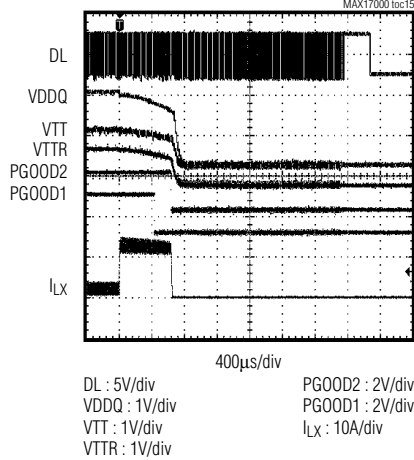


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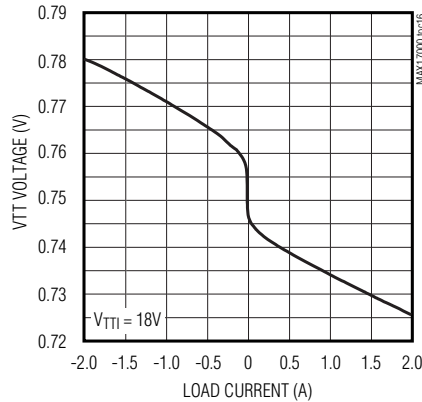
## Typical Operating Characteristics (continued)

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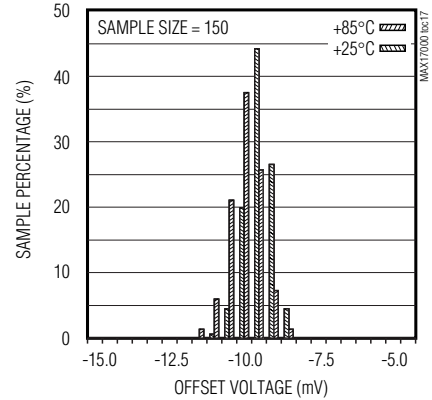
**OUTPUT OVERLOAD WAVEFORM**



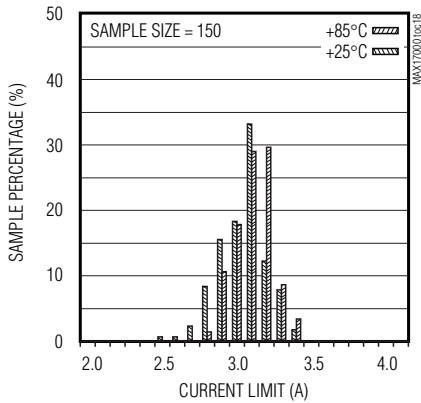
**VTT VOLTAGE vs. SOURCE/SINK LOAD CURRENT**



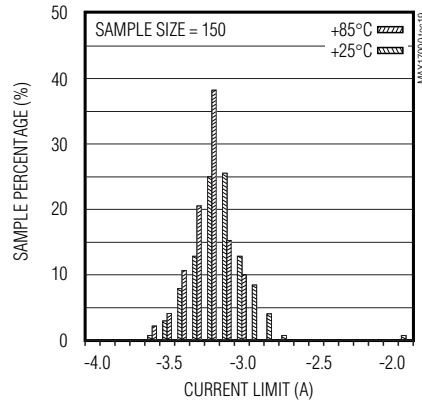
**VTT OFFSET VOLTAGE DISTRIBUTION AT 300mA LOAD**



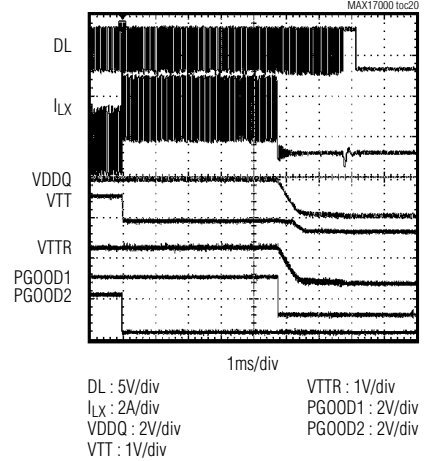
**VTT SOURCE CURRENT LIMIT**



**VTT SINK CURRENT LIMIT**



**VTT OVERLOAD FAULT WAVEFORMS (5ms TIMER)**



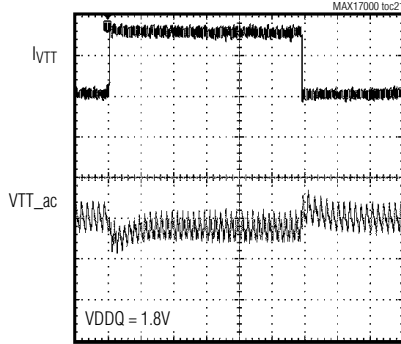
# Complete DDR2 and DDR3 Memory Power-Management Solution

MAX17000

## Typical Operating Characteristics (continued)

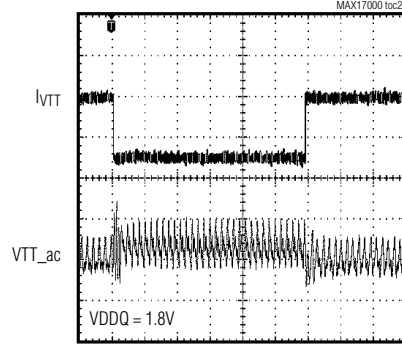
(MAX17000 Circuit of Figure 1,  $V_{IN} = 12V$ ,  $V_{DD} = V_{CC} = 5V$ ,  $\overline{SKIP} = GND$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

**VTT LOAD-TRANSIENT RESPONSE (SOURCE)  
I<sub>VTT</sub> BETWEEN 10mA AND 1.5A**



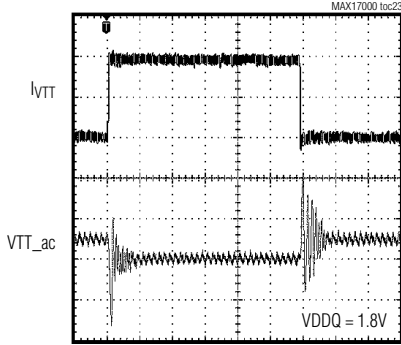
I<sub>VTT</sub> : 1A/div  
VTT : 20mV/div

**VTT LOAD-TRANSIENT RESPONSE  
(SINK)**



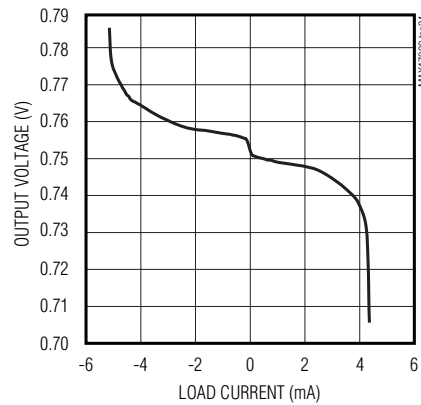
I<sub>VTT</sub> : 1A/div  
VTT : 20mV/div

**VTT LOAD-TRANSIENT RESPONSE  
(SOURCE/SINK)**



I<sub>VTT</sub> : 1A/div  
VTT : 20mV/div

**VVTR OUTPUT VOLTAGE  
vs. LOAD CURRENT**



# Complete DDR2 and DDR3 Memory Power-Management Solution

## Pin Description

PIN	NAME	FUNCTION
1	OVP	OVP Mode Control. This input selectively enables/disables the SMPS OV protection feature and output discharge mode. When enabled, the SMPS OV protection feature is enabled. Connect OVP to the following voltage levels for the desired function: High (> 2.4V) = Enable SMPS OV protection, and SMPS and VTT discharge FETs. Low (AGND) = Disable SMPS OV protection, and SMPS and VTT discharge FETs.
2	PGOOD1	Open-Drain Power-Good Output. PGOOD1 is low when the SMPS output voltage is more than 15% (typ) beyond the normal regulation point, during soft-start, and in shutdown. After the soft-start circuit has terminated, PGOOD1 becomes high impedance if the SMPS output is in regulation.
3	PGOOD2	Open-Drain Power-Good Output. PGOOD2 is low when the VTT output voltage is more than 10% (typ) beyond the normal regulation point, in shutdown, in standby, and during soft-start. After the SMPS soft-start circuit has terminated, PGOOD2 becomes high impedance if the VTT output is in regulation.
4	$\overline{\text{STDBY}}$	Standby Control Input. When $\overline{\text{SHDN}}$ is high and $\overline{\text{STDBY}}$ is low, the MAX17000 enters a low-quiescent current mode, putting the SMPS in ultra-skip operation and turning off the VTT output (high-Z). This mode helps save converter power loss in computer standby operation. When $\overline{\text{STDBY}}$ is high, normal SMPS operation resumes and the VTT output is enabled.
5	VTTs	Sense Pin for Termination Supply Output. Normally connected to the VTT pin to allow accurate regulation to $V_{\text{CSL}}/2$ or the REFIN voltage.
6	VTTR	Termination Reference Buffer Output. VTTR tracks $V_{\text{CSL}}/2$ when REFIN is connected to $V_{\text{CC}}$ . VTTR tracks $V_{\text{REFIN}}$ when a voltage between 0.5V to 1.5V is set at REFIN. Decouple VTTR to AGND with a 0.33 $\mu$ F ceramic capacitor.
7	PGND2	Power Ground for VTT. Connect PGND2 externally to the underside of the exposed pad.
8	VTT	Termination Power-Supply Output. Connect VTT to VTTs to regulate the VTT voltage to the VTTs regulation setting.
9	VTTI	Termination Power-Supply Input. VTTI is the input power supply to the VTT linear regulator. Normally connected to the output of the SMPS regulator for DDR applications.
10	REFIN	External Reference Input. REFIN sets the feedback regulation voltage ( $V_{\text{TTR}} = V_{\text{TTS}} = V_{\text{REFIN}}$ ) of the MAX17000. Connect REFIN to $V_{\text{CC}}$ to use the internal $V_{\text{CSL}}/2$ divider. Connect a 0.5V to 1.5V voltage input to set the adjustable output for VTT, VTTs, and VTTR.
11	FB	Feedback Input for SMPS Output. Connect to $V_{\text{CC}}$ for a fixed +1.8V output or to AGND for a fixed +1.5V output. For an adjustable output (1.0V to 2.7V), connect FB to a resistive divider from the output voltage. FB regulates to +1.0V.
12	CSL	Negative Input of the PWM Output Current-Sense and Supply Input for VTTR. Connect CSL to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. CSL is also the path for the internal 16 $\rightarrow$ discharge MOSFET when $V_{\text{CC}}$ UVLO occurs with OVP enabled.
13	CSH	Positive Input of the PWM Output Current Sense. Connect CSH to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.



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## Pin Description (continued)

MAX17000

PIN	NAME	FUNCTION
14	TON	Switching Frequency Setting Input. An external resistor between the input power source and this pin sets the switching frequency per phase according to the following equation: $T_{SW} = C_{TON} \times (R_{TON} + 6.5k\Omega)$ where $C_{TON} = 16.26pF$ . TON is high impedance in shutdown.
15	DH	High-Side Gate-Driver Output. Swings from LX to BST. DH is low when in shutdown or UVLO.
16	LX	Inductor Connection. Connect LX to the switched side of the inductor as shown in Figure 1.
17	BST	Boost Flying Capacitor Connection. Connect to an external 0.1 $\mu$ F, 6V capacitor as shown in Figure 1. The MAX17000 contains an internal boost switch.
18	DL	Synchronous-Rectifier Gate-Driver Output. DL swings from V <sub>DD</sub> to PGND1.
19	V <sub>DD</sub>	Supply Voltage Input for the DL Gate Driver and 3.3V Reference/Analog Supply. Connect to the system supply voltage (+4.5V to +5.5V). Bypass V <sub>DD</sub> to power ground with a 1 $\mu$ F or greater ceramic capacitor.
20	PGND1	Power Ground. Ground connection for the low-side MOSFET gate driver.
21	AGND	Analog Ground. <b>Connect backside exposed pad to AGND.</b>
22	$\overline{SKIP}$	Pulse-skipping Control Input. This input determines the mode of operation under normal steady-state conditions and dynamic output voltage transitions: High (> 2.4V) = Forced-PWM operation Low (AGND) = Pulse-skipping mode
23	V <sub>CC</sub>	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass V <sub>CC</sub> to AGND with a 1 $\mu$ F or greater ceramic capacitor.
24	$\overline{SHDN}$	Shutdown Control Input. Connect to V <sub>CC</sub> for normal operation. When $\overline{SHDN}$ is pulled low, the MAX17000 slowly ramps down the output voltage to ground. When the internal target voltage reaches 25mV, the controller forces DL low, and enters the low current (1 $\mu$ A) shutdown state.  When discharge mode is enabled by OVP (OVP = high), the CSL and VTT internal 16 $\rightarrow$ discharge MOSFETs are enabled in shutdown. When discharge mode is disabled by OVP (OVP = low), LX, VTT, and VTTR are high impedance in shutdown.  A rising edge on $\overline{SHDN}$ clears the fault OV protection latch.
—	EP	Exposed Pad. <b>Connect backside exposed pad to AGND.</b>

# Complete DDR2 and DDR3 Memory Power-Management Solution

## Standard Application Circuits

The MAX17000 standard application circuit (Figure 1) generates the VDDQ, VTT, and VTTR rails for DDR,

DDR2, or DDR3 in a notebook computer. See Table 1 for component selections. Table 2 lists the component manufacturers. Table 3 is the operating mode truth table.

**Table 1. Component Selection for Standard Applications**

COMPONENT	V <sub>OUT</sub> = 1.5V TO 1.8V AT 10A	V <sub>OUT</sub> = 1.5V TO 1.8V AT 6A
	V <sub>IN</sub> = 7V TO 20V (300kHz)	V <sub>IN</sub> = 7V TO 16V (500kHz)
Input Capacitor	(2x) 10μF, 25V Taiyo Yuden TMK432BJ106KM	10μF, 25V Taiyo Yuden TMK432BJ106KM
Output Capacitor	(2x) 330μF, 2.5V, 12m (C2 case) SANYO 2R5TPE330MCC2	(2x) 220μF, 2.5V, 21m (B2 case) SANYO 2R5TPE220MLB
Inductor	1.4μH, 12A, 3.4m→(typ) Sumida CDEP105(L)NP-1R4	1.4μH, 12A, 3.4m (typ) Sumida CDEP105(L)NP-1R4
Current-Sensing Resistor	2m→ 0.5W (2010) Vishay WSL20102L000FEA	3m→ 0.5W (2010) Vishay WSL20103L000FEA
MOSFETs	30V, 20A n-channel MOSFET (high side) Fairchild FDMS8690; 30V, 40A n-channel MOSFET (low side) Fairchild FDMS8660S	30V 20A n-channel MOSFET (high side) Fairchild FDMS8690; 30V 40A n-channel MOSFET (low side) Fairchild FDMS8660S

**Table 2. Component Suppliers**

SUPPLIER	PHONE	WEBSITE
<b>INDUCTORS</b>		
Dale (Vishay)	402-563-6866 (USA)	www.vishay.com
NEC/TOKIN America, Inc.	510-324-4110 (USA)	www.nec-tokinamerica.com
Panasonic Corp.	65-231-3226 (Singapore), 408-749-9714 (USA)	www.panasonic.com
Sumida Corp.	408-982-9660 (USA)	www.sumida.com
TOKO America, Inc.	858-675-8013 (USA)	www.tokoam.com
<b>CAPACITORS</b>		
AVX Corp.	843-448-9411 (USA)	www.avxcorp.com
KEMET Corp.	408-986-0424 (USA)	www.kemet.com
Panasonic Corp.	65-231-3226 (Singapore), 408-749-9714 (USA)	www.panasonic.com
SANYO Electric Co., Ltd.	81-72-870-6310 (Japan), 619-661-6835 (USA)	www.sanyodevice.com
Taiyo Yuden	03-3667-3408 (Japan), 408-573-4150 (USA)	www.t-yuden.com
TDK Corp.	847-803-6100 (USA), 81-3-5201-7241 (Japan)	www.component.tdk.com
<b>SENSING RESISTORS</b>		
Vishay	402-563-6866 (USA)	www.vishay.com
<b>MOSFET</b>		
Fairchild Semiconductor	800-341-0392 (USA)	www.fairchildsemi.com
<b>DIODES</b>		
Central Semiconductor Corp.	631-435-1110	www.centalsemi.com
Nihon Inter Electronics Corp.	81-3-3343-84-3411 (Japan)	www.niec.co.jp

# Complete DDR2 and DDR3 Memory Power-Management Solution

MAX17000

Table 3. Operating Mode Truth Table

	$\overline{\text{SHDN}}$	$\overline{\text{STDBY}}$	$\overline{\text{SKIP}}$	OPERATION
1	L → H	L → H	X	SMPS output ramps up in skip mode with a 1.4ms (typ) ramp time. PGOOD1 is held low until the SMPS output is in regulation. VTT and VTTR ramp up to the final voltage based on $V_{\text{CSL}/2}$ or $V_{\text{REFIN}}$ . PGOOD2 is held low until VTT is in regulation.
2	L → H	L	X	SMPS output ramps up in skip mode with a 1.4ms ramp time. PGOOD1 is held low until the SMPS output is in regulation. Once CSL or FB is in regulation, the PWM block turns off and enters standby mode. VTT remains off throughout since $\overline{\text{STDBY}}$ is low. PGOOD2 stays low throughout. The VTT discharge FET is enabled if OVP is high, but disabled if OVP is low. VTTR ramps up to the final voltage based on $V_{\text{CSL}/2}$ or $V_{\text{REFIN}}$ .
3	H	L → H	X	Ultra-skip and standby modes are exited and the full current capability of the MAX17000 is available. VTT ramps up after the internal SMPS block is ready. VTT ramps to the final voltage based on $V_{\text{CSL}/2}$ or $V_{\text{REFIN}}$ . PGOOD2 goes high when VTT is in regulation.
4	H	H	H	SMPS output is in forced-PWM mode. VTT and VTTR are enabled. PGOOD1 is high when the SMPS output is in regulation. PGOOD2 is high when VTT is in regulation.
5	H	H	L	SMPS output is in normal skip mode. VTT and VTTR are enabled. PGOOD1 is high when the SMPS output is in regulation. PGOOD2 is high when VTT is in regulation.
6	H	L	X	SMPS output is in ultra-skip mode. VTT is off and is high impedance. PGOOD2 is forced low. VTTR is active and regulates to $V_{\text{CSL}/2}$ or $V_{\text{REFIN}}$ .
7	H → L	H	X	Ultra-skip or skip mode is exited as the MAX17000 ramps the output down to zero. VTTR tracks $V_{\text{CSL}/2}$ or $V_{\text{REFIN}}$ during shutdown. After the SMPS output reaches 25mV, DL goes low.
8	H → L	L	X	Ultra-skip or skip mode is exited as the MAX17000 ramps the output down to zero. VTTR tracks $V_{\text{CSL}/2}$ or $V_{\text{REFIN}}$ during shutdown. After the SMPS output reaches 25mV, DL goes low. VTT is not enabled throughout soft-shutdown.
9	L	X	X	DL low. Internal 16Ω discharge MOSFETs on CSL and VTT enabled if OVP is high, but disabled if OVP is low.

# Complete DDR2 and DDR3 Memory Power-Management Solution

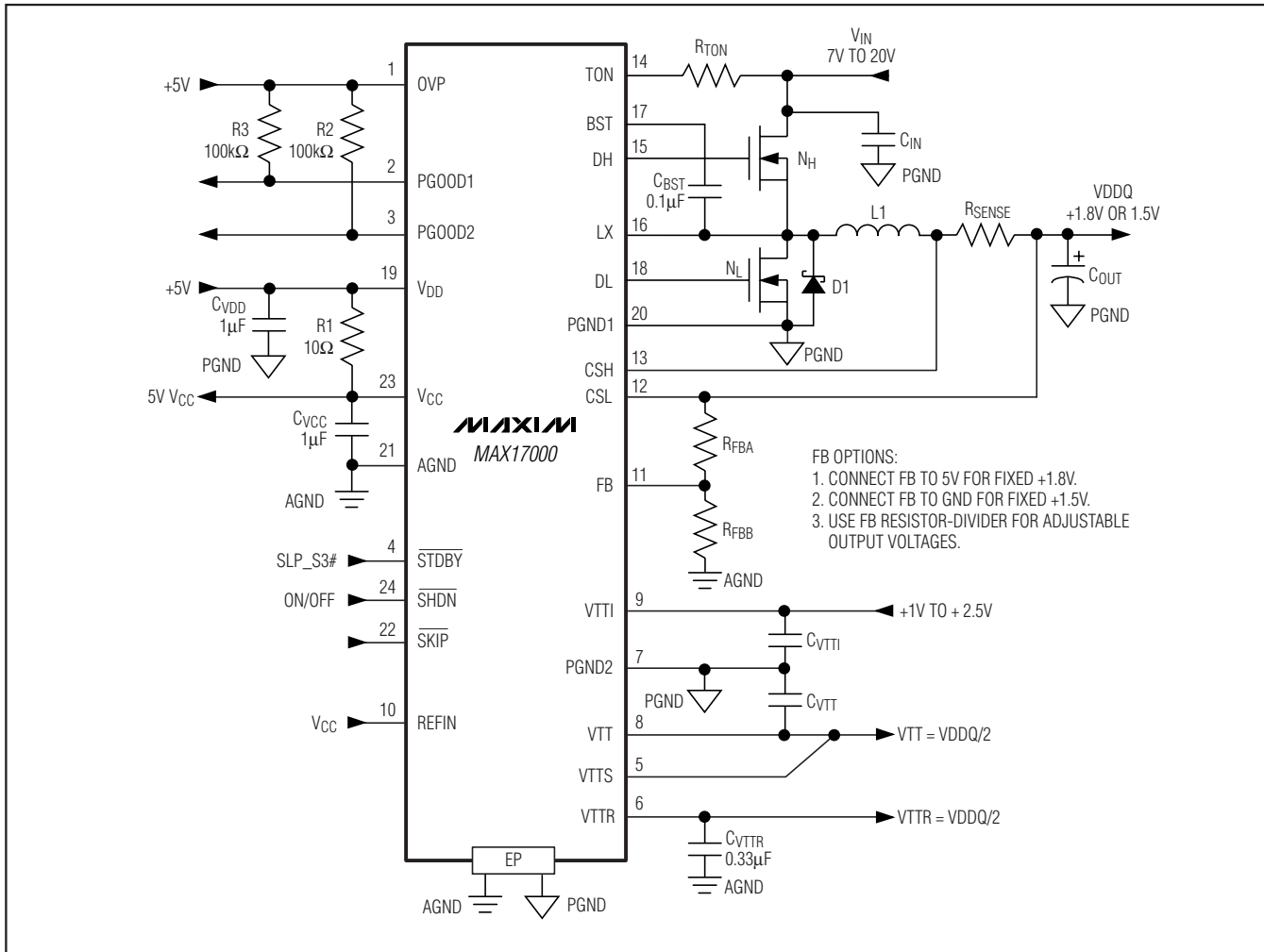


Figure 1. MAX17000 Standard Application Circuit

## Detailed Description

The MAX17000 complete DDR solution comprises a step-down controller, a source/sink LDO regulator, and a reference buffer. Maxim's proprietary Quick-PWM pulse-width modulator in the MAX17000 is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs, while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes. Figure 1 is the MAX17000 standard application circuit and Figure 2 is the MAX17000 functional diagram.

The MAX17000 includes a  $\pm 2A$  source/sink LDO regulator for the memory termination rail. The source/sink regulator features a dead band that either sources or sinks, ideal for the fast-changing short-period loads presenting in memory termination applications. This feature also reduces the VTT output capacitance requirement down to  $1\mu F$ , though load-transient response can still require higher capacitance values between  $10\mu F$  and  $20\mu F$ .

The reference buffer sources and sinks  $\pm 3mA$ , generating a reference rail for use in the memory controller and memory devices.

# Complete DDR2 and DDR3 Memory Power-Management Solution

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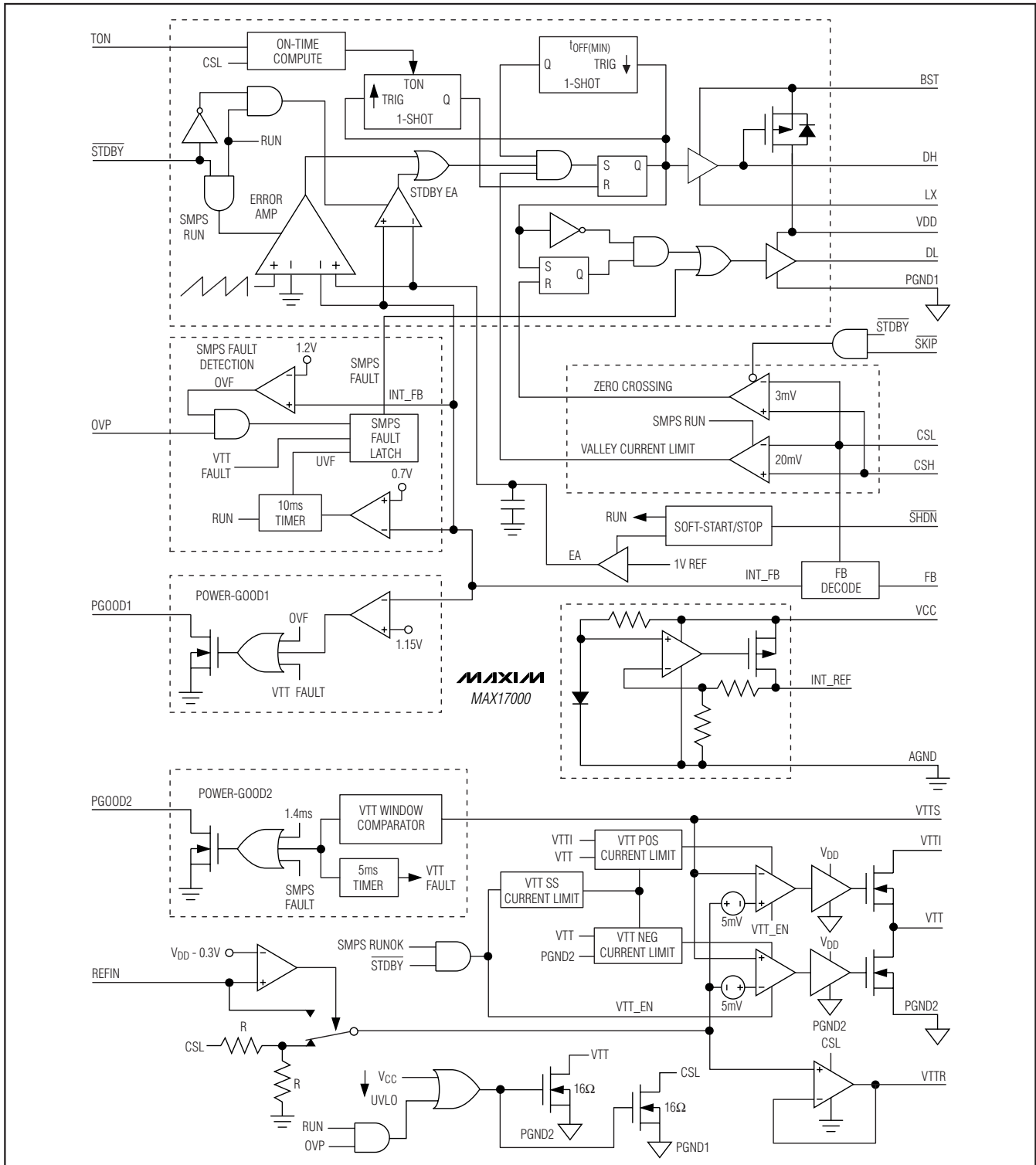


Figure 2. MAX17000 Functional Diagram



# Complete DDR2 and DDR3 Memory Power-Management Solution

## +5V Bias Supply (V<sub>DD</sub>, V<sub>CC</sub>)

The MAX17000 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95% efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator such as the MAX1615.

The 5V bias supply powers both the PWM controller and internal gate-drive power, so the maximum current drawn is:

$$I_{BIAS} = I_Q + f_{SW}Q_G(\text{MOSFETs}) = 2\text{mA to } 20\text{mA (typ)}$$

where  $I_Q$  is the current for the PWM control circuit,  $f_{SW}$  is the switching frequency, and  $Q_G(\text{MOSFETs})$  is the total gate-charge specification limits at  $V_{GS} = 5\text{V}$  for the internal MOSFETs.

## Free-Running Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode regulator with voltage feed-forward. This architecture utilizes the output filter capacitor's ESR to act as a current-sense resistor, so the output ripple voltage can provide the PWM ramp signal. In addition to the general Quick-PWM, the MAX17000 also senses the inductor current through DCR method or with a sensing resistor. Therefore, it is less dependent on the output capacitor ESR for stability. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (250ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

## On-Time One-Shot

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltages. The high-side switch on-time is inversely proportional to the battery voltage as measured by the  $V_{IN}$  input, and proportional to the output voltage.

An external resistor between the input power source and TON pin sets the switching frequency per phase according to the following equation:

$$t_{ON} = \frac{C_{TON} \times (R_{TON} + 6.5\text{k}\Omega) \times (V_{CSL} + 0.075\text{V})}{V_{IN}}$$

$$f_{SW} = \frac{1}{C_{TON} \times (R_{TON} + 6.5\text{k}\Omega)}$$

where  $C_{TON} = 16.26\text{pF}$ , and  $0.075\text{V}$  is an approximation to accommodate for the expected drop across the low-side MOSFET switch. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator.

For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is:

$$f_{SW} = \frac{V_{OUT} + V_{DIS}}{t_{ON} \times (V_{IN} - V_{CHG} + V_{DIS})}$$

where  $V_{DIS}$  is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances;  $V_{CHG}$  is the sum of the parasitic voltage drops in the charging path, including the high-side switch, inductor, and PCB resistances; and  $t_{ON}$  is the on-time calculated by the MAX17000.

## Automatic Pulse-Skipping Mode (SKIP = AGND)

In skip mode ( $\overline{\text{SKIP}} = \text{AGND}$ ), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing.

DC output-accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX17000 regulates the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction ( $\overline{\text{SKIP}} = \text{AGND}$  and  $I_{OUT} < I_{LOAD}(\text{SKIP})$ ), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation. However, the internal integrator corrects for most of it, resulting in very little load regulation.

$\overline{\text{STDBY}} = \text{AGND}$  overrides the  $\overline{\text{SKIP}}$  pin setting, forcing the MAX17000 into standby.

# Complete DDR2 and DDR3 Memory Power-Management Solution

The MAX17000 always uses skip mode during startup, regardless of the  $\overline{\text{SKIP}}$  and  $\overline{\text{STDBY}}$  setting. The  $\overline{\text{SKIP}}$  and  $\overline{\text{STDBY}}$  controls take effect after soft-start is done. See Figure 3.

### Forced-PWM Mode ( $\overline{\text{SKIP}} = \text{VCC}$ )

The low-noise forced-PWM mode ( $\overline{\text{SKIP}} = \text{VCC}$ ) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH maintains a duty factor of  $V_{\text{OUT}}/V_{\text{IN}}$ . The benefit of forced-PWM mode is to keep a fairly constant switching frequency. However, forced-PWM operation comes at a cost: the no-load 5V bias

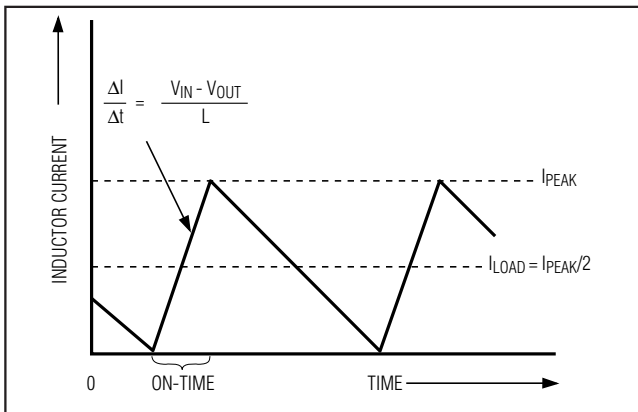


Figure 3. Pulse-Skipping/Discontinuous Crossover Point

current remains between 2mA to 20mA, depending on the switching frequency.

$\overline{\text{STDBY}} = \text{AGND}$  overrides the  $\overline{\text{SKIP}}$  pin setting, forcing the MAX17000 into standby.

The MAX17000 switches to forced-PWM mode during shutdown, regardless of the state of  $\overline{\text{SKIP}}$  and  $\overline{\text{STDBY}}$  levels.

### Standby Mode ( $\overline{\text{STDBY}}$ )

It should be noted that standby mode in the MAX17000 corresponds to computer system standby operation, and is not referring to the MAX17000 shutdown status.

When standby mode is enabled ( $\overline{\text{STDBY}} = \text{AGND}$ ), the MAX17000 switches over from the fast internal PWM block to a low-quiescent current mode using a low-power valley comparator to initiate an on-time pulse. The zero-crossing comparator is enabled so that the MAX17000 only operates in discontinuous mode, reducing the maximum available output current by 1/6. The system is NOT expected to have any fast load transients in such a state. While in standby, VTT is disabled (high impedance) but VTTR remains active.  $\overline{\text{SKIP}}$  is ignored when standby mode is enabled.

When standby mode is disabled ( $\overline{\text{STDBY}} = \text{VCC}$ ), the MAX17000 reenables its fast internal PWM block. Once the internal SMPS block is ready, the VTT block is enabled and the VTT output capacitor is charged. The VTT soft-start current limit increases linearly from zero to its maximum current limit in 160 $\mu\text{s}$  (typ), keeping the input VTTI inrush low. See Figure 4.

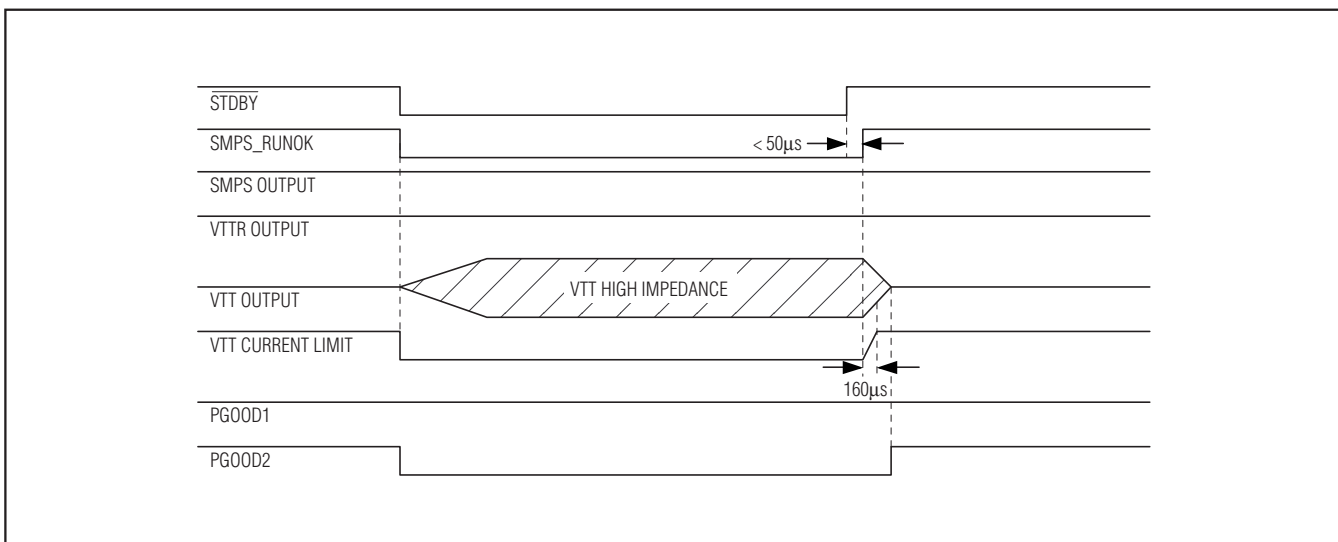


Figure 4. MAX17000 Standby Mode Timing

# Complete DDR2 and DDR3 Memory Power-Management Solution

## Valley Current-Limit Protection

The MAX17000 uses the same valley current-limit protection employed on all Maxim Quick-PWM controllers. If the current exceeds the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and battery voltage. When combined with the undervoltage-protection circuit, this current-limit method is effective in almost every circumstance.

In forced-PWM mode, the MAX17000 also implements a negative current limit to prevent excessive reverse inductor currents when  $V_{OUT}$  is sinking current. The negative current-limit threshold is set to approximately 115% of the positive current limit. See Figure 5.

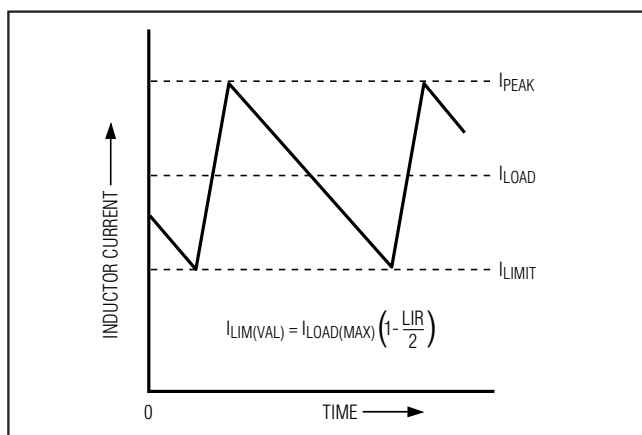


Figure 5. Valley Current-Limit Threshold Point

## Power-Good Outputs (PGOOD1 and PGOOD2)

The MAX17000 features two power-good outputs. PGOOD1 is the open-drain output for a window comparator that continuously monitors the SMPS output. PGOOD1 is actively held low in shutdown and during soft-start and soft-shutdown. After the soft-start terminates, PGOOD1 becomes high impedance as long as the SMPS output voltage is between 115% (typ) and 85% (typ) of the regulation voltage. When the SMPS output voltage exceeds the 115%/85% regulation window, the MAX17000 pulls PGOOD1 low. Any fault condition on the SMPS output forces PGOOD1 and PGOOD2 low and latches off until the fault latch is cleared by toggling  $\overline{SHDN}$  or cycling  $V_{CC}$  power below 1V. Detection of an OVP event immediately pulls PGOOD1 low, regardless of the OVP state (OVP enabled or disabled).

PGOOD2 is the open-drain output for a window comparator that continuously monitors the VTT output. PGOOD2 is actively held low in standby, shutdown, and during soft-start. PGOOD2 becomes high impedance as long as the VTT output voltage is within  $\pm 10\%$  of the regulation voltage. When the VTT output exceeds the  $\pm 10\%$  threshold, the MAX17000 pulls PGOOD2 low. If PGOOD2 remains low for 5ms (typ), the MAX17000 latches off with the soft-shutdown sequence.

For logic-level output voltages, connect an external 100k $\Omega$  pullup resistor from PGOOD1 and PGOOD2 to  $V_{DD}$ .

## POR, UVLO

Power-on reset (POR) occurs when  $V_{CC}$  rises above approximately 2V, resetting the fault latch and soft-start circuit and preparing the controller for power-up. When OVP is enabled, a rising edge on POR turns on the 16 $\Omega$  discharge MOSFET on CSL and VTT. When OVP is disabled, the internal 16 $\Omega$  discharge MOSFETs on CSL and VTT also remain off.

$V_{CC}$  undervoltage lockout (UVLO) circuitry inhibits switching until  $V_{CC}$  reaches 4.1V (typ). When  $V_{CC}$  rises above 4.1V, the controller activates the PWM controller and initializes soft-start. When  $V_{CC}$  drops below the UVLO threshold (falling edge), the controller stops, DL is pulled low, and the internal 16 $\Omega$  discharge MOSFETs on the CSL and VTT outputs are enabled, if OVP is enabled.

## Soft-Start and Soft-Shutdown

Soft-start and soft-shutdown for the MAX17000 PWM block is voltage based. Soft-start begins when  $\overline{SHDN}$  is driven high. During soft-start, the PWM output is ramped up from 0V to the final set voltage in 1.4ms. This reduces inrush current and provides a predictable ramp-up time for power sequencing. The MAX17000 always uses skip mode during startup, regardless of the SKIP and STDBY setting. The SKIP and STDBY controls take effect after soft-start is done.

The MAX17000 VTT LDO regulator uses a current-limited soft-start function. When the VTT block is enabled, the internal source and sink current limits are linearly increased from zero to the full-scale limit in 160 $\mu$ s. Full-scale current limit is available when the VTT output is in regulation, or after 160 $\mu$ s, whichever is earlier. The VTTR reference buffer does not have any soft-start control.

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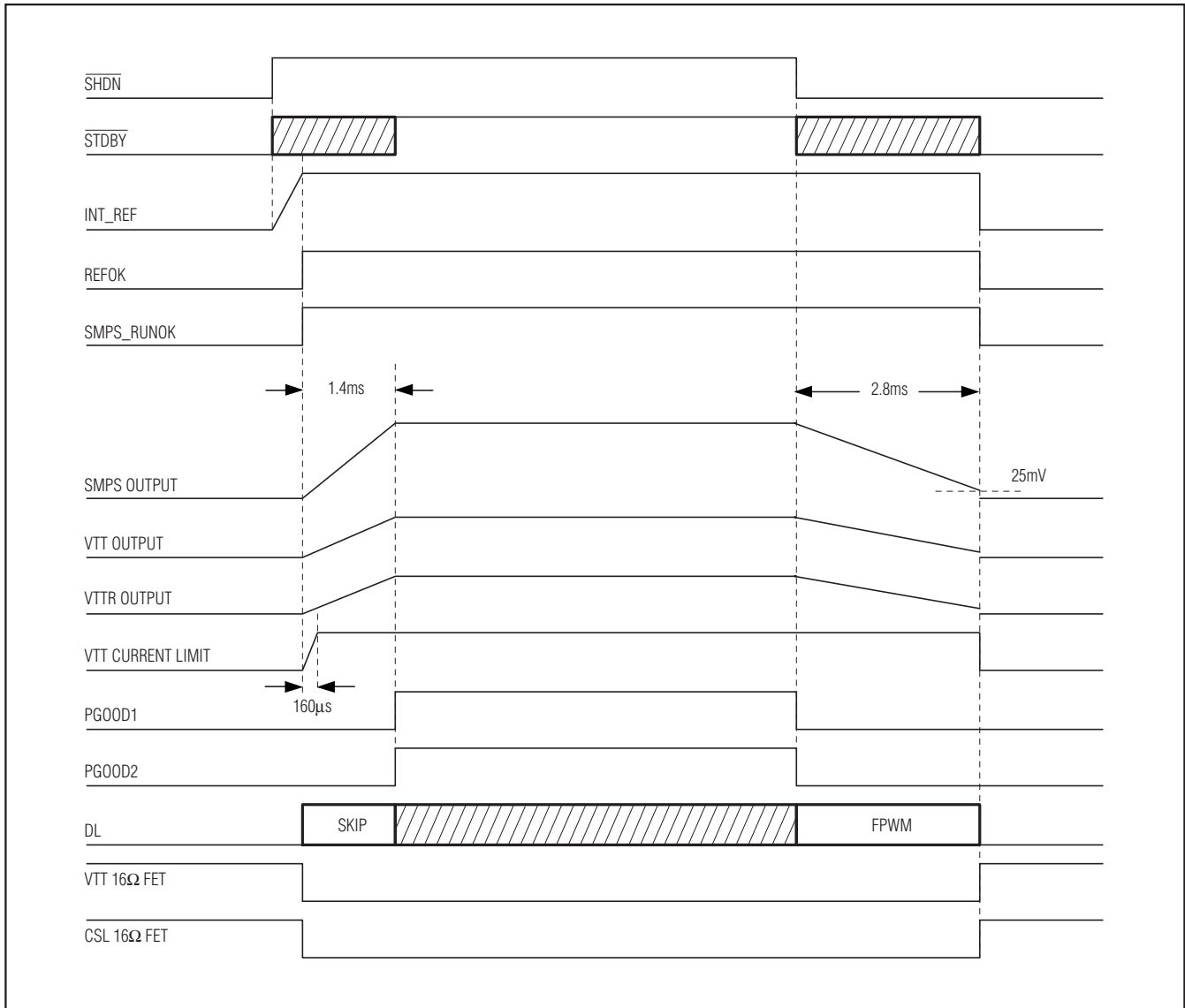


Figure 6. MAX17000 Startup/Shutdown Timing when OVP Is Enabled

Soft-shutdown begins after  $\overline{\text{SHDN}}$  goes low, an output undervoltage fault occurs, or a thermal fault occurs. A fault on the SMPS (UV fault for more than 200μs (typ)), or fault on the VTT output that persists for more than 5ms (typ), triggers shutdown of the whole IC. During soft-shutdown, the output is ramped down to 0V in 2.8ms, reducing negative inductor currents that can cause negative voltages on the output. At the end of soft-shutdown, DL is driven low.

When OVP is enabled (OVP = VCC), the internal 16Ω discharging MOSFETs on CSL and VTT are enabled until startup is triggered again by a rising edge of  $\overline{\text{SHDN}}$ . When OVP is disabled (OVP = AGND), the CSL and VTT internal 16Ω discharging MOSFETs are not enabled in shutdown.

## Output Fault Protection

The MAX17000 provides overvoltage/undervoltage fault protections for the PWM output. Drive OVP to enable and disable fault protection as shown in Table 4.

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Table 4. Fault Protection and Shutdown Setting Truth Table

OVP	MODE	REACTION/DRIVER STATE	COMMENT
OVP Disabled Discharge Disabled (OVP = Low)	Shutdown (SHDN = low)	DL immediately pulled low. VTTR tracks the SMPS output during soft-shutdown. CSL and VTT are high impedance at the end of soft-shutdown (16 discharge MOSFETs disabled).	Outputs high-impedance in shutdown.
	SMPS UVP	DL immediately pulled low. VTTR tracks the SMPS output during soft-shutdown. CSL and VTT are high impedance at the end of soft-shutdown (16 discharge MOSFETs disabled).	SMPS latched fault condition.
	SMPS OVP (disabled)	Controller remains active (normal operation). <b>Note:</b> An OVP detection still pulls PGOOD1 low.	Only PGOOD1 pulled low; fault not latched.
	VTT < -90% or VTT > +110%	PGOOD2 immediately pulled low. Soft-shutdown initiated if fault persists for more than 5ms (typ). DH not used in soft-shutdown. DL low after soft-shutdown completed. VTTR tracks the SMPS output soft-shutdown.	VTT latched fault condition if fault persists for more than 5ms (typ).
	V <sub>CC</sub> UVLO falling edge	DL and DH immediately pulled low. PGOOD1 and PGOOD2 immediately forced low. VTT and VTTR blocks immediately disabled (high impedance, no 16 discharge on outputs).	—
OVP Enabled Discharge Enabled (OVP = High)	Shutdown (SHDN = low)	Soft-shutdown initiated. DL high after soft-shutdown completed. VTTR tracks the SMPS output during soft-shutdown. Internal 16→discharge MOSFETs on CSL and VTT enabled after soft-shutdown.	16→discharge MOSFETs on CSL and VTT enabled in shutdown.
	SMPS UVP	Soft-shutdown initiated. DH not used in soft-shutdown. DL low after soft-shutdown completed. VTTR tracks the SMPS output during soft-shutdown. Internal 16→discharge MOSFETs on CSL and VTT enabled after soft-shutdown.	SMPS latched fault condition.
	SMPS OVP (enabled)	DL immediately latched high, DH forced low. PGOOD1 and PGOOD2 immediately forced low. VTT and VTTR blocks immediately shut down. Internal 16→discharge MOSFETs on CSL and VTT enabled.	SMPS latched fault condition.
	VTT < 90% or VTT > 110%	PGOOD2 immediately pulled low. Soft-shutdown initiated if fault persists for more than 5ms (typ). DH not used in soft-shutdown. DL low after soft-shutdown completed. VTTR tracks the SMPS output during soft-shutdown. Internal 16→discharge MOSFETs on CSL and VTT enabled after soft-shutdown.	VTT latched fault condition if fault persists for more than 5ms (typ).
OVP Enabled Discharge Enabled (OVP = High)	V <sub>CC</sub> UVLO falling edge	DL and DH immediately pulled low. PGOOD1 and PGOOD2 immediately forced low. VTT and VTTR blocks immediately disabled. Internal 16→discharge MOSFETs on CSL and VTT enabled immediately.	—



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**Table 4. Fault Protection and Shutdown Setting Truth Table (continued)**

OVP	MODE	REACTION/DRIVER STATE	COMMENT
General Shutdown and Fault Conditions	Thermal fault	DL and DH immediately pulled low. PGOOD1 and PGOOD2 immediately forced low. VTT and VTTR blocks immediately disabled (high impedance, no 16→discharge on outputs).	Active-fault condition.
	V <sub>CC</sub> UVLO rising edge	Activate INT_REF once V <sub>CC</sub> rises above UVLO, and $\overline{\text{SHDN}}$ = high. Once REFOK is valid (high), initiate the soft-start sequence. DL remains low until switching/soft-start begins.	—
	V <sub>CC</sub> POR rising edge	DL forced low.	—
	V <sub>CC</sub> POR falling edge	DL = Don't care. V <sub>CC</sub> less than 2VT is not sufficient to turn on the MOSFETs.	—

### SMPS Overvoltage Protection (OVP)

If the output voltage of the SMPS rises 115% above its nominal regulation voltage while OVP is enabled (OVP = V<sub>CC</sub>), the controller sets its overvoltage fault latch, pulls PGOOD1 and PGOOD2 low, and forces DL high. The VTT and VTTR block shut down immediately, and the internal 16Ω discharge MOSFETs on CSL and VTT are turned on. If the condition that caused the overvoltage persists (such as a shorted high-side MOSFET), the battery fuse blows. Cycle V<sub>CC</sub> below 1V or toggle  $\overline{\text{SHDN}}$  to clear the overvoltage fault latch and restart the controller.

OVP is disabled when OVP is connected to AGND (Table 4). PGOOD1 upper threshold remains active at 115% of nominal regulation voltage even when OVP is disabled, and the 16Ω discharge MOSFETs on CSL and VTT are not enabled in shutdown.

### SMPS Undervoltage Protection (UVP)

If the output voltage of the SMPS falls below 85% of its regulation voltage for more than 200μs (typ), the controller sets its undervoltage fault latch, pulls PGOOD1 and PGOOD2 low, and begins soft-shutdown pulsing DL. DH remains off during the soft-shutdown sequence initiated by an undervoltage fault. After soft-shutdown has completed, the MAX17000 forces DL and DH low, and enables the internal 16Ω discharge MOSFETs on CSL and VTT. Cycle V<sub>CC</sub> below 1V or toggle  $\overline{\text{SHDN}}$  to clear the undervoltage fault latch and restart the controller.

### VTT Overvoltage and Undervoltage Protection

If the output voltage of the VTT regulator exceeds ±10% of its regulation voltage for more than 5ms (typ), the controller sets its fault latch, pulls PGOOD1 and PGOOD2 low, and begins soft-shutdown pulsing DL. DH remains off during the soft-shutdown sequence initiated by an undervoltage fault. After soft-shutdown has

completed, the MAX17000 forces DL and DH low, and enables the internal 16Ω discharge MOSFETs on CSL and VTT. Cycle V<sub>CC</sub> below 1V or toggle  $\overline{\text{SHDN}}$  to clear the undervoltage fault latch and restart the controller.

### Thermal-Fault Protection

The MAX17000 features a thermal-fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD1 and PGOOD2 low, and shuts down using the shutdown sequence. Toggle  $\overline{\text{SHDN}}$  or cycle V<sub>CC</sub> power below V<sub>CC</sub> POR to reactivate the controller after the junction temperature cools by 15°C.

### Design Procedure

Firmly establish the input voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range:** The maximum value (V<sub>IN(MAX)</sub>) must accommodate the worst-case input supply voltage allowed by the notebook's AC adapter voltage. The minimum value (V<sub>IN(MIN)</sub>) must account for the lowest input voltage after drops due to connectors, fuses, and battery selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum Load Current:** There are two values to consider. The peak load current (I<sub>LOAD(MAX)</sub>) determines the instantaneous component stresses and filtering requirements, and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I<sub>LOAD</sub>) determines the thermal

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stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components. Most notebook loads generally exhibit  $I_{LOAD} = I_{LOAD(MAX)} \times 80\%$ .

- Switching Frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage, due to MOSFET switching losses that are proportional to frequency and  $V_{IN}^2$ . The optimum frequency is also a moving target, due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- Inductor Operating Point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output noise. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output noise due to increased ripple current. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values lower than this grant no further size-reduction benefit. The optimum operating point is usually found between 20% and 50% ripple current.

### Inductor Selection

The switching frequency and operating point (% ripple current or LIR) determine the inductor value as follows:

$$L = \left( \frac{V_{IN} - V_{OUT}}{f_{SW} \times I_{LOAD(MAX)} \times LIR} \right) \times \left( \frac{V_{OUT}}{V_{IN}} \right)$$

Find a low-loss inductor having the lowest possible DC resistance that fits in the allotted dimensions. Ferrite cores are often the best choice, although powdered

iron is inexpensive and can work well at 200kHz. The core must be large enough not to saturate at the peak inductor current ( $I_{PEAK}$ ):

$$I_{PEAK} = I_{LOAD(MAX)} \times \left( 1 + \frac{LIR}{2} \right)$$

### Setting the Valley Current Limit

The minimum current-limit threshold must be high enough to support the maximum load current when the current limit is at the minimum tolerance value. The valley of the inductor current occurs at  $I_{LOAD(MAX)}$  minus half the ripple current; therefore:

$$I_{LIMIT(LOW)} > I_{LOAD(MAX)} \times \left( 1 - \frac{LIR}{2} \right)$$

where  $I_{LIMIT(LOW)}$  equals the minimum current-limit threshold voltage divided by the output sense element (inductor DCR or sense resistor).

The valley current limit is fixed at 17mV (min) across the CSH to CSL differential input.

Special attention must be made to the tolerance and thermal variation of the on-resistance in the case of DCR sensing. Use the worst-case maximum value for  $R_{DCR}$  from the inductor data sheet, and add some margin for the rise in  $R_{DCR}$  with temperature. A good general rule is to allow 0.5% additional resistance for each °C of temperature rise, which must be included in the design margin unless the design includes an NTC thermistor in the DCR network to thermally compensate the current-limit threshold.

The current-sense method (Figure 7) and magnitude determine the achievable current-limit accuracy and power loss. The sense resistor can be determined by:

$$R_{SENSE} = V_{LIMIT}/I_{LIMIT}$$

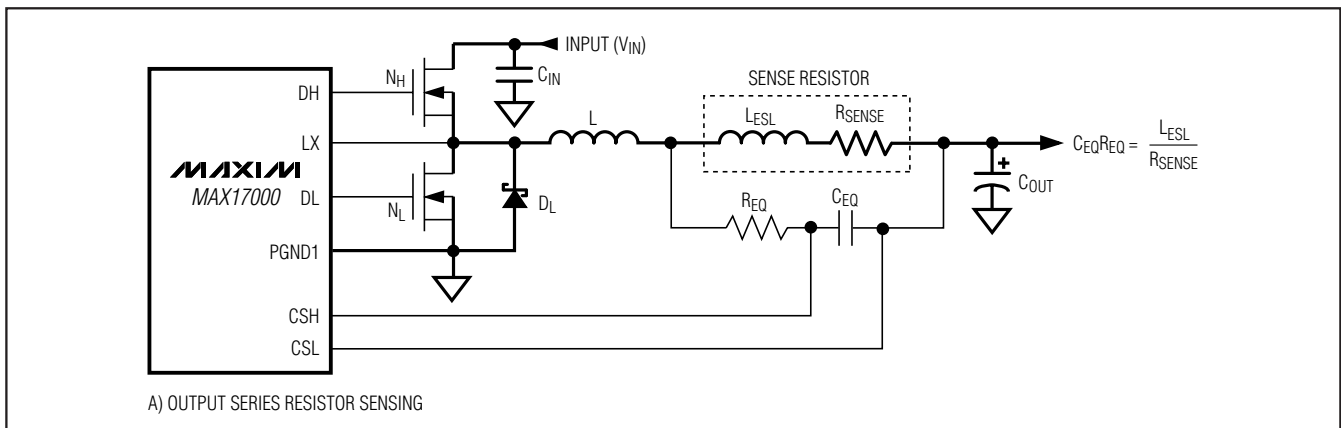


Figure 7a. Current-Sense Configurations (Sheet 1 of 2)

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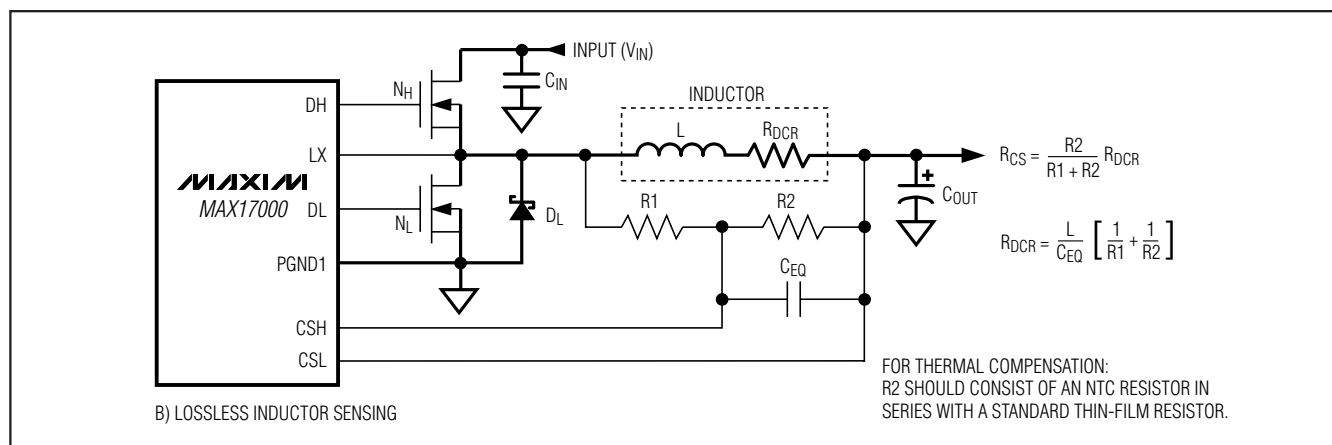


Figure 7b. Current-Sense Configurations (Sheet 2 of 2)

For the best current-sense accuracy and overcurrent protection, use a 1% tolerance current-sense resistor between the inductor and output as shown in Figure 7a. This configuration constantly monitors the inductor current, allowing accurate current-limit protection. However, the parasitic inductance of the current-sense resistor can cause current-limit inaccuracies, especially when using low-value inductors and current-sense resistors. This parasitic inductance ( $L_{ESL}$ ) can be cancelled by adding an RC circuit across the sense resistor with an equivalent time constant:

$$C_{EQ} \times R_{EQ} = \frac{L_{ESL}}{R_{SENSE}}$$

Alternatively, low-cost applications that do not require highly accurate current-limit protection could reduce the overall power dissipation by connecting a series RC circuit across the inductor (Figure 7b) with an equivalent time constant:

$$R_{CS} = \frac{R_2}{R_1 + R_2} \times R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}} \times \left[ \frac{1}{R_1} + \frac{1}{R_2} \right]$$

where  $R_{CS}$  is the required current-sense resistance, and  $R_{DCR}$  is the inductor's series DC resistance. Use the worst-case inductance and  $R_{DCR}$  values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load.

## MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large  $V_{IN} - V_{OUT}$  differential exists. The high-side gate driver (DH) sources and sinks 1.2A, and the low-side gate driver (DL) sources 1.0A and sinks 2.4A. This ensures robust gate drive for high-current applications. The DH high-side MOSFET driver is powered by an internal boost switch charge pump at BST, while the DL synchronous-rectifier driver is powered directly by the 5V bias supply ( $V_{DD}$ ).

## PWM Output Capacitor Selection

The output filter capacitor must have low enough effective series resistance (ESR) to meet output ripple and load-transient requirements, yet have high enough ESR to satisfy stability requirements.

In core and chipset converters and other applications where the output is subject to large-load transients, the output capacitor's size typically depends on how much ESR is needed to prevent the output from dipping too low under a load transient. Ignoring the sag due to finite capacitance:

$$(R_{ESR} + R_{PCB}) \leq \frac{V_{STEP}}{\Delta I_{LOAD(MAX)}}$$

In low-power applications, the output capacitor's size often depends on how much ESR is needed to maintain an acceptable level of output ripple voltage. The output ripple voltage of a step-down controller equals the total inductor ripple current multiplied by the output capacitor's ESR.