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EVALUATION KIT AVAILABLE

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

General Description

The MAX17007A/MAX17007B/MAX17008 are dual Quick-PWM™ step-down controllers intended for general power generation in battery-powered systems. The two switched-mode power supplies (SMPSs) can also be combined to operate in a two-phase single-output mode. Constant on-time Quick-PWM operation provides fast response to load transients and handles wide input/output (I/O) voltage ratios with ease, while maintaining a relatively constant switching frequency. The switching frequency can be individually adjusted between 200kHz and 600kHz with external resistors. Differential output current sensing allows output sense-resistor sensing for an accurate current limit, or lossless inductor direct-current resistance (DCR) current sensing for lower power dissipation while maintaining 0.7% output accuracy. Overvoltage (MAX17007A/MAX17007B only), undervoltage protection, and accurate user-selectable current limits (15mV, 30mV, 45mV, and 60mV) ensure robust operations.

The SMPS outputs can operate in skip mode or in ultrasonic mode for improved light-load efficiency. The ultrasonic mode eliminates audible noises by maintaining a minimum switching frequency of 25kHz in pulse-skipping mode.

The output voltage of SMPS1 can be dynamically adjusted by changing the voltage at the REFIN1 pin. The device includes a 0.5% accurate reference output that can be used to set the REFIN1 voltage. An external 5V bias supply is required to power the internal circuitry and its gate drivers.

Independent on/off controls with well-defined logic thresholds and independent open-drain power-good outputs provide flexible system configurations. To prevent current surges at startup, the internal voltage target is slowly ramped up from zero to the final target with a slew rate of 1.3mV/µs for SMPS1 at CSL1 and 0.65mV/µs for SMPS2 at FB2. To prevent the output from ringing off below ground in shutdown, the internal voltage target is ramped down from its previous value to zero with the same respective slew rates. Integrated bootstrap switches eliminate the need for external bootstrap diodes.

The MAX17007A/MAX17007B/MAX17008 are available in a space-saving, 28-pin, 4mm x 4mm, TQFN package with an exposed backside pad. The MAX17007B improves crosstalk performance over the MAX17007A.

Applications

Notebook Computers	GPU Core Supplies
Low-Power I/O Supplies	2 to 4 Li+ Cells Battery-Powered Devices

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Features

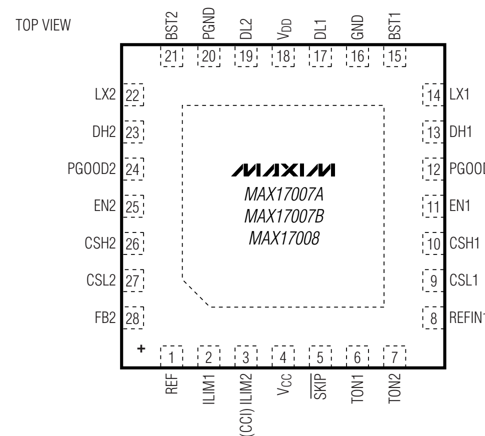
- ♦ **Dual Quick-PWM with Fast Transient Response**
- ♦ **Automatic Dynamic REFIN1 Detection and PGOOD1/Fault Blanking**
- ♦ **Fixed and Adjustable Output Voltages**
  - **±0.7% Output Accuracy Over Line and Load**
  - **OUT1: 0 to 2V Dynamic Output or Preset 1.05V**
  - **OUT2: 0.7V to 2V Range or Preset 1.5V**
- ♦ **Resistor-Programmable Switching Frequency**
- ♦ **Integrated BST Switches**
- ♦ **Differential Current-Sense Inputs**
  - **Low-Cost DCR Sensing or Accurate Current-Sense Resistors**
  - **Internally Coupled Current-Sense Compensation**
- ♦ **Combinable Mode Supports High-Current Dynamic Output Voltages**
- ♦ **Selectable Forced-PWM, Pulse Skip, or Ultrasonic Mode Operation**
- ♦ **26V Maximum Input Voltage Rating**
- ♦ **Independent Enable Inputs**
- ♦ **Independent Power-Good Outputs**
- ♦ **Overvoltage Protection (MAX17007A/MAX17007B Only)**
- ♦ **Undervoltage/Thermal Protection**
- ♦ **Voltage Soft-Start and Soft-Shutdown**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17007AGTI+	-40°C to +105°C	28 TQFN-EP*
MAX17007BGTI+	-40°C to +105°C	28 TQFN-EP*
MAX17008GTI+	-40°C to +105°C	28 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Pin Configuration



THIN QFN
(4mm x 4mm)

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

ABSOLUTE MAXIMUM RATINGS

BST1, BST2 to GND ....-0.3V to +34V
BST1, BST2 to V_{DD} ....-0.3V to +28V
TON1, TON2 to GND ....-0.3V to +28V
V_{DD} to GND ....-0.3V to +6V
V_{DD} to V_{CC} ....-0.3V to +0.3V
LX1 to BST1 ....-6V to +0.3V
LX2 to BST2 ....-6V to +0.3V
DH1 to LX1 ....-0.3V to (V_{BST1} + 0.3V)
DH2 to LX2 ....-0.3V to (V_{BST2} + 0.3V)
ILIM1, ILIM2, REF to GND ....-0.3V to (V_{CC} + 0.3V)
CSH1, CSH2, CSL1, CSL2, FB2, REFIN1 to GND....-0.3V to +6V
EN1, EN2, $\overline{SKIP}$, PGOOD1, PGOOD2 to GND.........-0.3V to +6V
DL1 to GND ....-0.3V to (V_{DD} + 0.3V)
DL2 to PGND ....-0.3V to (V_{DD} + 0.3V)
PGND to GND ....-0.3V to + 0.3V
REF Short Circuit to GND ....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin TQFN T2844-1
(derate 20.8mW/°C above +70°C) 1667mW
Extended Operating Temperature Range ....-40°C to +105°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN1} = V_{EN2} = 5V, V_{REFIN1} = 2V, $\overline{SKIP}$ = GND, **T_A = 0 to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range	V_{IN}			4.5		26	V
Quiescent Supply Current (V_{DD}, V_{CC})	I_{DD} + I_{CC}	Output forced above regulation voltage, V_{EN1} = V_{EN2} = 5V			1.7	2.5	mA
Shutdown Supply Current (V_{DD}, V_{CC})	I_{SHDN}	EN1 = EN2 = GND, T_A = +25°C			0.1	5	µA
On-Time (Note 1)	t_{ON1}, t_{ON2}	V_{IN} = 12V, V_{CSL1} = V_{CSL2} = V_{CCI} = 1.2V, separate or combined mode	R_{TON1} = R_{TON2} = 97.5kΩ (600kHz)	142 (-15%)	174	194 (+15%)	ns
			R_{TON1} = R_{TON2} = 200kΩ (300kHz)	305 (-10%)	336	368 (+10%)	
			R_{TON1} = R_{TON2} = 302.5kΩ (200kHz)	425 (-15%)	500	575 (+15%)	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 1)			250	400	ns
TON1, TON2, Shutdown Supply Current	I_{TON1}, I_{TON2}	EN1 = EN2 = GND, V_{TON1} = V_{TON2} = 26V, V_{DD} = 0 or 5V, T_A = +25°C			0.01	1	µA
REFIN1 Voltage Range	V_{REFIN1}	(Note 2)		0		V_{REF}	V
FB2 Regulation Voltage	V_{FB2}	Adjustable mode			0.7		V
FB2 Input Voltage Range		Preset mode		1.7		2.3	V
FB2 Combined-Mode Threshold		Combined mode		3.8	V_{CC} - 1V	V_{CC} - 0.4	V
REFIN1 Dual Mode™ Switchover Threshold				3.8	V_{CC} - 1V	V_{CC} - 0.4	V
REFIN1, FB2 Bias Current	I_{REFIN1}, I_{FB2}	REFIN1 = 0.5V to 2V; V_{FB2} = 0.7V, T_A = +25°C		-0.1		+0.1	µA
SMPS1 Voltage Accuracy	V_{CSL1}	Measured at CSL1, REFIN1 = V_{CC}, V_{IN} = 2V to 26V, $\overline{SKIP}$ = V_{CC} (Note 2)		1.043	1.05	1.057	V
	V_{CSL1} - V_{REFIN1}	REFIN1 = 500mV, $\overline{SKIP}$ = V_{CC}	T_A = +25°C	-12		+12	mV
			T_A = 0°C to +85°C	-20		+20	
		REFIN1 = 2V, $\overline{SKIP}$ = V_{CC}		-20		+20	

Dual Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN1} = V_{EN2} = 5V, V_{REFIN1} = 2V, $\overline{SKIP}$ = GND, **T_A = 0 to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMPS2 Voltage Accuracy	V_{CSL2}	Measured at CSL2, FB2 = REF, V_{IN} = 2V to 26V, $\overline{SKIP}$ = V_{CC}	1.489	1.5	1.511	V
Load Regulation Error		I_{LOAD} = 0 to full load, $\overline{SKIP}$ = V_{CC} (Note 3)		0.1		%
Line Regulation Error		V_{DD} = 4.5V to 5.5V, V_{IN} = 4.5V to 26V (Note 3)		0.25		%
CSL1 Soft-Start/-Stop Slew Rate	SR_{SS1}	Rising/falling edge on EN1		1.25		mV/µs
FB2 Soft-Start/-Stop Slew Rate	SR_{SS2}	Rising/falling edge on EN2		0.63		mV/µs
Dynamic REFIN1 Slew Rate	SR_{DYN}	Rising edge on REFIN1		11.4		mV/µs
INTERNAL REFERENCE						
Reference Voltage	V_{REF}	V_{DD} = 4.5V to 5.5V	1.990	2.000	2.010	V
Reference Lockout Voltage	$V_{REF(UVLO)}$	Rising edge, hysteresis = 230mV		1.8		V
Reference Load Regulation		I_{REF} = -10µA to +100µA	1.980		2.015	mV
FAULT DETECTION						
SMPS1 Overvoltage Trip Threshold and PGOOD1 Upper Threshold (MAX17007A Only)	V_{OVP1}, V_{PG1_H}	With respect to the internal target voltage (error comparator threshold); rising edge; hysteresis = 50mV	260	300	340	mV
		Dynamic transition		V_{REF} + 0.30		V
		Minimum OVP threshold		0.7		V
SMPS2 Adjustable Mode Overvoltage Trip Threshold and PGOOD2 Upper Threshold (MAX17007A Only)	V_{OVP2}, V_{PG2_H}	With respect to the internal target voltage 0.7V (error comparator threshold); hysteresis = 50mV	120	150	180	mV
Output Overvoltage Fault Propagation Delay (MAX17007A Only)	t_{OVP}	CSL1/FB2 forced 25mV above trip threshold		5		µs
SMPS1 Undervoltage Protection Trip Threshold and Lower PGOOD1 Threshold	V_{UVP1}, V_{PG1_L}	With respect to the internal target voltage (error comparator threshold); falling edge; hysteresis = 50mV	-240	-200	-160	mV
SMPS2 Undervoltage Protection Trip Threshold and Lower PGOOD2 Threshold	V_{UVP2}, V_{PG2_L}	With respect to the internal target voltage 0.7V (error comparator threshold); falling edge; hysteresis = 50mV	-130	-100	-70	mV
Output Undervoltage Fault Propagation Delay	t_{UVP}	CSL1/FB2 forced 25mV below trip threshold	90	205	360	µs
PGOOD_ Propagation Delay	t_{PGOOD}	UVP falling edge, 25mV overdrive		5		µs
		OVP rising edge, 25mV overdrive		5		µs
		Startup delay from regulation	90	205	360	µs
PGOOD_ Output Low Voltage		I_{SINK} = 3mA			0.4	V
PGOOD_ Leakage Current	I_{PGOOD}	CSL1 = REFIN1, FB2 = 0.7V (PGOOD_ high impedance), PGOOD_ forced to 5V, T_A = +25°C			1	µA
Dynamic REFIN1 Transition Fault-Blanking Threshold		Fault blanking initiated; REFIN1 deviation from the internal target voltage (error comparator threshold); hysteresis = 10mV		±50		mV
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C (Note 3)		160		°C
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, PWM disabled below this level, hysteresis = 100mV	3.95	4.20	4.45	V

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN1} = V_{EN2} = 5V, V_{REFIN1} = 2V, $\overline{SKIP}$ = GND, **T_A = 0 to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT LIMIT							
Current-Sense Input Range		CSH1, CSH2		0		2.3	V
		CSL1, CSL2		0		2.3	
Current-Sense Input (CSH_) Leakage Current		CSH_ = GND or V_{CC}, T_A = +25°C		-0.2		+0.2	µA
Current-Sense Input (CSL_) Leakage Current		CSL_= CSL_ = 2V, T_A = +25°C				1	µA
Current-Limit Threshold (Fixed)	$V_{CSLIMIT}$	$V_{CSH\_}$ - $V_{CSL\_}$ ILIM1 = ILIM2 = REF	T_A = +25°C	28	30	32	mV
			T_A = 0°C to +85°C	27	30	33	
		$V_{CSH\_}$ - $V_{CSL\_}$, ILIM1 = ILIM2 = V_{CC}		56	60	64	
		$V_{CSH\_}$ - $V_{CSL\_}$, ILIM1 = ILIM2 = OPEN		42	45	48	
		$V_{CSH\_}$ - $V_{CSL\_}$, ILIM1 = ILIM2 = GND		13	15	17	
Current-Limit Threshold (Negative)	V_{NEG}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{SKIP}$ = V_{CC}			-1.2 x $V_{CSLIMIT}$		mV
Current-Limit Threshold (Zero Crossing)	V_{ZX}	$V_{CSH\_}$ - $V_{CSL\_}$, $\overline{SKIP}$ = GND or OPEN; ILIM1 = ILIM2 = REF			1		mV
Ultrasonic Frequency		$\overline{SKIP}$ = open (3.3V); V_{CSL1} = V_{REFIN1} + 50mV; V_{CSL2} = V_{FB2} + 50mV		20			kHz
Ultrasonic Current-Limit Threshold		$\overline{SKIP}$ = open (3.3V)	V_{CSL1} = V_{REF1} + 50mV	22	33	46	mV
			V_{CSL2} = V_{FB2}+ 50mV	18	30	46	
Current-Balance Amplifier (GMI) Offset		[V(CSH1,CSL1) - V(CSH2,CSL2)] at I_{CCI} = 0		-3		+3	mV
Current-Balance Amplifier (GMI) Transconductance		$\Delta I_{CCI}/\Delta$[V(CSH1,CSL1) - V(CSH2,CSL2)]; V_{CCI} = V_{CSL1} = V_{CSL2} = 0.5V to 2V, and V(CSH_,CSL_) = -60.0mV to +60.0mV, ILIM1 = GND			180		µS
GATE DRIVERS							
DH1, DH2 Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V	Low state (pulldown)		1.7	4.0	Ω
			High state (pullup)		1.7	4.0	
DL1, DL2 Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			1.3	3.0	Ω
		Low state (pulldown)			0.6	2.5	
DH1, DH2 Gate-Driver Source/Sink Current	I_{DH}	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			1.2		A
DL1, DL2 Gate-Driver Source Current	$I_{DL(SOURCE)}$	DL_ forced to 2.5V			1		A
DL1, DL2 Gate-Driver Sink Current	$I_{DL(SINK)}$	DL_ forced to 2.5V			2.4		A
Driver Propagation Delay		DH_ low to DL high		10	25	40	ns
		DL_ low to DH high		15	30	45	

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN1} = V_{EN2} = 5V, V_{REFIN1} = 2V, $\overline{SKIP}$ = GND, **T_A = 0 to +85°C,** unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DL_ Transition Time		DL_ falling, C_{DL} = 3nF		10	20		ns
		DL_ rising, C_{DL} = 3nF		10	20		
DH_ Transition Time		DH_ falling, C_{DH} = 3nF		10	20		ns
		DH_ rising, C_{DH} = 3nF		10	20		
Internal BST_ Switch On-Resistance	$R_{BST\_}$	$I_{BST\_}$ = 10mA, V_{DD} = 5V			6.5	11.0	Ω
INPUTS AND OUTPUTS							
EN1, EN2 Logic-Input Threshold		EN1, EN2 rising edge, hysteresis = 300mV/600mV (min/max)		1.20	1.70	2.20	V
Logic-Input Current		EN1, EN2, T_A = +25°C		-0.5		+0.5	µA
Quad-Level Input-Logic Levels		$\overline{SKIP}$, ILIM1, ILIM2	High (5V)	V_{CC} - 0.3			V
			Open (3.3V)	3.0		3.6	
			Ref (2.0V)	1.7		2.3	
			Low (GND)			0.4	
Quad-Level Logic-Input Current		$\overline{SKIP}$, ILIM1, ILIM2 forced to GND or V_{CC}, T_A = +25°C		-2		+2	µA

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN1} = V_{EN2} = 5V, V_{REFIN1} = 2V, $\overline{SKIP}$ = GND, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER						
Input Voltage Range	V_{IN}			4.5	26	V
Quiescent Supply Current (V_{DD}, V_{CC})	I_{DD} + I_{CC}	Output forced above regulation voltage, V_{EN1} = V_{EN2} = 5V			2.5	mA
On-Time (Note 1)	t_{ON1}, t_{ON2}	V_{IN} = 12V, V_{CSL1} = V_{CSL2} = V_{CCI} = 1.2V, separate or combined mode	R_{TON1} = R_{TON2} = 97.5kΩ (600kHz)	142	194	ns
			R_{TON1} = R_{TON2} = 200kΩ (300kHz)	305	368	
			R_{TON1} = R_{TON2} = 302.5kΩ (200kHz)	425	575	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 1)			400	ns
REFIN1 Voltage Range	V_{REFIN1}			0	V_{REF}	V
FB2 Input Voltage Range		Preset mode		1.7	2.3	V
FB2 Combined-Mode Threshold		Combined mode		3.75	V_{CC} - 0.4	V
REFIN1, FB2 Bias Current	I_{REFIN1}, I_{FB2}			-0.1	+0.1	µA

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN1} = V_{EN2} = 5V, V_{REFIN1} = 2V, $\overline{SKIP}$ = GND, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
REFIN1 Dual-Mode Switchover Threshold				3.75	V_{CC} - 0.4	V
SMPS1 Voltage Accuracy	V_{CSL1}	Measured at CSL1, REFIN1 = V_{CC}; V_{IN} = 2V to 26V, $\overline{SKIP}$ = V_{CC} (Note 2)		1.039	1.061	V
SMPS2 Voltage Accuracy	V_{CSL2}	Measured at CSL2, FB2 = REF; V_{IN} = 2V to 26V, $\overline{SKIP}$ = V_{CC} (Note 2)		1.485	1.515	V
INTERNAL REFERENCE						
Reference Voltage	V_{REF}	V_{DD} = 4.5V to 5.5V		1.985	2.015	V
FAULT DETECTION						
SMPS1 Overvoltage Trip Threshold and PGOOD1 Upper Threshold (MAX17007A Only)	V_{OVP1}, V_{PG1_H}	With respect to the internal target voltage (error comparator threshold); rising edge; hysteresis = 50mV		260	340	mV
SMPS2 Overvoltage Trip Threshold and PGOOD2 Upper Threshold (MAX17007A Only)	V_{OVP2}, V_{PG2_H}	With respect to the internal target voltage 0.7V (error comparator threshold); hysteresis = 50mV		120	180	mV
SMPS1 Undervoltage Protection Trip Threshold and Lower PGOOD1 Threshold	V_{UVP1}, V_{PG1_L}	With respect to the internal target voltage (error comparator threshold) falling edge; hysteresis = 50mV		-240	-160	mV
SMPS2 Undervoltage Protection Trip Threshold and Lower PGOOD2 Threshold	V_{UVP2}, V_{PG2_L}	With respect to the internal target voltage 0.7V (error comparator threshold) falling edge; hysteresis = 50mV		-130	-70	mV
Output Undervoltage Fault Propagation Delay	t_{UVP}	REFIN1/FB2 forced 25mV below trip threshold		90	360	µs
PGOOD_ Propagation Delay	t_{PGOOD}	Startup delay from regulation		90	360	µs
PGOOD_ Output Low Voltage		I_{SINK} = 3mA			0.4	V
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, PWM disabled below this level; hysteresis = 100mV		3.8	4.45	V
CURRENT LIMIT						
Current-Sense Input Range		CSH1, CSH2		0	2.3	V
		CSL1, CSL2		0	2.3	
Current-Limit Threshold (Fixed)	$V_{CSLIMIT}$	$V_{CSH\_}$ - $V_{CSL\_}$, ILIM1 = ILIM2 = REF		27	33	mV
Ultrasonic Frequency		$\overline{SKIP}$ = OPEN (3.3V); V_{CSL1} = V_{REFIN1} + 50mV; V_{CSL2} = V_{FB2} + 50mV		18		kHz
Ultrasonic Current-Limit Threshold		$\overline{SKIP}$ = OPEN (3.3V)	V_{CSL1} = V_{REF1} + 50mV	22	46	mV
			V_{CSL2} = V_{FB2} + 50mV	18	46	
Current-Balance Amplifier (GMI) Offset		[V(CSH1,CSL1) - V(CSH2,CSL2)] at I_{CCI} = 0		-3	+3	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{DD} = V_{CC} = V_{EN1} = V_{EN2} = 5V, V_{REFIN1} = 2V, $\overline{SKIP}$ = GND, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
GATE DRIVERS						
DH1, DH2 Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V	Low state (pulldown)		4.5	Ω
			High state (pullup)		4.0	
DL1, DL2 Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			3	Ω
		Low state (pulldown)			2.5	
Driver Propagation Delay		DH_ low to DL high		8	42	ns
		DL_ low to DH high		12	48	
Internal BST_ Switch On-Resistance	$R_{BST\_}$	$I_{BST\_}$ = 10mA, V_{DD} = 5V			12	Ω
INPUTS AND OUTPUTS						
EN1, EN2 Logic-Input Threshold		EN1, EN2 rising edge; hysteresis = 300mV/600mV (min/max)		1.20	2.20	V
Quad-Level Input Logic Levels		$\overline{SKIP}$, ILIM1, ILIM2	High (5V)	V_{CC} - 0.3		V
			Open (3.3V)	3.0	3.6	
			Ref (2.0V)	1.7	2.3	
			Low (GND)		0.4	

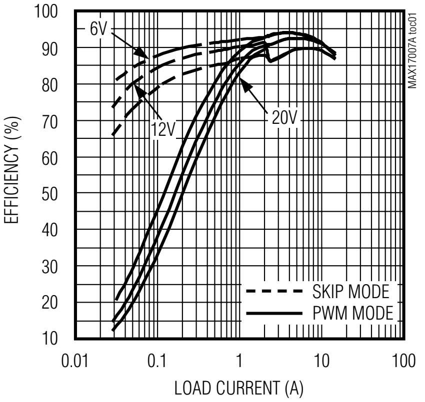
Note 1: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = GND, V_{BST} = 5V, and a 250pF capacitor connected from DH to LX. Actual in-circuit times might differ due to MOSFET switching speeds.
Note 2: The 0 to 0.5V range is guaranteed by design, not production tested.
Note 3: Not production tested.
Note 4: Specifications at T_A = -40°C to +105°C are guaranteed by design, not production tested.

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

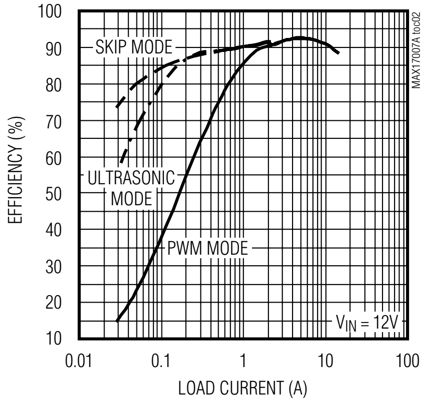
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, $\overline{SKIP}$ = GND, T_A = +25°C, unless otherwise noted.)

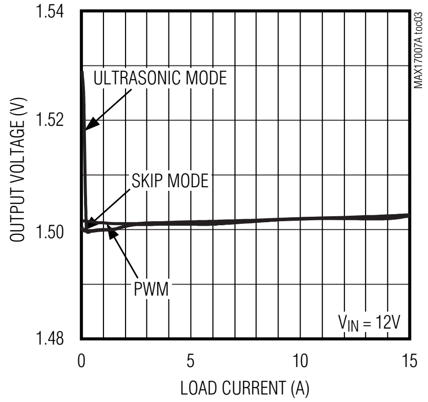
SMPS2 1.5V EFFICIENCY vs. LOAD CURRENT



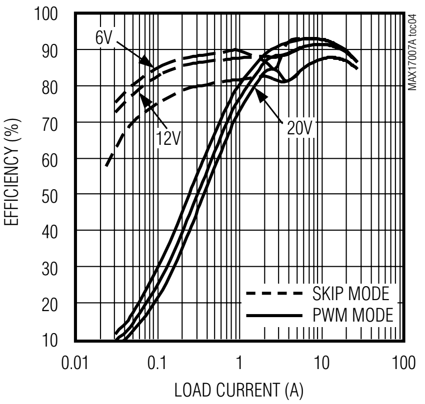
SMPS2 1.5V EFFICIENCY vs. LOAD CURRENT



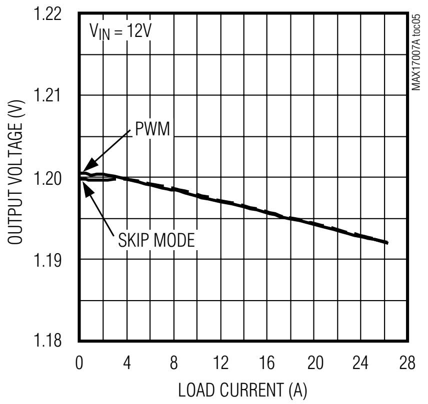
SMPS2 1.5V OUTPUT VOLTAGE vs. LOAD CURRENT



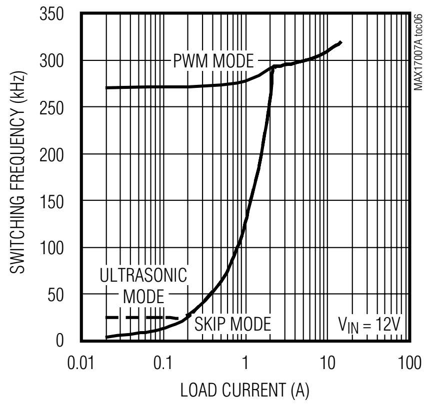
COMBINED 1.2V EFFICIENCY vs. LOAD CURRENT



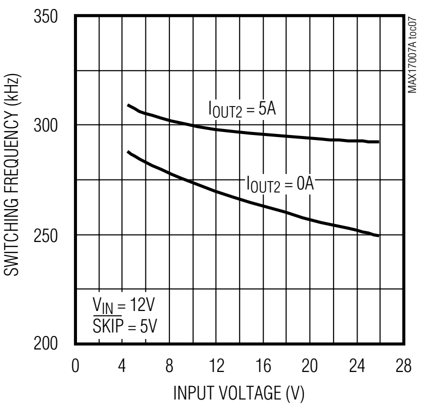
COMBINED 1.2V OUTPUT VOLTAGE vs. LOAD CURRENT



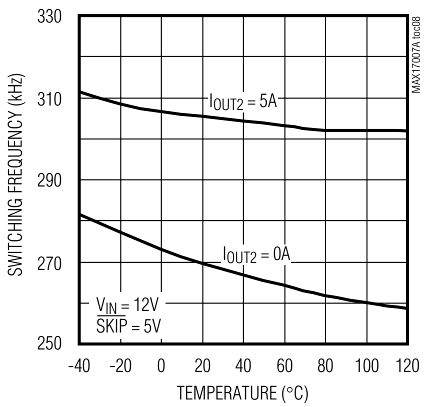
SMPS2 SWITCHING FREQUENCY vs. LOAD CURRENT



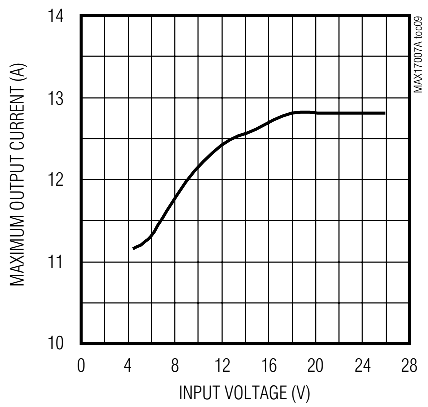
SMPS2 SWITCHING FREQUENCY vs. INPUT VOLTAGE



SMPS2 SWITCHING FREQUENCY vs. TEMPERATURE



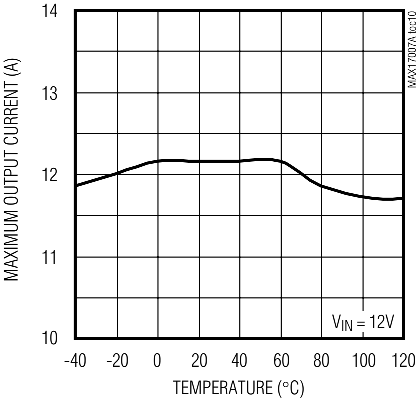
SMPS2 MAXIMUM OUTPUT CURRENT vs. INPUT VOLTAGE



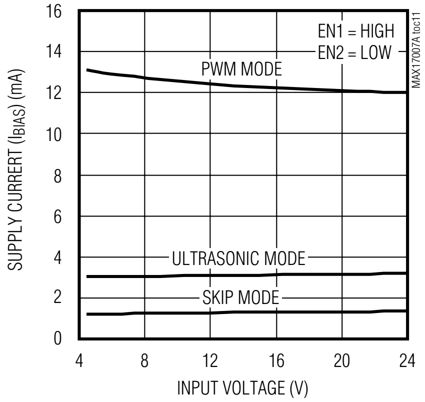
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, $\overline{SKIP}$ = GND, T_A = +25°C, unless otherwise noted.)

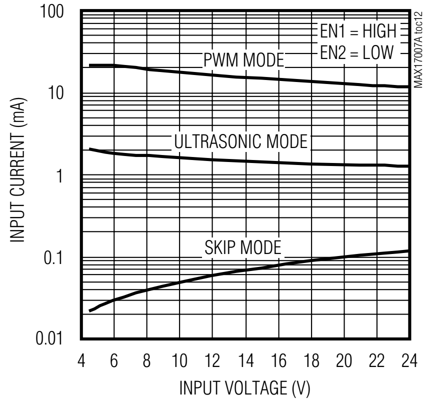
SMPS2 MAXIMUM OUTPUT CURRENT vs. TEMPERATURE



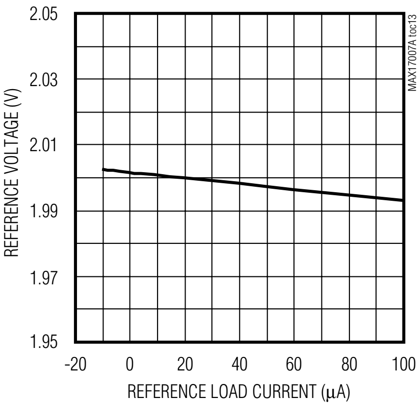
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



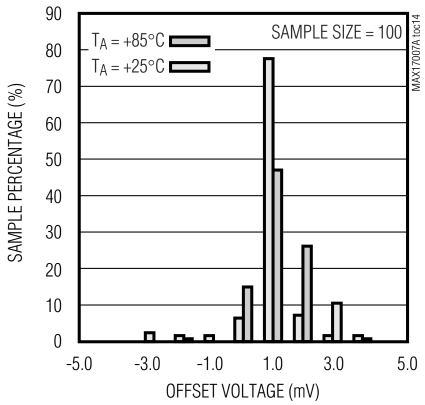
NO-LOAD INPUT CURRENT vs. INPUT VOLTAGE



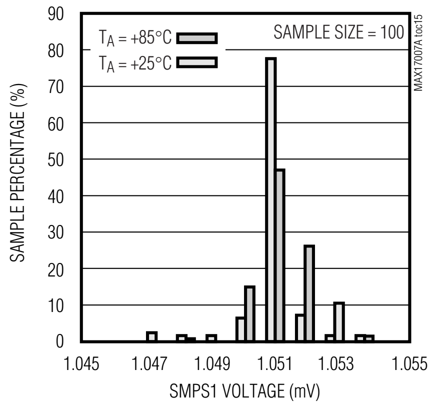
REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT



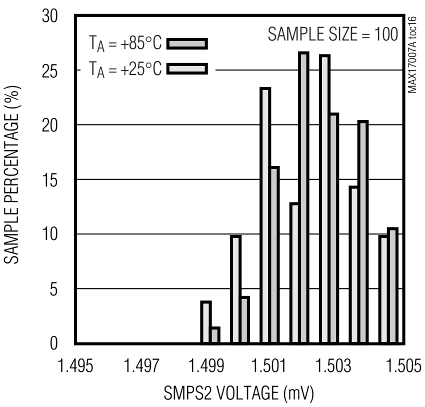
REFIN1 TO CSL1 OFFSET VOLTAGE DISTRIBUTION



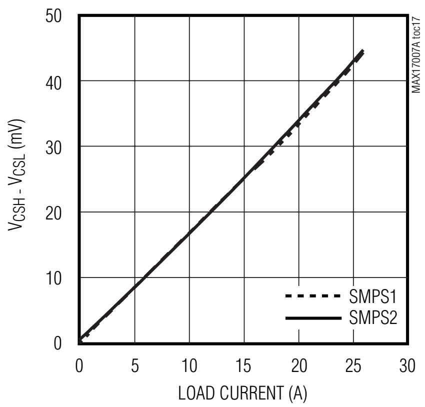
SMPS1 PRESET 1.05V VOLTAGE DISTRIBUTION



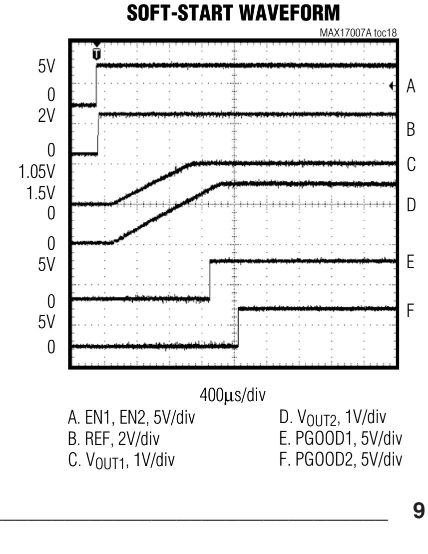
SMPS2 PRESET 1.5V VOLTAGE DISTRIBUTION



COMBINED-MODE CURRENT BALANCE vs. LOAD CURRENT



SOFT-START WAVEFORM

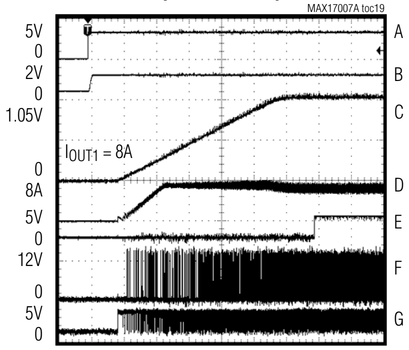


Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

Typical Operating Characteristics (continued)

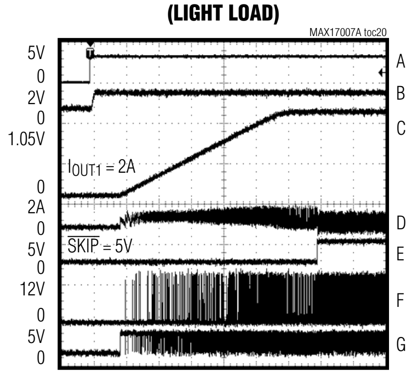
(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, $\overline{SKIP}$ = GND, T_A = +25°C, unless otherwise noted.)

SMPS1 STARTUP WAVEFORM (HEAVY LOAD)



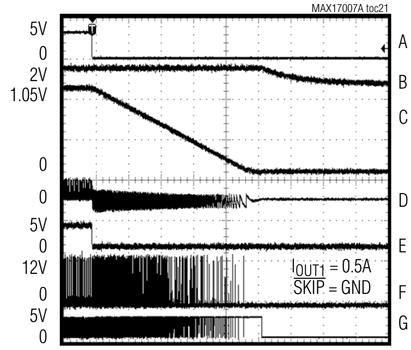
200µs/div
A. EN1, 5V/div
B. REF, 2V/div
C. V_{OUT1}, 500mV/div
D. I_{LX1}, 10A/div
E. PGOOD1, 10V/div
F. LX1, 10V/div
G. DL1, 10V/div

SMPS1 STARTUP WAVEFORM (LIGHT LOAD)



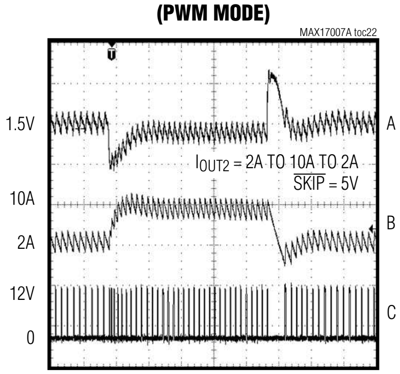
200µs/div
A. EN1, 5V/div
B. REF, 2V/div
C. V_{OUT1}, 500mV/div
D. I_{LX1}, 5A/div
E. PGOOD1, 10V/div
F. LX1, 10V/div
G. DL1, 10V/div

SMPS1 SHUTDOWN WAVEFORM



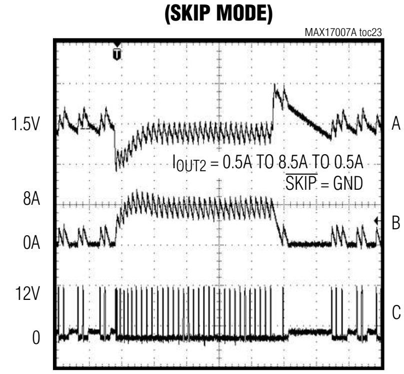
200µs/div
A. EN1, 5V/div
B. REF, 5V/div
C. V_{OUT1}, 500mV/div
D. I_{LX1}, 5A/div
E. PGOOD1, 10V/div
F. LX1, 10V/div
G. DL1, 10V/div

SMPS2 LOAD-TRANSIENT RESPONSE (PWM MODE)



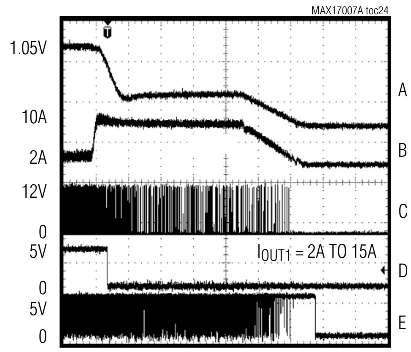
20µs/div
A. V_{OUT2}, 50mV/div
B. I_{LX2}, 10A/div
C. LX2, 10V/div

SMPS2 LOAD-TRANSIENT RESPONSE (SKIP MODE)



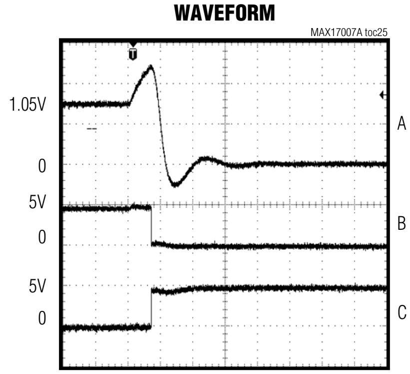
20µs/div
A. V_{OUT2}, 50mV/div
B. I_{LX2}, 10A/div
C. LX2, 10V/div

SMPS1 OUTPUT OVERLOAD WAVEFORM



200µs/div
A. V_{OUT1}, 500mV/div
B. I_{LX1}, 10A/div
C. LX1, 10V/div
D. PGOOD1, 5V/div
E. DL1, 5V/div

SMPS1 OUTPUT OVERVOLTAGE WAVEFORM

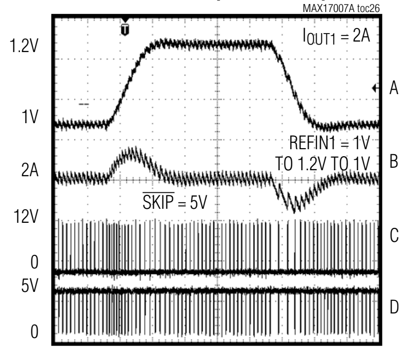


40µs/div
A. V_{OUT1}, 1V/div
B. PGOOD1, 5V/div
C. DL1, 5V/div

Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = 5V, $\overline{SKIP}$ = GND, T_A = +25°C, unless otherwise noted.)

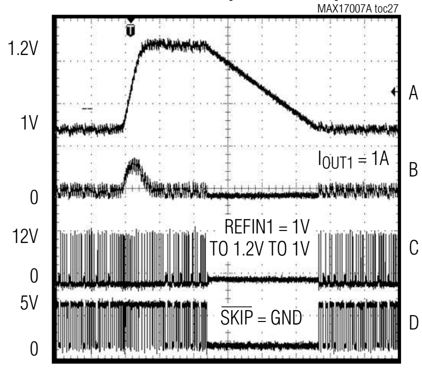
DYNAMIC OUTPUT VOLTAGE TRANSITION (PWM MODE)



20µs/div

A. V_{OUT1}, 100mV/div C. LX1, 10V/div
B. I_{LX1}, 10A/div D. DL1, 5V/div

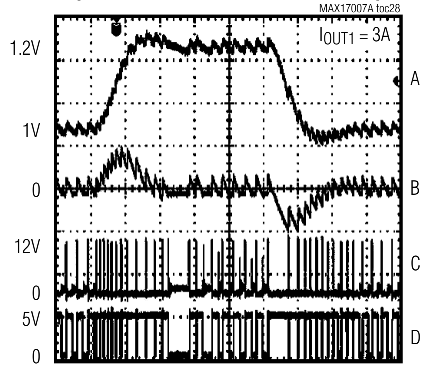
DYNAMIC OUTPUT VOLTAGE TRANSITION (SKIP MODE)



40µs/div

A. V_{OUT1}, 100mV/div C. LX1, 10V/div
B. I_{LX1}, 10A/div D. DL1, 5V/div

DYNAMIC OUTPUT-VOLTAGE TRANSITION (SKIP MODE-FORCED TRANSITION)



20µs/div

A. V_{OUT1}, 100mV/div C. LX1, 10V/div
B. I_{LX2}, 10A/div D. DL1, 5V/div
I_{OUT1} = 1A
REFIN1 = 1V TO 1.2V TO 1V
$\overline{SKIP}$ = REF

Pin Description

PIN	NAME	FUNCTION
1	REF	2V Reference Voltage Output. Bypass REF to GND with a 2.2nF ceramic capacitor. The reference can source up to 100µA. Loading REF degrades output-voltage accuracy according to the REF load regulation error (see the *Typical Operating Characteristics*). The reference shuts down when both EN1 and EN2 are low.
2	ILIM1	This four-level input determines the CSH1 to CSL1 current limit for SMPS1: V_{CC} (5V) = 60mV current limit Open (3.3V) = 45mV current limit REF (2V) = 30mV current limit GND = 15mV current limit In combined mode, ILIM1 sets the current-limit threshold for both sides.
3	ILIM2 (CCI)	This four-level input determines the CSH2 to CSL2 current limit for SMPS2: V_{CC} (5V) = 60mV current limit Open (3.3V) = 45mV current limit REF (2V) = 30mV current limit GND = 15mV current limit In combined mode, ILIM2 is the current balance integrator (CCI) output pin. Connect a capacitor (C_{CCI}) between CCI and the output. The CCI capacitor value depends on the ILIM1 setting based on the following table: **ILIM1** — **C_{CCI} at ILIM2 (pF)** V_{CC} (5V) — 120 Open (3.3V) — 180 REF (2V) — 220 GND — 470
4	V_{CC}	5V Analog Supply Input. Bypass V_{CC} from V_{DD} using a 10Ω resistor, and to analog ground using a 1µF ceramic capacitor.

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers

Pin Description (continued)

PIN	NAME	FUNCTION
5	$\overline{SKIP}$	Pulse-Skipping Control Input. This four-level input determines the mode of operation under normal steady-state conditions and dynamic output-voltage transitions: V_{DD} (5V) = Forced-PWM operation Open (3.3V) = Ultrasonic mode (without forced-PWM during transitions) REF (2V) = Pulse-skipping mode (with forced-PWM during transitions) GND = Pulse-skipping mode (without forced-PWM during transitions) There are no dynamic transitions for SMPS2, so $\overline{SKIP}$ = 2V and $\overline{SKIP}$ = GND have the same pulse-skipping behavior for SMPS2 without any forced-PWM transitions. In combined mode, the ultrasonic mode is disabled, and the $\overline{SKIP}$ = open (3.3V) setting is identical to the $\overline{SKIP}$ = GND setting.
6	TON1	Frequency-Setting Input for SMPS1. An external resistor between the input power source and TON1 sets the switching period (T_{SW1}) of SMPS1: $T_{SW1} = C_{TON} (R_{TON1} + 6.5k\Omega)$ where C_{TON} = 16.26pF. TON1 is high impedance in shutdown. In combined mode, TON1 sets the switching period for both SMPS1 and SMPS2.
7	TON2	Frequency-Setting Input for SMPS2. An external resistor between the input power source and TON2 sets the switching period (T_{SW2}) of SMPS2: $T_{SW2} = C_{TON} (R_{TON2} + 6.5k\Omega)$ where C_{TON} = 16.26pF. Set TON2 to a switching frequency different from TON1. A 10% to 30% difference in switching frequency between SMPS1 and SMPS2 is recommended. TON2 is high impedance in shutdown. In combined mode, TON2 may be left open.
8	REFIN1	External Reference Input for SMPS1. REFIN1 sets the feedback regulation voltage of CSL1. SMPS1 includes an internal window comparator to detect REFIN1 voltage changes that are greater than ±50mV (typ), allowing the controller to blank PGOOD1 and the fault protection, and force the output transition, if enabled. When REFIN1 is tied to V_{CC}, SMPS1 regulates the output to 1.05V. In combined mode, REFIN1 sets the feedback regulation voltage of the combined output.
9	CSL1	Output-Sense and Negative Current-Sense Input for SMPS1. When using the internal preset 1.05V feedback divider (REFIN1 = V_{CC}), the controller uses CSL1 to sense the output voltage. Connect to the negative terminal of the current-sense element. Figure 14 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
10	CSH1	Positive Current-Sense Input for SMPS1. Connect to the positive terminal of the current-sense element. Figure 14 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
11	EN1	Enable Control Input for SMPS1. Connect to V_{CC} for normal operation. Pull EN1 low to disable SMPS1. The controller slowly ramps down the output voltage to ground and after the target voltage reaches 0.1V, the controller forces DL1 low. When both EN1 and EN2 are low, the device enters the low-power shutdown state. In combined mode, EN1 controls the combined SMPS output. EN2 is unused and must be grounded.
12	PGOOD1	Open-Drain Power-Good Output for SMPS1. PGOOD1 is low when the SMPS1 voltage is more than 200mV below or 300mV above the target voltage, during soft-start, and in shutdown. After the SMPS1 soft-start circuit has terminated, PGOOD1 becomes high impedance 200µs after the output is in regulation. PGOOD1 is blanked (forced high-impedance state) when a dynamic REFIN1 transition is detected.
13	DH1	High-Side Gate-Driver Output for SMPS1. DH1 swings from LX1 to BST1. DH1 is low in shutdown.

Pin Description (continued)

PIN	NAME	FUNCTION
14	LX1	Inductor Connection for SMPS1. Connect LX1 to the switched side of the inductor. LX1 serves as the lower supply rail for the DH1 high-side gate driver.
15	BST1	Bootstrap Capacitor Connection for SMPS1. The MAX17007A/MAX17007B/MAX17008 include an internal boost switch/diode connected between V_{DD} and BST1. Connect to an external capacitor as shown in Figure 1.
16	GND	Ground. Analog and power ground connection for the low-side gate driver of SMPS1.
17	DL1	Low-Side Gate Driver Output for SMPS1. DL1 swings from GND to V_{DD}. DL1 is forced low after the shutdown sequence has completed. DL1 is also forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that may be present. DL1 is forced low in V_{CC} UVLO.
18	V_{DD}	5V Driver Supply Input. Connect V_{DD} to V_{CC} through a 10∧ resistor. Bypass to ground through a 2.2µF or greater ceramic capacitor. V_{DD} is internally connected to the BST diodes and the low-side gate drivers.
19	DL2	Low-Side Gate-Driver Output for SMPS2. DL2 swings from PGND to V_{DD}. DL2 is forced low after the shutdown sequence has completed. DL2 is also forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that may be present. DL2 is forced low in V_{CC} UVLO.
20	PGND	Power Ground for the Low-Side Gate Driver of SMPS2
21	BST2	Bootstrap Capacitor Connection for SMPS2. The MAX17007A/MAX17007B/MAX17008 include an internal boost switch/diode connected between V_{DD} and BST2. Connect to an external capacitor as shown in Figure 1.
22	LX2	Inductor Connection for SMPS2. Connect LX2 to the switched side of the inductor. LX2 serves as the lower supply rail for the DH2 high-side gate driver.
23	DH2	High-Side Gate-Driver Output for SMPS2. DH2 swings from LX2 to BST2. DH2 is low in shutdown.
24	PGOOD2	Open-Drain Power-Good Output for SMPS2. PGOOD2 is low when the FB2 voltage is more than 100mV below or 150mV above the target voltage, during soft-start, and in shutdown. After the SMPS2 soft-start circuit has terminated, PGOOD2 becomes high impedance 200µs after the output is in regulation. In combined mode, PGOOD2 is not used and can be left open.
25	EN2	SMPS2 Enable Input. Connect to V_{CC} for normal operation. Pull EN2 low to disable SMPS2. The controller slowly ramps down the output voltage to ground, and after the target voltage reaches 0.1V, the controller forces DL2 low. When both EN1 and EN2 are low, the device enters the low-power shutdown state. In combined mode, EN2 is not used and should be connected to GND.
26	CSH2	Positive Current-Sense Input for SMPS2. Connect to the positive terminal of the current-sense element. Figure 14 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
27	CSL2	Output-Sense and Negative Current-Sense Input for SMPS2. When using the internal preset 1.5V feedback divider (FB2 = REF), the controller uses CSL2 to sense the output voltage. Connect to the negative terminal of the current-sense element. Figure 14 describes two different current-sensing options—using accurate sense resistors or lossless inductor DCR sensing.
28	FB2	SMPS2 Feedback Input. Adjust the SMPS2 voltage with a resistive voltage-divider between SMPS2 output and GND. Connect FB2 to REF for preset 1.5V output. Tie FB2 to V_{CC} to configure the MAX17007A/MAX17007B/MAX17008 for combined-mode operation.
—	EP	Exposed Backside Pad. Connect to analog ground.

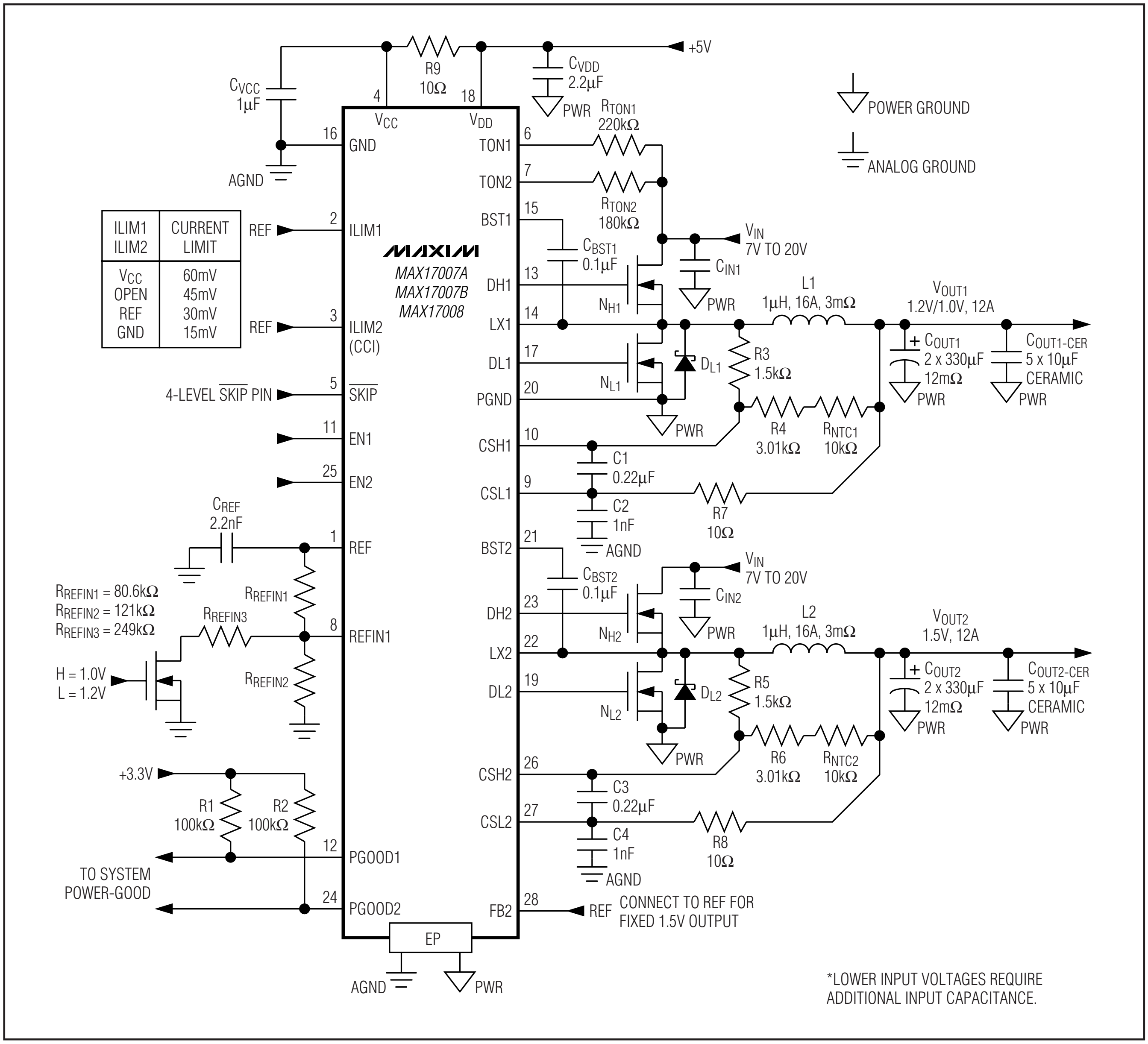


Figure 1. MAX17007A/MAX17007B/MAX17008 Separate-Mode Standard Application Circuit

Table 1. Component Selection for Standard Applications

COMPONENT	V_{OUT1} = 1.0V/1.2V AT 12A (FIGURE 1)	V_{OUT} = 1.5V AT 12A (FIGURE 1)
	V_{IN} = 7V to 20V TON1 = 220kΩ (270kHz)	V_{IN} = 7V to 20V TON2 = 180kΩ (330kHz)
Input Capacitor (per Phase)	(2x) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(2x) 10µF, 25V Taiyo Yuden TMK432BJ106KM
Output Capacitor	(2x) 330µF, 2.5V, 12mΩ, C case SANYO 2R5TPE330MCC2	(2x) 330µF, 2.5V, 12mΩ, C case SANYO 2R5TPE330MCC2
Inductor	1µH, 3.25mΩ, 16A Würth Electronics 7443552100	1µH, 3.25mΩ, 16A Würth Electronics 7443552100
Schottky Diode	2A, 30V Schottky diode (SMA) Nihon EC21QS03L Central Semiconductor CMSH2-40M	2A, 30V Schottky diode (SMA) Nihon EC21QS03L Central Semiconductor CMSH2-40M
High-Side MOSFET	Fairchild Semiconductor (1x) FDS8690 8.6mΩ/11.4mΩ (typ/max)	Fairchild Semiconductor (1x) FDS8690 8.6mΩ/11.4mΩ (typ/max)
Low-Side MOSFET	Fairchild Semiconductor (1x) FDS8670 4.2mΩ/5mΩ (typ/max)	Fairchild Semiconductor (1x) FDS8670 4.2mΩ/5mΩ (typ/max)

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
AVX Corp.	www.avxcorp.com
BI Technologies	www.bitechnologies.com
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp.	www.kemet.com
NEC TOKIN America, Inc.	www.nec-tokinamerica.com
Panasonic Corp.	www.panasonic.com
Pulse Engineering	www.pulseeng.com
Renesas Technology Corp.	www.renesas.com
SANYO Electric Company, Ltd.	www.sanyodevice.com
Siliconix (Vishay)	www.vishay.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com

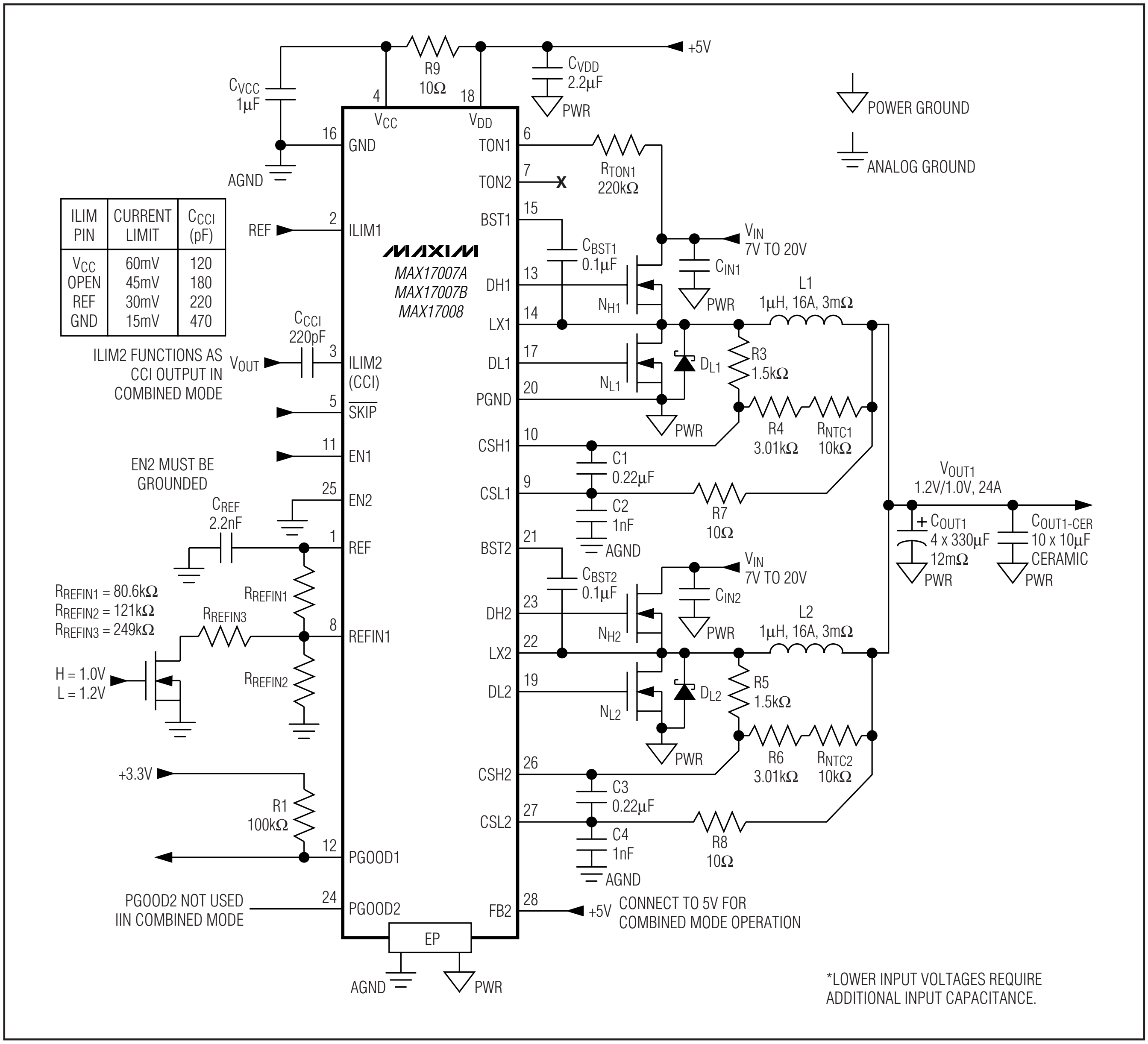
Detailed Description

The MAX17007A/MAX17007B/MAX17008 standard application circuit (Figure 1) generates the 1V to 1.2V/12A and 1.5V/12A chipset voltages in a notebook computer. The input supply range is 7V to 20V for the specific application. Table 1 lists component selections, while Table 2 lists the component manufacturers. Figure 2 shows the combined-mode standard application circuit and Figure 3 is the MAX17007A/MAX17007B/MAX17008 functional diagram.

The MAX17007A/MAX17007B/MAX17008B contain two constant on-time step-down controllers designed for low-voltage power supplies. The two SMPSs can also be combined to operate as a two-phase high-current single-output regulator. Constant on-time Quick-PWM operation provides fast response to load transients and handles wide I/O voltage ratios with ease, while maintaining a relatively constant switching frequency. The switching frequency can be adjusted between 200kHz and 600kHz with external resistors. Differential output current sensing allows output sense-resistor sensing for an accurate current-limit, lossless inductor DCR current sensing for lower power dissipation while maintaining 0.7% output accuracy. Overvoltage (MAX17007A/MAX17007B) and undervoltage protection and accurate user-selectable current limits (four different levels) ensure robust operations.

The MAX17007A/MAX17007B/MAX17008 feature a special combined-mode configuration that allows higher current outputs to be supported. A current-balance integrator maintains equal currents in the two phases, improving efficiency and power distribution.

Dual and Combinable QPWM Graphics Core Controllers for Notebook Computers



ILIM PIN	CURRENT LIMIT	C_{CCI} (pF)
V_{CC}	60mV	120
OPEN	45mV	180
REF	30mV	220
GND	15mV	470

Figure 2. MAX17007A/MAX17007B/MAX17008 Combined-Mode Standard Application Circuit

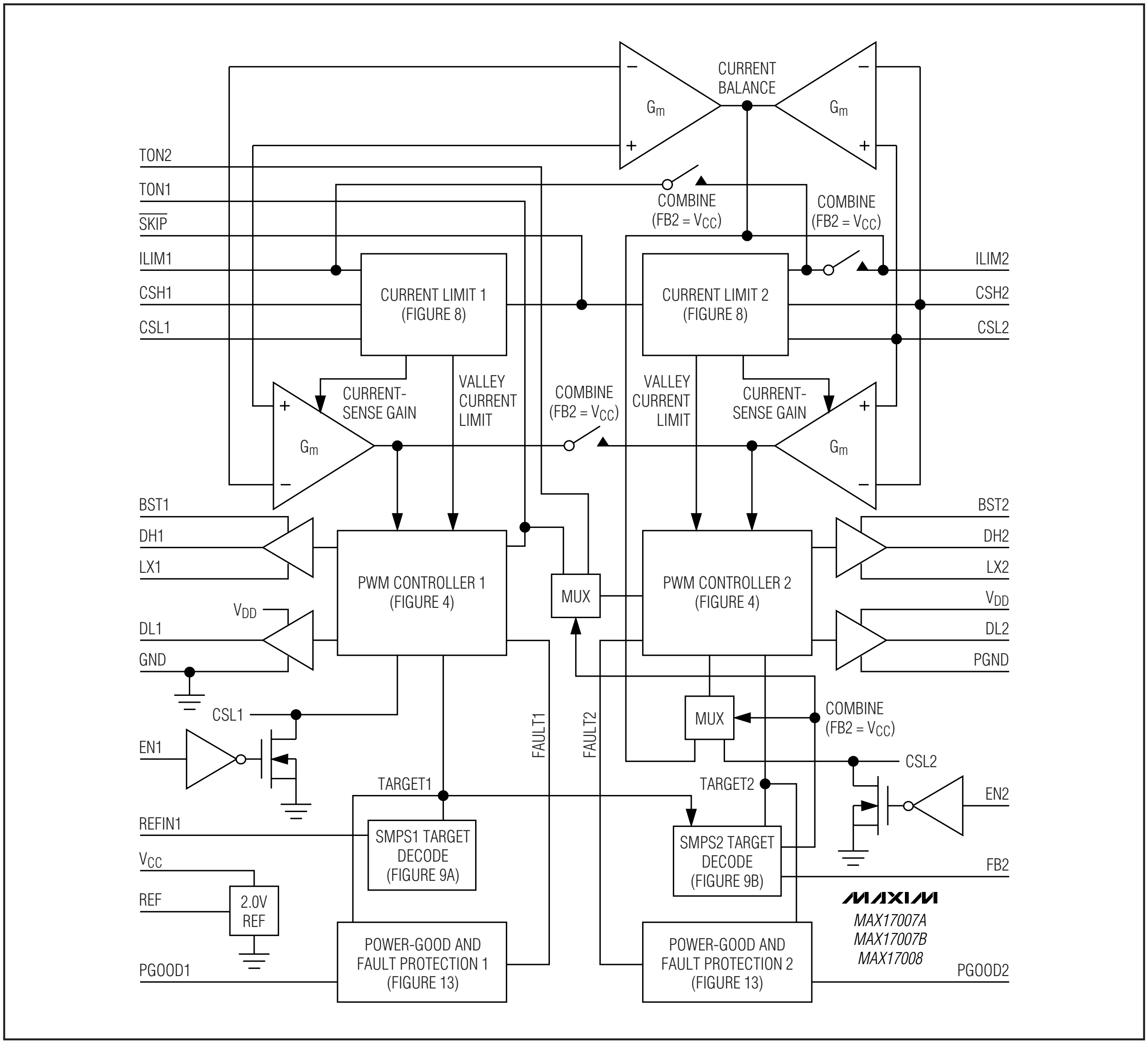


Figure 3. MAX17007A/MAX17007B/MAX17008 Functional Diagram

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+5V Bias Supply (V_{CC}, V_{DD})

The MAX17007A/MAX17007B/MAX17008 require an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's 95%-efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the 5V supply can be generated with an external linear regulator such as the MAX1615.

The 5V bias supply powers both the PWM controllers and internal gate-drive power, so the maximum current drawn depends on the external MOSFET's gate capacitance, and the selected switching frequency:

$$I_{BIAS} = I_Q + f_{SW1}Q_{G(SMPS1)} + f_{SW2}Q_{G(SMPS2)}$$
$$= 4mA \text{ to } 40mA \text{ (typ)}$$

Bypass V_{CC} with a 1µF or greater ceramic capacitor to the analog ground. Bypass V_{DD} with a 2.2µF or greater ceramic capacitor to the power ground. V_{CC} and V_{DD} should be separated with a 10Ω resistor (Figure 1).

2V Reference

The 2V reference is accurate to ±1% over temperature and load, making REF useful as a precision system reference. Bypass REF to GND with a 2.2nF. The reference sources up to 100µA and sinks 10µA to support external loads.

Combined-Mode Operation (FB2 = V_{CC})

Combined-mode operation allows the MAX17007A/MAX17007B/MAX17008 to support even higher output currents by sharing the load current between two phases, distributing the power dissipation over several power components to improve the efficiency. The MAX17007A/MAX17007B/MAX17008 are configured in combined mode by connecting FB2 to V_{CC}. See Figure 2 for the combined-mode standard application circuit.

Table 3 lists the pin function differences between combined mode and separate mode. See the *Pin Description* for additional details.

Table 3. Pin Function in Combined and Separate Modes

PIN	COMBINED MODE	SEPARATE MODE
FB2	Connect to V_{CC} to configure MAX17007A/MAX17007B/MAX17008 for combined-mode operation	Connect to REF for preset 1.5V, or use a resistor-divider to set the SMPS2 output voltage
REFIN1	Sets the combined output voltage—dynamic, fixed, and preset voltages supported	Sets the SMPS1 output voltage—dynamic, fixed, and preset voltages supported
EN1	Enables/disables combined output	Enables/disables SMPS1
EN2	Not used; connect to GND	Enables/disables SMPS2
PGOOD1	Power-good indicator for combined output voltage	Power-good indicator for SMPS1
PGOOD2	Not used; can be left open	Power-good indicator for SMPS2
TON1	Sets the per-phase switching frequency for both SMPSs	Sets the switching frequency for SMPS1
TON2	Not used; leave open	Sets the switching frequency for SMPS2
ILIM1	Sets the per-phase current limit for both SMPSs	Sets SMPS1 current limit
ILIM2 (CCI)	Current-balance integrator output; connect a capacitor from CCI to the output	Sets SMPS2 current limit
$\overline{SKIP}$	Only three distinct modes of operation; ultrasonic mode not supported	Supports all four modes of operation

SMPS Detailed Description

Free-Running Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward. This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (150ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out. Figure 4 is the PWM controller block diagram.

On-Time One-Shot

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. In independent mode, the high-side switch on-time is inversely proportional to the battery voltage as sensed by the TON1 and TON2 inputs, and proportional to the voltages on CSL1 and CSL2 pins:

SMPS1 On-Time $t_{ON1} = T_{SW1}(V_{CSL1}/V_{IN})$

SMPS2 On-Time $t_{ON2} = T_{SW2}(V_{CSL2}/V_{IN})$

where T_{SW1} (switching period of SMPS1) is set by the resistance between TON1 and V_{IN}, T_{SW2} is set by the resistance between TON2 and V_{IN}. This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator.

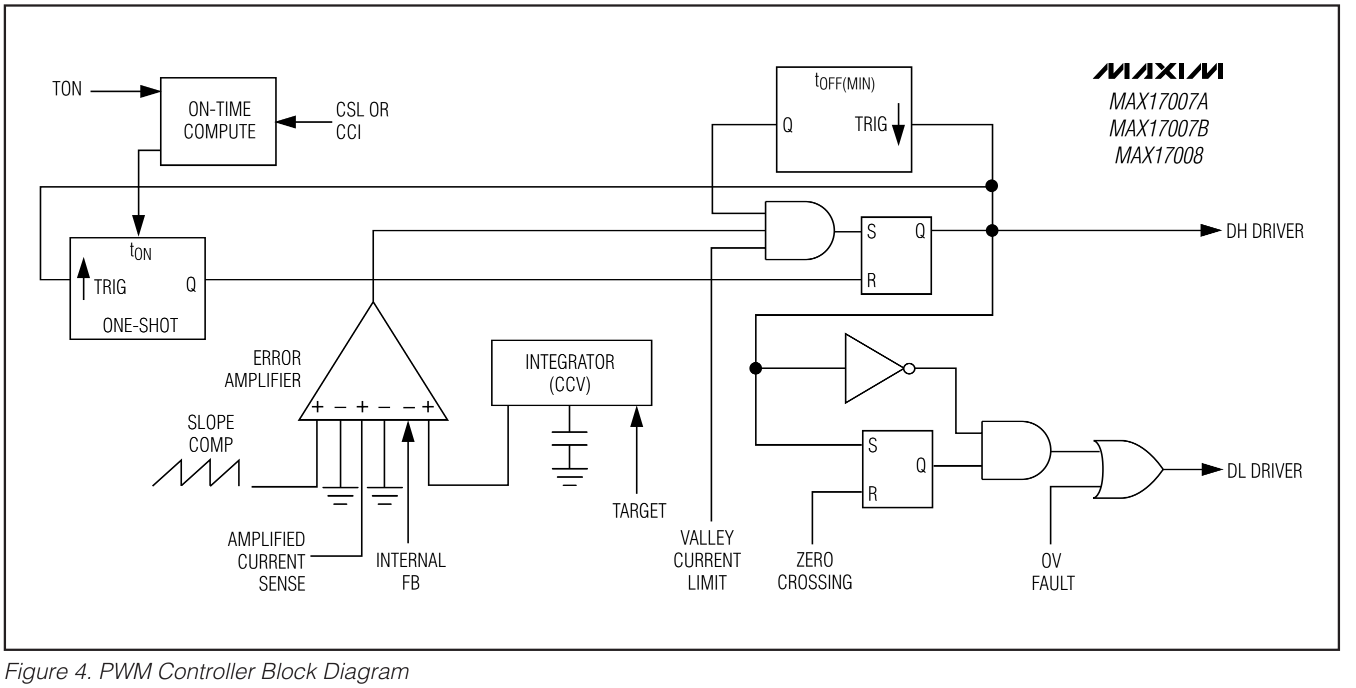

Figure 4. PWM Controller Block Diagram

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Switching Frequency

The MAX17007A/MAX17007B/MAX17008 feature independent resistor-programmable switching frequencies for each SMPS, providing flexibility for applications where one SMPS operates at a lower switching frequency when connected to a high-voltage input rail while the other SMPS operates at a higher switching frequency when connected to a lower voltage rail as a second-stage regulator. Connect a resistor (R_{TON}) between TON and V_{IN} to set the switching period $T_{SW} = 1/f_{SW}$:

$$T_{SW1} = C_{TON}(R_{TON1} + 6.5k\Omega)$$

$$T_{SW2} = C_{TON}(R_{TON2} + 6.5k\Omega)$$

where C_{TON} = 16.26pF. A 97.5kΩ to 302.5kΩ corresponds to switching periods of 1.67µs (600kHz) to 5µs (200kHz) for SMPS1 and SMPS2. High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

For continuous conduction operation, the actual switching frequency can be estimated by:

$$f_{SW} = \frac{V_{OUT} + V_{DIS}}{t_{ON}(V_{IN} + V_{CHG})}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and printed-circuit board (PCB) resistances; V_{CHG} is the sum of the resistances in the charging path, including the high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time calculated by the on-time block.

When operating in separate mode, it is recommended that both SMPS switching frequencies be set apart by 10% to 30% to prevent the two sides from beating against each other.

Combined-Mode On-Time One-Shot

In combined mode (FB2 = V_{CC}), TON1 sets the on-time, and hence the switching frequency, for both SMPS. The on-time is programmed using the TON1 equation, which sets the switching frequency per phase. The effective switching frequency as seen on the input and output capacitors is twice the per-phase frequency.

Combined-Mode Current Balance

In combined mode, the one-shot for SMPS2 varies the on-time in response to the input voltage and the difference between the SMPS1 and SMPS2 inductor currents. The SMPS1 one-shot in combined mode behaves the same way as it does in separate mode. As such, SMPS2 regulates the current balance, while SMPS1 regulates the voltage.

Two identical transconductance amplifiers integrate the difference between SMPS1 and SMPS2 current-sense signals. The summed output is internally connected to CCI, allowing adjustment of the integration time constant with a compensation network (usually a capacitor) connected between CCI and the output.

The resulting compensation current and voltage are determined by the following equations:

$$I_{CCI} = G_m[(V_{CSH1} - V_{CSL1}) - (V_{CSH2} - V_{CSL2})]$$

$$V_{CCI} = V_{OUT} + I_{CCI}Z_{CCI}$$

where Z_{CCI} is the impedance at the CCI output. The SMPS2 on-time one-shot uses this integrated signal (V_{CCI}) to set the SMPS2 high-side MOSFETs on-time. When SMPS1 and SMPS2 current-sense signals ($V_{CSH1} - V_{CSL1}$ and $V_{CSH2} - V_{CSL2}$) become unbalanced, the transconductance amplifiers adjust the SMPS2 on-time, which increases or decreases the SMPS2 inductor current until the current-sense signals are properly balanced. In combined mode, the SMPS2 on-time is given by:

$$\text{SMPS2 On-Time } t_{ON2} = T_{SW2}(V_{CCI}/V_{IN})$$

SMPS Enable Controls (EN1, EN2)

EN1 and EN2 provide independent control of output soft-start and soft-shutdown. This allows flexible control of startup and shutdown sequencing. The outputs can be started simultaneously, sequentially, or independently. To provide sequential startup, connect EN of one regulator to PGOOD of the other. For example, with EN1 connected to PGOOD2, OUT1 soft-starts after OUT2 is in regulation.

When configured in separate mode, the two outputs are independent. A fault at one output does not trigger shutdown of the other.

When configured in combined mode (FB2 = V_{CC}), EN1 is the master control input that enables/disables the combined output, while EN2 has no function and must be connected to GND. The startup slew rate follows that of SMPS1.

Toggle EN low to clear the overvoltage, undervoltage, and thermal-fault latches.

Soft-Start

Soft-start begins when EN is driven high and REF is in regulation. During soft-start, the output is ramped up from 0V to the final set voltage at 1.3mV/µs slew rate for SMPS1, and 0.65mV/µs for SMPS2, reducing the inrush current and providing a predictable ramp-up time for power sequencing:

$$t_{START1} = t_{SHDN1} = \frac{V_{REFIN1}}{SR_{SS1}} = \frac{V_{REFIN1}}{1.3mV/\mu s}$$

$$t_{START2} = t_{SHDN2} = \frac{V_{FB2}}{SR_{SS2}} = \frac{V_{FB2}}{0.65mV/\mu s}$$

The soft-start circuitry does not use a variable current limit, so full output current is available immediately. The respective PGOOD becomes high impedance approximately 200µs after the target voltage has been reached. The MAX17007A/MAX17007B/MAX17008 automatically use pulse-skipping mode during soft-start and use forced-PWM mode during soft-shutdown, regardless of the $\overline{SKIP}$ configuration.

For automatic startup, the battery voltage should be present before V_{CC}. If the controller attempts to bring the output into regulation without the battery voltage present, the fault latch trips. The controller remains shut down until the fault latch is cleared by toggling EN or cycling the V_{CC} power supply below 0.5V.

Soft-Shutdown

Soft-shutdown begins when the system pulls EN low, an output undervoltage fault, or a thermal fault. During soft-shutdown, the respective PGOOD is pulled low immediately and the output voltage ramps down with the same startup slew rate for the respective outputs. After the controller reaches the 0V target, the drivers are disabled (DL_ and DH_ pulled low) and the internal 10Ω discharge on CSL_ activated. The MAX17007A/MAX17007B/MAX17008 shut down completely when both EN are low—the reference turns off after both SMPSs have reached the 0V target, and the supply current drops to about 1µA (max).

Slowly discharging the output capacitors by slewing the output over a long period of time (typically 0.5ms to 2ms) keeps the average negative inductor current low (damped response), thereby preventing the negative output-voltage excursion that occurs when the controller discharges the output quickly by permanently turning on the low-side MOSFET (underdamped response). This eliminates the need for the Schottky diode normally connected between the output and ground to clamp the negative output-voltage excursion.

Modes of Operation

Forced-PWM Mode ($\overline{SKIP}$ = 5V)

The low-noise forced-PWM mode ($\overline{SKIP}$ = 5V) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH maintains a duty factor of V_{OUT}/V_{IN}. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V bias current remains between 2mA to 5mA, depending on the switching frequency.

The MAX17007A/MAX17007B/MAX17008 automatically use forced-PWM operation during shutdown, regardless of the $\overline{SKIP}$ configuration.

Automatic Pulse-Skipping Mode ($\overline{SKIP}$ = GND or 2V)

In skip mode ($\overline{SKIP}$ = GND or 2V), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator threshold is set by the differential across CSL_ and CSH_.

DC output-accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX17007A/MAX17007B/MAX17008 regulate the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction ($\overline{SKIP}$ = GND or 2V and $I_{OUT} < I_{LOAD(SKIP)}$), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation. However, the internal integrator corrects for most of it, resulting in very little load regulation.

When $\overline{SKIP}$ = 2V, the MAX17007A/MAX17007B/MAX17008 use forced-PWM operation during all dynamic output-voltage transitions until 100µs after the transition has been completed—REFIN1 and the internal target are within ±50mV (typ) and an error-amplifier transition is detected. Since SMPS2 does not support dynamic transitions, $\overline{SKIP}$ = 2V and $\overline{SKIP}$ = GND have the same pulse-skipping behavior without any forced-PWM transitions.

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When $\overline{SKIP}$ is pulled to GND, the MAX17007A/MAX17007B/MAX17008 remain in pulse-skipping mode. Since the output is not able to sink current, the timing for negative dynamic output-voltage transitions depends on the load current and output capacitance. Letting the output voltage drift down is typically recommended in order to reduce the potential for audible noise since this eliminates the input current surge during negative output-voltage transitions. Figure 5 shows the pulse-skipping/discontinuous crossover point.

Ultrasonic Mode ($\overline{SKIP}$ = Open = 3.3V)

Leaving $\overline{SKIP}$ unconnected or connecting $\overline{SKIP}$ to 3.3V activates a unique pulse-skipping mode with a minimum switching frequency of 25kHz. This ultrasonic pulse-skipping mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the controller automatically transitions to fixed-frequency PWM operation when the load reaches the same critical conduction point ($I_{LOAD(SKIP)}$) that occurs when normally pulse skipping.

An ultrasonic pulse occurs when the controller detects that no switching has occurred within the last 30µs. Once triggered, the ultrasonic controller pulls DL high, turning on the low-side MOSFET to induce a negative inductor current (Figure 6). After the inductor current reaches the negative ultrasonic current threshold, the controller turns off the low-side MOSFET (DL pulled low) and triggers a constant on-time (DH driven high). When the on-time has expired, the controller reenables the low-side MOSFET until the controller detects that the inductor current dropped below the zero-crossing threshold. Starting with a DL pulse greatly reduces the peak output voltage when compared to starting with a DH pulse.

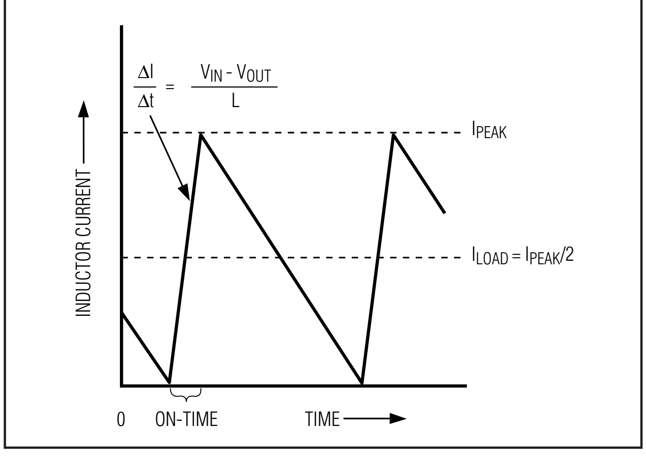

Figure 5. Pulse-Skipping/Discontinuous Crossover Point

The output voltage at the beginning of the ultrasonic pulse determines the negative ultrasonic current threshold, resulting in the following equations for SMPS1:

$$V_{ISONIC1} = I_{L1}R_{CS1} = \left(V_{REFIN1} - V_{CSL1}\right) \times 0.65$$

(SMPS1 adjustable mode)

$$V_{ISONIC1} = I_{L1}R_{CS1} = \left(1.05V - V_{CSL1}\right) \times 0.65$$

(SMPS1 preset mode)

where $V_{CSL1} > V_{REFIN1}$ in adjustable mode, $V_{CSL1} >$ 1.05V in preset mode, and R_{CS1} is the current-sense resistance seen across CSH1 to CSL1.

Similarly for SMPS2:

$$V_{ISONIC2} = I_{L2}R_{CS2} = \left(0.7V - V_{FB2}\right) \times 0.65$$

(SMPS2 adjustable mode)

$$V_{ISONIC2} = I_{L2}R_{CS2} = \left(1.5V - V_{CSL2}\right) \times 0.65$$

(SMPS2 preset mode)

where $V_{CSL2} >$ 0.7V in adjustable mode, $V_{CSL2} >$ 1.5V in preset mode, and R_{CS2} is the current-sense resistance seen across CSH2 to CSL2.

In combined mode, ultrasonic mode setting is disabled, and the $\overline{SKIP}$ = open (3.3V) setting is identical to the $\overline{SKIP}$ = GND setting.

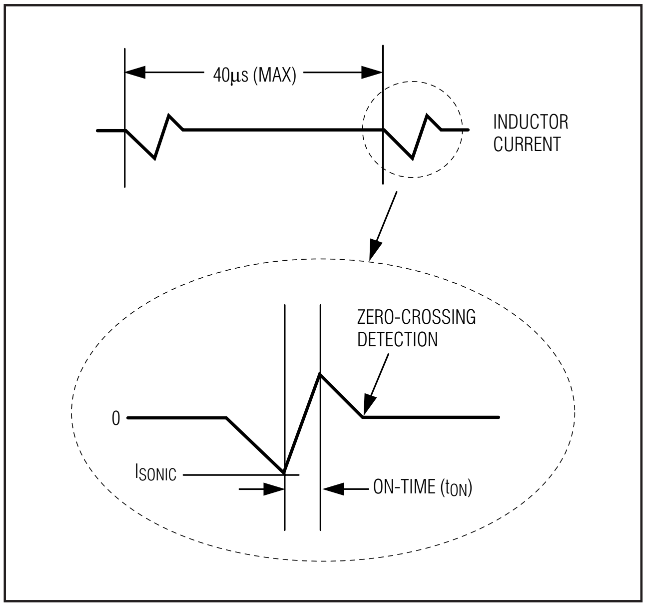

Figure 6. Ultrasonic Waveform

Valley Current-Limit Protection

The current-limit circuit employs a unique "valley" current-sensing algorithm that senses the inductor current across the output current-sense element—inductor DCR or current-sense resistor, which generates a voltage between CSH_ and CSL_. If the current exceeds the valley current-limit threshold during the low-side MOSFET conduction time, the PWM controller is not allowed to initiate a new cycle. The valley current-limit threshold is set by the four-level ILIM_ pin, with selectable limits of 15mV, 30mV, 45mV, and 60mV.

The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current (Figure 7). Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance. See Figure 8.

In forced-PWM mode, the MAX17007A/MAX17007B/MAX17008 also implement a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit.

In combined mode, ILIM1 sets the per-phase current limit for both phases.

MOSFET Gate Drivers (DH, DL)

The DH and DL drivers are optimized for driving moderate-sized high-side, and larger low-side power MOSFETs. This is consistent with the low duty factor seen in notebook applications, where a large V_{IN} - V_{OUT} differential exists. The high-side gate driver (DH) sources and sinks 1.2A, and the low-side gate driver (DL) sources 1.0A and sinks 2.4A. This ensures robust gate drive for high-current applications. The DH floating high-side MOSFET driver is powered by internal boost switch charge pumps at BST, while the DL synchronous-rectifier driver is powered directly by the 5V bias supply (V_{DD}).

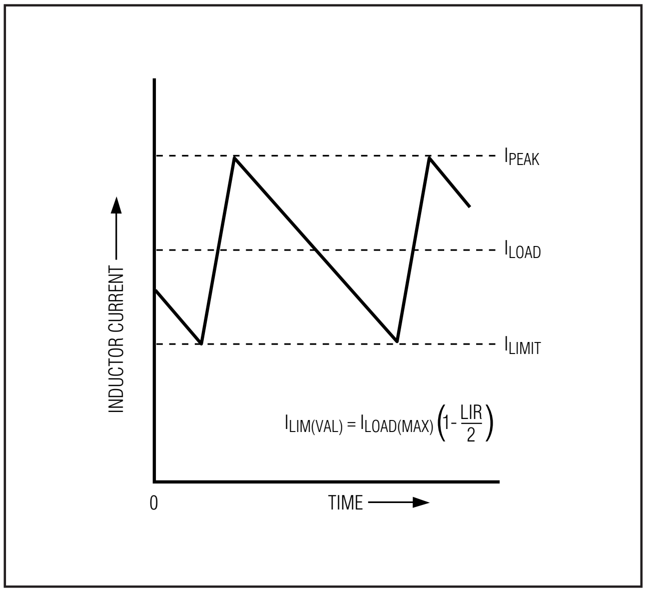

Figure 7. "Valley" Current-Limit Threshold Point

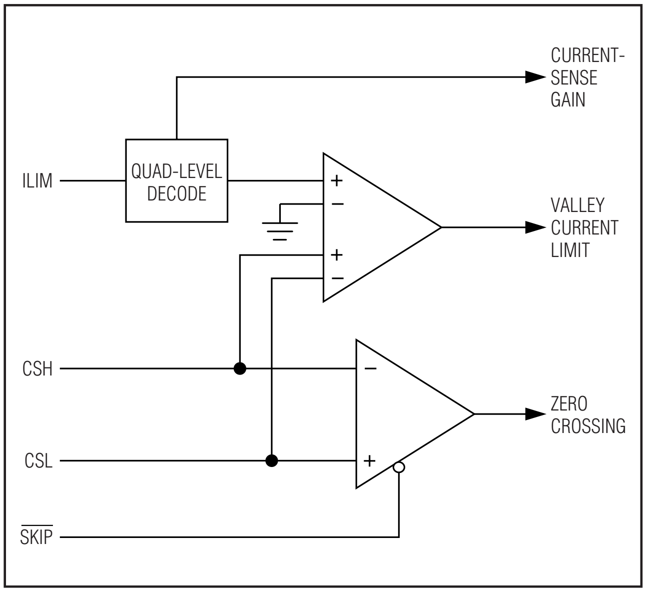

Figure 8. Current-Limit Block Diagram

Output Voltage

The MAX17007A/MAX17007B/MAX17008 feature preset and adjustable output voltages for both SMPSs, and dynamic output voltages for SMPS1. In combined mode, the output voltage is set by REFIN1, and all features for SMPS1 output-voltage configuration and dynamic voltage changes apply to the combined output. Figure 9 is the SMPS target decode block diagram.

Preset/Adjustable Output Voltages (Dual-Mode Feedback)

Connect REFIN1 to V_{CC} to set the SMPS1 voltage to preset 1.05V. Connect FB2 to REF to set the SMPS2 voltage to preset 1.5V. The SMPS1 output voltage can be adjusted up to 2V by changing REFIN1 voltage without using an external resistive voltage-divider. The output voltage of SMPS2 can be adjusted with an external resistive voltage-divider between CSL2 and GND with the center tap connected to FB2 (Figure 10). Choose R_{FB2LO} (resistance from FB2 to GND) to be approximately 10kΩ and solve for R_{FB2HI} (resistance from CSL2 to FB2) using the equation:

$$R_{FB2HI} = R_{FB2LO}\left(\frac{V_{CSL2}}{0.7V} - 1\right)$$

The MAX17007A/MAX17007B/MAX17008 regulate the valley of the output ripple, so the actual DC output voltage is higher than the slope compensated target by 50% of the output ripple voltage. Under steady-state conditions, the MAX17007A/MAX17007B/MAX17008s' internal integrator corrects for this 50% output ripple voltage error, resulting in an output-voltage accuracy that is dependent only on the offset voltage of the integrator amplifier provided in the *Electrical Characteristics* table.

Dynamic Output Voltages (REFIN1)

The MAX17007A/MAX17007B/MAX17008 regulate the output to the voltage set at REFIN1. By changing the voltage at REFIN1 (Figure 11), the MAX17007A/MAX17007B/MAX17008 can be used in applications that require dynamic output voltage changes between two set points. For a step-voltage change at REFIN1, the rate of change of the output voltage is limited either by the internal 9.5mV/µs slew-rate circuit or by the component selection—inductor current ramp, the total output capacitance, the current limit, and the load during the transition—whichever is slower. The total output capacitance determines how much current is needed to change the output voltage, while the inductor limits the current ramp

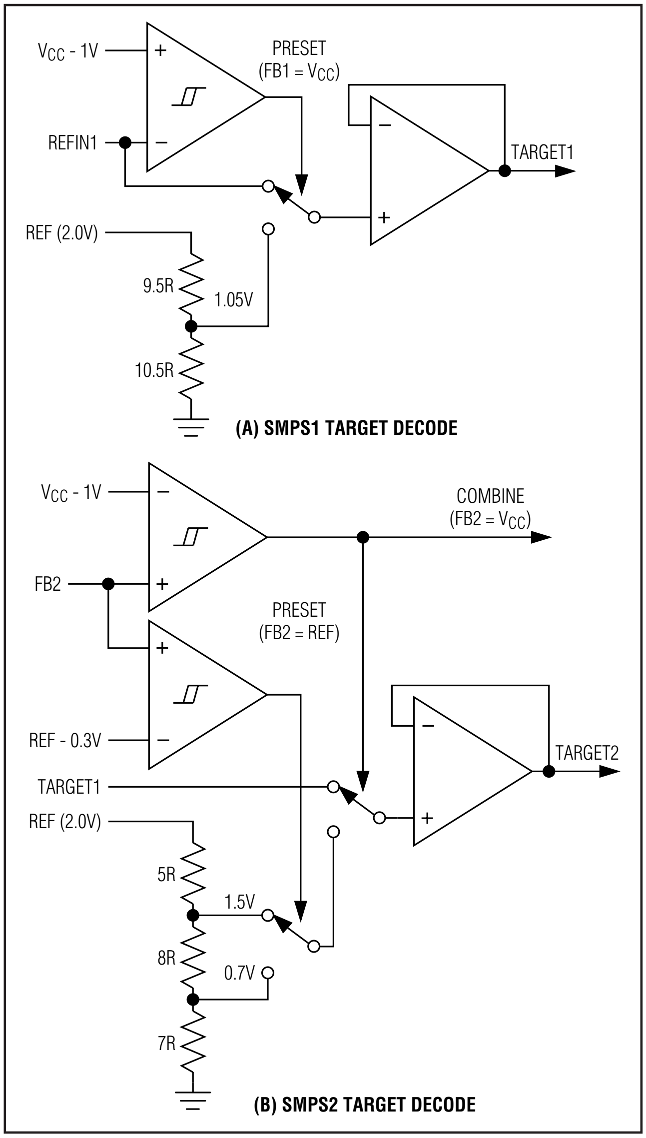

Figure 9. SMPS Target Decode Block Diagram

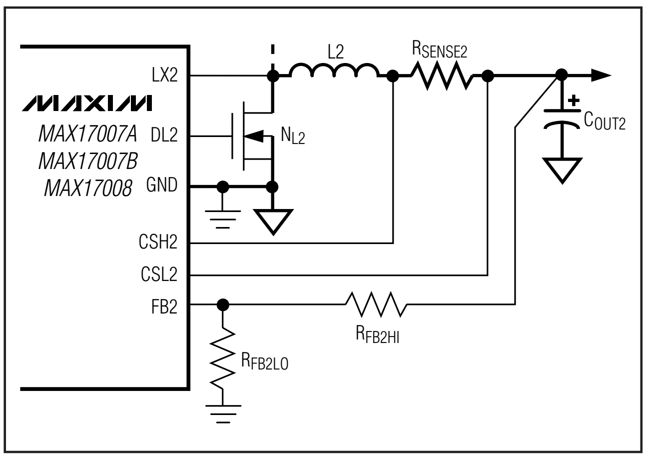

Figure 10. Setting V_{OUT2} with a Resistive Voltage-Divider

rate. Additional load current can slow down the output voltage change during a positive REFIN1 voltage change, and can speed up the output voltage change during a negative REFIN1 voltage change.

Automatic Fault Blanking (SMPS1)

When the MAX17007A/MAX17007B/MAX17008 detect that the internal target and REFIN1 are more than ±50mV (typ) apart, the controller automatically blanks PGOOD1, blanks the UVP protection, and sets the OVP threshold to max REF + 300mV. The blanking remains until 1) the internal target and REFIN1 are within ±50mV of each other, and 2) an edge is detected on the error amplifier signifying that the output is in regulation. This prevents the system or internal fault protection from shutting down the controller during transitions. Figure 11 shows the dynamic REFIN1 transition ($\overline{SKIP}$ = GND) and Figure 12 shows the dynamic REFIN1 transition ($\overline{SKIP}$ = REF).

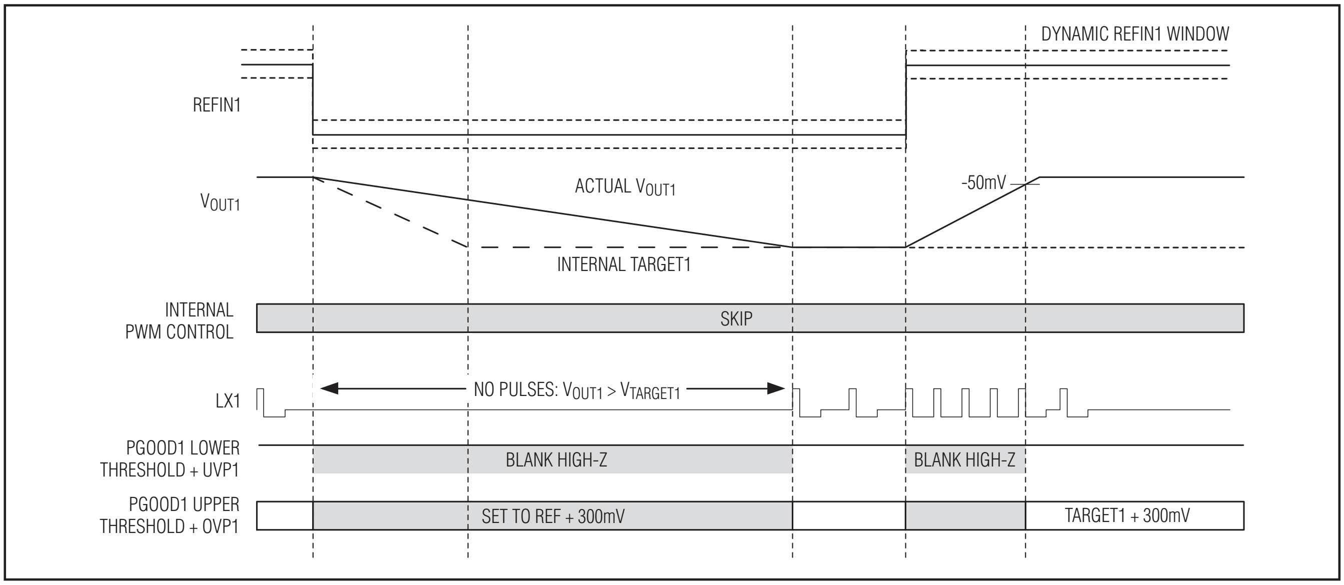

Figure 11. Dynamic REFIN1 Transition ($\overline{SKIP}$ = GND)

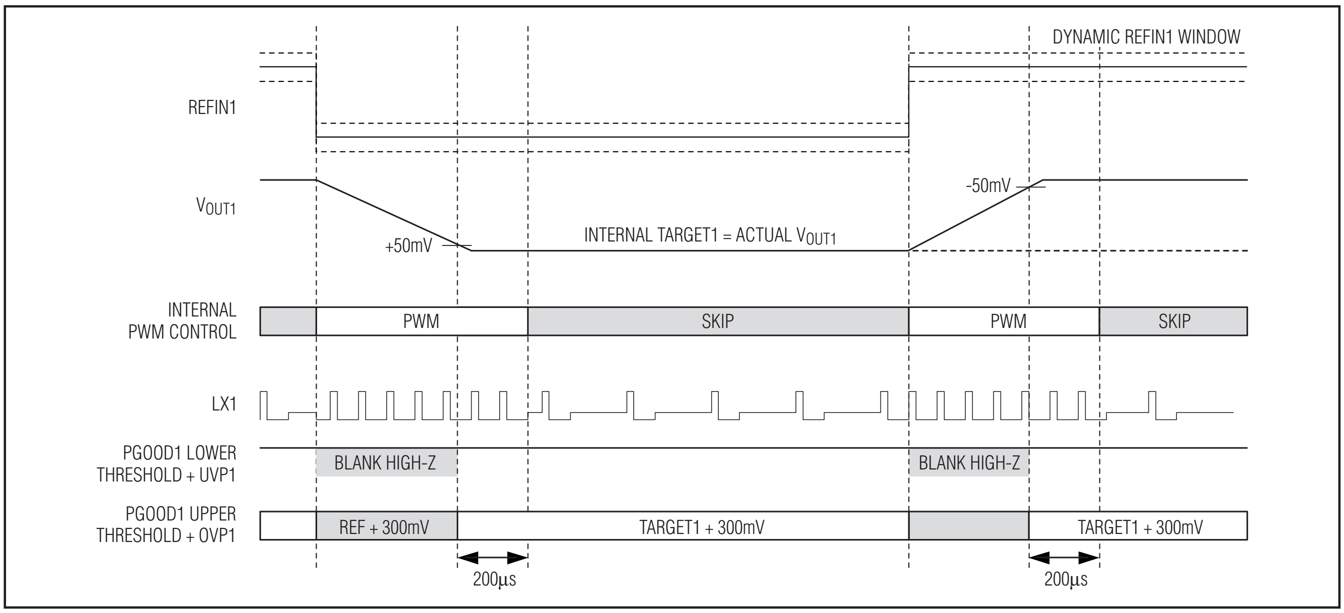

Figure 12. Dynamic REFIN1 Transition ($\overline{SKIP}$ = REF)