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EVALUATION KIT AVAILABLE

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

General Description

The MAX17009 is a 2-phase, step-down interleaved, fixed-frequency controller for AMD's® serial VID interface (SVI) CPU core supplies. Power-on detection of the CPU configures the MAX17009 as two independent single-phase regulators for a dual CPU core application, or one high-current, dual-phase, combined-output regulator for a unified core application. A reference buffer output (NBV_BUF) sets the voltage-regulation level for a North Bridge (NB) regulator, completing the total CPU cores and NB power requirements.

The MAX17009 is fully AMD SVI compliant. Output voltages are dynamically changed through a 2-wire serial interface, allowing the switching regulator and the reference buffer to be individually programmed to different voltages. A programmable slew-rate controller enables controlled transitions between VID codes, soft-start limits the inrush current, and soft-shutdown brings the output voltage back down to zero without any negative ring.

Transient phase repeat improves the response of the fixed-frequency architecture. Independently programmable AC and DC droop and selectable offset improve stability and reduce the total output-capacitance requirement. A thermistor-based temperature sensor allows for a programmable thermal-fault output ($\overline{VRHOT}$). The MAX17009 includes thermal-fault protection, undervoltage protection (UVP), and selectable output overvoltage protection (OVP). When any of these protection features detect a fault, the controller shuts down. True differential current sensing improves current limit, load-line accuracy, and current balance when operating in combined mode. The MAX17009 has an adjustable switching frequency, allowing 100kHz to 1.2MHz per-phase operation.

Applications

Mobile AMD SVI Core Supply

Multiphase CPU Core Supply

Voltage-Positioned, Step-Down Converters

Notebook/Desktop Computers

Pin Configuration appears at end of data sheet.

AMD is a registered trademark of Advanced Micro Devices, Inc.

Features

- **Dual-Output, Fixed-Frequency, Core Supply Controller**
- **Separate or Combinable Outputs Detected at Power-Up**
- **Reference Buffer Output for NB Controller**
- **±0.4% V_{OUT} Accuracy Over Line, Load, and Temperature**
- **AMD SVI-Compliant Serial Interface**
- **7-Bit On-Board DAC: 0 to +1.550V Output Adjust Range**
- **Dynamic Phase Selection Optimizes Active/Sleep Efficiency**
- **Transient Phase Repeat Reduces Output Capacitance**
- **True Out-of-Phase Operation Reduces Input Capacitance**
- **Integrated Boost Switches**
- **Programmable AC and DC Droop**
- **Programmable 100kHz to 1.2MHz Switching Frequency**
- **Accurate Current Balance and Current Limit**
- **Adjustable Slew-Rate Control**
- **Power-Good (PWRGD) and Thermal-Fault ($\overline{VRHOT}$) Outputs**
- **System Power-OK (PGD_IN) Input**
- **Drives Large Synchronous-Rectifier MOSFETs**
- **4V to 26V Battery Input-Voltage Range**
- **Overvoltage, Undervoltage, and Thermal-Fault Protection**
- **Power Sequencing and Timing**
- **Soft-Startup and Soft-Shutdown**
- **< 1µA Typical Shutdown Current**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX17009GTL+	-40°C to +105°C	40 TQFN-EP*, 5mm x 5mm	T4055-1

+Denotes a lead-free package.

**EP = Exposed pad.*

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

ABSOLUTE MAXIMUM RATINGS

V_{DD1}, V_{DD2}, V_{CC}, V_{DDIO} to GND_ ..... -0.3V to +6V
PWRGD to GND_ ..... -0.3V to +6V
FBDC_, FBAC_, $\overline{PRO}$ to GND_ ..... -0.3V to (V_{CC} + 0.3V)
GNDS2, THRM, $\overline{VRHOT}$ to GND_ ..... -0.3V to +6V
CSP_, CSN_, ILIM to GND_ ..... -0.3V to +6V
SVC, SVD, PGD_IN to GND_ ..... -0.3V to +6V
NBV_BUF, $\overline{NBSKP}$ to GND_ ..... -0.3V to (V_{CC} + 0.3V)
REF, OSC, TIME, OPTION to GND_ ..... -0.3V to (V_{CC} + 0.3V)
BST1, BST2 to GND_ ..... -0.3V to +36V
BST1 to V_{DD1} ..... -0.3V to +30V
BST2 to V_{DD2} ..... -0.3V to +30V
LX1 to BST1 ..... -6V to +0.3V
LX2 to BST2 ..... -6V to +0.3V
DH1 to LX1 ..... -0.3V to (V_{BST1} + 0.3V)
DH2 to LX2 ..... -0.3V to (V_{BST2} + 0.3V)
DL1 to GND_ ..... -0.3V to (V_{DD1} + 0.3V)
DL2 to GND_ ..... -0.3V to (V_{DD2} + 0.3V)
GNDS1, GNDS_NB to GND_ ..... -0.3V to +0.3V
Continuous Power Dissipation (T_A = +70°C)
  Multilayer PCB (derate 35.7mW/°C above +70°C) 2857mW
  Single-Layer PCB (derate 22.2mW/°C above +70°C) .. 1778mW
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
Input Voltage Range	V_{IN}	Drain of external high-side MOSFET	4		26	V
	V_{BIAS}	V_{CC}, V_{DD1}, V_{DD2}	4.5		5.5	
	V_{DDIO}		1.0		2.7	
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	V_{CC} rising 50mV typical hysteresis	4.10	4.25	4.45	V
V_{CC} Power-On Reset Threshold	V_{CC}	Falling edge, typical hysteresis = 1.1V, faults cleared and DL_ forced high when V_{CC} falls below this level		1.8		V
V_{DDIO} Undervoltage-Lockout Threshold		V_{DDIO} rising 100mV typical hysteresis	0.7	0.8	0.9	V
Quiescent Supply Current (V_{CC})	I_{CC}	Skip mode, FBDC_ forced above their regulation points		5	10	mA
Quiescent Supply Currents (V_{DD1}, V_{DD2})	I_{DD1}, I_{DD2}	Skip mode, FBDC_ forced above their regulation points		0.01	1	µA
Quiescent Supply Current (V_{DDIO})	I_{DDIO}			10	25	µA
Shutdown Supply Current (V_{CC})		$\overline{SHDN}$ = GND		0.01	1	µA
Shutdown Supply Currents (V_{DD1}, V_{DD2})		$\overline{SHDN}$ = GND		0.01	1	µA
Shutdown Supply Current (V_{DDIO})		$\overline{SHDN}$ = GND		0.01	1	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, no REF load	1.986	2.000	2.014	V
Reference Load Regulation		Sourcing: I_{REF} = 0 to 500µA	-2	-0.2		mV
		Sinking: I_{REF} = 0 to -100µA		0.21	6.2	
REF Fault Lockout Voltage		Typical hysteresis = 85mV		1.84		V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SMPS CONTROLLERS						
DC Output-Voltage Accuracy (Note 1)	V_{OUT}	DAC codes from 0.8375V to 1.5500V	-0.4		+0.4	%
		DAC codes from 0.5000V to 0.8250V	-4		+4	mV
		DAC codes below 0.4875V	-10		+10	
DC Load Regulation		Either SMPS, PWM mode, droop disabled, zero to full load		-0.1		%
Line-Regulation Error		Either SMPS, 4V < V_{IN} < 26V		0.03		%/V
GNDS_ Input Range	$V_{GNDS\_}$	Separate mode	-200		+200	mV
GNDS_ Gain	$A_{GNDS\_}$	Separate: $\Delta V_{OUT\_}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV; combined: $\Delta V_{OUT}/\Delta V_{GNDS1}$, -200mV ≤ V_{GNDS1} ≤ +200mV	0.95	1.00	1.05	V/V
GNDS_ Input Bias Current	$I_{GNDS\_}$		-2		+2	µA
Combined-Mode Detection Threshold		GNDS2, detection after REFOK, latched, cleared by cycling $\overline{SHDN}$	0.7	0.8	0.9	V
FBDC_ Input Bias Current	$I_{FBDC0\_}$	CSP_ = CSN_	-3		+3	µA
Switching-Frequency Accuracy	f_{OSC}	R_{OSC} = 143kΩ (f_{OSC} = 300kHz nominal)	-5		+5	%
		R_{OSC} = 35.7kΩ (f_{OSC} = 1.2MHz nominal) to 432kΩ (f_{OSC} = 99kHz nominal)	-7.5		+7.5	
Maximum Duty Factor	D_{MAX}		90	92		%
Minimum On-Time	t_{ONMIN}				175	ns
SMPS1-to-SMPS2 Phase Shift		SMPS2 starts after SMPS1		50		%
				180		Degrees
TIME Slew-Rate Accuracy		During transition: R_{TIME} = 143kΩ, SR = 6.25mV/µs	-10		+10	%
		During transition: R_{TIME} = 35.7kΩ to 357kΩ, SR = 25mV/µs to 2.5mV/µs	-15		+15	
		Startup and shutdown		1		mV/µS
CURRENT LIMIT						
Current-Limit Threshold Tolerance	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$ = 0.05 x (V_{REF} - V_{ILIM}), (V_{REF} - V_{ILM}) = 0.2V to 1.0V	-3		+3	mV
Zero-Crossing Threshold	V_{ZX}	$V_{GND\_}$ - $V_{LX\_}$, SKIP mode		3		mV
Idle Mode™ Threshold Tolerance	V_{IDLE}	$V_{CSP\_}$ - $V_{CSN\_}$, SKIP mode, 0.15 x V_{LIMIT}	-1.5		+1.5	mV
CS_ Input-Leakage Current		CSP_ and CSN_	-0.2		+0.2	µA
CS_ Common-Mode Input Range		CSP_ and CSN_	0		2	V
Phase-Disable Threshold		CSP2	3	V_{CC} - 1	V_{CC} -0.4	V

Idle Mode is a trademark of Maxim Integrated Products, Inc.

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DROOP AND CURRENT BALANCE							
DC Droop Amplifier Transconductance	$G_{m(FBDC\_)}$	$\Delta I_{FBDC\_}/(\Delta V_{CS\_})$, $V_{FBDC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = -60mV to +60mV		0.97	1.00	1.03	mS
DC Droop and Current-Balance Amplifier Offset		$I_{FBDC\_}/G_{m(FBDC\_)}$		-1.5		+1.5	mV
AC Droop and Current-Balance Amplifier Transconductance	$G_{m(FBAC\_)}$	$\Delta I_{FBAC\_}/(\Delta V_{CS\_})$, $V_{FBAC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = -60mV to +60mV		0.97	1.00	1.03	mS
AC Droop and Current-Balance Amplifier Offset		$I_{FBAC\_}/G_{m(FBAC\_)}$		-1.5		+1.5	mV
No-Load Positive Offset with Offset Enabled		Offset enabled, OPTION = REF or GND			12.5		mV
Transient Detection Threshold		Measured at FBDC_ with respect to steady-state FBDC_ regulation voltage, 5mV hysteresis (typ), transient phase-repeat enabled, OPTION = OPEN or GND		-32		-18	mV
NB BUFFER							
NBV_BUF Output Voltage Accuracy	V_{NBV_BUF}	DAC codes from 0.8375V to 1.5500V		-0.4		+0.4	%
		DAC codes from 0.5000V to 0.8250V		-4		+4	mV
		DAC codes below 0.4875V to 0.0125V		-10		+10	
NBV_BUF Short-Circuit Current (Sets Slew Rate Together with External Capacitor C_{NBV_BUF})		DAC code set to 1.2V, V_{NBV_BUF} = 0.4V and 2V	R_{TIME} = 143kΩ, I_{NBV_BUF} = 7.0µA	-10		+10	%
			R_{TIME} = 35.7kΩ to 357kΩ, I_{NBV_BUF} = 28µA to 2.8µA	-15		+15	
GNDS_NB Input Range	V_{GNDS_NB}			-200		+200	mV
GNDS_NB Gain	A_{GNDS_NB}	$\Delta V_{NBV\_BUF}/\Delta V_{GNDS\_NB}$, -200mV ≤ V_{GNDS_NB} ≤ +200mV		0.95	1.00	1.05	V/V
GNDS_NB Input Bias Current	I_{GNDS_NB}			-2		+2	µA
FAULT DETECTION							
Output Overvoltage Trip Threshold	$V_{OVP\_}$	Measured at FBDC_, rising edge	Normal operation	250	300	350	mV
			Output not in regulation after a downward VID transition	1.80	1.85	1.90	V
			Minimum OVP threshold		0.8		
Output Overvoltage Fault-Propagation Delay	t_{OVP}	FBDC_ forced 25mV above trip threshold			10		µs
Output Undervoltage-Protection Trip Threshold	V_{UVP}	Measured at FBDC_ with respect to unloaded output voltage		-450	-400	-350	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Undervoltage Fault-Propagation Delay	t_{UVP}	FBDC_ forced 25mV below trip threshold			10		µs
PWRGD Threshold		Measured at FBDC_ with respect to unloaded output voltage	Lower threshold, falling edge (undervoltage)	-350	-300	-250	V
		15mV hysteresis (typ)	Upper threshold, rising edge (overvoltage)	+150	+200	+250	
PWRGD Propagation Delay	$t_{PWRGD\_}$	FBDC_ forced 25mV outside the PWRGD trip thresholds			10		µs
PWRGD Output Low Voltage		I_{SINK} = 4mA				0.4	V
PWRGD Leakage Current	$I_{PWRGD\_}$	High state, PWRGD forced to 5.5V				1	µA
PWRGD Startup Delay and Transition Blanking Time	t_{BLANK}	Measured from the time when FBDC_ reaches the target voltage based on the slew rate set by R_{TIME}			20		µs
$\overline{VRHOT}$ Trip Threshold		Measured at THRM, with respect to V_{CC}, falling edge, 115mV hysteresis (typ)		29.5	30	30.5	%
$\overline{VRHOT}$ Delay	$t_{\overline{VRHOT}}$	THRM forced 25mV below the $\overline{VRHOT}$ trip threshold, falling edge			10		µs
$\overline{VRHOT}$ Output Low Voltage		I_{SINK} = 4mA				0.4	V
$\overline{VRHOT}$ Leakage Current		High state, $\overline{VRHOT}$ forced to 5V				1	µA
THRM Input Leakage				-100		+100	nA
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = 15°C			160		°C
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V	High state (pullup)		0.9	2.0	Ω
			Low state (pulldown)		0.7	2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	DL_, high state			0.7	2.0	Ω
		DL_, low state			0.25	0.6	
DH_ Gate-Driver Source/Sink Current	$I_{DH\_}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.2		A
DL_ Gate-Driver Source Current	$I_{DL\_}$ (SOURCE)	DL_ forced to 2.5V			2.7		A
DL_ Gate-Driver Sink Current	$I_{DL\_}$ (SINK)	DL_ forced to 2.5V			8		A
Dead Time	t_{DH_DL}	DH_ low to DL_ high		15	25	40	ns
	t_{DL_DH}	DL_ low to DH_ high		9	20	35	
Internal Boost Diode Switch R_{ON}		BST1 to V_{DD1}, BST2 to V_{DD2}; measure with 10mA of current			10	20	Ω

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
2-WIRE SVI BUS LOGIC INTERFACE							
SVI Logic Input Current		SVC, SVD		-1		+1	µA
SVI Logic Input Threshold		SVC, SVD, rising edge, hysteresis = 0.15V_{DDIO}		0.3 x V_{DDIO}		0.7 x V_{DDIO}	V
SVC Clock Frequency	f_{SVC}					3.4	MHz
START Condition Hold Time	$t_{HD,STA}$			160			ns
Repeated START Condition Setup Time	$t_{SU,STA}$			160			ns
STOP Condition Setup Time	$t_{SU,STO}$			160			ns
Data Hold	$t_{HD,DAT}$	A master device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IL} of SCK signal) to bridge the undefined region of SCL's falling edge				70	ns
Data Setup Time	$t_{SU,DAT}$			10			ns
SVC Low Period	t_{LOW}			160			ns
SVC High Period	t_{HIGH}			60			ns
SVC/SVD Rise and Fall Time	t_R, t_F	Measured from 10% to 90% of V_{DDIO}				40	ns
Pulse Width of Spike Suppression		Input filters on SVD and SVC suppress noise spikes less than 50ns			20		ns
INPUTS AND OUTPUTS							
Logic Input Current		$\overline{SHDN}$, PGD_IN		-1		+1	µA
		$\overline{PRO}$, OPTION		-3		+3	
Logic Input Threshold		$\overline{SHDN}$, rising edge, hysteresis = 225mV		0.8		2.0	V
Four-Level Input-Logic Levels		OPTION	High	V_{CC} - 0.4			V
			Open	3.15		3.85	
			REF	1.65		2.35	
			Low			0.4	
Tri-Level Input-Logic Levels		$\overline{PRO}$	High	V_{CC} - 0.4			V
			Open	3.15		3.85	
			Low			0.4	
PGD_IN Logic Input Threshold		PGD_IN		0.3 x V_{DDIO}		0.7 x V_{DDIO}	V
$\overline{NBSKP}$ Logic Output Voltage		Low state, I_{SINK} = 3mA				0.4	V
		High state, I_{SOURCE} = 3mA		V_{CC} - 0.4			

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
INPUT SUPPLIES						
Input Voltage Range	V_{IN}	Drain of external high-side MOSFET		4	26	V
	V_{BIAS}	V_{CC}, V_{DD1}, V_{DD2}		4.5	5.5	
	V_{DDIO}			1.0	2.7	
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	V_{CC} rising 50mV typical hysteresis		4.10	4.45	V
V_{DDIO} Undervoltage-Lockout Threshold		V_{DDIO} rising 100mV typical hysteresis		0.8	0.9	V
Quiescent Supply Current (V_{CC})	I_{CC}	Skip mode, FBDC_ forced above their regulation points			10	mA
Quiescent Supply Currents (V_{DD1}, V_{DD2})	I_{DD1}, I_{DD2}	Skip mode, FBDC_ forced above their regulation points, T_A = -40°C to +85°C			1	µA
Quiescent Supply Current (V_{DDIO})	I_{DDIO}				25	µA
Shutdown Supply Current (V_{CC})		$\overline{SHDN}$ = GND, T_A = -40°C to +85°C			1	µA
Shutdown Supply Currents (V_{DD1}, V_{DD2})		$\overline{SHDN}$ = GND, T_A = -40°C to +85°C			1	µA
Shutdown Supply Current (V_{DDIO})		T_A = -40°C to +85°C			1	µA
Reference Voltage	V_{REF}	V_{CC} = 4.5V to 5.5V, no REF load		1.98	2.02	V
Reference Load Regulation		Sourcing: I_{REF} = 0 to 500µA		-2		mV
		Sinking: I_{REF} = 0 to -100µA			6.2	
MAIN SMPS CONTROLLERS						
DC Output-Voltage Accuracy (Note 1)	V_{OUT}	DAC codes from 0.8375V to 1.5500V		-0.6	+0.6	%
		DAC codes from 0.5000V to 0.8250V		-6	+6	mV
		DAC codes from 0.4875V to 0.0125V		-15	+15	
GNDS_ Input Range	$V_{GNDS\_}$	Separate mode		-200	+200	mV
GNDS_ Gain	$A_{GNDS\_}$	Separate: $\Delta V_{OUT\_}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV, Combined: $\Delta V_{OUT}/\Delta V_{GNDS1}$, -200mV ≤ V_{GNDS1} ≤ +200mV		0.95	1.05	V/V
Combined-Mode Detection Threshold		GNDS2, detection after REFOK, latched, cleared by cycling $\overline{SHDN}$		0.7	0.9	V
Switching-Frequency Accuracy	f_{OSC}	R_{OSC} = 143kΩ (f_{OSC} = 300kHz nominal)		-7.5	+7.5	%
		R_{OSC} = 35.7kΩ (f_{OSC} = 1.2MHz nominal) to 432kΩ (f_{OSC} = 99kHz nominal)		-10	+10	
Maximum Duty Factor	DMAX			90		%
Minimum On-Time	t_{ONMIN}				185	ns
TIME Slew-Rate Accuracy		During transition	R_{TIME} = 143kΩ, SR = 6.25mV/µs	-10	+10	%
			R_{TIME} = 35.7kΩ to 357kΩ, SR = 25mV/µs to 2.5mV/µs	-15	+15	

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
CURRENT LIMIT						
Current-Limit Threshold Tolerance	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$ = 0.05 x (V_{REF} - V_{ILIM}), (V_{REF} - V_{ILM}) = 0.2V to 1.0V		-3	+3	mV
Idle Mode Threshold Tolerance	V_{IDLE}	$V_{CSP\_}$ - $V_{CSN\_}$, SKIP mode, 0.15 x V_{LIMIT}		-1.5	+1.5	mV
CS_ Common-Mode Input Range		CSP_ and CSN_		0	2	V
Phase Disable Threshold		CSP2		3	V_{CC} - 0.4	V
DROOP AND CURRENT BALANCE						
DC Droop Amplifier Transconductance	$G_{m(FBDC\_)}$	$\Delta I_{FBDC\_}/(\Delta V_{CS\_})$, $V_{FBDC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = -60mV to +60mV		0.97	1.03	mS
DC Droop Amplifier Offset		$I_{FBDC\_}/G_{m(FBDC\_)}$		-1.5	+1.5	mV
AC Droop and Current-Balance Amplifier Transconductance	$G_{m(FBAC\_)}$	$\Delta I_{FBAC\_}/(\Delta V_{CS\_})$, $V_{FBAC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = -60mV to +60mV		0.97	1.03	mS
AC Droop and Current-Balance Amplifier Offset		$I_{FBAC\_}/G_{m(FBAC\_)}$		-1.5	+1.5	mV
Transient-Detection Threshold		Measured at FBDC_ with respect to steady-state FBDC_ regulation voltage, 5mV hysteresis (typ), transient phase repeat enabled, OPTION = OPEN or GND		-32	-18	mV
NB BUFFER						
NBV_BUF Output-Voltage Accuracy	V_{NBV_BUF}	DAC codes from 0.8375V to 1.5500V		-0.6	+0.6	%
		DAC codes from 0.5000V to 0.8250V		-6	+6	mV
		DAC codes from 0.4875V to 0.0125V		-15	+15	
NBV_BUF Short-Circuit Current (Sets Slew Rate Together with External Capacitor C_{NBV_BUF})		DAC code set to 1.2V, V_{NBV_BUF} = 0.4V and 2V	R_{TIME} = 143kΩ, I_{NBV_BUF} = 7.0µA	-10	+10	%
			R_{TIME} = 35.7kΩ to 357kΩ, I_{NBV_BUF} = 28µA to 2.8µA	-15	+15	
GNDS_NB Input Range	V_{GNDS_NB}			-200	+200	mV
GNDS_NB Gain	A_{GNDS_NB}	$\Delta V_{NBV\_BUF}/\Delta V_{GNDS\_NB}$, -200mV ≤ V_{GNDS_NB} ≤ +200mV		0.95	1.05	V/V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
FAULT DETECTION						
Output Overvoltage Trip Threshold	$V_{OVP\_}$	Measured at FBDC_, rising edge	Normal operation	250	350	mV
Output Undervoltage-Protection Trip Threshold	V_{UVP}	Measured at FBDC_ with respect to unloaded output voltage		-450	-350	mV
PWRGD Threshold		Measured at FBDC_ with respect to unloaded output voltage	Lower threshold, falling edge (undervoltage)	-350	-250	V
		15mV hysteresis (typ)	Upper threshold, rising edge (overvoltage)	+150	+250	
PWRGD Output Low Voltage		I_{SINK} = 4mA			0.4	V
$\overline{VRHOT}$ Trip Threshold		Measured at THRM, with respect to V_{CC}, falling edge, 115mV hysteresis (typ)		29.5	30.5	%
$\overline{VRHOT}$ Output Low Voltage		I_{SINK} = 4mA			0.4	V
GATE DRIVERS						
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V	High state (pullup)		2.0	Ω
			Low state (pulldown)		2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	DL_, high state			2.0	Ω
		DL_, low state			0.6	
Dead Time	t_{DH_DL}	DH_ low to DL_ high		15	40	ns
	t_{DL_DH}	DL_ low to DH_ high		9	40	
Internal Boost Diode Switch R_{ON}		BST1 to V_{DD1}, BST2 to V_{DD2}, measured with 10mA of current			20	Ω
2-WIRE SVI BUS LOGIC INTERFACE						
SVI Logic Input Threshold		SVC, SVD, rising edge, hysteresis = 0.15 x V_{DDIO}		0.3 x V_{DDIO}	0.7 x V_{DDIO}	V
SVC Clock Frequency	f_{SVC}				3.4	MHz
START Condition Hold Time	$t_{HD,STA}$			160		ns
Repeated START Condition Setup Time	$t_{SU,STA}$			160		ns
STOP Condition Setup Time	$t_{SU,STO}$			160		ns
Data Hold	$t_{HD,DAT}$	A master device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IL} of SCK signal) to bridge the undefined region of SCL's falling edge			70	ns
Data Setup Time	$t_{SU,DAT}$			10		ns
SVC Low Period	t_{LOW}			160		ns
SVC High Period	t_{HIGH}			60		ns
SVC/SVD Rise and Fall Time	t_R, t_F	Measured from 10% to 90% of V_{DDIO}			40	ns

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD1} = V_{DD2} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, $\overline{PRO}$ = OPTION = GNDS_NB = GNDS_ = GND_, FBDC_ = FBAC_ = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
INPUTS AND OUTPUTS						
Logic Input Threshold		$\overline{SHDN}$, rising edge, hysteresis = 225mV		0.8	2.0	V
Four-Level Input Logic Levels		OPTION	High	V_{CC} - 0.4		V
			Open	3.15	3.85	V
			REF	1.65	2.35	
			Low		0.4	
Tri-Level Input Logic Levels		$\overline{PRO}$	High	V_{CC} - 0.4		V
			Open	3.15	3.85	
			Low		0.4	
PGD_IN Logic Input Threshold		PGD_IN		0.3 x V_{DDIO}	0.7 x V_{DDIO}	V

Note 1: When the inductor is in continuous conduction, the output voltage has a DC regulation level lower than the error comparator threshold by 50% of the ripple. In discontinuous conduction, the output voltage will have a DC regulation level higher than the error comparator threshold by 50% of the ripple.

Note 2: Specifications to T_A = -40°C to +105°C are guaranteed by design, not production tested.

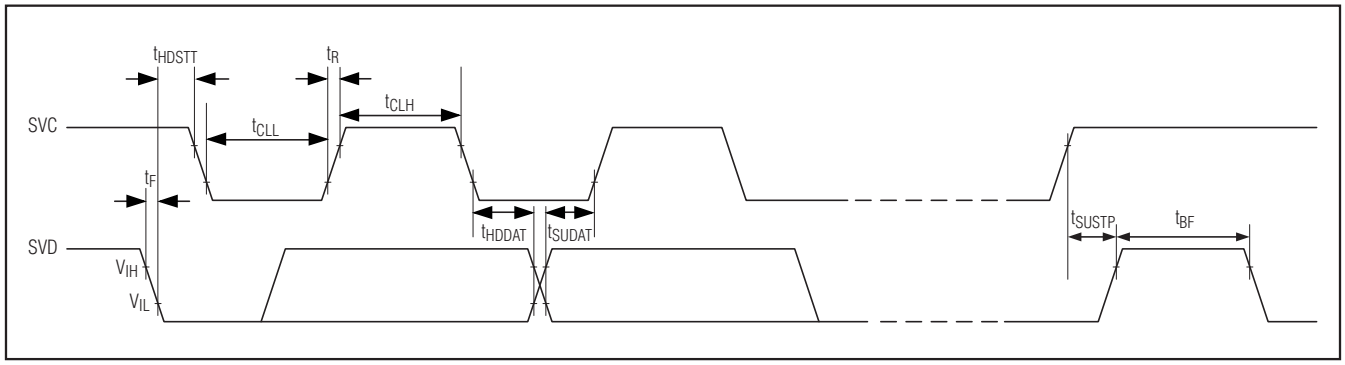
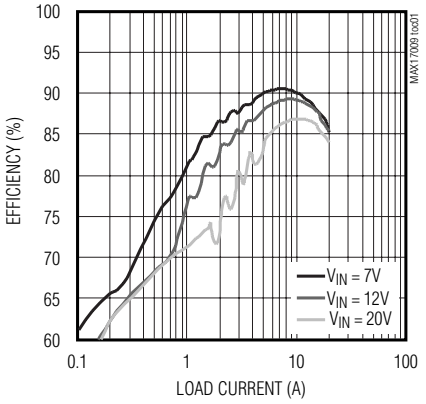


Figure 1. Timing Definitions Used in the Electrical Characteristics

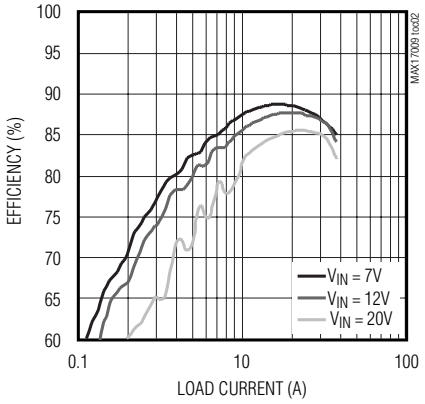
Typical Operating Characteristics

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

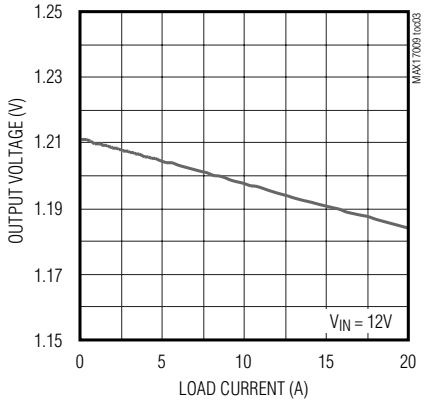
1-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.2125V)



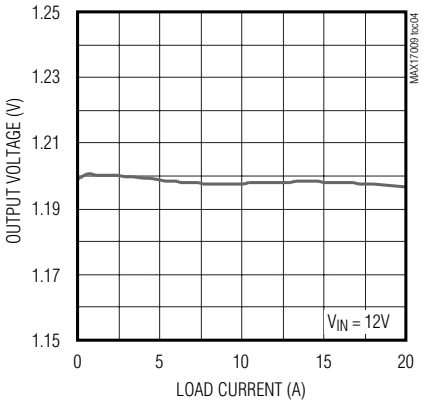
2-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.2125V)



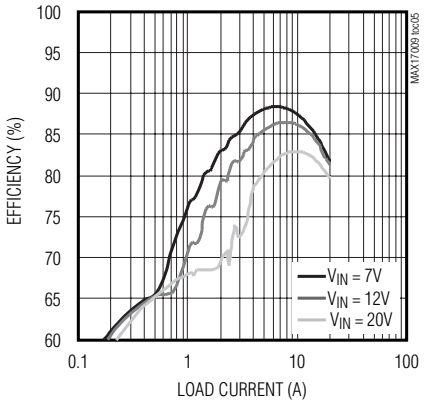
1-PHASE OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.2125V, -1.2mV/A DROOP)



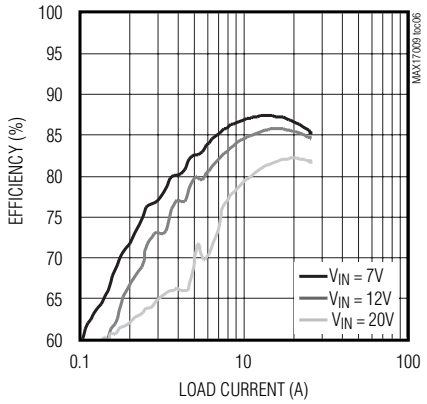
1-PHASE OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.2000V, NO DROOP)



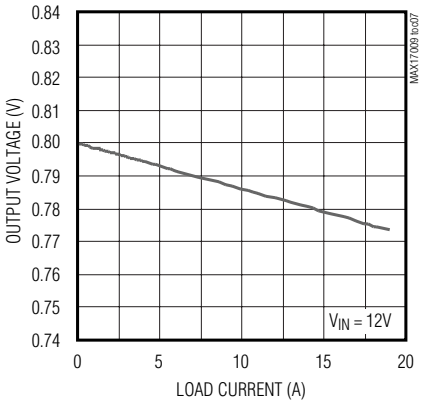
1-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.8000V)



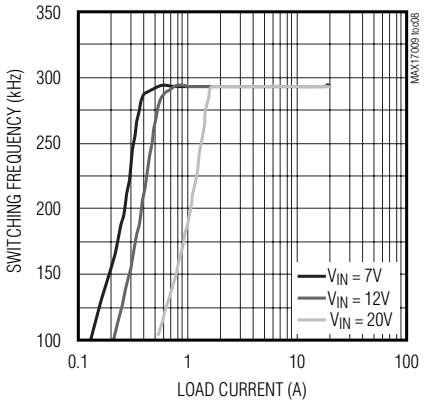
2-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.8000V)



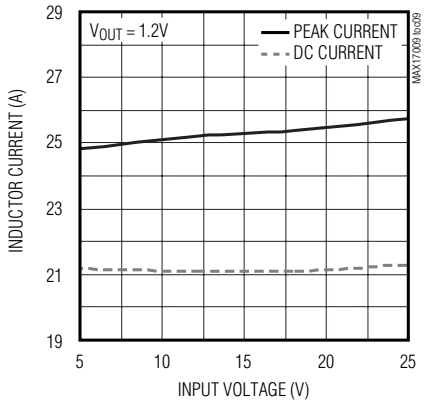
1-PHASE OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 0.8000V, -1.2mV/A DROOP)



1-PHASE SWITCHING FREQUENCY vs. LOAD CURRENT



MAXIMUM INDUCTOR CURRENT vs. INPUT VOLTAGE

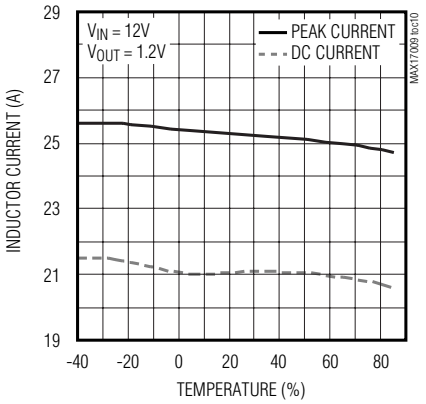


AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

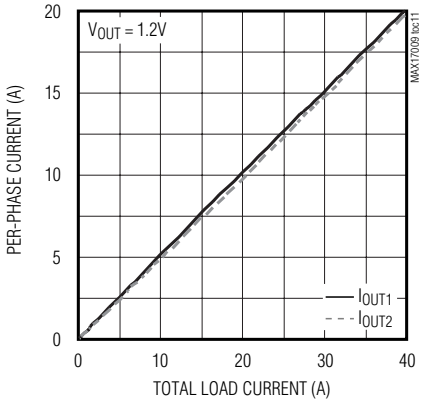
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

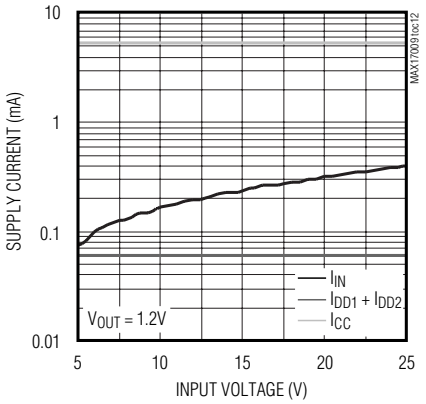
MAXIMUM INDUCTOR CURRENT vs. TEMPERATURE



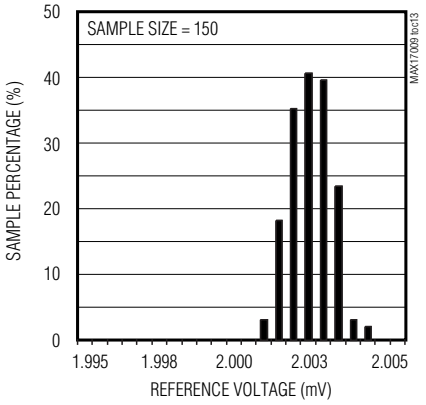
CURRENT BALANCE vs. LOAD CURRENT



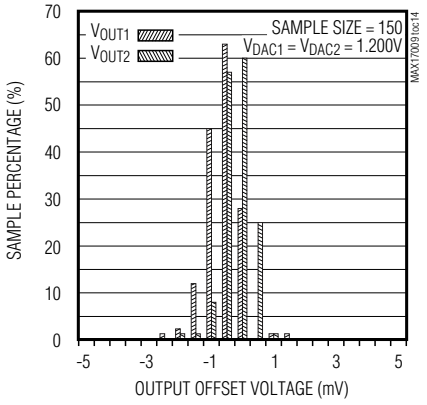
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



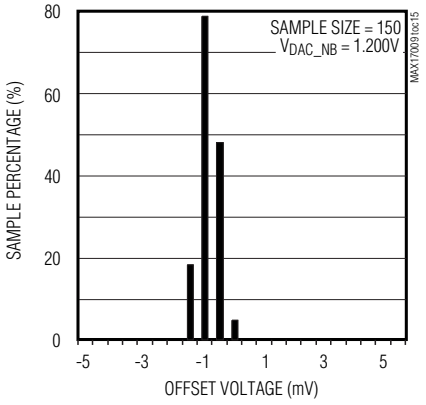
REFERENCE VOLTAGE DISTRIBUTION



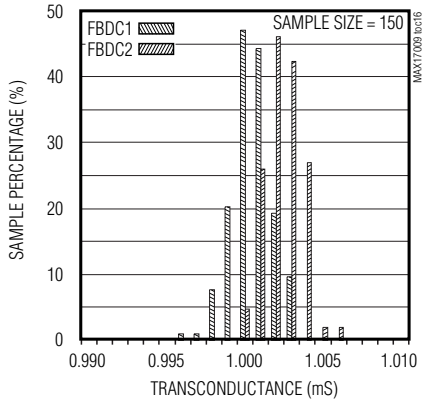
SMPS OUTPUT OFFSET VOLTAGE DISTRIBUTION



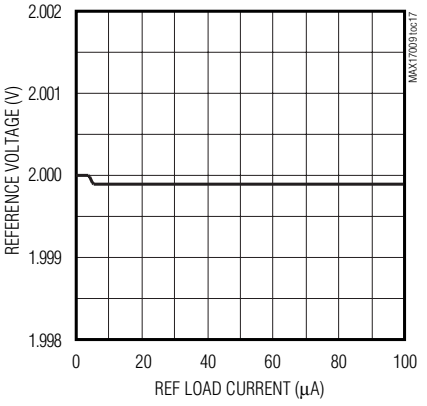
NBV_BUF OFFSET VOLTAGE DISTRIBUTION



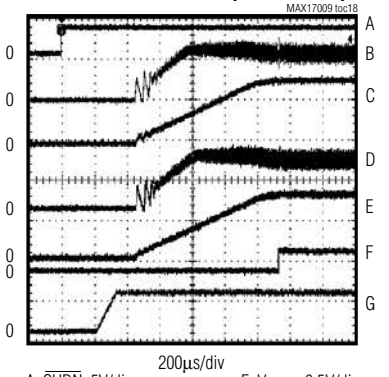
FBDC TRANSCONDUCTANCE DISTRIBUTION



REFERENCE VOLTAGE vs. LOAD CURRENT



STARTUP WAVEFORMS (HEAVY LOAD)



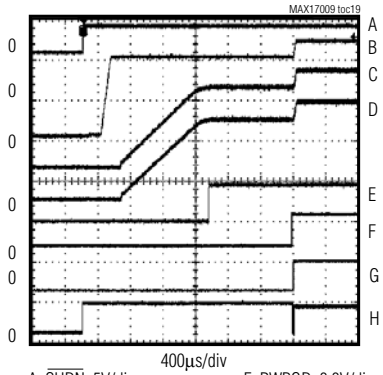
A. $\overline{SHDN}$, 5V/div
B. I_{LX1}, 10A/div
C. V_{OUT1}, 0.5V/div
D. I_{LX2}, 10A/div
E. V_{OUT2}, 0.5V/div
F. PWRGD, 5V/div
G. V_{NBV_BUF}, 0.5V/div

V_{IN} = 12V, V_{BOOT} = 0.8V, I_{LOAD1} = I_{LOAD2} = 12A

Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

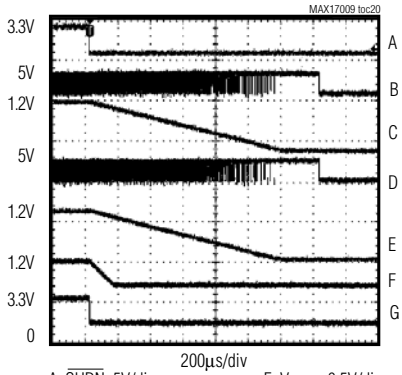
STARTUP SEQUENCE WAVEFORMS



A. $\overline{SHDN}$, 5V/div
B. V_{NBV_BUF}, 0.5V/div
C. V_{OUT1}, 0.5V/div
D. V_{OUT2}, 0.5V/div
E. PWRGD, 3.3V/div
F. PGD_IN, 3.3V/div
G. SVC, 2V/div
H. SVD, 2V/div

V_{IN} = 12V, V_{BOOT} = 1.0V, I_{LOAD1} = I_{LOAD2} = 3A

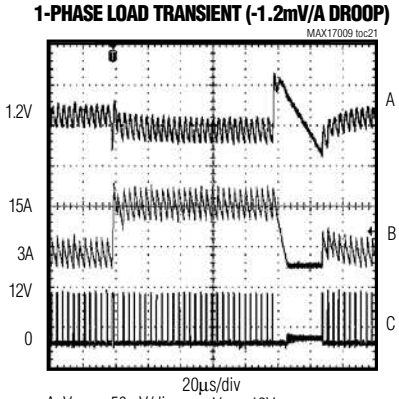
SHUTDOWN WAVEFORMS



A. $\overline{SHDN}$, 5V/div
B. DL1, 10V/div
C. V_{OUT1}, 0.5V/div
D. DL2, 10V/div
E. V_{OUT2}, 0.5V/div
F. V_{NBV_BUF}, 2V/div
G. PWRGD, 5V/div

V_{IN} = 12V, I_{LOAD1} = I_{LOAD2} = 3A

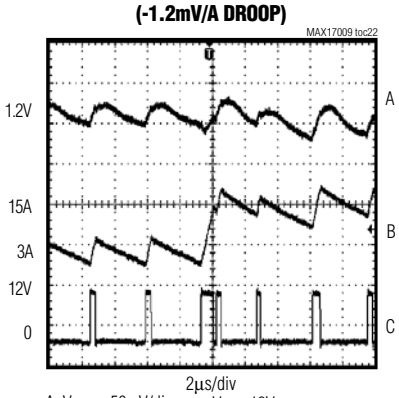
1-PHASE LOAD TRANSIENT (-1.2mV/A DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. LX1, 10V/div

V_{IN} = 12V
I_{LOAD1} = 3A TO 15A TO 3A

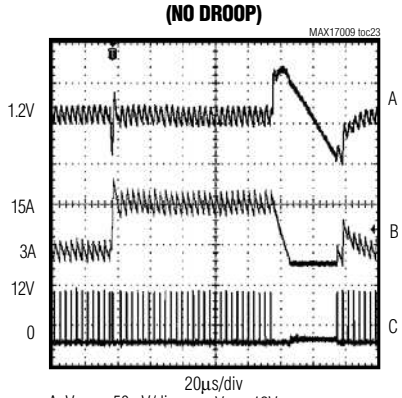
1-PHASE TRANSIENT PHASE REPEAT (-1.2mV/A DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. LX1, 10V/div

V_{IN} = 12V
I_{LOAD1} = 3A TO 15A TO 3A

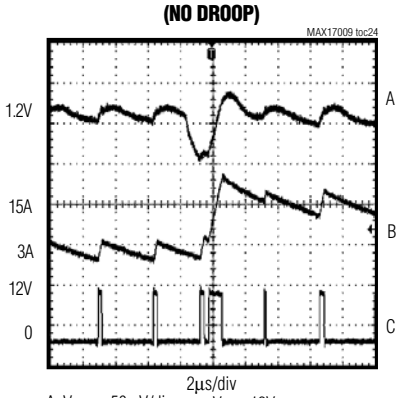
1-PHASE LOAD TRANSIENT (NO DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. LX1, 10V/div

V_{IN} = 12V
I_{LOAD1} = 3A TO 15A TO 3A

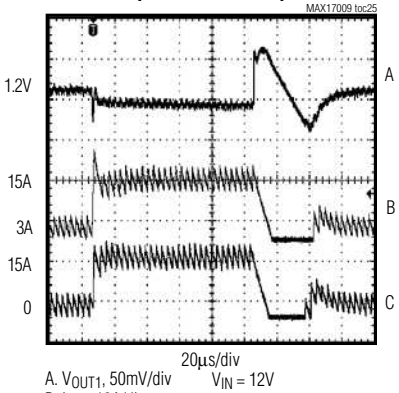
1-PHASE TRANSIENT PHASE REPEAT (NO DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. LX1, 10V/div

V_{IN} = 12V
I_{LOAD1} = 3A TO 15A TO 3A

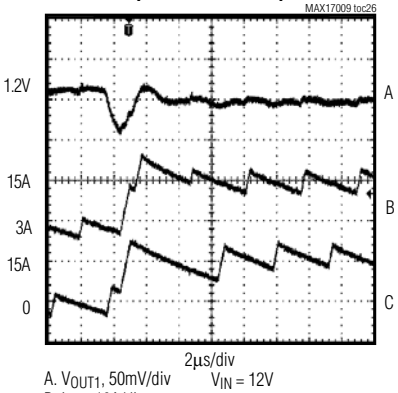
2-PHASE LOAD TRANSIENT (-1.2mV/A DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. I_{LX2}, 10A/div

V_{IN} = 12V
I_{LOAD} = 6A TO 30A TO 6A

2-PHASE TRANSIENT PHASE REPEAT (-1.2mV/A DROOP)



A. V_{OUT1}, 50mV/div
B. I_{LX1}, 10A/div
C. I_{LX2}, 10A/div

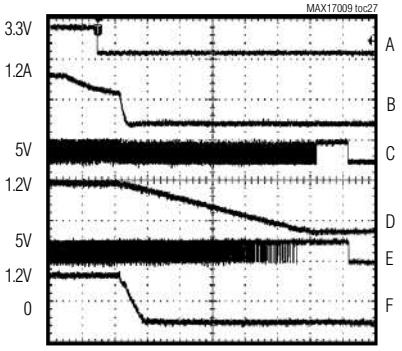
V_{IN} = 12V
I_{LOAD} = 6A TO 30A TO 6A

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

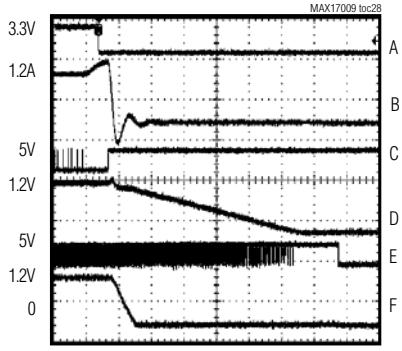
1-PHASE OUTPUT OVERLOAD



A. PWRGD, 5V/div
B. V_{OUT1}, 1V/div
C. DL1, 10V/div
D. V_{OUT2}, 1V/div
E. DL2, 10V/div
F. V_{NBV_BUF}, 1V/div

V_{IN} = 12V, I_{LOAD1} = 3A TO 30A, I_{LOAD2} = 3A

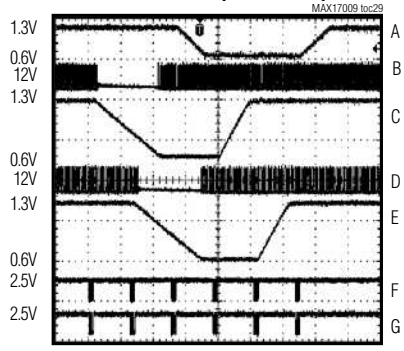
1-PHASE OUTPUT OVERVOLTAGE



A. PWRGD, 5V/div
B. V_{OUT1}, 1V/div
C. DL1, 10V/div
D. V_{OUT2}, 1V/div
E. DL2, 10V/div
F. V_{NBV_BUF}, 1V/div

V_{IN} = 12V, I_{LOAD1} = 50mA, I_{LOAD2} = 3A

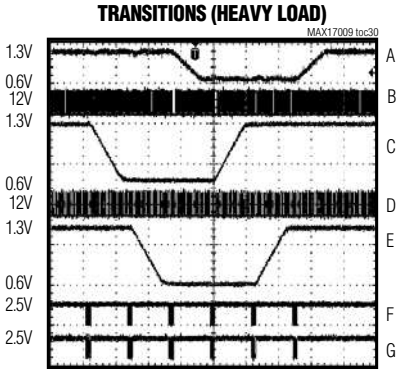
DYNAMIC OUTPUT-VOLTAGE TRANSITIONS (LIGHT LOAD)



A. V_{NBV_BUF}, 1V/div
B. LX1, 20V/div
C. V_{OUT1}, 0.5V/div
D. LX2, 20V/div
E. V_{OUT2}, 0.5V/div
F. SVC, 5V/div
G. SVD, 5V/div

V_{IN} = 12V, V_{DACS} = 1.3V TO 0.6V TO 1.3V,
I_{LOAD1} = I_{LOAD2} = 3A

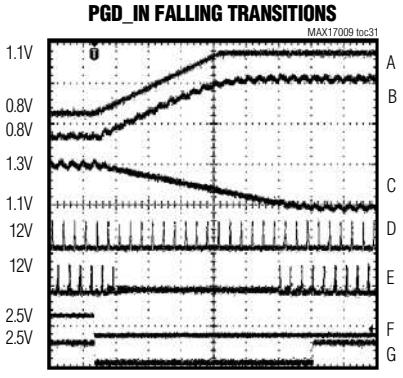
DYNAMIC OUTPUT-VOLTAGE TRANSITIONS (HEAVY LOAD)



A. V_{NBV_BUF}, 1V/div
B. LX1, 20V/div
C. V_{OUT1}, 0.5V/div
D. LX2, 20V/div
E. V_{OUT2}, 0.5V/div
F. SVC, 5V/div
G. SVD, 5V/div

V_{IN} = 12V, V_{DACS} = 1.3V TO 0.6V TO 1.3V,
I_{LOAD1} = I_{LOAD2} = 10A

PGD_IN FALLING TRANSITIONS



A. V_{NBV_BUF}, 200mV/div
B. V_{OUT1}, 200mV/div
C. V_{OUT2}, 200V/div
D. LX1, 20V/div
E. LX2, 20V/div
F. PGD_IN, 5V/div
G. PWRGD, 5V/div

V_{IN} = 12V, V_{BOOT} = 1.1V, V_{DAC1} = 0.8V, V_{DAC2} = 1.3V,
V_{NBV_BUF} = 0.8V, I_{LOAD1} = I_{LOAD2} = 3A

Pin Description

<table>
<tr><th>PIN</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>1</td><td>PWRGD</td><td>Open-Drain, Power-Good Output. PWRGD indicates when both SMPSs are in regulation.
PWRGD is forced high impedance whenever the slew-rate controller is active (output-voltage transitions). After output-voltage transitions, except during power-up and power-down, if FBDC_ is in regulation, then PWRGD is high impedance.
During startup, PWRGD is held low an additional 20µs after the MAX17009 reaches the startup boot voltage set by the SVC, SVD pins. The MAX17009 stores the boot VID when PWRGD first goes high. The stored boot VID is cleared by rising $\overline{SHDN}$.
PWRGD is forced low in shutdown.
When in pulse-skipping mode, the upper PWRGD threshold comparator is blanked during a lower VID transition. The upper PWRGD threshold comparator is reenabled once the output is in regulation (Figure 4).</td></tr>
<tr><td>2</td><td>NBV_BUF</td><td>North Bridge Buffered Reference Voltage. This output is connected to the REFIN input of the NB controller (switcher or LDO) to set the NB regulator voltage. The NBV_BUF output current is set by the TIME resistor. The NBV_BUF current and the total output capacitance set the NBV_BUF slew rate:
$I_{NBV\_BUF} = (7\mu A) \times (143k\Omega / R_{TIME})$
NBV_BUF Slew rate = $I_{NBV\_BUF} / C_{NBV\_BUF}$
I_{NBV_BUF} is the same during startup, shutdown, and any VID transition.
Bypass to GND with a 100pF minimum low-ESR (ceramic) capacitor at the NBV_BUF pin.</td></tr>
<tr><td>3</td><td>$\overline{SHDN}$</td><td>Shutdown Control Input. Connect high (2V to V_{CC}) for normal operation. Connect to ground to put the IC into its 1µA max shutdown state.
During startup, the SMPS output voltages and the NBV_BUF voltage are ramped up to the voltage set by the SVC, SVD inputs. The SMPSs start up and shut down at a fixed slew rate of 1mV/µs.
<table>
<tr><th>SVC</th><th>SVD</th><th>BOOT VOLTAGE (V_{BOOT}) ($\overline{PRO}$ = V_{CC} OR GND)</th><th>BOOT VOLTAGE (V_{BOOT}) ($\overline{PRO}$ = OPEN)</th></tr>
<tr><td>0</td><td>0</td><td>1.1</td><td>1.1</td></tr>
<tr><td>0</td><td>1</td><td>1.0</td><td>1.2</td></tr>
<tr><td>1</td><td>0</td><td>0.9</td><td>1.0</td></tr>
<tr><td>1</td><td>1</td><td>0.8</td><td>0.8</td></tr>
</table>
The MAX17009 stores the boot VID when PWRGD first goes high. The stored boot VID is cleared by rising $\overline{SHDN}$.</td></tr>
<tr><td>4</td><td>REF</td><td>2.0V Reference Output. Bypass to GND with a 1µF maximum low-ESR (ceramic) capacitor. REF sources up to 500µA for external loads. Loading REF degrades output accuracy, according to the REF load-regulation error.</td></tr>
<tr><td>5</td><td>ILIM</td><td>Current-Limit Adjust Input. The positive current-limit threshold voltage is precisely 1/20 of the voltage between REF and ILIM over a 0.2V to 1.0V range of V(REF, ILIM). The I_{MIN} minimum current-limit threshold voltage in skip mode is precisely 15% of the corresponding positive current-limit threshold voltage.</td></tr>
<tr><td>6</td><td>OSC</td><td>Oscillator Adjustment Input. Connect a resistor (R_{OSC}) between OSC and GND to set the switching frequency (per phase):
$f_{OSC} = 300kHz \times 143k\Omega / R_{OSC}$
A 35.7kΩ to 432kΩ corresponds to switching frequencies of 1.2MHz to 100kHz, respectively. Switching-frequency selection is limited by the minimum on-time. See the Switching frequency bullet in the SMPS Design Procedure section.</td></tr>
</table>

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

Pin Description (continued)

PIN	NAME	FUNCTION
7	TIME	Slew-Rate Adjustment Pin. Connect a resistor R_{TIME} from TIME to GND to set the internal slew rate: PWM Slew rate = (6.25mV/µs) x (143kΩ / R_{TIME}) NBV_BUF Slew rate = (7µA) x (143kΩ / R_{TIME}) / C_{NBV_BUF} where R_{TIME} is between 35.7kΩ and 357kΩ for corresponding slew rates between 25mV/µs to 2.5mV/µs, respectively, for the SMPSs, and NBV_BUF currents between 28µA and 2.8µA, respectively, for the NBV_BUF. This slew rate applies to both upward and downward VID transitions, and to the transition from boot mode to VID mode. Downward VID transition slew rate can appear slower because the output transition is not forced by the SMPS. The SMPS slew rate for startup and shutdown is fixed at 1mV/µs. The NBV_BUF slew rate is the same during startup, shutdown, and normal VID transitions.
8	SVC	Serial VID Clock. During the power-up sequence and in debug mode, SVC is the MSB of the 2-bit VID DAC.
9	SVD	Serial VID Data. During the power-up sequence and in debug mode, SVD is the LSB of the 2-bit VID DAC.
10	THRM	Input of Internal Comparator. Connect the output of a resistor- and thermistor-divider (between V_{CC} and GND) to THRM. Select the components so the voltage at THRM falls below 1.5V (30% of V_{CC}) at the desired high temperature.
11	GNDS2	SMPS2 Remote Ground-Sense Input. Normally connected to GND directly at the load. GNDS2 internally connects to a transconductance amplifier that fine tunes the output voltage compensating for voltage drops from the regulator ground to the load ground. Connect GNDS2 above 0.9V combined-mode operation (unified core). When operating in combined mode, GNDS1 is used as the remote ground-sense input.
12	FBDC2	Output of the DC Voltage-Positioning Transconductance Amplifier for SMPS2. Connect a resistor R_{FBDC2} between FBDC2 and the positive side of the feedback remote sense to set the DC steady-state droop based on the voltage-positioning gain requirement: $R_{FBDC2} = R_{DROOPDC} / (R_{SENSE2} \times G_{m(FBDC2)})$ where $R_{DROOPDC}$ is the desired voltage positioning slope and $G_{m(FBDC2)}$ = 1mS typ. R_{SENSE2} is the value of the current-sense resistor that is used to provide the (CSP2, CSN2) current-sense voltage. To disable the load-line, short FBDC2 to the positive remote-sense point. FBDC2 is high impedance in shutdown.
13	FBAC2	Output of the AC Voltage-Positioning Transconductance Amplifier for SMPS2. The resistance between this pin and the positive side of the remote-sensed output voltage sets the transient AC droop: $R_{FBAC2} = R_{DROOPAC} / (R_{SENSE2} \times G_{m(FBAC2)})$ where $R_{DROOPAC}$ is the transient (AC) voltage-positioning slope that provides an acceptable tradeoff between stability and load transient response, $G_{m(FBAC2)}$ and R_{SENSE2} is the value of the current-sense resistor that is used to provide the (CSP2, CSN2) current-sense voltage. The maximum difference between transient (AC) droop and DC droop should not exceed ±80mV at the maximum allowed load current (DC droop is set at the FBDC2 pin). Internally, V(FBDC2 - GNDS2) goes to the internal voltage integrator (slow DC loop), whereas V(FBAC2 - GNDS2) goes to the error comparator (fast transient loop). FBAC2 is high impedance in shutdown. **Note:** The AC and DC droop cannot be different by more than ±3mV/A.
14	V_{DDIO}	CPU I/O Voltage (1.8V or 1.5V). Logic thresholds for SVD and SVC are relative to the voltage at V_{DDIO}.
15	GNDS_NB	North Bridge Feedback Remote-Sense Input, Negative Side. Normally connected to GND directly at the load. GNDS_NB internally connects to a transconductance amplifier that fine tunes the NBV_BUF output voltage compensating for voltage drops from the regulator ground to the load ground.

Pin Description (continued)

PIN	NAME	FUNCTION
16	CSN2	Negative Current-Sense Input for SMPS2. Connect to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
17	CSP2	Positive Current-Sense Input for SMPS2. Connect to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. Connect CSP2 to V_{CC} to disable SMPS2. This allows the MAX17009 to operate as a 1-phase regulator.
18	V_{CC}	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with 1µF minimum. A V_{CC} UVLO event that occurs while the IC is functioning is latched, and can only be cleared by cycling V_{CC} power or by toggling $\overline{SHDN}$.
19	$\overline{NBSKP}$	North Bridge Skip Push-Pull Control Output. When $\overline{NBSKP}$ is high, the NB switching regulator is set to forced-PWM mode. When $\overline{NBSKP}$ is low, the NB switching regulator is set to pulse-skipping mode. The $\overline{NBSKP}$ level is set through the serial interface during normal operation. $\overline{NBSKP}$ is high in shutdown and during soft-shutdown. $\overline{NBSKP}$ is high in startup until commanded otherwise.
20	DH2	SMPS2 High-Side, Gate-Driver Output. DH2 swings from LX2 to BST2. Low in shutdown.
21	LX2	SMPS2 Inductor Connection. LX2 is the internal lower supply rail for the DH2 high-side gate driver. Also used as an input to phase 2's zero-crossing comparator.
22	BST2	Boost Flying-Capacitor Connection for the DH2 High-Side Gate Driver. An internal switch between V_{DD2} and BST2 charges the flying capacitor during the time the low-side FET is on.
23	V_{DD2}	Supply Voltage Input for the DL2 Driver. V_{DD2} is also the supply voltage used to internally recharge the BST2 flying capacitor during the off-time of phase 2. Connect V_{DD2} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD2} to GND with a 1µF or greater ceramic capacitor.
24	DL2	SMPS2 Low-Side Gate-Driver Output. DL2 swings from GND2 to V_{DD2}. DL2 is forced low in shutdown. DL2 is also forced high when an output overvoltage fault is detected. DL2 is forced low in skip mode after an inductor current zero crossing (GND2 - LX2) is detected.
25	GND2	Power Ground for SMPS2. Ground connection for the DL2 driver. Also used as an input to SMPS2's zero-crossing comparator. GND1 and GND2 are internally connected.
26	GND1	Power Ground for SMPS1. Ground connection for the DL1 driver. Also used as an input to SMPS1's zero-crossing comparator. GND1 and GND2 are internally connected.
27	DL1	SMPS1 Low-Side, Gate-Driver Output. DL1 swings from GND1 to V_{DD1}. DL1 is forced low in shutdown. DL1 is also forced high when an output overvoltage fault is detected. DL1 is forced low in skip mode after an inductor current zero crossing (GND1 - LX1) is detected.
28	V_{DD1}	Supply Voltage Input for the DL1 Driver. V_{DD1} is also the supply voltage used to internally recharge the BST1 flying capacitor during the off-time of phase 1. Connect V_{DD1} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD1} to GND with a 1µF or greater ceramic capacitor.
29	BST1	Boost Flying-Capacitor Connection for the DH1 High-Side Gate Driver. An internal switch between V_{DD1} and BST1 charges the flying capacitor during the time the low-side FET is on.
30	LX1	SMPS1 Inductor Connection. LX1 is the internal lower supply rail for the DH1 high-side gate driver. Also used as an input to phase 1's zero-crossing comparator.
31	DH1	SMPS1 High-Side, Gate-Driver Output. DH1 swings from LX1 to BST1. Low in shutdown.
32	$\overline{VRHOT}$	Open-Drain Output of Internal Comparator. $\overline{VRHOT}$ is pulled low when the voltage at THRM goes below 1.5V (30% of V_{CC}). $\overline{VRHOT}$ is high impedance in shutdown.

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Pin Description (continued)

PIN	NAME	FUNCTION
33	$\overline{PRO}$	Protection Disable. $\overline{PRO}$ also sets the MAX17009 in debug mode. Connect $\overline{PRO}$ high to disable OVP protection. Connect $\overline{PRO}$ to GND to enable OVP protection. When $\overline{PRO}$ is floated, the MAX17009 disables the OVP protection and also enters debug mode (see the $\overline{SHDN}$ pin description). When PGD_IN is low in debug mode, the MAX17009 DAC voltages are set by the 2-bit boot VID. When PGD_IN is high, the MAX17009 changes to serial VID mode.
34	CSP1	Positive Current-Sense Input for SMPS1. Connect to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
35	CSN1	Negative Current-Sense Input for SMPS1. Connect to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
36	PGD_IN	System Power-Good Input. Indicates to the MAX17009 that the system is ready to enter serial VID mode. PGD_IN is low when $\overline{SHDN}$ first goes high, the MAX17009 decodes the boot VID to determine the boot voltage. The boot VID can be changed dynamically while PGD_IN remains low and PWRGD. The boot VID is stored after PWRGD goes high. PGD_IN goes high after the MAX17009 reaches the boot voltage. This indicates that the SVI block is active, and the MAX17009 starts to respond to the serial-interface commands. After PGD_IN has gone high, if at anytime PGD_IN should go low, the MAX17009 regulates to the previously stored boot VID.
37	OPTION	Four-Level Input to Enable Offset and Transient-Phase Repeat **OPTION** / **OFFSET ENABLED** / **TRANSIENT-PHASE REPEAT ENABLED** V_{CC} / 0 / 0 OPEN / 0 / 1 REF / 1 / 0 GND / 1 / 1 When OFFSET is enabled, the MAX17009 enables a fixed +12.5mV offset on each of the SMPS VID codes after PGD_IN goes high. This configuration is intended for applications that implement a load-line. An external resistor at FBDC_ sets the load-line. The offset can be disabled by setting the PSI_L bit to zero through the serial interface. When OFFSET is disabled, the intended application has no load-line, and the FBDC_ pins are directly connected to the remote-sense points. Transient phase repeat allows the MAX17009 to reenable the current phase in response to a load transient, even after that phase has finished its on-pulse.
38	FBAC1	Output of the AC Voltage-Positioning Transconductance Amplifier for SMPS1. The resistance between this pin and the positive side of the remote-sensed output voltage sets the transient AC droop: $R_{FBAC1} = R_{DROOPAC} / (R_{SENSE1} \times G_{m(FBAC1)})$ where $R_{DROOPAC}$ is the transient (AC) voltage-positioning slope that $\overline{PRO}$vides an acceptable tradeoff between stability and load-transient response, $G_{m(FBAC1)}$ and R_{SENSE1} is the value of the current-sense resistor that is used to $\overline{PRO}$vide the (CSP1, CSN1) current-sense voltage. The maximum difference between transient (AC) droop and DC droop should not exceed ±80mV at the maximum allowed load current (DC droop is set at the FBDC2 pin). Internally, V(FBDC1 - GNDS1) goes to the internal voltage integrator (slow DC loop), whereas V(FBAC1 - GNDS1) goes to the error comparator (fast-transient loop). FBAC1 is high impedance in shutdown. **Note:** The AC and DC droop cannot be different by more than ±3mV/A.

Pin Description (continued)

PIN	NAME	FUNCTION
39	FBDC1	Output of the DC Voltage-Positioning Transconductance Amplifier for SMPS1. Connect a resistor R_{FBDC1} between FBDC1 and the positive side of the feedback remote sense to set the DC steady-state droop based on the voltage-positioning gain requirement: $R_{FBDC1} = R_{DROOPDC} / (R_{SENSE1} \times G_{m(FBDC1)})$ where $R_{DROOPDC}$ is the desired voltage-positioning slope and $G_{m(FBDC1)}$ = 1mS typ. R_{SENSE1} is the value of the current-sense resistor that is used to $\overline{PRO}$vide the (CSP1, CSN1) current-sense voltage. To disable the load-line, short FBDC2 to the positive remote-sense point. FBDC1 is high impedance in shutdown.
40	GNDS1	SMPS1 Remote Ground-Sense Input. Normally connected to GND directly at the load. GNDS1 internally connects to a transconductance amplifier that fine tunes the output voltage compensating for voltage drops from the regulator ground to the load ground. GNDS1 is the remote ground-sense input in combined-mode operation.
EP	EP	Exposed Pad. Connect the exposed backside pad to GND1 and GND2.

Table 1 shows the component selection for standard applications and Table 2 lists component suppliers.

Table 1. Component Selection for Standard Applications

COMPONENT	V_{IN} = 7V TO 20V V_{OUT} = 1.0V - 1.3V / 18A PER PHASE	V_{IN} = 4.5V TO 14V $V_{OUT\_}$ = 1.0V - 1.3V / 18A PER PHASE
MODE	Separate, 2-phase mobile (GNDS2 not high)	Separate, 2-phase mobile (GNDS2 not high)
Switching Frequency	280kHz (R_{OSC} = 154kΩ)	600kHz (R_{OSC} = 71.5kΩ)
$C_{IN\_}$, Input Capacitor (per Phase)	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(2) 10µF, 16V Taiyo Yuden TMK432BJ106KM
$C_{OUT\_}$, Output Capacitor (per Phase)	(2) 470µF, 2V, 6mΩ, low-ESR capacitor NEC/Tokin PSGD0E477M6 or Panasonic EEFUD0D471L6	(2) 330µF, 2.5V, 6mΩ, low-ESR capacitor Panasonic EEFSD0D331XR
$N_{H\_}$ High-Side MOSFET	(1) Fairchildsemi FDMS8690	(1) International Rectifier IRF7811W
$N_{L\_}$ Low-Side MOSFET	(2) Vishay Si7336ADP	(2) Fairchildsemi FDMS8660S
$D_{L\_}$ Schottky Rectifier	3A, 40V Schottky diode Central Semiconductor CMSH3-40	None
L_ Inductor	0.45µH, 30A, 1.1mΩ power inductor TOKO FDUE1040D-R45M or NEC/Tokin MPC1040LR45	0.22µH, 25A, 1mΩ power inductor NEC/Tokin MPC0730LR20

Note: Mobile applications should be designed for separate mode operation. Component selection dependent on AMD CPU AC and DC specifications.

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
AVX	www.avxcorp.com
BI Technologies	www.bitechnologies.com
Central Semiconductor	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET	www.kemet.com
NEC Tokin	www.nec-tokin.com
Panasonic	www.panasonic.com

MANUFACTURER	WEBSITE
Pulse	www.pulseeng.com
Renesas	www.renesas.com
SANYO	www.secc.co.jp
Siliconix (Vishay)	www.vishay.com
Sumida	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK	www.component.tdk.com
TOKO	www.tokoam.com

Standard Application Circuits

The MAX17009 standard application circuit (Figure 2) generates two independent 18A outputs for AMD mobile CPU applications. See Table 1 for component selections. Table 2 lists the component manufacturers.

Detailed Description

The MAX17009 consists of a dual-fixed-frequency PWM controller that generates the supply voltage for two independent CPU cores. A reference buffer output (NBV_BUF) sets the regulation voltage for a separate NB regulator. The CPU cores can be configured as independent outputs, or as a combined output based on the GNDS2 pin strap (GNDS2 pulled to 1.5V - 1.8V, which are the respective voltages for DDR3 and DDR2).

Both SMPS outputs and the NB buffer can be programmed to any voltage in the VID table (see Table 4) using the SVI. The CPU is the SVI bus master, while the MAX17009 is the SVI slave. Voltage transitions are commanded by the CPU as a single-step command from one VID code to another. The MAX17009 slews the SMPS outputs at the slew rate programmed by the external R_{TIME} resistor. For the NB buffer, the slew rate is set by the combination of R_{TIME} and the total capacitance on the output of the buffer.

By default, the MAX17009 SMPSs are always in pulse-skip mode. In separate mode, the PSI_L bit does not change the mode of operation, but removes the +12.5mV offset, if enabled by the OPTION pin. In combined mode, the PSI_L bit removes the +12.5mV offset and switches from 2-phase to 1-phase operation. The $\overline{NB\_SKP}$ output always follows the state of PSI_L for the NB regulator.

+5V Bias Supply (V_{CC}, V_{DD})

The MAX17009 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's main 95%-efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers.

The 5V bias supply powers both the PWM controller and internal gate-drive power, so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW}Q_G = 10mA \text{ to } 60mA \text{ (typ)}$$

where I_{CC} is provided in the *Electrical Characteristics* table, and $f_{SW}Q_G$ (per phase) is the driver's supply current, as defined in the MOSFET's data sheet. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (OSC)

Connect a resistor (R_{OSC}) between OSC and GND to set the switching frequency (per phase):

$$f_{SW} = 300kHz \times 143k\Omega / R_{OSC}$$

A 35.7kΩ to 432kΩ corresponds to switching frequencies of 1.2MHz to 100kHz, respectively. High-frequency (1.2MHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (100kHz) operation offers the best overall efficiency at the expense of component size and board space. Minimum on-time ($t_{ON(MIN)}$) must also be taken into consideration. See the Switching frequency bullet in the *SMPS Design Procedure* section.

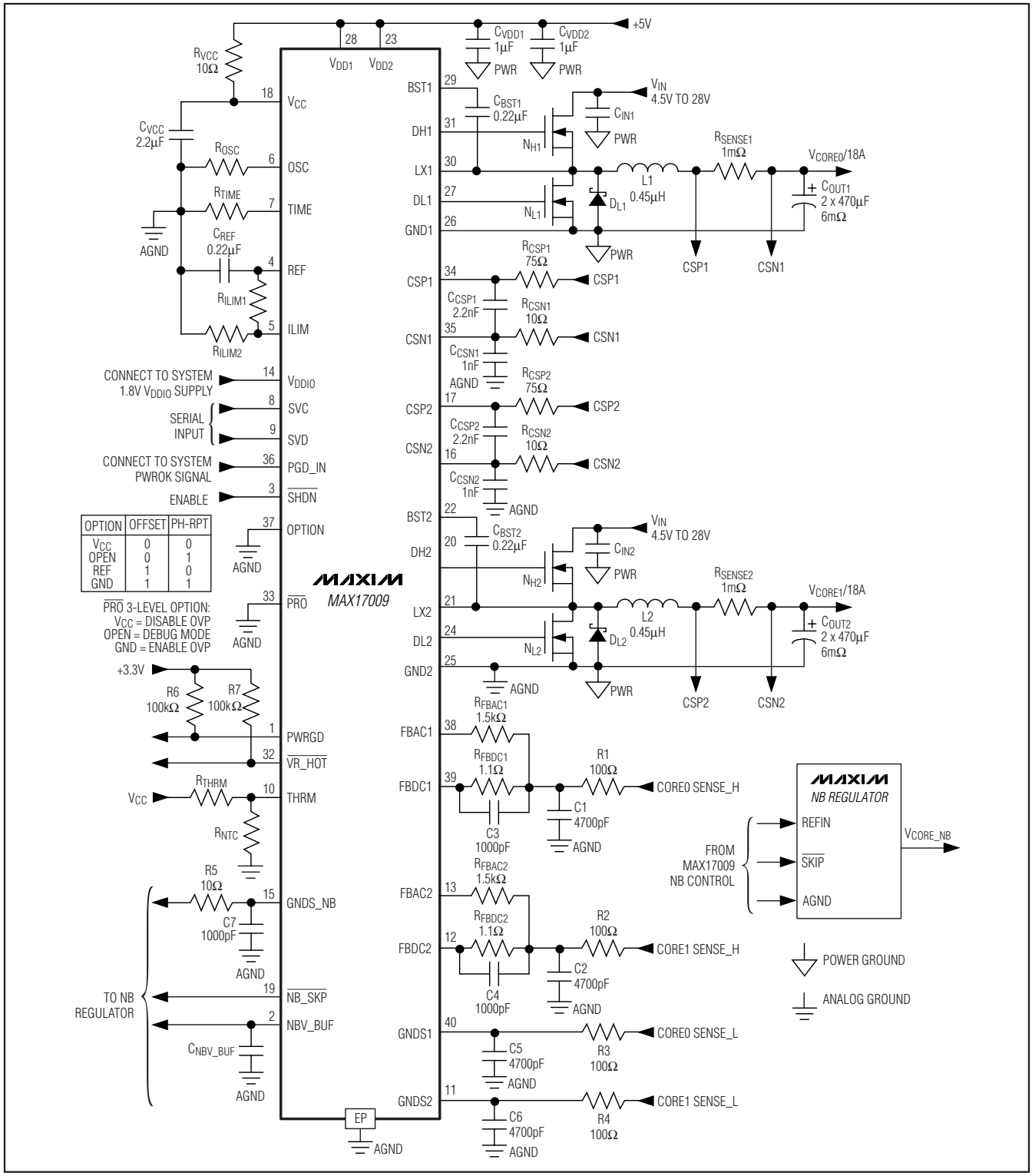

Figure 2. Standard Application Circuit

AMD Mobile Serial VID Dual-Phase Fixed-Frequency Controller

Interleaved Multiphase Operation

The MAX17009 interleaves both phases—resulting in 180° out-of-phase operation that minimizes the input and output filtering requirements, reduces electromagnetic interference (EMI), and improves efficiency. The high-side MOSFETs do not turn on simultaneously during normal operation. The instantaneous input current is effectively reduced by the number of active phases, resulting in reduced input-voltage ripple, ESR power loss, and RMS ripple current (see the *Input-Capacitor Selection* section). Therefore, the controller achieves high performance while minimizing the component count, which reduces cost, saves board space, and lowers component power requirements, making the MAX17009 ideal for high-power, cost-sensitive applications.

Transient-Phase Repeat

When a transient occurs, the output-voltage deviation depends on the controller's ability to quickly detect the transient and slew the inductor current. A fixed-frequency controller typically responds only when a clock edge occurs, resulting in a delayed transient response. To minimize this delay time, the MAX17009 includes enhanced transient detection and transient- phase-repeat capabilities. If the controller detects that the output voltage has dropped by 25mV, the transient-detection comparator immediately retriggers the phase that completed its on-time last. The controller triggers the subsequent phases as normal on the appropriate oscillator edges. This effectively triggers a phase a full cycle early, increasing the total inductor-current slew rate and providing an immediate transient response.

The OPTION pin setting enables or disables the transient phase-repeat feature. Keep OPTION OPEN or connected to GND to enable transient-phase repeat. Connect OPTION to V_{CC} or REF to disable transient-phase repeat. See the *Offset and Transient-Phase Repeat (OPTION)* section.

Feedback Adjustment Amplifiers

Steady-State Voltage-Positioning Amplifier (DC Droop)

Each of the MAX17009 SMPS controllers includes two transconductance amplifiers—one for steady-state DC droop, and another for AC droop. The amplifiers' inputs are generated by summing their respective current-sense inputs, which differentially sense the voltage across either current-sense resistors or the inductor's DCR.

The DC droop amplifier's output (FBDC) connects to the remote-sense point of the output through a resistor that sets each phase's DC voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FBDC} I_{FBDC}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output-Voltage Selection* section, and the FBDC amplifier's output current (I_{FBDC}) is determined by each phase's current-sense voltage:

$$I_{FBDC} = G_{m(FBDC)} V_{CS}$$

where $V_{CS} = V_{CSP} - V_{CSN}$ is the differential current-sense voltage, and $G_{M(FBDC)}$ is typically 1mS as defined in the *Electrical Characteristics* table.

DC droop is typically used together with the +12.5mV offset feature to keep within the DC tolerance window of the application. See the *Offset and Transient-Phase Repeat* (*OPTION)* section. The ripple voltage on FBDC must be less than the 18mV (min) transient phase repeat threshold:

$$\Delta I_L R_{SENSE} G_{m(FBDC)} R_{FBDC} + \Delta I_L R_{ESR} \le 18mV$$

$$R_{FBDC} \le \left(\frac{18mV}{\Delta I_L} - R_{ESR} \right) - R_{SENSE} G_{m(FBDC)}$$

where ΔI_L is the inductor ripple current, R_{ESR} is the effective output ESR at the remote sense point, R_{SENSE} is the current-sense element, and $G_{m(FBDC)}$ is 1.03mS (max) as defined in the *Electrical Characteristics* table. The worst-case inductor ripple occurs at the maximum input voltage and the minimum output-voltage conditions:

$$\Delta I_{L(MAX)} = \frac{V_{OUT(MIN)} \left(V_{IN(MAX)} - V_{OUT(MIN)} \right)}{V_{IN(MAX)} f_{OSC} L}$$

To disable voltage positioning, set R_{FBDC} to zero.

Transient Voltage-Positioning Amplifier (AC Droop)

The AC droop amplifier's output (FBAC) connects to the remote-sense point of the output through a resistor that sets each phase's AC voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FBAC} I_{FBAC}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output-Voltage Selection* section, and the FBAC amplifier's output current (I_{FBAC}) is determined by each phase's current-sense voltage:

$$I_{FBAC} = G_{m(FBAC)} V_{CS}$$

where $V_{CS} = V_{CSP} - V_{CSN}$ is the differential current-sense voltage, and $G_{M(FBAC)}$ is 1.03mS (max), as defined in the *Electrical Characteristics* table.

AC droop is required for stable operation of the MAX17009. A minimum of 1mV/A is recommended. AC droop must not be disabled.

The maximum allowable AC droop is limited by the recommended integrator correction range of ±100mV and on the DC droop:

$$\left|R_{FBAC} - R_{FBDC}\right| \le \frac{100mV}{1.03mS I_{LOAD(MAX)} R_{SENSE}}$$

Differential Remote Sense

The MAX17009 controller includes independent differential, remote-sense inputs for each CPU core to eliminate the effects of voltage drops along the PC board (PCB) traces and through the processor's power pins. The feedback-sense (FBDC_) input connects to the voltage-positioning resistor ($R_{FBDC\_}$). The ground-sense (GNDS_) input connects to an amplifier that adds an offset directly to the target voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the feedback-sense (FBDC_) voltage-positioning resistor ($R_{FBDC\_}$), and ground-sense (GNDS_) input directly to the respective CPU core's remote-sense outputs as shown in Figure 2.

GNDS2 has a dual function. At power-on, the voltage level on GNDS2 configures the MAX17009 as two independent switching regulators, or one higher current two-phase regulator. Keep GNDS2 low during power-up to configure the MAX17009 in separate mode. Connect GNDS2 to a voltage above 0.8V (typ) for combined-mode operation. In the AMD mobile system, this is automatically done by the CPU that is plugged into the socket that pulls GNDS2 to the V_{DDIO} voltage level.

The MAX17009 checks the GNDS2 level at the time when the internal REFOK signal goes high, and latches the operating mode information (separate or combined mode). This latch is cleared by cycling the $\overline{SHDN}$ pin.

Integrator Amplifier

An internal integrator amplifier forces the DC average of the FBDC_ voltage to equal the target voltage. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 3), allowing accurate DC output-voltage regulation regardless of the output-ripple voltage. The integrator amplifier has the ability to shift the output voltage by ±100mV (min).

The MAX17009 disables the integrator by connecting the amplifier inputs together at the beginning of all VID transitions done in pulse-skipping mode. The integrator remains disabled until 20µs after the transition is completed (the internal target settles), and the output is in regulation (edge detected on the error comparator).

When voltage positioning is disabled ($R_{FBDC\_} = 0\Omega$), the AC droop setting must be less than the ±100mV minimum adjustment range of the integrator amplifier to guarantee proper DC output-voltage accuracy. See the *Steady State Voltage-Positioning Amplifiers (DC Droop)* and the *Transient Voltage-Positioning Amplifiers (AC Droop)* sections.

2-Wire Serial Interface (SVC, SVD)

The MAX17009 supports the 2-wire, write only, serial-interface bus as defined by the AMD Serial VID Interface Specification. The serial interface is similar to the high-speed 3.4MHz I^2C bus, but without the master mode sequence. The bus consists of a clock line (SVC) and a data line (SVD). The CPU is the bus master, and the MAX17009 is the slave. The MAX17009 serial interface works from 100kHz to 3.4MHz. In the AMD mobile application, the bus runs at 3.4MHz.

The serial interface is active only after PGD_IN goes high in the startup sequence. The CPU sets the VID voltage of the three internal DACs and the PSI_L bit through the serial interface.

During the startup sequence, the SVC and SVD inputs serve an alternate function to set the 2-bit boot VID for all three DACs while PWRGD is low. In debug mode, the SVC and SVD inputs function in the 2-bit VID mode when PGD_IN is low, and in the serial-interface mode when PGD_IN is high.

Nominal Output-Voltage Selection

SMPS Output Voltage

The nominal no-load output voltage ($V_{TARGET\_}$) for each SMPS is defined by the selected voltage reference (VID DAC) plus the remote ground-sense adjustment (V_{GNDS}) and the offset voltage (V_{OFFSET}) as defined in the following equation:

$$V_{TARGET} = V_{FBDC} = V_{DAC} + V_{GNDS} + V_{OFFSET}$$

where V_{DAC} is the selected VID voltage of the SMPS DAC, V_{GNDS} is the ground-sense correction voltage, and V_{OFFSET} is the +12.5mV offset enabled by the OPTION pin, when the PSI_L is set high.

NBV_BUF Output Voltage

The nominal output voltage (V_{TARGET}) for the NBV_BUF is defined by the selected voltage reference (VID DAC) plus the remote ground-sense adjustment (V_{GNDS}), as defined in the following equation:

$$V_{TARGET} = V_{NBV\_BUF} = V_{DAC} + V_{GNDS\_NB}$$

where $V_{DAC\_}$ is the selected VID voltage of the NBV_BUF DAC, and $V_{GNDS\_NB\_}$ is the ground-sense correction voltage. The offset voltage (V_{OFFSET}) is not applied to NBV_BUF.

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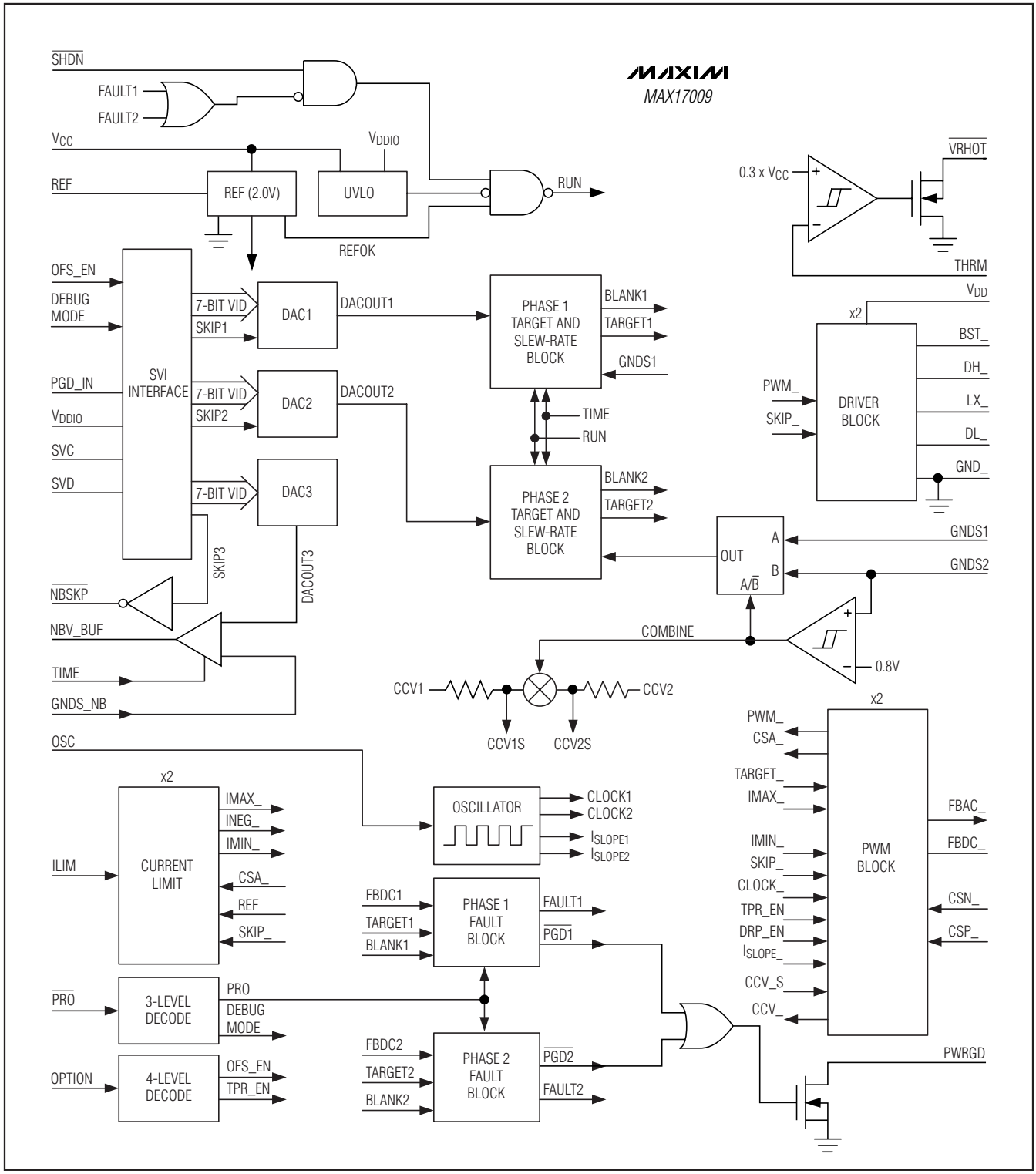

Figure 3. Functional Diagram

7-Bit DAC

Inside the MAX17009 are three 7-bit digital-to-analog converters (DACs). Each DAC can be individually programmed to different voltage levels through the serial-interface bus. The DAC sets the target for the output voltage for the SMPSs and the NB buffer output (NBV_BUF). The available DAC codes and resulting output voltages are compatible with the AMD SVI (Table 4) specifications

Boot Voltage

On startup, the MAX17009 slews the target for all three DACs from ground to the boot voltage set by the SVC and SVD pin voltage levels. While the output is still below regulation, the SVC and SVD levels can be changed, and the MAX17009 sets the DACs to the new boot voltage. Once the programmed boot voltage is reached and PWRGD goes high, the MAX17009 stores the boot VID. Changes in the SVC and SVD settings do not change the output voltage once the boot VID is stored. When PGD_IN goes high, the MAX17009 exits boot mode, and the three DACs can be independently set to any voltage in the VID table through the serial interface.

If PGD_IN goes from high to low anytime after the boot VID is stored, the MAX17009 sets all three DACs back to the voltage of the stored boot VID.

When in debug mode ($\overline{PRO}$ = OPEN), the MAX17009 uses a different boot-voltage code set. Keeping PGD_IN low allows the SVC and SVD inputs to set the three DACs to different voltages in the boot-voltage code table. When PGD_IN is subsequently set high, the three DACs can be independently set to any voltage in the VID table serial interface. Table 3 shows the boot-voltage code table.

Table 3. Boot-Voltage Code Table

SVC	SVD	BOOT VOLTAGE (V_{BOOT}) ($\overline{PRO}$ = V_{CC} OR GND)	BOOT VOLTAGE (V_{BOOT}) ($\overline{PRO}$ = OPEN)
0	0	1.1	1.4
0	1	1.0	1.2
1	0	0.9	1.0
1	1	0.8	0.8

Offset

A +12.5mV offset can be added to both SMPS DAC voltages for applications that include DC droop. The offset is applied only after the MAX17009 exits boot mode (PGD_IN going from low to high), and the MAX17009 enters the serial-interface mode. The offset is disabled when the PSI_L bit is set, saving more power when the load is light.

The OPTION pin setting enables or disables the +12.5mV offset. Connect OPTION to REF or GND to enable the offset. Keep OPTION open or connected to V_{CC} to disable the offset. See the *Offset and Transient-Phase Repeat* (*OPTION)* section.

Output-Voltage Transition Timing

SMPS Output-Voltage Transition

The MAX17009 performs positive voltage transitions in a controlled manner, automatically minimizing input surge currents. This feature allows the circuit designer to achieve nearly ideal transitions, guaranteeing just-in-time arrival at the new output voltage level with the lowest possible peak currents for a given output capacitance. The slew rate (set by resistor R_{TIME}) must be set fast enough to ensure that 35.7kΩ and 357kΩ for corresponding slew rates between 25mV/µs to 2.5mV/µs, respectively, for the SMPSs.

At the beginning of an output-voltage transition, the MAX17009 blanks both PWRGD comparator thresholds, preventing the PWRGD open-drain output from changing states during the transition. At the end of an upward VID transition, the controller enables both PWRGD thresholds approximately 20µs after the slew-rate controller reaches the target output voltage. At the end of a downward VID transition, the upper PWRGD threshold is enabled only after the output reaches the lower VID code setting.

The MAX17009 automatically controls the current to the minimum level required to complete the transition in the calculated time. The slew-rate controller uses an internal capacitor and current source programmed by R_{TIME} to transition the output voltage. The total transition time depends on R_{TIME}, the voltage difference, and the accuracy of the slew-rate controller (C_{SLEW} accuracy). The slew rate is not dependent on the total output capacitance, as long as the surge current is less than the current limit set by ILIM. For all dynamic positive VID transitions, the transition time (t_{TRAN}) is given by:

$$t_{TRAN} = \frac{|V_{NEW} - V_{OLD}|}{(dV_{TARGET}/dt)}$$

where dV_{TARGET}/dt = 6.25mV/µs x 143kΩ / R_{TIME} is the slew rate, V_{OLD} is the original output voltage, and V_{NEW} is the new target voltage. See the TIME Slew-Rate Accuracy row in the *Electrical Characteristics* table for slew-rate limits.

The output voltage tracks the slewed target voltage, making the transitions relatively smooth. The average inductor current per phase required to make an output-voltage transition is: