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EVALUATION KIT AVAILABLE

# Low-Cost Multiple-Output Power Supply for LCD TVs

MAX17014A

## General Description

The MAX17014A multiple-output power-supply controller generates all the supply rails for thin-film transistor (TFT) liquid-crystal display (LCD) panels in TVs and monitors operating from a regulated 12V input. It includes a step-down and a step-up regulator, a positive and a negative charge pump, two operational amplifiers, and a Dual Mode™ logic-controlled high-voltage switch control block. The MAX17014A can operate from 8V to 16.5V input voltages and is optimized for LCD TV panel and LCD monitor applications running directly from 12V supplies.

The step-up and step-down regulators feature internal power MOSFETs and high-frequency operation allowing the use of small inductors and capacitors, resulting in a compact solution. Both switching regulators use fixed-frequency current-mode control architectures, providing fast load-transient response and easy compensation. A current-limit function for internal switches and output-fault shutdown protect the step-up and step-down power supplies against fault conditions. The MAX17014A provides soft-start functions to limit inrush current during startup. The MAX17014A provides adjustable power-up timing.

The positive and negative charge-pump regulators provide TFT gate driver supply voltages. Both output voltages can be adjusted with external resistive voltage-dividers. The switch control block allows the manipulation of the positive TFT gate driver voltage.

The MAX17014A includes two high-current operational amplifiers designed to drive the LCD backplane (VCOM). The amplifier features high output current (±150mA), fast slew rate (100V/µs), wide bandwidth (20MHz), and rail-to-rail inputs and outputs. A series p-channel MOSFET is integrated to sequence power to $AV_{DD}$ after the MAX17014A has proceeded through normal startup, and provides True Shutdown™.

The MAX17014A is available in a small (7mm x 7mm), low-profile (0.8mm), 48-pin thin QFN package and operates over a -40°C to +85°C temperature range.

## Applications

LCD TV Panels

LCD Monitor Panels

## Features

- ♦ **Optimized for 10.8V to 13.2V Input Supply**
- ♦ **8V to 16.5V Input Supply Range**
- ♦ **Selectable Frequency (600kHz/1.2MHz)**
- ♦ **Current-Mode Step-Up Regulator**
  - **Built-In 20V, 3.7A, 110mΩ n-Channel MOSFET**
  - **High-Accuracy Output Voltage (1%)**
  - **True Shutdown**
  - **Fast Load-Transient Response**
  - **High Efficiency**
  - **3ms Internal Soft-Start**
- ♦ **Current-Mode Step-Down Regulator**
  - **Built-In 20V, 2.5A, 120mΩ n-Channel MOSFET**
  - **Fast Load-Transient Response**
  - **Adjustable Output Voltage Down to 1.25V**
  - **Skip Mode at Light Load**
  - **High Efficiency**
  - **3ms Internal Soft-Start**
- ♦ **Adjustable Positive and Negative Charge-Pump Regulators**
- ♦ **Soft-Start and Timer-Delay Fault Latch for All Outputs**
- ♦ **Logic-Controlled High-Voltage Integrated Switches with Adjustable Delay**
- ♦ **Two High-Speed Operational Amplifiers**
  - **±150mA Short-Circuit Current**
  - **100V/µs Slew Rate**
  - **20MHz, -3dB Bandwidth**
- ♦ **120mΩ p-Channel FET for $AV_{DD}$ Sequencing**
- ♦ **Input Undervoltage Lockout and Thermal-Overload Protection**
- ♦ **48-Pin, 7mm x 7mm Thin QFN Package**

## Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE |
|---|---|---|
| MAX17014AETM+ | -40°C to +85°C | 48 Thin QFN |

*+Denotes a lead-free/RoHS-compatible package.*



***Simplified Operating Circuit and Pin Configuration appear at end of data sheet.***

# Low-Cost Multiple-Output Power Supply for LCD TVs

## ABSOLUTE MAXIMUM RATINGS

$V_{IN}$, IN2, OVIN, SUP, EN1, EN2, FSEL to GND ......-0.3V to +24V
GND1, OGND, CPGND to GND ........................................±0.3V
MODE, DLP, CTL, THR, DEL1, DEL2, VL to GND ...-0.3V to +7.5V
REF, FBP, FBN, FB1, FB2, COMP,
OUT to GND ..........................................-0.3V to ($V_{VL}$ + 0.3V)
SWI, SWO to GND.................................................-0.3V to +24V
LX1 to GND1 .........................................................-0.3V to +24V
SWI to SWO...........................................................-0.3V to +24V
SWI to SUI ............................................................-0.3V to +7.5V
POS1, NEG1, OUT1, POS2, NEG2,
OUT2 to OGND..................................-0.3V to ($V_{OVIN}$ + 0.3V)
DRVN, DRVP to CPGND ..........................-0.3V to ($V_{SUP}$ + 0.3V)
LX2 to CPGND ..........................................-0.3V to ($V_{IN2}$ + 0.3V)
BST to VL..............................................................-0.3V to +24V
SRC to GND ..........................................................-0.3V to +48V
GON, DRN to GND ..................................-0.3V to ($V_{SRC}$ + 0.3V)
GON to DRN..........................................................-0.3V to +48V
POS_ to NEG_ RMS Current ..................................5mA (Note 1)

REF Short Circuit to GND ..........................................Continuous
RMS LX1 Current (total for both pins)..................................3.2A
RMS GND1 Current (total for both pins) ..............................3.2A
RMS IN2 Current (total for both pins)...................................3.2A
RMS LX2 Current (total for both pins) ..................................3.2A
RMS CPGND Current...........................................................0.8A
RMS SWI Current .................................................................2.4A
RMS SWO Current ...............................................................2.4A
RMS DRVN, DRVP Current ..................................................0.8A
RMS VL Current .................................................................50mA
Continuous Power Dissipation ($T_A$ = +70°C)
48-Pin Thin QFN
(derate 38.5mW/°C above +70°C) ........................3076.9mW
Operating Temperature Range ..........................-40°C to +85°C
Junction Temperature .....................................................+160°C
Storage Temperature Range .............................-65°C to +165°C
Lead Temperature (soldering, 10s) ................................+300°C

**Note 1:** See Figure 6 for the op amp clamp structures.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, $V_{IN}$ = IN2 = 12V, $AV_{DD}$ = OVIN = SUP = 15V, **$T_A$ = 0°C to +85°C**. Typical values are at $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **GENERAL** | | | | | |
| $V_{IN}$, IN2 Input Voltage Range | | 8.0 | | 16.5 | V |
| $V_{IN}$ + IN2 Quiescent Current | Only LX2 switching ($V_{FB1}$ = $V_{FBP}$ = 1.5V, $V_{FBN}$ = 0); EN1 = EN2 = VL, $V_{FSEL}$= 0 | | 8 | | mA |
| $V_{IN}$ + IN2 Standby Current | LX2 not switching ($V_{FB1}$ = $V_{FB2}$ = $V_{FBP}$ = 1.5V, $V_{FBN}$ = 0); EN1 = EN2 = VL, $V_{FSEL}$= 0 | | 2 | | mA |
| $V_{IN}$ + IN2 Shutdown Current | EN1 = EN2 = GND (shutdown) | | 300 | | µA |
| SUP + OVIN Shutdown Current | EN1 = EN2 = GND (shutdown) | | 10 | | µA |
| SMPS Operating Frequency | FSEL = $V_{IN}$ | 1020 | 1200 | 1380 | kHz |
| | FSEL = GND | 510 | 600 | 690 | |
| Phase Difference Between Step-Down/Positive and Step-Up/Negative Regulators | | | 180 | | Degrees |
| $V_{IN}$ Undervoltage Lockout Threshold | $V_{IN}$ rising edge, 200mV typical hysteresis | 6.0 | 7.0 | 8.0 | V |
| **VL REGULATOR** | | | | | |
| VL Output Voltage | $I_{VL}$ = 25mA, $V_{FB1}$ = $V_{FB2}$ = $V_{FBP}$ = 1.1V, $V_{FBN}$ = 0.4V (all regulators switching) | 4.9 | 5.0 | 5.1 | V |
| VL Undervoltage Lockout Threshold | VL rising edge, 100mV typical hysteresis | 3.5 | 3.9 | 4.3 | V |

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN}$ = IN2 = 12V, $AV_{DD}$ = OVIN = SUP = 15V, **$T_A$ = 0°C to +85°C**. Typical values are at $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **REFERENCE** | | | | | | |
| REF Output Voltage | No external load | | 1.235 | 1.250 | 1.265 | V |
| REF Load Regulation | 0 < $I_{LOAD}$ < 50µA | | | | 10 | mV |
| REF Sink Current | In regulation | | 10 | | | µA |
| REF Undervoltage Lockout Threshold | Rising edge; 20mV typical hysteresis | | | 1.0 | 1.2 | V |
| **STEP-DOWN REGULATOR** | | | | | | |
| OUT Voltage in Fixed Mode | FB2 = GND, no load (Note 2) | 0°C < $T_A$ < +85°C | 3.25 | 3.30 | 3.35 | V |
| | | $T_A$ = +25°C | 3.267 | | 3.333 | |
| FB2 Voltage in Adjustable Mode | $V_{OUT}$ = 2.5V, no load (Note 2) | 0°C < $T_A$ < +85°C | 1.23 | 1.25 | 1.27 | V |
| | | $T_A$ = +25°C | 1.2375 | | 1.2625 | |
| FB2 Adjustable-Mode Threshold Voltage | Dual-mode comparator | | 0.10 | 0.15 | 0.20 | V |
| Output Voltage Adjust Range | Step-down output | | 1.5 | | 5.0 | V |
| FB2 Fault Trip Level | Falling edge | | 0.96 | 1.00 | 1.04 | V |
| FB2 Input Leakage Current | $V_{FB2}$ = 1.5V | | 50 | 125 | 200 | nA |
| DC Load Regulation | 0A < $I_{LOAD}$ < 2A | | | 0.5 | | % |
| DC Line Regulation | No load, 10.8V < $V_{IN2}$ < 13.2V | | | 0.1 | | %/V |
| LX2-to-IN2 nMOS Switch On-Resistance | | | | 120 | 240 | mΩ |
| LX2-to-CPGND nMOS Switch On-Resistance | | | 6 | 10 | 23 | Ω |
| BST-to-VL PMOS Switch On-Resistance | | | 7 | 12 | 20 | Ω |
| Low-Frequency Operation OUT Threshold | Step-down only | | | 0.8 | | V |
| Low-Frequency Operation Switching Frequency | FSEL = $V_{IN}$ | | | 217 | | kHz |
| | FSEL = GND | | | 108 | | |
| LX2 Positive Current Limit | | | 2.50 | 3 | 3.50 | A |
| Soft-Start Period | | | | 3 | | ms |
| Soft-Start Step Size | | | | $V_{REF}$ / 128 | | V |
| Maximum Duty Factor | | | 70 | 80 | 90 | % |
| **STEP-UP REGULATOR** | | | | | | |
| Output Voltage Range | | | $V_{VIN}$ | | 20 | V |
| Oscillator Maximum Duty Cycle | | | 69 | 75 | 81 | % |
| Minimum $t_{ON}$ | | | | 70 | | ns |
| FB1 Regulation Voltage | FB1 = COMP, $C_{COMP}$ = 1nF | 0°C < $T_A$ < +85°C | 1.235 | 1.25 | 1.265 | V |
| | | $T_A$ = +25°C | 1.2375 | | 1.2625 | |
| FB1 Fault Trip Level | Falling edge | | 0.96 | 1.00 | 1.04 | V |

# Low-Cost Multiple-Output Power Supply for LCD TVs

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN}$ = IN2 = 12V, $AV_{DD}$ = OVIN = SUP = 15V, **$T_A$ = 0°C to +85°C**. Typical values are at $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| FB1 Load Regulation | 0 < $I_{LOAD}$ < full, transient only | | | -1 | | % |
| FB1 Line Regulation | 10.8V < $V_{VIN}$ < 13.2V | | | 0.08 | 0.15 | %/V |
| FB1 Input Bias Current | $V_{FB1}$ = 1.25V | | 25 | 125 | 200 | nA |
| FB1 Transconductance | ΔI = ±2.5µA at COMP, FB1 = COMP | | 150 | 320 | 560 | µS |
| FB1 Voltage Gain | FB1 to COMP | | | 1400 | | V/V |
| LX1 Leakage Current | $V_{FB1}$ = 1.5V, $V_{LX1}$ = 20V | | | 4 | 40 | µA |
| LX1 Current Limit | $V_{FB1}$ = 1.1V, duty cycle = 25% | | 3.2 | 3.7 | 4.2 | A |
| Current-Sense Transresistance | | | 0.16 | 0.23 | 0.30 | V/A |
| LX1 On-Resistance | | | | 110 | 220 | mΩ |
| Soft-Start Period | | | | 3 | | ms |
| Soft-Start Step Size | | | | $I_{LIM}$ / 128 | | A |
| **POSITIVE AND NEGATIVE CHARGE-PUMP REGULATORS** | | | | | | |
| SUP Input Supply Range | | | 8.0 | | 18.5 | V |
| SUP Input Supply Current | $V_{FBP}$ = 1.5V, $V_{FBN}$ = 0.15V (not switching) | | | 0.2 | 0.4 | mA |
| SUP Overvoltage Threshold | SUP rising edge, 250mV typical hysteresis (Note 3) | | 18.5 | 19.25 | 20 | V |
| FBP Regulation Voltage | 0°C < $T_A$ < +85°C | | 1.23 | 1.25 | 1.27 | V |
| | $T_A$ = +25°C | | 1.2375 | | 1.2625 | |
| FBP Line-Regulation Error | 11V < $V_{SUP}$ < 16V, not in dropout | | | | 0.2 | %/V |
| FBP Input Bias Current | $V_{FBP}$ = 1.5V | | -50 | | +50 | nA |
| DRVP p-Channel MOSFET On-Resistance | | | | 1.0 | 3.0 | Ω |
| DRVP n-Channel MOSFET On-Resistance | | | | 0.5 | 1.0 | Ω |
| FBP Fault Trip Level | Falling edge | | 0.96 | 1.00 | 1.04 | V |
| Positive Charge-Pump Soft-Start Period | | | | 3 | | ms |
| Positive Charge-Pump Soft-Start Step Size | | | | $V_{REF}$ / 128 | | V |
| FBN Regulation Voltage | $V_{REF}$ - $V_{FBN}$ | 0°C < $T_A$ < +85°C | 0.988 | 1.000 | 1.012 | V |
| | | $T_A$ = +25°C | 0.99 | 1.00 | 1.01 | |
| FBN Input Bias Current | $V_{FBN}$ = 0mV | | -50 | | +50 | nA |
| FBN Line Regulation Error | 11V < $V_{SUP}$ < 16V, not in dropout | | | | 0.2 | %/V |
| DRVN p-Channel On-Resistance | | | | 1.0 | 3.0 | Ω |
| DRVN n-Channel On-Resistance | | | | 0.5 | 1.0 | Ω |
| FBN Fault Trip Level | Rising edge | | 450 | 500 | 550 | mV |
| Negative Charge-Pump Soft-Start | | | | 3 | | ms |
| Negative Charge-Pump Soft-Start Step Size | | | | ($V_{REF}$ - $V_{FBN}$) / 128 | | V |

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN}$ = IN2 = 12V, $AV_{DD}$ = OVIN = SUP = 15V, **$T_A$ = 0°C to +85°C**. Typical values are at $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **$AV_{DD}$ SWITCH** | | | | | |
| SWI Supply Range | | 8.0 | | 18.5 | V |
| SWI Overvoltage Fault Threshold | SWI rising edge, 250mV typical hysteresis (Note 3) | 18.50 | 19.25 | 20.00 | V |
| SWI-SWO Switch Resistance | | | 120 | 240 | mΩ |
| SUI-SWI Pullup Resistance | EN2 = GND | | 30 | | Ω |
| SUI Output Sink Current | EN2 = DEL2 = VL | 24 | 30 | 36 | µA |
| SWI-SUI Done Threshold | EN2 = DEL2 = VL | 4.4 | 5.0 | 5.6 | V |
| **OPERATIONAL AMPLIFIERS** | | | | | |
| OVIN Supply Range | | 8 | | 18.5 | V |
| OVIN Overvoltage Fault Threshold | OVIN rising edge, 250mV typical hysteresis (Note 3) | 18.5 | 19.25 | 20 | V |
| OVIN Supply Current | Buffer configuration, $V_{POSx}$ = $V_{OVIN}$ / 2, no load | | 4.2 | 6 | mA |
| Input Offset Voltage | 2V < ($V_{NEGx}$, $V_{POSx}$) < ($V_{OVIN}$ - 2V), $T_A$ = +25°C | -10 | | +10 | mV |
| Input Bias Current | 2V < ($V_{NEGx}$, $V_{POSx}$) < ($V_{OVIN}$ - 2V) | -1 | | +1 | µA |
| Input Common-Mode Voltage Range | | 0 | | $V_{OVIN}$ | V |
| Input Common-Mode Rejection | 2V < ($V_{NEGx}$, $V_{POSx}$) < ($V_{OVIN}$ - 2V) | | 100 | | dB |
| Output Voltage Swing High | $I_{OUTx}$ = 25mA | $V_{OVIN}$ - 300 | $V_{OVIN}$ - 150 | | mV |
| Output Voltage Swing Low | $I_{OUTx}$ = -25mA | | 150 | 300 | mV |
| Large-Signal Voltage Gain | 2V < ($V_{NEGx}$, $V_{POSx}$) < ($V_{OVIN}$ - 2V) | | 80 | | dB |
| Slew Rate | 2V < ($V_{NEGx}$, $V_{POSx}$) < ($V_{OVIN}$ - 2V) | | 100 | | V/µs |
| -3dB Bandwidth | 2V < ($V_{NEGx}$, $V_{POSx}$) < ($V_{OVIN}$ - 2V) | | 20 | | MHz |
| Short-Circuit Current | Short to $V_{OVIN}$ / 2, sourcing | | 150 | | mA |
| | Short to $V_{OVIN}$ / 2, sinking | | 250 | | |
| **HIGH-VOLTAGE SWITCH ARRAY** | | | | | |
| SRC Supply Range | | | | 44 | V |
| SRC Supply Current | | | 200 | 500 | µA |
| GON-to-SRC Switch On-Resistance | $V_{DLP}$ = 2V, CTL = VL | | 10 | 20 | Ω |
| GON-to-SRC Switch Saturation Current | ($V_{SRC}$ - $V_{GON}$) > 5V | 150 | 390 | | mA |
| GON-to-DRN Switch On-Resistance | $V_{DLP}$ = 2V, CTL = GND | | 20 | 50 | Ω |
| GON-to-DRN Switch Saturation Current | ($V_{GON}$ - $V_{DRN}$) > 5V | 75 | 180 | | mA |
| GON-to-GND Switch On-Resistance | DLP = GND | 1.5 | 3.0 | 4.5 | kΩ |
| CTL Input Low Voltage | | | | 0.6 | V |
| CTL Input High Voltage | | 1.6 | | | V |
| CTL Input Current | CTL = GND or VL | -1 | | +1 | µA |

# Low-Cost Multiple-Output Power Supply for LCD TVs

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN}$ = IN2 = 12V, $AV_{DD}$ = OVIN = SUP = 15V, **$T_A$ = 0°C to +85°C**. Typical values are at $T_A$ = +25°C, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| CTL-to-GON Rising Propagation Delay | 1kΩ from DRN to GND, CTL = GND to VL step, no load on GON, measured from $V_{CTL}$ = 2V to GON = 20% | | 100 | | ns |
| CTL-to-GON Falling Propagation Delay | 1kΩ from DRN to GND, CTL = VL to GND step, no load on GON, measured from $V_{CTL}$ = 0.6V to GON = 80% | | 100 | | ns |
| MODE Switch On-Resistance | | | 1250 | | Ω |
| Mode 1 Voltage Threshold | $V_{MODE}$ rising edge | | 3.75 | 4.5 | V |
| MODE Capacitor Charge Current (Mode 2) | $V_{MODE}$ < MODE current-source stop voltage threshold | 40 | 50 | 60 | µA |
| MODE Voltage Threshold for Enabling DRN Switch Control in Mode 2 | GON connects to DRN | 1.20 | 1.25 | 1.30 | V |
| MODE Current-Source Stop Voltage Threshold | MODE rising edge | 2 | | 3 | V |
| THR-to-GON Voltage Gain | | 9.4 | 10.0 | 10.6 | V/V |
| **SEQUENCE CONTROL** | | | | | |
| EN1, EN2, Input Low Voltage | | | | 0.6 | V |
| EN1, EN2 Input High Voltage | | 1.6 | | | V |
| EN1, EN2 Pulldown Resistance | | | 1 | | MΩ |
| DEL1, DEL2, DLP Charge Current | $V_{DEL1}$ = $V_{DEL2}$ = $V_{DLP}$ = 1V | 6 | 8 | 10 | µA |
| DEL1, DEL2, DLP Turn-On Threshold | | 1.19 | 1.25 | 1.31 | kV |
| DEL1, DEL2, DLP Discharge Switch On-Resistance | EN1 = GND or fault tripped | | 10 | | Ω |
| FBN Discharge Switch On-Resistance | EN2 = GND or fault tripped | | 3 | | kΩ |
| **FAULT DETECTION** | | | | | |
| Duration to Trigger Fault | | | 50 | | ms |
| Duration to Restart After Fault | | | 160 | | ms |
| Number of Restart Attempts Before Shutdown | | | 3 | | Times |
| Thermal-Shutdown Threshold | 15°C typical hysteresis | | +160 | | °C |
| **SWITCHING FREQUENCY SELECTION** | | | | | |
| FSEL Input Low Voltage | 600kHz | | | 0.6 | V |
| FSEL Input High Voltage | 1.2MHz | 1.6 | | | V |
| FSEL Pulldown Resistance | | | 1 | | MΩ |

## ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, $V_{IN}$ = IN2 = 12V, $AV_{DD}$ = OVIN = SUP = 15V, **$T_A$ = -40°C to +85°C**. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 4)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **GENERAL** | | | | | |
| $V_{IN}$, IN2 Input Voltage Range | | 8.0 | | 16.5 | V |
| SMPS Operating Frequency | FSEL = $V_{IN}$ | 1020 | | 1380 | kHz |
| | FSEL = GND | 510 | | 690 | |
| $V_{IN}$ Undervoltage Lockout Threshold | $V_{IN}$ rising edge, 200mV typical hysteresis | 6.0 | | 8.0 | V |
| **VL REGULATOR** | | | | | |
| VL Output Voltage | $I_{VL}$ = 25mA, $V_{FB1}$ = $V_{FB2}$ = $V_{FBP}$ = 1.1V, $V_{FBN}$ = 0.4V (all regulators switching) | 4.9 | | 5.1 | V |
| VL Undervoltage Lockout Threshold | VL rising edge, 100mV typical hysteresis | 3.5 | | 4.3 | V |
| **REFERENCE** | | | | | |
| REF Output Voltage | No external load | 1.235 | | 1.265 | V |
| REF Load Regulation | 0 < $I_{LOAD}$ < 50µA | | | 10 | mV |
| REF Undervoltage Lockout Threshold | Rising edge; 20mV typical hysteresis | | | 1.2 | V |
| **STEP-DOWN REGULATOR** | | | | | |
| OUT Voltage in Fixed Mode | FB2 = GND, no load (Note 2) | 3.25 | | 3.35 | V |
| FB2 Voltage in Adjustable Mode | $V_{OUT}$ = 2.5V, no load (Note 2) | 1.23 | | 1.27 | V |
| FB2 Adjustable-Mode Threshold Voltage | Dual-mode comparator | 0.10 | | 0.20 | V |
| Output Voltage Adjust Range | Step-down output | 1.5 | | 5.0 | V |
| LX2-to-IN2 nMOS Switch On-Resistance | | | | 240 | mΩ |
| LX2-to-CPGND nMOS Switch On-Resistance | | 6 | | 23 | Ω |
| BST-to-VL pMOS Switch On-Resistance | | 7 | | 20 | Ω |
| LX2 Positive Current Limit | | 2.50 | | 3.50 | A |
| Maximum Duty Factor | | 70 | | 90 | % |
| **STEP-UP REGULATOR** | | | | | |
| Output Voltage Range | | $V_{VIN}$ | | 20 | V |
| Oscillator Maximum Duty Cycle | | 69 | | 81 | % |
| FB1 Regulation Voltage | FB1 = COMP, $C_{COMP}$ = 1nF | 1.23 | | 1.27 | V |
| LX1 Current Limit | $V_{FB1}$ = 1.1V, duty cycle = 25% | 3.2 | | 4.2 | A |
| Current-Sense Transresistance | | 0.16 | | 0.30 | V/A |
| LX1 On-Resistance | | | | 220 | mΩ |

# Low-Cost Multiple-Output Power Supply for LCD TVs

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN}$ = IN2 = 12V, $AV_{DD}$ = OVIN = SUP = 15V, **$T_A$ = -40°C to +85°C**. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 4)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **POSITIVE- AND NEGATIVE-CHARGE-PUMP REGULATORS** | | | | | |
| SUP Input Supply Range | | 8 | | 18.5 | V |
| SUP Overvoltage Threshold | SUP rising edge, 200mV typical hysteresis (Note 3) | 18.5 | | 20 | V |
| FBN Regulation Voltage | | 1.23 | | 1.27 | V |
| DRVP p-Channel MOSFET On-Resistance | | | | 3 | Ω |
| DRVP n-Channel MOSFET On-Resistance | | | | 1 | Ω |
| FBN Regulation Voltage | $V_{REF}$ - $V_{FBN}$ | 0.985 | | 1.015 | V |
| DRVN p-Channel On-Resistance | | | | 3 | Ω |
| DRVN n-Channel On-Resistance | | | | 1 | Ω |
| **AVDD SWITCH** | | | | | |
| SWI Supply Range | | 8.0 | | 18.5 | V |
| SWI Overvoltage Fault Threshold | $V_{OVIN}$ = rising, hysteresis = 200mV (Note 3) | 18.5 | | 20 | V |
| SWI-SWO Switch Resistance | | | | 240 | mΩ |
| SUI Output Sink Current | EN2 = DEL2 = VL | 24 | | 36 | µA |
| SWI-SUI Done Threshold | EN2 = DEL2 = VL | 4.4 | | 5.6 | V |
| **OPERATIONAL AMPLIFIERS** | | | | | |
| OVIN Supply Range | | 8 | | 18.5 | V |
| OVIN Overvoltage Fault Threshold | SWI rising edge, 200mV typical hysteresis (Note 2) | 18.5 | | 20 | V |
| Input Common-Mode Voltage Range | | 0 | | $V_{OVIN}$ | V |
| Output Voltage Swing High | $I_{OUTx}$ = 25mA | $V_{OVIN}$ - 300 | | | mV |
| Output Voltage Swing Low | $I_{OUTx}$ = -25mA | | | 300 | mV |
| **HIGH-VOLTAGE SWITCH ARRAY** | | | | | |
| SRC Supply Range | | | | 44 | V |
| GON-to-SRC Switch On-Resistance | $V_{DLP}$ = 2V, CTL = VL | | | 20 | Ω |
| GON-to-DRN Switch On-Resistance | $V_{DLP}$ = 2V, CTL = GND | | | 50 | Ω |
| GON-to-GND Switch On-Resistance | DLP = GND | 1.5 | | 4.5 | kΩ |
| CTL Input-Low Voltage | | | | 0.6 | V |
| CTL Input-High Voltage | | 1.6 | | | V |
| MODE 1 Voltage Threshold | $V_{MODE}$ rising edge | | | 4.5 | V |

## ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, $V_{IN}$ = IN2 = 12V, $AV_{DD}$ = OVIN = SUP = 15V, **$T_A$ = -40°C to +85°C**. Typical values are at $T_A$ = +25°C, unless otherwise noted.) (Note 4)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| MODE Voltage Threshold for Enabling DRN Switch Control in Mode 2 | GON connects to DRN | 1.2 | | 1.3 | V |
| MODE Current-Source Stop Voltage Threshold | MODE rising edge | 2 | | 3 | V |
| THR-to-GON Voltage Gain | | 9.4 | | 10.6 | V/V |
| **SEQUENCE CONTROL** | | | | | |
| EN1, EN2 Input Low Voltage | | | | 0.6 | V |
| EN1, EN2 Input High Voltage | | 1.6 | | | V |
| **SWITCHING FREQUENCY SELECTION** | | | | | |
| FSEL Input Low Voltage | 600kHz | | | 0.6 | V |
| FSEL Input High Voltage | 1.2MHz | 1.6 | | | V |

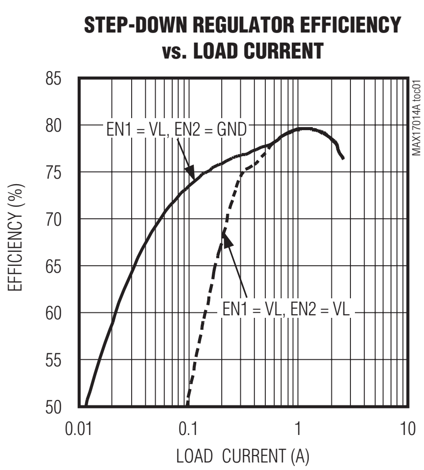
**Note 2:** When the inductor is in continuous conduction (EN2 = VL or heavy load), the output voltage has a DC regulation level lower than the error comparator threshold by 50% of the output voltage ripple. In discontinuous conduction (EN2 = GND with light load), the output voltage has a DC regulation level higher than the error comparator threshold by 50% of the output voltage ripple.

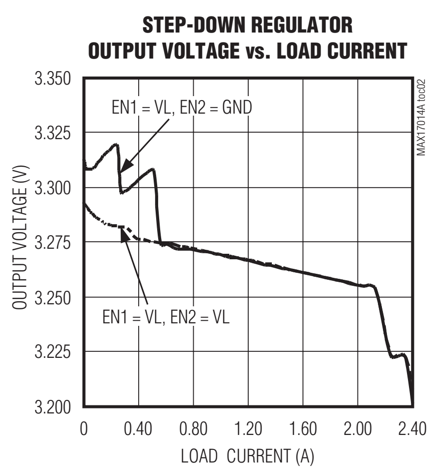
**Note 3:** Disables boost switching if either SUP, SWI, or OVIN exceeds the threshold. Switching resumes when no threshold is exceeded.

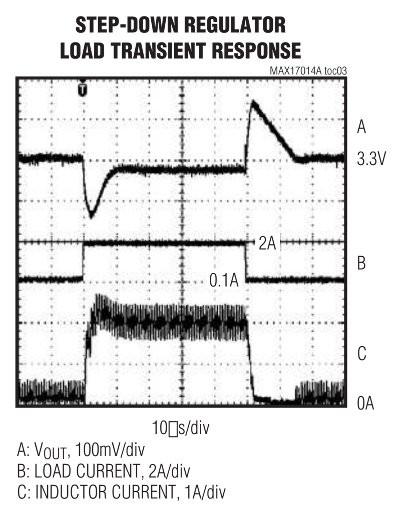
**Note 4:** Specifications to -40°C are guaranteed by design, not production tested.

## *Typical Operating Characteristics*

(Circuit of Figure 1. $V_{IN}$ = $V_{INL}$ = $V_{SUPP}$ = 12V, $AV_{DD}$ = 16V, $V_{GON}$ = 34.5V, $V_{GOFF}$ = -6V, $V_{OUT1}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.)



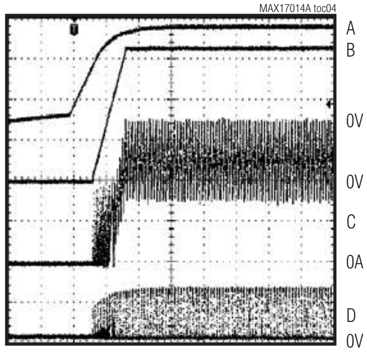



# Low-Cost Multiple-Output Power Supply for LCD TVs

## Typical Operating Characteristics (continued)

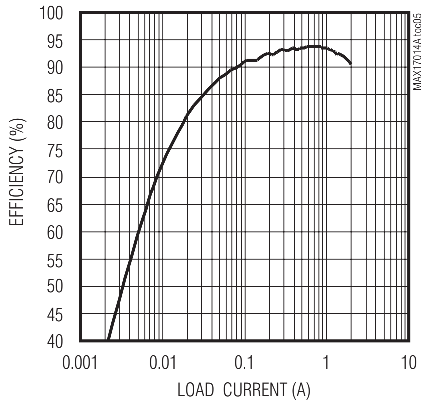
(Circuit of Figure 1. $V_{IN} = V_{INL} = V_{SUPP}$ = 12V, $AV_{DD}$ = 16V, $V_{GON}$ = 34.5V, $V_{GOFF}$ = -6V, $V_{OUT1}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.)

**STEP-DOWN REGULATOR SOFT-START (HEAVY LOAD)**

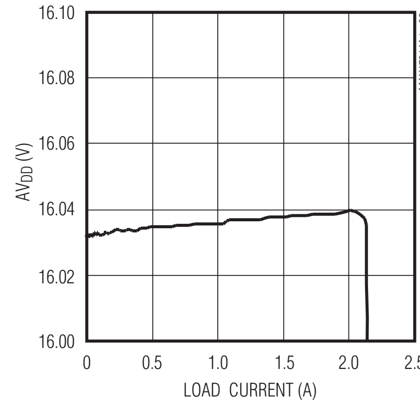



4.00ms/div
A: $V_{IN}$, 5V/div
B: $V_{OUT}$, 1V/div
C: INDUCTOR CURRENT, 500mA/div
D: $V_{LX2}$, 10V/div

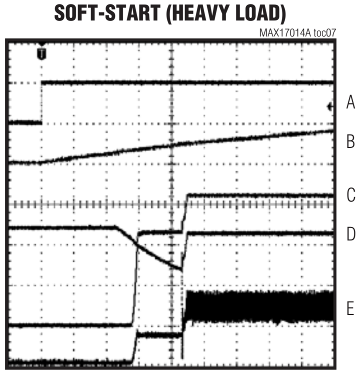
**STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT**




**STEP-UP REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT**

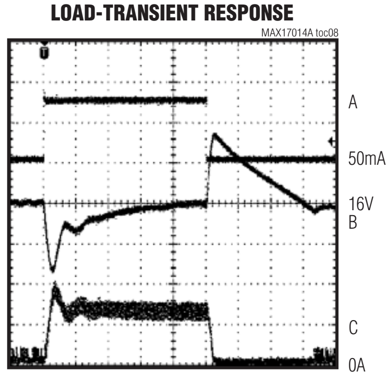



**STEP-UP REGULATOR SOFT-START (HEAVY LOAD)**



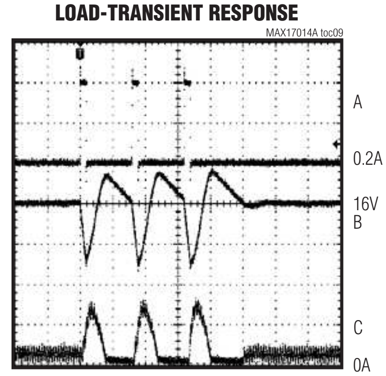

10.00ms/div
A: EN2, 5V/div
B: DEL2, 5V/div
C: $AV_{DD}$, 5V/div
D: $V_{SUI}$, 5V/div
E: INDUCTOR CURRENT, 1.00A/div

**STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE**




20.0μs/div
A: LOAD CURRENT, 1A/div
B: $AV_{DD}$, 200mV/div
C: INDUCTOR CURRENT, 2A/div

**STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE**

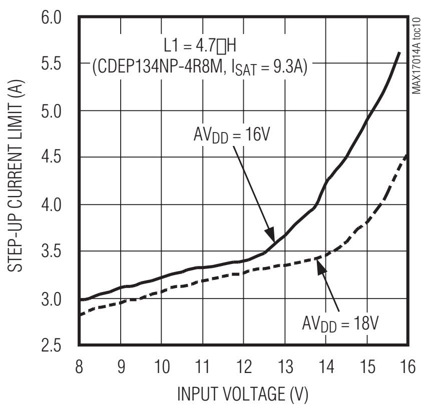



10.0μs/div
A: LOAD CURRENT, 1A/div
B: $AV_{DD}$, 200mV/div
C: INDUCTOR CURRENT, 2A/div

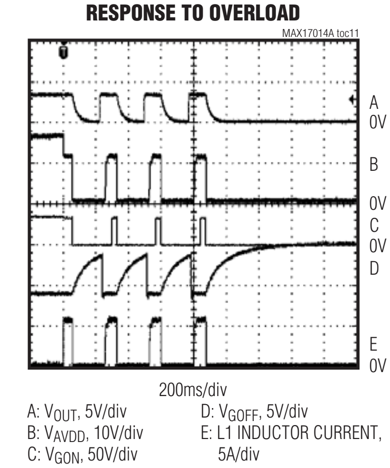
## Typical Operating Characteristics (continued)

(Circuit of Figure 1. $V_{IN} = V_{INL} = V_{SUPP}$ = 12V, $AV_{DD}$ = 16V, $V_{GON}$ = 34.5V, $V_{GOFF}$ = -6V, $V_{OUT1}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.)

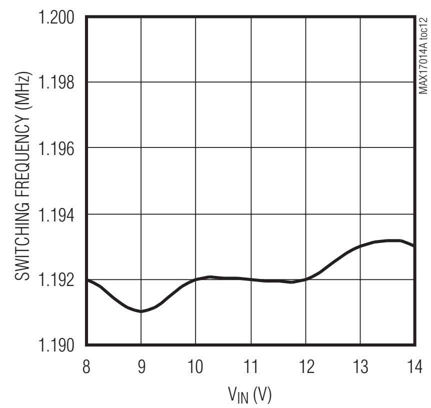
**STEP-UP REGULATOR CURRENT LIMIT vs. INPUT VOLTAGE**



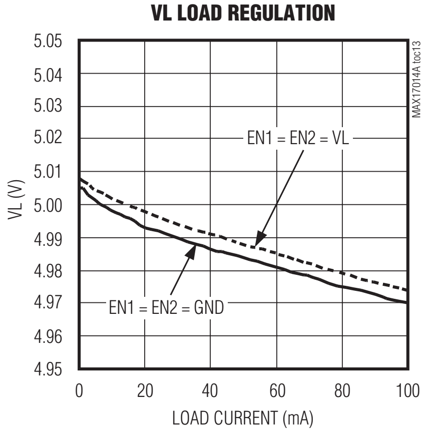

**TIME-DELAY LATCH RESPONSE TO OVERLOAD**



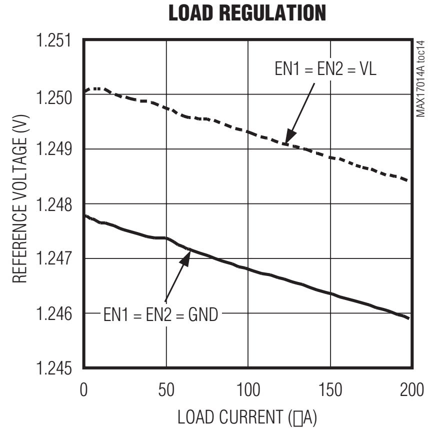

**SWITCHING FREQUENCY vs. INPUT VOLTAGE**



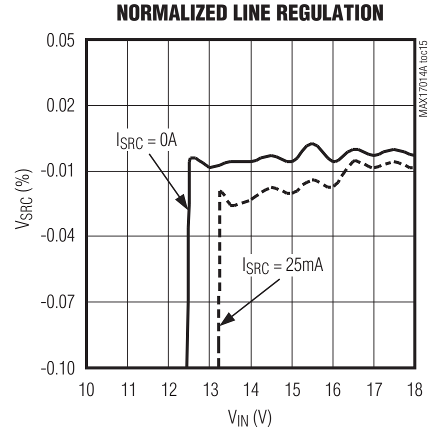

**VL LOAD REGULATION**




**REFERENCE VOLTAGE LOAD REGULATION**




**POSITIVE CHARGE-PUMP REGULATOR NORMALIZED LINE REGULATION**

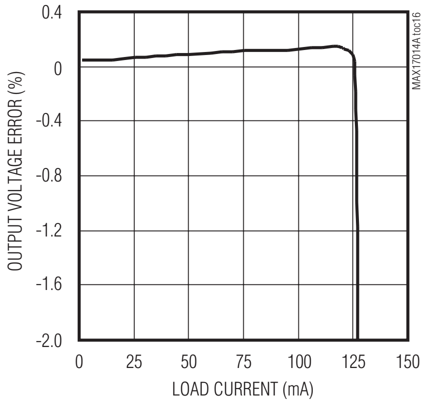


# Low-Cost Multiple-Output Power Supply for LCD TVs

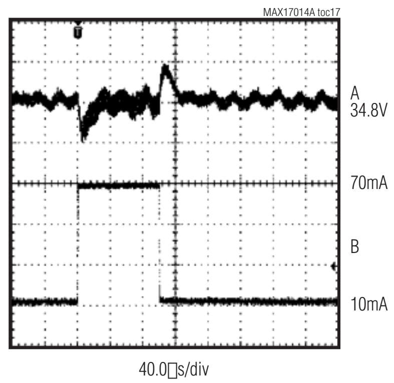
## Typical Operating Characteristics (continued)

(Circuit of Figure 1. $V_{IN} = V_{INL} = V_{SUPP}$ = 12V, $AV_{DD}$ = 16V, $V_{GON}$ = 34.5V, $V_{GOFF}$ = -6V, $V_{OUT1}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.)

**POSITIVE CHARGE-PUMP REGULATOR NORMALIZED LOAD REGULATION**

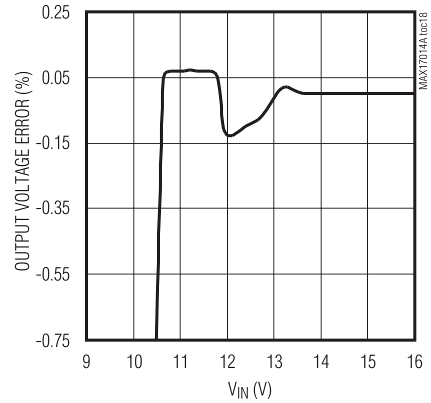



**POSITIVE CHARGE-PUMP REGULATOR LOAD-TRANSIENT RESPONSE**

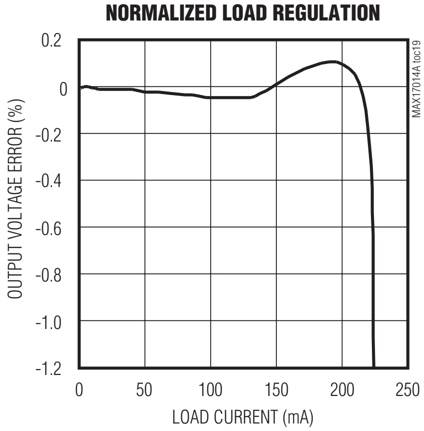



A: $V_{SRC}$, 100mV/div
B: LOAD CURRENT, 20mA/div

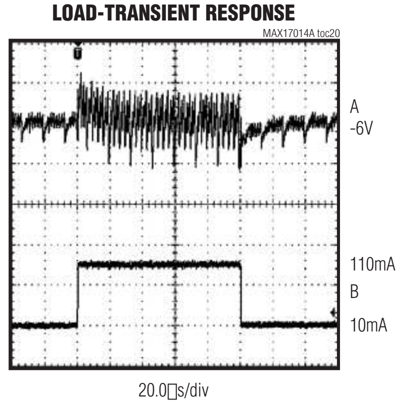
**NEGATIVE CHARGE-PUMP REGULATOR NORMALIZED LINE REGULATION**




**NEGATIVE CHARGE-PUMP REGULATOR NORMALIZED LOAD REGULATION**

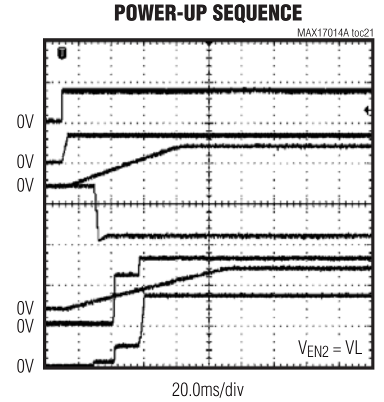



**NEGATIVE CHARGE-PUMP REGULATOR LOAD-TRANSIENT RESPONSE**




A: $V_{GOFF}$, 100mV/div
B: LOAD CURRENT, 65mA/div

**POWER-UP SEQUENCE**

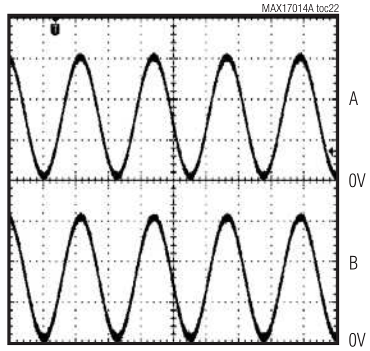



A: $V_{EN1}$, 5V/div
B: $V_{OUT}$, 5V/div
C: $V_{DEL1}$, 5V/div
D: $V_{GOFF}$, 5V/div
E: $V_{AVDD}$, 10V/div
F: $V_{DEL2}$, 5V/div
G: $V_{SRC}$, 20V/div

## Typical Operating Characteristics (continued)

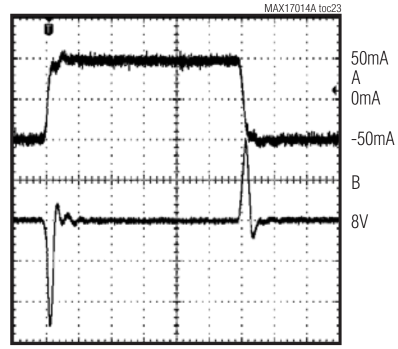
(Circuit of Figure 1. $V_{IN}$ = $V_{INL}$ = $V_{SUPP}$ = 12V, $AV_{DD}$ = 16V, $V_{GON}$ = 34.5V, $V_{GOFF}$ = -6V, $V_{OUT1}$ = 3.3V, $T_A$ = +25°C, unless otherwise noted.)

**OPERATIONAL AMPLIFIER RAIL-TO-RAIL INPUT/OUTPUT**



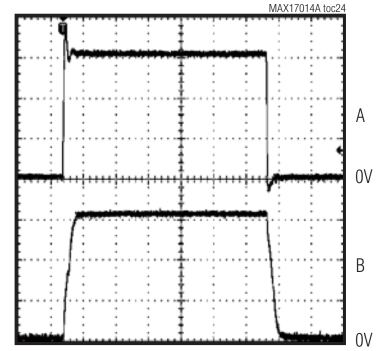

4.0µs/div
A: INPUT SIGNAL, 5V/div
B: OUTPUT SIGNAL, 5V/div

**OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE**



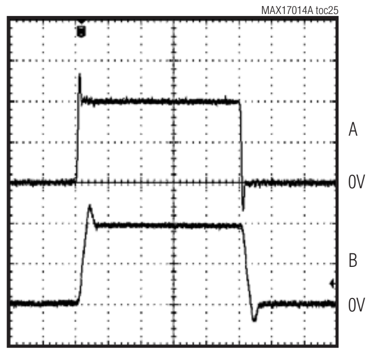

200ns/div
A: OUTPUT CURRENT, 50mA/div
B: OUTPUT VOLTAGE, 500mV/div

**OPERATIONAL AMPLIFIER LARGE-SIGNAL RESPONSE**



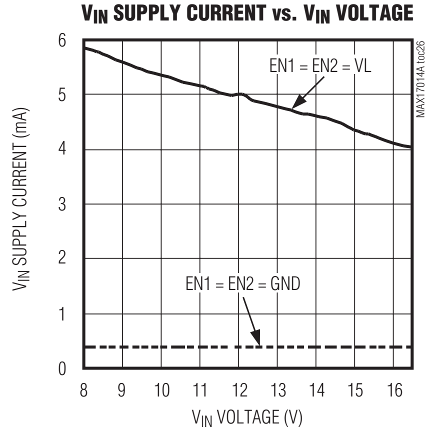

400ns/div
A: INPUT SIGNAL, 5V/div
B: OUTPUT SIGNAL, 5V/div

**OPERATIONAL AMPLIFIER SMALL-SIGNAL RESPONSE**

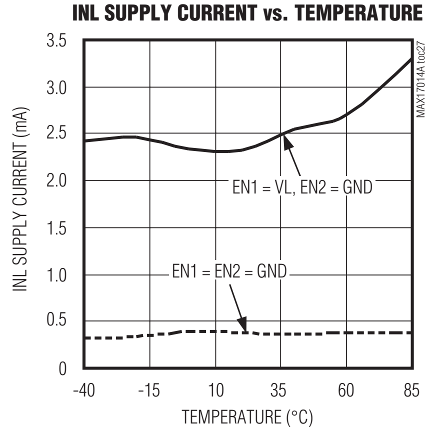



100ns/div
A: INPUT SIGNAL, 200mV/div
B: OUTPUT SIGNAL, 200mV/div

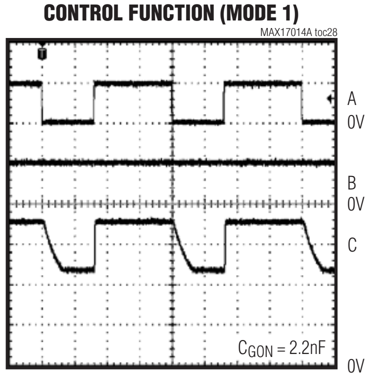
**$V_{IN}$ SUPPLY CURRENT vs. $V_{IN}$ VOLTAGE**




**INL SUPPLY CURRENT vs. TEMPERATURE**

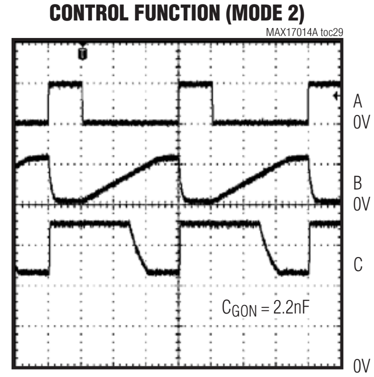



**HIGH-VOLTAGE SWITCH CONTROL FUNCTION (MODE 1)**




4.00µs/div
A: $V_{CTL}$, 5V/div
B: $V_{MODE}$, 5V/div
C: $V_{GON}$, 10V/div

**HIGH-VOLTAGE SWITCH CONTROL FUNCTION (MODE 2)**




4.00µs/div
A: $V_{CTL}$, 5V/div
B: $V_{MODE}$, 2V/div
C: $V_{GON}$, 10V/div

# Low-Cost Multiple-Output Power Supply for LCD TVs

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | POS1 | Operational Amplifier 1 Noninverting Input |
| 2 | OUT1 | Operational Amplifier 1 Output |
| 3 | THR | GON Low-Level Regulation Set-Point Input. Connect THR to the center of a resistive voltage-divider between $AV_{DD}$ and GND to set the $V_{GON}$ falling regulation level. The regulation level is 10 x $V_{THR}$. See the *High-Voltage Switch Control* section for details. |
| 4 | MODE | High-Voltage Switch-Control Block Mode Selection Input and Timing-Adjustment Input. See the *High-Voltage Switch Control* section for details. MODE is high impedance when it is connected to VL. MODE is internally pulled to GND by a 10Ω resistor for 0.1µs typical when the high-voltage switch-control block is enabled. |
| 5 | CTL | High-Voltage Switch-Control Block Timing Control Input. See the *High-Voltage Switch Control* section for details. |
| 6 | DLP | GON Output Enable. See the *High-Voltage Switch Control* section for details. |
| 7 | DRN | Switch Input. Drain of the internal high-voltage p-channel MOSFET between DRN and GON. |
| 8 | GON | Internal High-Voltage MOSFET Switch Common Terminal. GON is the output of the high-voltage switch-control block. |
| 9 | SRC | Switch Input. Source of the internal high-voltage p-channel MOSFET between SRC and GON. |
| 10 | FBP | Positive Charge-Pump Regulator Feedback Input. Connect FBP to the center of a resistive voltage-divider between the positive charge-pump regulator output and GND to set the positive charge-pump regulator output voltage. Place the resistive voltage-divider within 5mm to FBP. |
| 11 | CPGND | Charge Pump and Step-Down Regulator Power Ground |
| 12 | DRVP | Positive Charge-Pump Driver Output. Connect DRVP to the positive charge-pump flying capacitor(s). |
| 13 | SUP | Supply Input for the Charge-Pump Drivers. Connect this pin to the output of the boost regulator SWI and bypass to CPGND with a 0.1µF capacitor. |
| 14 | DRVN | Negative Charge-Pump Driver Output. Connect DRVN to the negative charge-pump flying capacitor(s). |
| 15, 34 | GND | Analog Ground |
| 16 | FBN | Negative Charge-Pump Regulator Feedback Input. Connect FBN to the center of a resistive voltage-divider between the negative output and REF to set the negative charge-pump regulator output voltage. Place the resistive voltage-divider within 5mm of FBN. |
| 17 | REF | Reference Output. Connect a 0.22µF capacitor from REF to GND. All power outputs are disabled until REF exceeds its UVLO threshold. REF is active whenever $V_{IN}$ is above $V_{IN}$ UVLO threshold. |
| 18 | DEL1 | Negative Charge-Pump Delay Input. Connect a capacitor from DEL1 and GND to set the delay time between the step-down output and the negative output. An 8µA current source charges $C_{DEL1}$. DEL1 is internally pulled to GND through 10Ω resistance when EN1 is low or VL is below its UVLO. |
| 19 | N.C. | No Connection. Not internally connected. |
| 20 | OUT | Step-Down Regulator Output-Voltage Sense. Connect OUT to the step-down regulator output. |
| 21 | FB2 | Step-Down Regulator Feedback Input. Connect FB2 to GND to select the step-down converter's 3.3V fixed mode. For adjustable mode, connect FB2 to the center of a resistive voltage-divider between the step-down regulator output and GND to set the step-down regulator output voltage. Place the resistive voltage-divider within 5mm of FB2. |
| 22 | BST | Step-Down Regulator Bootstrap Capacitor Connection for High-Side Gate Driver. Connect a 0.1µF ceramic capacitor from BST to LX2. |

## Pin Description (continued)

| PIN | NAME | FUNCTION |
|---|---|---|
| 23, 24 | LX2 | Step-Down Regulator Switching Node. LX2 is the source of the internal n-channel MOSFET connected between IN2 and LX2. Connect the inductor and Schottky catch diode close to both LX2 pins to minimize the trace area for low EMI. |
| 25, 26 | IN2 | Step-Down Regulator Power Input. Drain of the internal n-channel MOSFET connected between IN2 and LX2. |
| 27 | $V_{IN}$ | Input of the Internal 5V Linear Regulator and the Startup Circuitry. Bypass $V_{IN}$ to GND with 0.22µF close to the IC. |
| 28 | FSEL | Frequency-Select Pin. Connect FSEL to GND for 600kHz operation. Connect to VL or $V_{IN}$ for 1.2MHz operation. |
| 29 | DEL2 | Step-Up Regulator and Positive Charge-Pump Delay Input. Connect a capacitor from DEL2 and GND to set the delay time between EN2 and the startup of these regulators, or between the step-down startup and the startup of these regulators if EN1 is high before the step-down starts. An 8µA current source charges $C_{DEL2}$. DEL2 is internally pulled to GND through 10Ω resistance when EN1 or EN2 is low or when VL is below its UVLO threshold. |
| 30 | VL | 5V Internal Linear Regulator Output. Bypass VL to GND with 1µF minimum. Provides power for the internal MOSFET driving circuit, the PWM controllers, charge-pump regulators, logic, and reference and other analog circuitry. Provides 25mA load current when all switching regulators are enabled. VL is active whenever $V_{IN}$ is above $V_{IN}$ UVLO threshold. |
| 31 | COMP | Compensation Pin for the Step-Up Error Amplifier. Connect a series resistor and capacitor from COMP to ground. |
| 32 | EN2 | Step-Up and Positive Charge-Pump Regulator Enable Input. Input HIGH also enables DEL2 pullup current. EN2 is inactive when EN1 is low. See the *Power-Up Sequence* section for details. |
| 33 | EN1 | Step-Down and Negative Charge-Pump Regulator Enable Input. Input HIGH also enables DEL1 pullup current. |
| 35, 36 | GND1 | Step-Up Regulator Power Ground. Source of the internal power n-channel MOSFET. |
| 37, 38 | LX1 | Step-Up Regulator Power MOSFET n-Channel Drain and Switching Node. Connect the inductor and Schottky catch diode to both LX1 pins and minimize the trace area for lowest EMI. |
| 39 | SWI | Step-Up Regulator Internal p-Channel MOSFET Pass Switch Source Input. Connect to the cathode of the step-up regulator Schottky catch diode. |
| 40 | SUI | Step-Up Regulator Internal p-Channel MOSFET Pass Switch Gate Input. Connect a capacitor from SUI to SWI to set the delay time. A 30µA current source pulls down on $C_{SUI}$ when DEL2 is high. |
| 41 | FB1 | Boost Regulator Feedback Input. Connect FB1 to the center of a resistive voltage-divider between the boost regulator output and GND to set the boost regulator output voltage. Place the resistive voltage-divider within 5mm of FB1. |
| 42 | SWO | Step-Up Regulator Internal p-Channel MOSFET Pass Switch Drain Output |
| 43 | OVIN | Operational Amplifier Power Input |
| 44 | NEG2 | Operational Amplifier 2 Inverting Input |
| 45 | POS2 | Operational Amplifier 2 Noninverting Input |
| 46 | OUT2 | Operational Amplifier Output 2 |
| 47 | OGND | Operational Amplifier Power Ground |
| 48 | NEG1 | Operational Amplifier 1 Inverting Input |
| — | EP | Exposed Pad = GND |

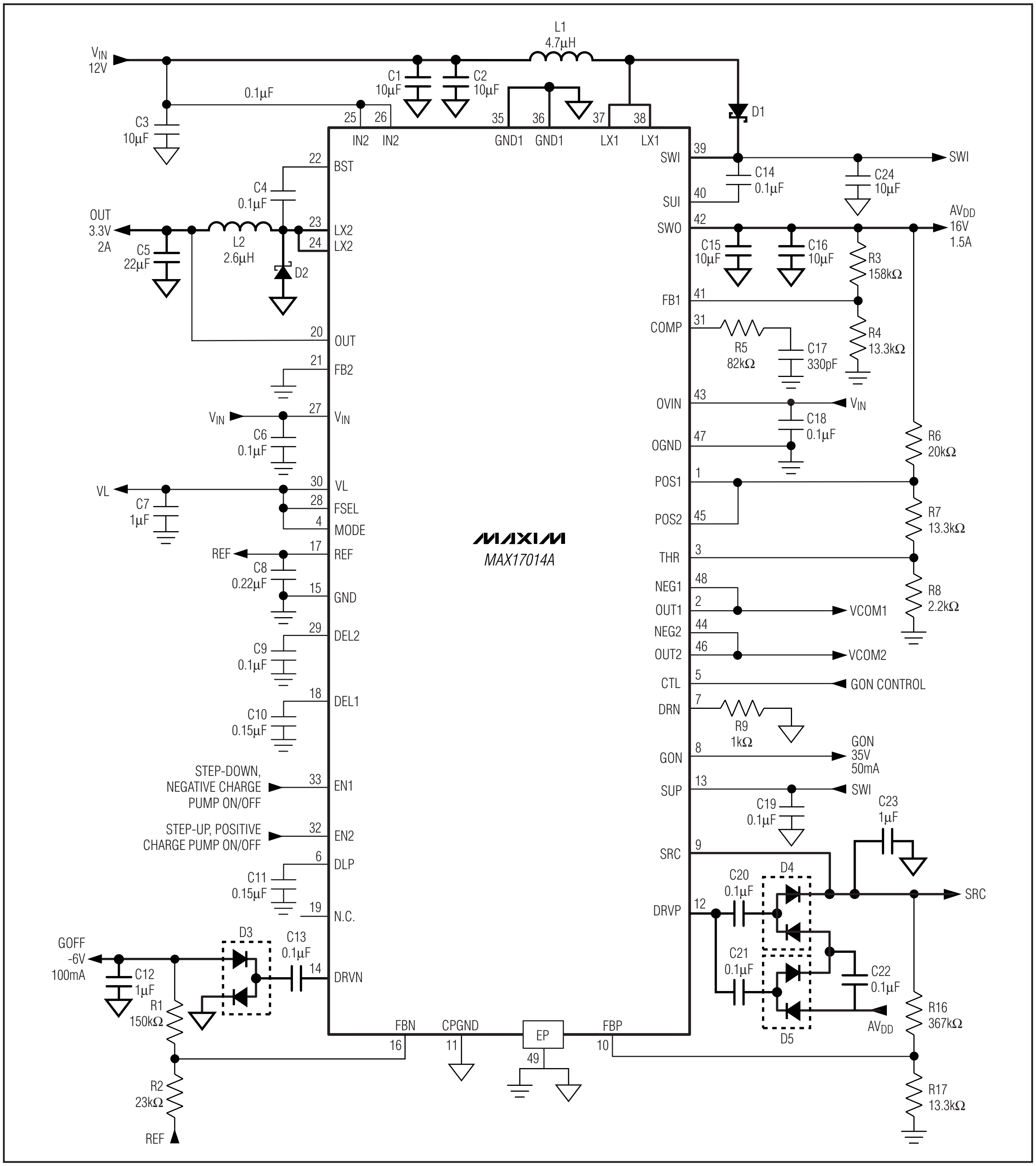


Figure 1. Typical Operating Circuit

## Typical Operating Circuit

The typical operating circuit (Figure 1) of the MAX17014A is a complete power-supply system for TFT LCD panels in monitors and TVs. The circuit generates a +3.3V logic supply, a +16V source driver supply, a +34.5V positive gate driver supply, and a -6V negative gate driver supply from a 12V ±10% input supply. Table 1 lists some selected components and Table 2 lists the contact information for component suppliers.

### Table 1. Component List

| DESIGNATION | DESCRIPTION |
|---|---|
| C1, C2, C3 | 10µF ±20%, 16V X5R ceramic capacitors (1206)<br>Taiyo Yuden EMK325BJ106MD<br>TDK C3225X7R1C106M |
| C5 | 22µF ±10%, 6.3V X5R ceramic capacitor (1206)<br>Taiyo Yuden JMK316BJ226KL<br>Murata GRM31CR60J226M |
| C15, C16, C24 | 10µF ±20%, 25V X5R ceramic capacitors (1210)<br>TDK C3225X5R1E106M |
| D1, D2 | 3A, 30V Schottky diodes (M-Flat)<br>Toshiba CMS02 (TE12L,Q)<br>Central Semiconductor |
| D3, D4, D5 | 200mA, 100V dual ultra-fast diodes (SOT23)<br>Fairchild MMBD4148SE (top mark D4)<br>Central Semiconductor CMPD1001S lead free (top mark L21) |
| L1 | Low-profile 4.7µH, 3.5A inductor (2mm height)<br>TOKO FDV0620-4R7M |
| L2 | Low-profile 2.4µH, 2.6A inductor (1.8mm height)<br>TOKO 1124BS-2R4M (2.4µH)<br>Wurth 744052002 (2.5µH) |

## Detailed Description

The MAX17014A is a multiple-output power supply designed primarily for TFT LCD panels used in monitors and TVs. It contains a step-down switching regulator to generate the logic supply rail, a step-up switching regulator to generate the source driver supply, and two charge-pump regulators to generate the gate driver supplies. Each regulator features adjustable output voltage, digital soft-start, and timer-delayed fault protection. Both the step-down and step-up regulators use a fixed-frequency current-mode control architecture. The two switching regulators are 180° out-of-phase to minimize the input ripple. The internal oscillator offers two pin-selectable frequency options (600kHz/1.2MHz), allowing users to optimize their designs based on the specific application requirements. The MAX17014A includes two high-performance operational amplifiers designed to drive the LCD backplane (VCOM). The amplifiers feature high output current (±150mA), fast slew rate (100V/µs), wide bandwidth (20MHz), and rail-to-rail inputs and outputs. In addition, the MAX17014A features a high-voltage switch-control block, an internal 5V linear regulator, a 1.25V reference output, well-defined power-up and power-down sequences, and thermal-overload protection. Figure 2 shows the MAX17014A functional diagram.

### Step-Down Regulator

The step-down regulator consists of an internal n-channel MOSFET with gate driver, a lossless current-sense network, a current-limit comparator, and a PWM controller block. The external power stage consists of a Schottky diode rectifier, an inductor, and output capacitors. The output voltage is regulated by changing the duty cycle of the n-channel MOSFET. A bootstrap circuit that uses a 0.1µF flying capacitor between LX2 and BST provides the supply voltage for the high-side gate driver. Although the MAX17014A also includes a 10Ω (typ) low-side MOSFET, this switch is used to charge the bootstrap capacitor during startup and maintains fixed-frequency operation at light load and cannot be used as a synchronous rectifier. An external Schottky diode (D2 in Figure 1) is always required.

### Table 2. Component Suppliers

| SUPPLIER | PHONE | FAX | WEBSITE |
|---|---|---|---|
| Fairchild Semiconductor | 408-822-2000 | 408-822-2102 | www.fairchildsemi.com |
| Sumida | 847-545-6700 | 847-545-6720 | www.sumida.com |
| TDK | 847-803-6100 | 847-390-4405 | www.component.tdk.com |
| Toshiba | 949-455-2000 | 949-859-3963 | www.toshiba.com/taec |

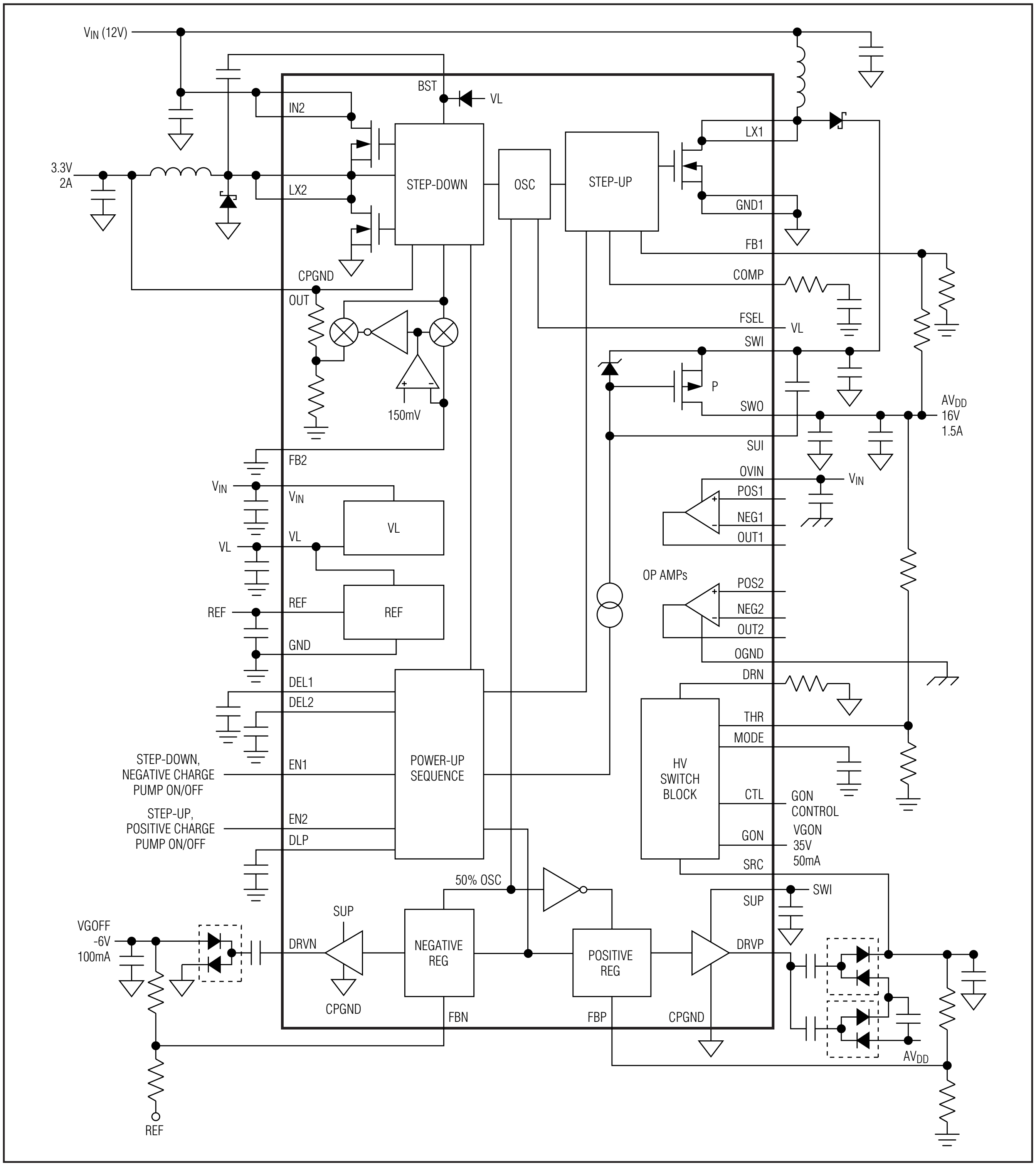



*Figure 2. Functional Diagram*

#### PWM Controller Block

The heart of the PWM control block is a multi-input, open-loop comparator that sums three signals: the output voltage signal with respect to the reference voltage, the current-sense signal, and the slope compensation. The PWM controller is a direct-summing type, lacking a traditional error amplifier and the phase shift associated with it. This direct-summing configuration approaches ideal cycle-by-cycle control over the output voltage.

When EN1 and EN2 are high, the controller always operates in fixed-frequency PWM mode. Each pulse from the oscillator sets the main PWM latch that turns on the high-side switch until the PWM comparator changes state.

When EN1 is high and EN2 is low, the controller operates in skip mode. The skip mode dramatically improves light-load efficiency by reducing the effective frequency, which reduces switching losses. It keeps the peak inductor current at about 0.9A (typ) in an active cycle, allowing subsequent cycles to be skipped. Skip mode transitions seamlessly to fixed-frequency PWM operation as load current increases.

#### Current Limiting and Lossless Current Sensing

The current-limit circuit turns off the high-side MOSFET switch whenever the voltage across the high-side MOSFET exceeds an internal threshold. The actual current limit is 3A (typ).

For current-mode control, an internal lossless sense network derives a current-sense signal from the inductor DCR. The time constant of the current-sense network is not required to match the time constant of the inductor and has been chosen to provide sufficient current ramp signal for stable operation at both operating frequencies. The current-sense signal is AC-coupled into the PWM comparator, eliminating most DC output-voltage variation with load current.

#### Low-Frequency Operation

The step-down regulator of the MAX17014A enters into low-frequency operating mode if the voltage on OUT is below 0.8V. In the low-frequency mode, the switching frequency of the step-down regulator is 1/6 the oscillator frequency. This feature prevents potentially uncontrolled inductor current if OUT is overloaded or shorted to ground.

#### Dual-Mode Feedback

The step-down regulator of the MAX17014A supports both fixed and adjustable output voltages. Connect FB2 to GND to enable the 3.3V fixed output voltage. Connect a resistive voltage-divider between OUT and GND with the center tap connected to FB2 to adjust the output voltage. Choose RB (resistance from FB2 to GND) to be between 5kΩ and 50kΩ, and solve for RA (resistance from OUT1 to FB1) using the equation:

$$RA = RB \times \left( \frac{V_{OUT}}{V_{FB2}} - 1 \right)$$

where $V_{FB2}$ = 1.25V, and $V_{OUT}$ can vary from 1.25V to 5V.

Because of FB2's (pin 21) close proximity to the noisy BST (pin 22), a noise filter is required for FB2 adjustable-mode operation. Place a 100pF capacitor from FB2 to GND to prevent unstable operation. No filter is required for 3.3V fixed-mode operation.

#### Soft-Start

The step-down regulator includes a 7-bit soft-start DAC that steps its internal reference voltage from 0 to 1.25V in 128 steps. The soft-start period is 3ms (typ) and FB1 fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup (see the Step-Down Regulator Soft-Start (Heavy Load) waveforms in the *Typical Operating Characteristics*).

### Step-Up Regulator

The step-up regulator employs a current-mode, fixed-frequency PWM architecture to maximize loop bandwidth and provide fast-transient response to pulsed loads typical of TFT LCD panel source drivers. The integrated MOSFET and the built-in digital soft-start function reduce the number of external components required while controlling inrush currents. The output voltage can be set from $V_{VIN}$ to 20V with an external resistive voltage-divider. The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{AVDD} - V_{VIN}}{V_{AVDD}}$$

where $V_{AVDD}$ is the output voltage of the step-up regulator.

#### PWM Controller Block

An error amplifier compares the signal at FB1 to 1.25V and changes the COMP output. The voltage at COMP sets the peak inductor current. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope compensation signal is summed with the current-sense signal.

# Low-Cost Multiple-Output Power Supply for LCD TVs

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

### Step-Up Regulator Internal p-Channel MOSFET Pass Switch

The MAX17014A includes an integrated 120mΩ high-voltage p-channel MOSFET to allow true shutdown of the step-up converter output ($AV_{DD}$). This switch is typically connected in series between the step-up regulator's Schottky catch diode and its output capacitors. In addition to allowing step-up output to discharge completely when disabled, this switch also controls the startup inrush current into the step-up regulator's output capacitors.

When EN2 is low, SUI is internally pulled up to SWI through an internal 1kΩ resistor. Once EN2 is high and the step-down regulator is in regulation, the MAX17014A starts pulling down SUI with a 30µA internal current source. The internal p-channel MOSFET turns on and connects the cathode of the step-up regulator Schottky catch diode to the step-up regulator load capacitors, when $V_{SUI}$ falls below the turn-on threshold of the MOSFET. When $V_{SUI}$ reaches ($V_{SWI}$ - 5V), the step-up regulator and the positive charge pump are enabled and initiate a soft-start routine.

### Soft-Start

The step-up regulator achieves soft-start by linearly ramping up its internal current limit. The soft-start terminates when the output reaches regulation or the full current limit has been reached. The current limit rises from zero to the full current limit in approximately 3ms. The soft-start feature effectively limits the inrush current during startup (see the Step-Up Regulator Soft-Start (Heavy Load) waveforms in the *Typical Operating Characteristics*).

## Positive Charge-Pump Regulator

The positive charge-pump regulator is typically used to generate the positive supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external resistive voltage-divider from its output to GND with the midpoint connected to FBP. The number of charge-pump stages and the setting of the feedback divider determine the output voltage of the positive charge-pump regulator. The charge pump includes a high-side p-channel MOSFET (P1) and a low-side n-channel MOSFET (N1) to control the power transfer as shown in Figure 3.

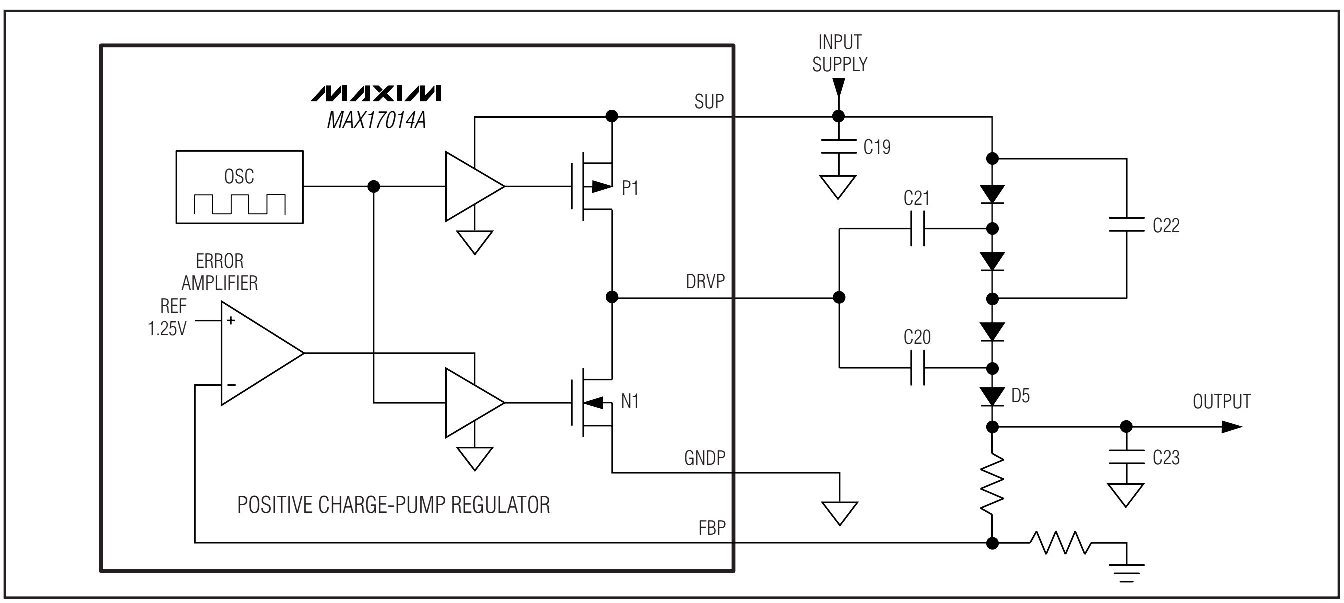



*Figure 3. Positive Charge-Pump Regulator Block Diagram*

During the first half-cycle, N1 turns on and charges flying capacitors C20 and C21 (Figure 3). During the second half cycle, N1 turns off and P1 turns on, level shifting C20 and C21 by $V_{SUP}$ volts. If the voltage across C23 plus a diode drop ($V_{OUT}$ + $V_D$) is smaller than the level-shifted flying capacitor voltage ($V_{C20}$ + $V_{SUP}$), charge flows from C20 to C23 until the diode (D5) turns off. The amount of charge transferred to the output is determined by the error amplifier that controls N1's on-resistance.

The positive charge-pump regulator's startup can be delayed by connecting an external capacitor from DEL2 to GND. An internal constant-current source begins charging the DEL2 capacitor when EN2 is logic-high, and the step-down regulator reaches regulation. When the DEL2 voltage exceeds $V_{REF}$, the positive charge-pump regulator is enabled. Each time it is enabled, the positive charge-pump regulator goes through a soft-start routine by ramping up its internal reference voltage from 0 to 1.25V in 128 steps. The soft-start period is 3ms (typ) and FBP fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup.

### *Negative Charge-Pump Regulator*

The negative charge-pump regulator is typically used to generate the negative supply rail for the TFT LCD gate driver ICs. The output voltage is set with an external resistive voltage-divider from its output to REF with the midpoint connected to FBN. The number of charge-pump stages and the setting of the feedback divider determine the output of the negative charge-pump regulator. The charge-pump controller includes a high-side p-channel MOSFET (P2) and a low-side n-channel MOSFET (N2) to control the power transfer as shown in Figure 4.

During the first half cycle, P2 turns on, and flying capacitor C13 charges to $V_{SUP}$ minus a diode drop (Figure 4). During the second half cycle, P2 turns off, and N2 turns on, level shifting C13. This connects C13 in parallel with reservoir capacitor C12. If the voltage across C12 minus a diode drop is greater than the voltage across C13, charge flows from C12 to C13 until the diode (D3) turns off. The amount of charge transferred from the output is determined by the error amplifier, which controls N2's on-resistance.

The negative charge-pump regulator is enabled when EN1 is logic-high and the step-down regulator reaches regulation. Each time it is enabled, the negative charge-pump regulator goes through a soft-start routine by ramping down its internal reference voltage from 1.25V to 250mV in 102 steps. The soft-start period is 3ms (typ) and FBN fault detection is disabled during this period. The soft-start feature effectively limits the inrush current during startup.

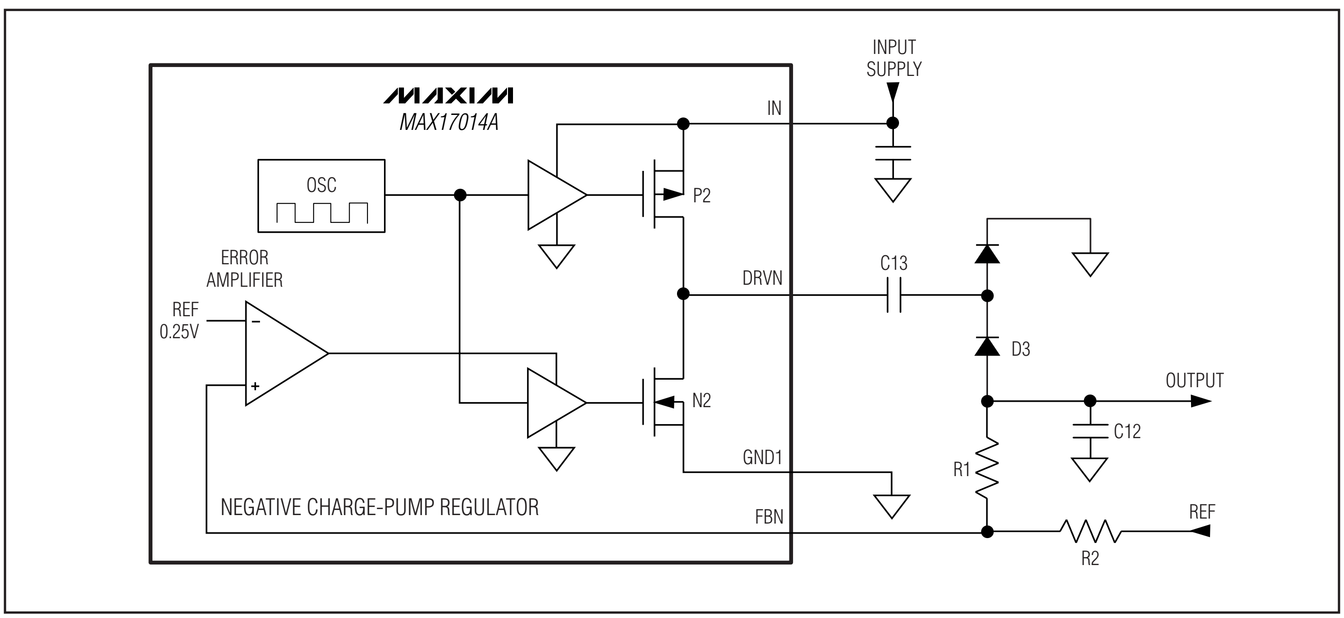



*Figure 4. Negative Charge-Pump Regulator Block Diagram*

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### High-Voltage Switch Control

The MAX17014A's high-voltage switch control block (Figure 5) consists of two high-voltage p-channel MOSFETs: Q1, between SRC and GON and Q2, between GON and DRN. The switch control block is enabled when $V_{DLP}$ exceeds $V_{REF}$. Q1 and Q2 are controlled by CTL and MODE. There are two different modes of operation (see the *Typical Operating Characteristics*).

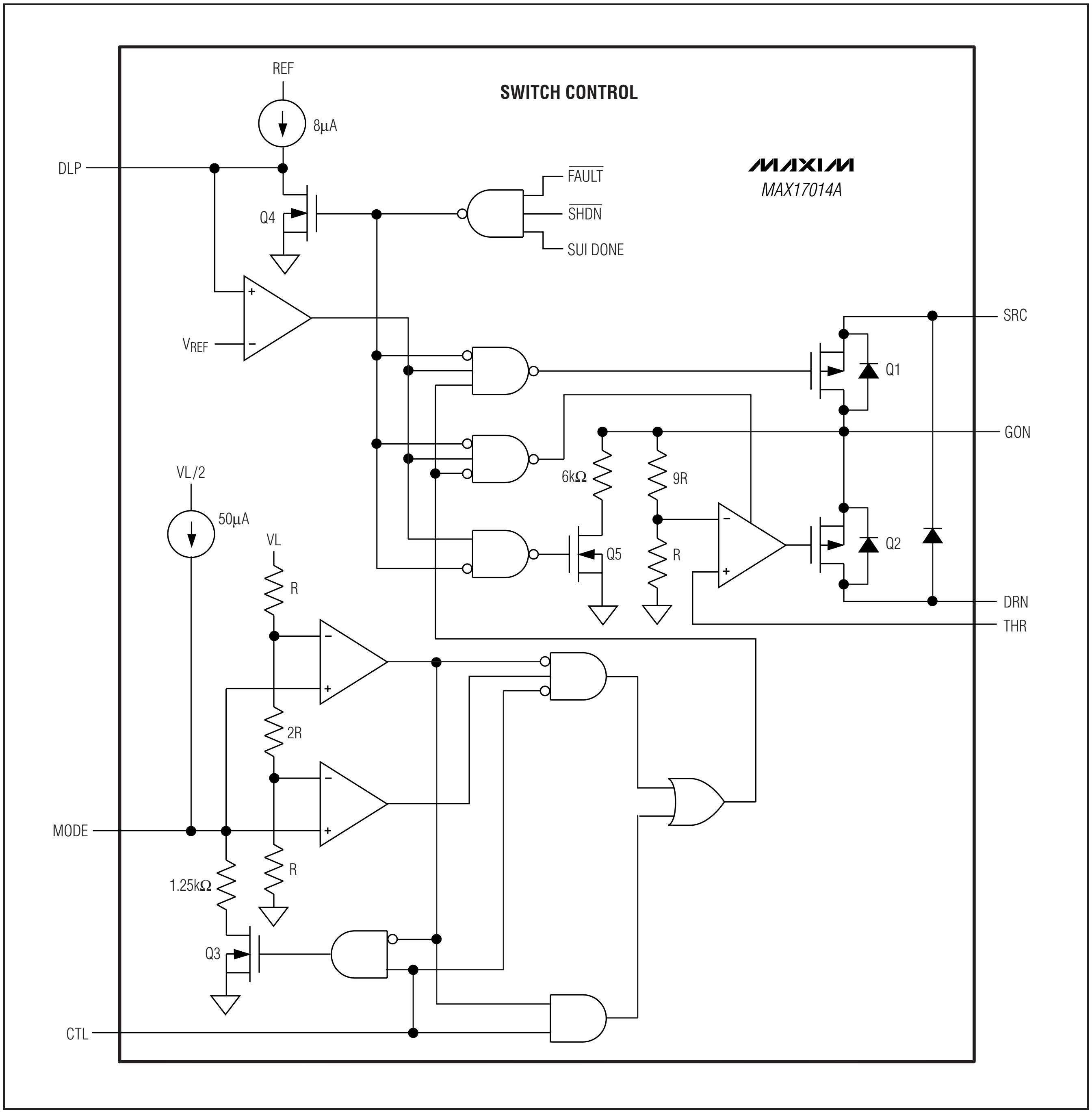


*Figure 5. Switch Control*

Select the first mode by connecting MODE to VL. When CTL is logic-high, Q1 turns on and Q2 turns off, connecting GON to SRC. When CTL is logic-low, Q1 turns off and Q2 turns on, connecting GON to DRN. GON can then be discharged through a resistor connected between DRN and GND or $AV_{DD}$. Q2 turns off and stops discharging GON when $V_{GON}$ reaches 10 times the voltage on THR.

When $V_{MODE}$ is less than 0.8 x $V_{VL}$, the switch control block works in the second mode. The rising edge of $V_{CTL}$ turns on Q1 and turns off Q2, connecting GON to SRC. An internal n-channel MOSFET, Q3, between MODE and GND is also turned on to discharge an external capacitor between MODE and GND. The falling edge of $V_{CTL}$ turns off Q3, and an internal 50µA current source starts charging the MODE capacitor. Once $V_{MODE}$ exceeds $V_{VL/4}$, the switch control block turns off Q1 and turns on Q2, connecting GON to DRN. GON can then be discharged through a resisor connected between DRN and GND or $AV_{DD}$. Q2 turns off and stops discharging GON when $V_{GON}$ reaches 10 times the voltage on THR.

The switch control block is disabled and DLP is held low when EN1 or EN2 is low or the IC is in a fault state.

### Operational Amplifiers

The MAX17014A has two operational amplifiers. The operational amplifiers are typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. They feature ±150mA output short-circuit current, 100V/µs slew rate, and 20MHz, -3dB bandwidth. While the op amp is a rail-to-rail input and output design, its accuracy is significantly degraded for input voltages within 2V of its supply rails (OVIN, OGND).

#### Short-Circuit Current Limit and Input Clamp

The operational amplifiers limit short-circuit current to approximately ±150mA (-250mA) if the output is directly shorted to OVIN (OGND). If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+160°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor immediately sets the thermal-fault latch, shutting off all the IC's outputs. The device remains inactive until the input voltage is cycled. The operational amplifiers have 4V input clamp structures in series with a 500Ω resistance (Figure 6).

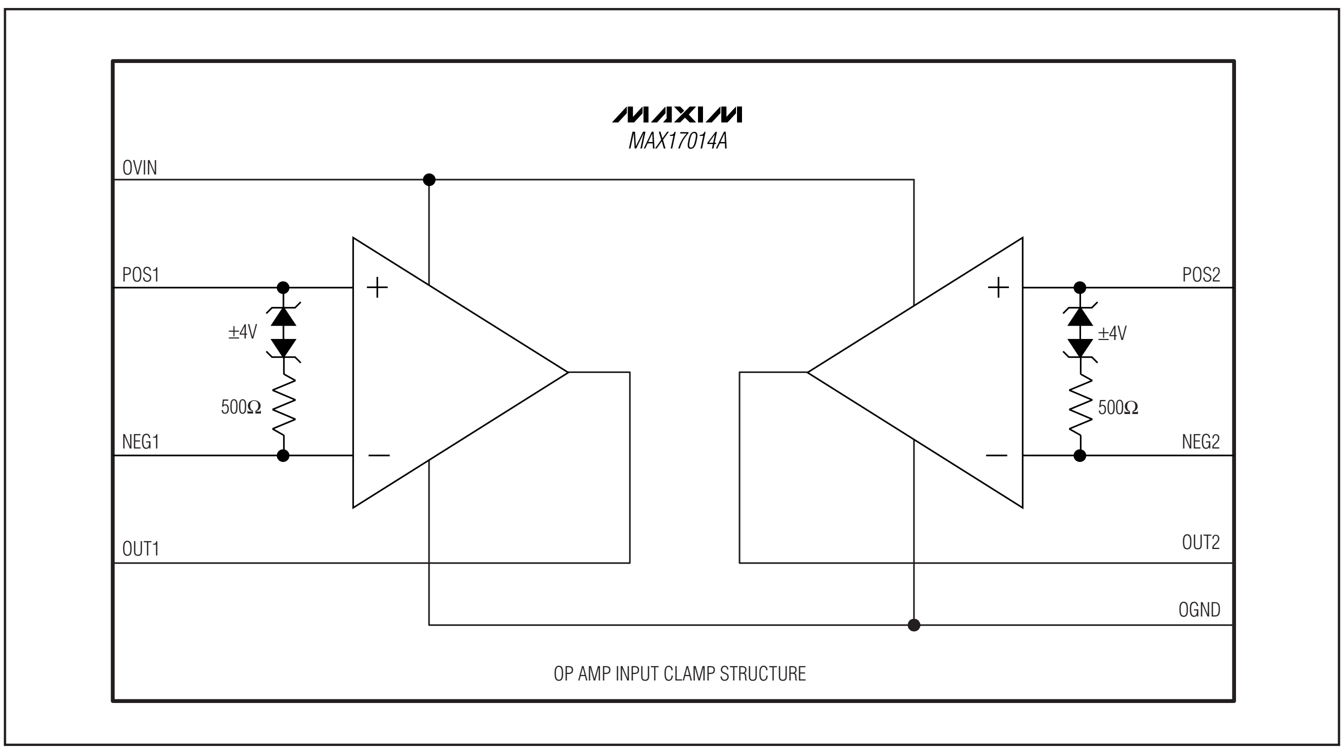


*Figure 6. Op Amp Input Clamp Structure*

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### Driving Pure Capacitive Load

The operational amplifiers are typically used to drive the LCD backplane (VCOM) or the gamma-correction divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation. As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between OUT_ and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω, and the typical value of the capacitor is 10nF.

### Linear Regulator (VL)

The MAX17014A includes an internal linear regulator. $V_{IN}$ is the input of the linear regulator. The input voltage range is between 8V and 16.5V. The output voltage is set to 5V. The regulator powers the internal MOSFET drivers, PWM controllers, charge-pump regulators, and logic circuitry. The total external load capability is 25mA. Bypass VL to GND with a minimum 1μF ceramic capacitor.

### Reference Voltage (REF)

The reference output is nominally 1.25V, and can source at least 50μA (see the *Typical Operating Characteristics*). VL is the input of the internal reference block. Bypass REF with a 0.22μF ceramic capacitor connected between REF and GND.

### Frequency Selection (FSEL)

The step-down regulator and step-up regulator use the same internal oscillator. The FSEL input selects the switching frequency. Table 3 shows the switching frequency based on the FSEL connection. High-frequency (1.2MHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. Low-frequency (600kHz) operation offers the best overall efficiency at the expense of component size and board space.

## Table 3. Frequency Selection

| FSEL | SWITCHING FREQUENCY (kHz) |
|---|---|
| $V_{IN}$ | 1200 |
| GND | 600 |

### Power-Up Sequence

The step-down regulator starts up when the MAX17014A's internal reference voltage (REF) is above its undervoltage lockout (UVLO) threshold and EN1 is logic-high. Once the step-down regulator reaches regulation, the FB2 fault-detection circuit and the negative charge-pump delay block are enabled. An 8μA current source at DEL1 charges $C_{DEL1}$ linearly. The negative charge-pump regulator soft-starts when $V_{DEL1}$ reaches $V_{REF}$. FBN fault detection is enabled once the negative charge-pump soft-start is done.

The step-up regulator, p-channel MOSFET pass switch, and positive charge-pump startup sequence begin when the step-down regulator reaches regulation and EN2 is logic-high. An 8μA current source at DEL2 charges $C_{DEL2}$ linearly and the p-channel MOSFET pass switch is enabled when $V_{DEL2}$ reaches $V_{REF}$. A 30μA current source pulls down on SUI, slowly turning on the p-channel MOSFET switch between SWI and SWO. The step-up regulator, positive charge pump, and the delay block for the high-voltage switch starts when the SWI to SUI voltage difference ($V_{SWI}$ - $V_{SUI}$) reaches the SUI-done threshold (5V, typ). An 8μA current source charges $C_{DLP}$ linearly and when $V_{DLP}$ reaches $V_{REF}$, the high-voltage switch is enabled and GON can be controlled by CTL.

The FB1 fault-detection circuit is enabled after the step-up regulator reaches regulation, and similarly the FBP fault-detection circuit is enabled after the positive charge pump reaches regulation. For nondelayed startups, capacitors can be omitted from DEL1, DEL2, and DLP. When their current sources pull the floating pins above their thresholds, the associated outputs start.

### Power-Down Control

The MAX17014A disables the step-up regulator, positive-charge-pump regulator input switch control block, delay block, and high-voltage switch control block when EN2 is logic-low, or when the fault latch is set. The step-down regulator and negative charge-pump regulator are disabled only when EN1 is logic-low or when the fault latch is set.

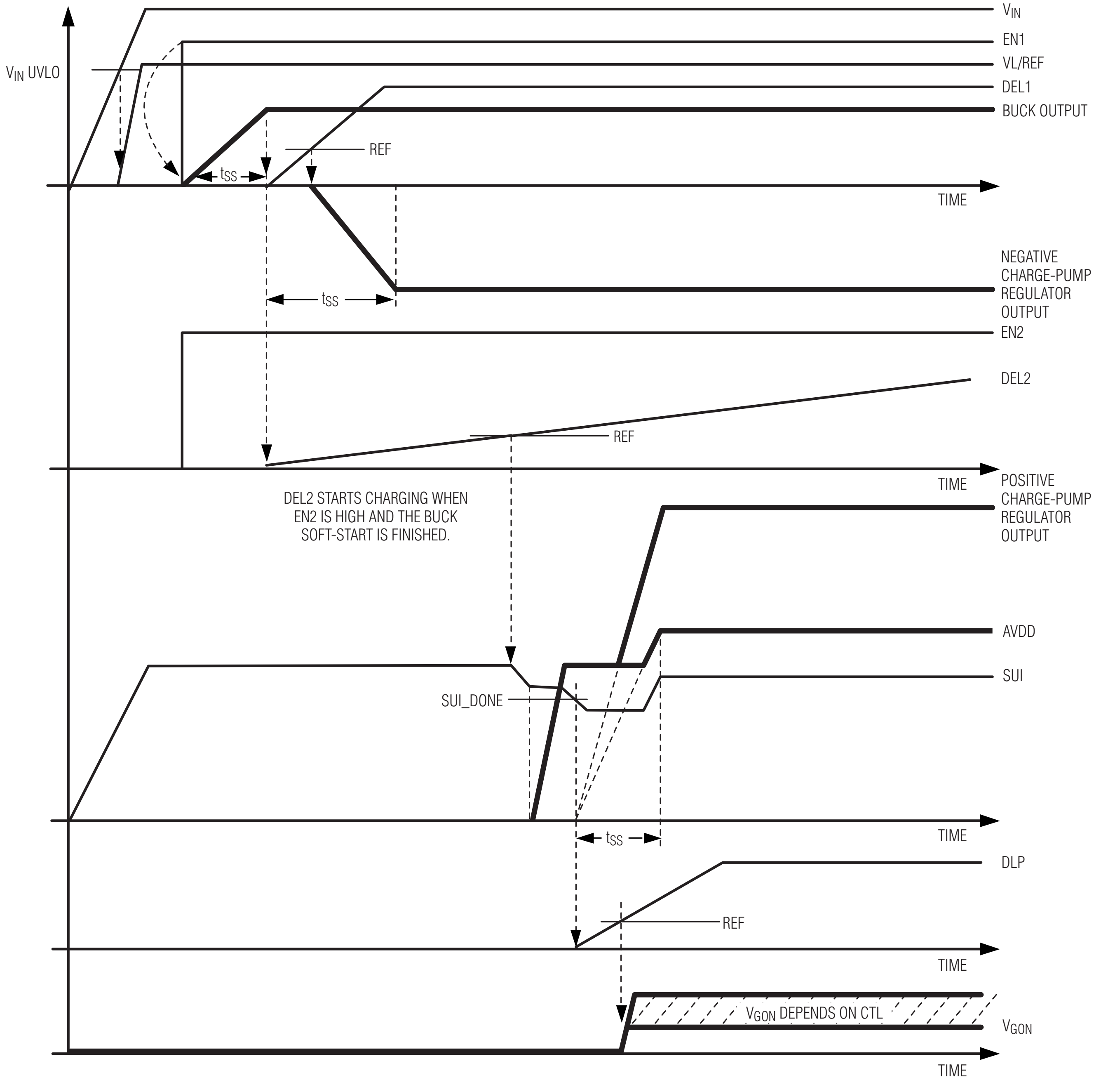


*Figure 7. Power-Up Sequence*