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Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

General Description

The MAX17020 is a dual Quick-PWM™ step-down power-supply (SMPS) controller with synchronous rectification, intended for main 5V/3.3V or I/O 1.5V/1.05V power generation in battery-powered systems. Low-side MOSFET sensing provides a simple low-cost, highly efficient current sense for valley current-limit protection. Combined with the output overvoltage and undervoltage protection features, this current limit ensures robust output supplies.

The 5V/3.3V or 1.5V/1.05V SMPS outputs can save power by operating in pulse-skipping mode or in ultrasonic mode to avoid audible noise. Ultrasonic mode forces the controller to maintain switching frequencies greater than 20kHz at light loads.

An internal 100mA linear regulator can be used to either generate the 5V bias needed for power-up or other lower power “always-on” suspend supplies. An independent bypass input allows automatic bypassing of the linear regulator when the SMPS is active.

This main controller also includes a secondary feedback input that triggers an ultrasonic pulse (DL1 turned on) if the SECFB voltage drops below its threshold voltage. This refreshes an external charge pump driven by DL1 without overcharging the output voltage.

The device includes independent shutdown controls to simplify power-up and power-down sequencing. To prevent current surges at startup, the internal voltage target is slowly ramped up from zero to the final target over a 1ms period. To prevent the output from ringing below ground in shutdown, the internal voltage target is ramped down from its previous value to zero over a 1ms period. Two independent power-good outputs simplify the interface with external controllers.

The MAX17020 is a pin-for-pin replacement of the MAX8778.

Applications

Notebook Computers
Main System Supply (5V and 3.3V Supplies)
I/O System Supply (1.5V and 1.05V Supplies)
Graphic Cards
DDR1, DDR2, DDR3 Power Supplies
Game Consoles
Low-Power I/O and Chipset Supplies
Two-to-Four Li+ Cell Battery-Powered Devices
PDAs and Mobile Communicators
Telecommunication

Features

- ◆ Dual Quick-PWM
- ◆ Internal 100mA 5V or Adjustable Linear Regulator
- ◆ Independent LDO Bypass Input
- ◆ Internal Boost Diodes
- ◆ Secondary Feedback Input Maintains Charge Pump
- ◆ 3.3V 5mA RTC Power (Always On)
- ◆ OUT1: 5V or 1.5V Fixed or 0.7V Adjustable Feedback
- ◆ OUT2: 3.3V or 1.05V Fixed or Dynamic Adjustable
- ◆ Dynamic 0V to 2V REFIN2 Input on Second SMPS
- ◆ 2V ±1% 50µA Reference
- ◆ 6V to 24V Input Range (28V max)
- ◆ Ultrasonic Mode
- ◆ Independent SMPS and LDO Enable Controls
- ◆ Independent SMPS Power-Good Outputs
- ◆ Minimal Component Count

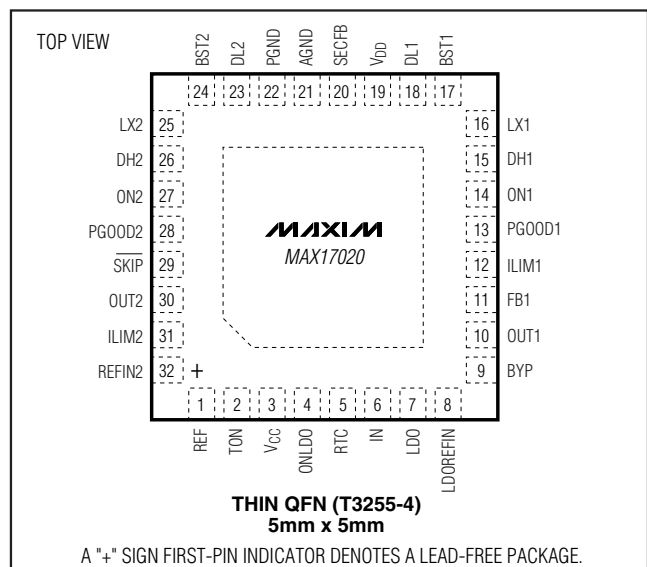
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17020ETJ+	-40°C to +85°C	32 TQFN

+ Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Pin Configuration



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Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

ABSOLUTE MAXIMUM RATINGS

IN, ONLDO to GND	-0.3V to +28V	BST1 to LX1	-0.3V to +6V
V _{DD} , V _{CC} to GND	-0.3V to +6V	DH2 to LX2	-0.3V to (V _{BST2} + 0.3V)
RTC, LDO to GND	-0.3V to +6V	BST2 to LX2	-0.3V to +6V
OUT ₁ to GND	-0.3V to +6V	LDO, RTC, REF Short Circuit to GND	Momentary
ON1, ON2 to GND	-0.3V to +6V	RTC Current Continuous	+5mA
PGOOD ₁ to GND	-0.3V to (V _{CC} + 0.3V)	LDO Current (Internal Regulator)	Continuous.....+100mA
REF, ILIM ₁ , TON, SKIP to GND	-0.3V to (V _{CC} + 0.3V)	LDO Current (Switched Over) Continuous	+200mA
FB1, REFIN2, LDOREFIN to GND	-0.3V to +6V	Continuous Power Dissipation (T _A = +70°C)	32-Pin 5mm x 5mm TQFN
SECFB to GND	-0.3V to +6V	(derate 34.5mW/°C above +70°C)2.76W
BYP to GND	-0.3V to (V _{LDO} + 0.3V)	Operating Temperature Range-40°C to +85°C
GND to PGND	-0.3V to +0.3V	Junction Temperature+150°C
DL ₁ to PGND	-0.3V to (V _{DD} + 0.3V)	Storage Temperature Range-65°C to +150°C
BST ₁ to GND	-0.3V to +34V	Lead Temperature (soldering, 10s)+300°C
BST ₁ to V _{DD}	-0.3V to +28V		
DH1 to LX1	-0.3V to (V _{BST1} + 0.3V)		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, no load on LDO, RTC, OUT₁, OUT₂, and REF, V_{IN} = 12V, V_{DD} = V_{CC} = V_{SECFB} = 5V, V_{REFIN2} = 1.0V, BYP = LDOREFIN = GND, ONLDO = IN, ON1 = ON2 = V_{CC}, T_A = 0°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
IN Standby Supply Current	I _{IN(STBY)}	V _{IN} = 6V to 24V, ON1 = ON2 = GND, ONLDO = V _{CC}		85	175	μA
IN Shutdown Supply Current	I _{IN(SHDN)}	V _{IN} = 4.5V to 24V, ON1 = ON2 = ONLDO = GND		50	70	μA
IN Supply Current	I _{IN}	ON1 = ON2 = REFIN2 = V _{CC} , SKIP = FB1 = GND, V _{OUT2} = 3.5V, V _{OUT1} = 5.3V		0.1	0.2	mA
V _{CC} Supply Current	I _{CC}	ON1 = ON2 = REFIN2 = V _{CC} , SKIP = FB1 = GND, V _{OUT2} = 3.5V, V _{OUT1} = 5.3V		1.0	1.5	mA
PWM CONTROLLERS						
OUT ₁ Output Voltage Accuracy (Note 1)	V _{OUT1}	5V preset output: FB1 = GND, V _{IN} = 12V, SKIP = V _{CC}	4.95	5.00	5.05	V
		1.5V preset output: FB1 = V _{CC} (5V), V _{IN} = 12V, SKIP = V _{CC}	1.485	1.50	1.515	
	V _{FB1}	Adjustable feedback output, V _{IN} = 12V, SKIP = V _{CC}	0.693	0.700	0.707	
OUT ₁ Voltage Adjust Range			0.7		5.5	V
FB1 Dual-Mode™ Threshold Voltage Levels		Low		0.04	0.110	V
		High		V _{CC} - 1.6V	V _{CC} - 0.7V	
FB1 Input Bias Current	I _{FB1}	V _{FB1} = 0.8V, T _A = +25°C	-0.2		+0.2	μA

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF, $V_{IN} = 12V$, $V_{DD} = V_{CC} = V_{SECFB} = 5V$, $V_{REFIN2} = 1.0V$, $BYP = LDOREFIN = GND$, $ONLDO = IN$, $ON1 = ON2 = V_{CC}$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
OUT2 Output Voltage Accuracy (Note 1)	V_{OUT2}	3.3V preset output: $REFIN2 = V_{CC} (5V)$, $V_{IN} = 12V$, $\overline{SKIP} = V_{CC}$	3.267	3.30	3.333	V	
		1.05V preset output: $REFIN2 = RTC (3.3V)$, $V_{IN} = 12V$, $\overline{SKIP} = V_{CC}$	1.040	1.050	1.060		
		Tracking output: $V_{REFIN2} = 1.0V$, $V_{IN} = 12V$, $\overline{SKIP} = V_{CC}$	0.995	1.00	1.005		
OUT2 Voltage-Adjust Range			0		2	V	
REFIN2 Voltage-Adjust Range			0		2	V	
REFIN2 Input Bias Current	I_{REFIN2}	$V_{REFIN2} = 2.2V$, $T_A = +25^{\circ}C$	-0.1		+0.1	μA	
		$V_{REFIN2} = 0$, $T_A = +25^{\circ}C$	-0.5		+0.1		
REFIN2 Dual-Mode Threshold Voltage Levels		Low ($REFIN2 = RTC$)	2.2		3.0	V	
		High ($REFIN2 = V_{CC}$)	$V_{CC} - 1.0V$		$V_{CC} - 0.4V$		
Load Regulation Error		Either SMPS, $\overline{SKIP} = V_{CC}$, $I_{LOAD} = 0$ to 5A		-0.1		%	
		Either SMPS, $\overline{SKIP} = REF$, $I_{LOAD} = 0$ to 5A		-1.7			
		Either SMPS, $\overline{SKIP} = GND$, $I_{LOAD} = 0$ to 5A		-1.5			
Line Regulation Error		Either SMPS, $V_{IN} = 6V$ to 24V		0.005		%/V	
DH1 On-Time	t_{ON1}	$V_{IN} = 12V$, $V_{OUT1} = 5.0V$ (Note 2)	TON = GND or REF (400kHz)	895	1052	1209	ns
			TON = V_{CC} (200kHz)	1895	2105	2315	
DH2 On-Time	t_{ON2}	$V_{IN} = 12V$, $V_{OUT2} = 3.3V$ (Note 2)	TON = GND (500kHz)	475	555	635	ns
			TON = REF or V_{CC} (300kHz)	833	925	1017	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 2)		250	400	ns	
Soft-Start/Stop Slew Rate	t_{SS}	Rising/falling edge on ON1 or ON2 (preset)		1		ms	
Soft-Start/Stop Slew Rate	t_{SS}	Rising/falling edge on ON2 (REFIN2 ADJ)		1		mV/ μs	
Dynamic REFIN2 Slew Rate	t_{DYN}	Rising edge on REFIN2		8		mV/ μs	
Ultrasonic Operating Frequency	$f_{SW(USONIC)}$	$\overline{SKIP} = open (REF)$	20	27		kHz	
SECFB Threshold Voltage	V_{SECFB}		1.94	2.0	2.06	V	
SECFB Input Bias Current	I_{SECFB}	$V_{SECFB} = 2.2V$, $T_A = +25^{\circ}C$	-0.2		+0.2	μA	
LINEAR REGULATOR (LDO)							
LDO Output-Voltage Accuracy	V_{LDO}	$V_{IN} = 24V$, $LDOREFIN = BYP = GND$, $0mA < I_{LDO} < 100mA$	4.90	5.0	5.10	V	
		$V_{IN} = 24V$, $LDOREFIN = V_{CC}$, $BYP = GND$, $0mA < I_{LDO} < 100mA$	3.23	3.3	3.37		
		$V_{IN} = 24V$, $BYP = GND$, $V_{LDOREFIN} = 0.5V$, $0mA < I_{LDO} < 100mA$	0.960	1.0	1.040		
LDOREFIN Input Range	$V_{LDOREFIN}$	$V_{LDO} = 2 \times V_{LDOREFIN}$	0.3		2.0	V	
LDOREFIN Leakage Current	$I_{LDOREFIN}$	$V_{LDOREFIN} = 0$ or 2V, $T_A = +25^{\circ}C$	-0.5		+0.5	μA	
LDOREFIN Dual-Mode Threshold Voltage		LDOREFIN low threshold	0.1	0.15	0.20	V	
		LDOREFIN high threshold	$V_{CC} - 2V$	$V_{CC} - 1.5V$	$V_{CC} - 0.9V$		

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF, $V_{IN} = 12V$, $V_{DD} = V_{CC} = V_{SECFB} = 5V$, $V_{REFIN2} = 1.0V$, $BYP = LDOREFIN = GND$, $ONLDO = IN$, $ON1 = ON2 = V_{CC}$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDO Short-Circuit Current	$I_{LIM}(LDO)$	LDO = GND	100		260	mA
LDO Regulation Reduction/ Bypass Switchover Threshold		With respect to the LDO voltage, falling edge of BYP	-11.0	-8.5	-6.0	%
LDO Bypass Switchover Threshold		With respect to the LDO voltage, rising edge of BYP		-6.5		%
LDO Bypass Switchover Startup Timeout	t_{BYP}	Rising edge of BYP to bypass gate pulled low		500		μs
LDO Bypass Switch Resistance		LDO to BYP, $V_{BYP} = 5V$ (Note 4)		1.2	4.5	Ω
V_{CC} Undervoltage-Lockout (UVLO) Threshold	$V_{UVLO}(V_{CC})$	Falling edge of V_{CC} , PWM disabled below this threshold	3.8	4.0	4.3	V
		Rising edge of V_{CC}		4.2		
Thermal-Shutdown Threshold	T_{SHDN}	Hysteresis = $10^{\circ}C$		+160		$^{\circ}C$
3.3V ALWAYS-ON LINEAR REGULATOR (RTC)						
RTC Output-Voltage Accuracy	V_{RTC}	ON1 = ON2 = GND, $V_{IN} = 6V$ to $24V$, $0 < I_{RTC} < 5mA$	3.23	3.33	3.43	V
		ON1 = ON2 = ONLDO = GND, $V_{IN} = 6V$ to $24V$, $0 < I_{RTC} < 5mA$	3.19		3.47	
RTC Short-Circuit Current	$I_{LIM}(RTC)$	RTC = GND	5		30	mA
REFERENCE (REF)						
Reference Voltage	V_{REF}	$V_{CC} = 4.5V$ to $5.5V$, $I_{REF} = 0$	1.980	2.00	2.020	V
Reference Load-Regulation Error	ΔV_{REF}	$I_{REF} = -20\mu A$ to $50\mu A$	-10		+10	mV
REF Lockout Voltage	$V_{REF}(UVLO)$	Rising edge, 350mV (typ) hysteresis		1.95		V
OUT1 FAULT DETECTION						
OUT1 Overvoltage Trip Threshold	$V_{OVP}(OUT1)$	With respect to error-comparator threshold	13	16	19	%
OUT1 Overvoltage Fault- Propagation Delay	t_{OVP}	FB1 forced 50mV above trip threshold		10		μs
OUT1 Undervoltage-Protection Trip Threshold	$V_{UVP}(OUT1)$	With respect to error-comparator threshold	65	70	75	%
OUT1 Output-Undervoltage Fault-Propagation Delay	t_{UVP}			10		μs
PGOOD1 Lower Trip Threshold		With respect to error-comparator threshold, falling edge, hysteresis = 1%	-19	-16	-13	%
PGOOD1 Propagation Delay	t_{PGOOD1}	FB1 forced 50mV beyond PGOOD1 trip threshold, falling edge		10		μs
PGOOD1 Output Low Voltage		$V_{FB1} = 0.56V$ (PGOOD1 low impedance), $I_{SINK} = 4mA$			0.3	V
PGOOD1 Leakage Current	I_{PGOOD1}	$V_{FB1} = 0.70V$ (PGOOD1 high impedance), PGOOD1 forced to 5.5V, $T_A = +25^{\circ}C$			1	μA

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF, $V_{IN} = 12V$, $V_{DD} = V_{CC} = V_{SECFB} = 5V$, $V_{REFIN2} = 1.0V$, $BYP = LDORFIN = GND$, $ONLDO = IN$, $ON1 = ON2 = V_{CC}$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
OUT2 FAULT DETECTION							
OUT2 Overvoltage Trip Threshold	$V_{OVP(OUT2)}$	Preset mode (REFIN2 = RTC or V_{CC}): with respect to error-comparator threshold	13	16	19	%	
		Dynamic transition, SKIP = REF or V_{CC} and $OUT2 > REF_{IN2}$		$V_{REF} + 0.20$		V	
		Tracking mode: with respect to REFIN2 voltage	170	200	230	mV	
		Minimum overvoltage threshold		0.7		V	
OUT2 Overvoltage Fault-Propagation Delay	t_{OVP}	OUT2 forced 50mV above trip threshold		10		μs	
OUT2 Undervoltage-Protection Trip Threshold	$V_{UVP(OUT2)}$	Preset mode: with respect to error-comparator threshold	65	70	75	%	
		Tracking mode: with respect to REFIN2 voltage	-250	-300	-350	mV	
OUT2 Overvoltage Fault-Propagation Delay	t_{OVP}	OUT2 forced 50mV above trip threshold		10		μs	
OUT2 Output Undervoltage Fault-Propagation Delay	t_{UVP}	OUT2 forced 50mV below trip threshold		10		μs	
Dynamic REFIN2 Transition PGOOD Blanking Threshold		Blanking initiated; REFIN2 deviation from the internal target voltage (error-comparator threshold); hysteresis = 5mV		± 25		mV	
PGOOD2 Lower Trip Threshold		Preset mode: with respect to error-comparator threshold, falling edge, hysteresis = 1%	-19	-16	-13	%	
		Tracking mode: with respect to REFIN2 voltage, falling edge, hysteresis = 12mV	-175	-150	-125	mV	
PGOOD2 Propagation Delay	t_{PGOOD2}	OUT2 forced 50mV beyond PGOOD1 trip threshold, falling edge		10		μs	
PGOOD2 Output-Low Voltage		$V_{OUT2} = V_{REFIN2} - 150mV$ (PGOOD2 low impedance), $I_{SINK} = 4mA$			0.3	V	
PGOOD2 Leakage Current	I_{PGOOD2}	OUT2 = REFIN2 (PGOOD2 high impedance), PGOOD2 forced to 5.5V, $T_A = +25^{\circ}C$			1	μA	
CURRENT LIMIT							
ILIM_ Adjustment Range	V_{ILIM}		0.2		2.0	V	
ILIM_ Current	I_{ILIM}			5		μA	
Valley Current-Limit Threshold (Adjustable)	V_{VALLEY}	$V_{AGND} - V_{LX_}$	$R_{ILIM_} = 100k\Omega$	44	50	56	mV
			$R_{ILIM_} = 200k\Omega$	90	100	110	
			$R_{ILIM_} = 400k\Omega$	180	200	220	
Current-Limit Threshold (Negative)	V_{NEG}	With respect to valley current-limit threshold, $\overline{SKIP} = V_{CC}$		-120		%	
Ultrasonic Current-Limit Threshold	$V_{NEG(US)}$	$V_{OUT1} = V_{OUT2} = V_{FB1} = 0.77V$, $V_{REFIN2} = 0.70V$		25		mV	
Current-Limit Threshold (Zero Crossing)	V_{ZX}	$V_{AGND} - V_{LX_}$, $\overline{SKIP} = GND$ or OPEN/REF		3		mV	

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF, $V_{IN} = 12V$, $V_{DD} = V_{CC} = V_{SECFB} = 5V$, $V_{REFIN2} = 1.0V$, $BYP = LDOREFIN = GND$, $ONLDO = IN$, $ON1 = ON2 = V_{CC}$, $T_A = 0^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}C$.)
(Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GATE DRIVERS						
DH_ Gate Driver On-Resistance	R_{DH}	BST1 - LX1 and BST2 - LX2 forced to 5V		1.5	3.5	Ω
DL_ Gate Driver On-Resistance	R_{DL}	DL1, DL2; high state		2.2	4.5	Ω
		DL1, DL2; low state		0.6	1.5	
DH_ Gate Driver Source/Sink Current	I_{DH}	DH1, DH2 forced to 2.5V, BST1 - LX1 and BST2 - LX2 forced to 5V		2		A
DL_ Gate Driver Source Current	I_{DL} (SOURCE)	DL1, DL2 forced to 2.5V		1.7		A
DL_ Gate Driver Sink Current	I_{DL} (SINK)	DL1, DL2 forced to 2.5V		3.3		A
Internal BST_ Switch On-Resistance	R_{BST}	$I_{BST_} = 10mA$, $V_{DD} = 5V$		5		Ω
BST_ Leakage Current	I_{BST}	$V_{BST_} = 26V$, $T_A = +25^{\circ}C$, OUT2 and FB1 above regulation threshold		0.1	5	μA
INPUTS AND OUTPUTS						
TON Input Logic Levels		High		$V_{CC} - 0.4V$		V
		REF or open		1.6	3.0	
		Low			0.4	
\overline{SKIP} Input Logic Levels		High (forced-PWM)		$V_{CC} - 0.4V$		V
		Open (ultrasonic)		1.6	3.0	
		Low (skip)			0.4	
\overline{SKIP} , TON Leakage Current	I_{SKIP} , I_{TON}	$V_{SKIP} = V_{TON} = 0$ or $5V$, $T_A = +25^{\circ}C$		-2	+2	μA
ON_ Input Logic Levels		68mV hysteresis	High (SMPS on)	2.4		V
			Low (SMPS off)			
ON_ Leakage Current	$I_{ON_}$	$V_{ON1} = V_{ON2} = 0$ or $5V$, $T_A = +25^{\circ}C$		-2	+2	μA
ONLDO Input Logic Levels		68mV hysteresis	High (SMPS on)	2.4		V
			Low (SMPS off)			
ONLDO Leakage Current	I_{ONLDO}	$V_{ONLDO} = 0$ or $24V$, $T_A = +25^{\circ}C$		-1	+1	μA

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ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF, $V_{IN} = 12V$, $V_{DD} = V_{CC} = V_{SECFB} = 5V$, $V_{REFIN2} = 1.0V$, $BYP = LDOREFIN = GND$, $ONLDO = IN$, $ON1 = ON2 = V_{CC}$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
INPUT SUPPLIES							
IN Standby Supply Current	$I_{IN(STBY)}$	$V_{IN} = 6V$ to $24V$, $ON1 = ON2 = GND$, $ONLDO = V_{CC}$			200	μA	
IN Shutdown Supply Current	$I_{IN(SHDN)}$	$V_{IN} = 4.5V$ to $24V$, $ON1 = ON2 = ONLDO = GND$			70	μA	
IN Supply Current	I_{IN}	$ON1 = ON2 = REFIN2 = V_{CC}$, $SKIP = FB1 = GND$, $V_{OUT2} = 3.5V$, $V_{OUT1} = 5.3V$			0.2	mA	
V_{CC} Supply Current	I_{CC}	$ON1 = ON2 = REFIN2 = V_{CC}$, $SKIP = FB1 = GND$, $V_{OUT2} = 3.5V$, $V_{OUT1} = 5.3V$			1.5	mA	
PWM CONTROLLERS							
OUT1 Output-Voltage Accuracy (Note 1)	V_{OUT1}	5V preset output: $FB1 = GND$, $V_{IN} = 12V$, $SKIP = V_{CC}$	4.90		5.10	V	
		1.5V preset output: $FB1 = V_{CC} (5V)$, $V_{IN} = 12V$, $SKIP = V_{CC}$	1.47		1.53		
	V_{FB1}	Adjustable feedback output, $V_{IN} = 12V$, $SKIP = V_{CC}$	0.685		0.715		
OUT1 Voltage-Adjust Range			0.7		5.5	V	
FB1 Dual-Mode Threshold Voltage		Low	0.040		0.125	V	
		High	$V_{CC} - 1.6V$		$V_{CC} - 0.7V$		
OUT2 Output-Voltage Accuracy (Note 1)	V_{OUT2}	3.3V preset output: $REFIN2 = V_{CC} (5V)$, $V_{IN} = 12V$, $SKIP = V_{CC}$	3.234		3.366	V	
		1.05V preset output: $REFIN2 = RTC (3.3V)$, $V_{IN} = 1.2V$, $SKIP = V_{CC}$	1.029		1.071		
		Tracking output: $V_{REFIN2} = 1.0V$, $V_{IN} = 12V$, $SKIP = V_{CC}$	0.985		1.015		
OUT2 Voltage-Adjust Range			0		2	V	
REFIN2 Voltage-Adjust Range			0		2	V	
REFIN2 Dual-Mode Threshold Voltage		Low ($REFIN2 = RTC$)	2.2		3.0	V	
		High ($REFIN2 = V_{CC}$)	$V_{CC} - 1.2V$		$V_{CC} - 0.4V$		
DH1 On-Time	t_{ON1}	$V_{IN} = 12V$, $V_{OUT1} = 5.0V$ (Note 2)	$TON = GND$ or REF (400kHz)	895		1209	ns
			$TON = V_{CC}$ (200kHz)	1895		2315	
DH2 On-Time	t_{ON2}	$V_{IN} = 12V$, $V_{OUT2} = 3.3V$ (Note 2)	$TON = GND$ (500kHz)	475		635	ns
			$TON = REF$ or V_{CC} (300kHz)	833		1017	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 2)			425	ns	
Ultrasonic Operating Frequency	$f_{SW(USONIC)}$	$SKIP = open$ (REF)	18			kHz	
SECFB Threshold Voltage	V_{SECFB}		1.92		2.08	V	

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF, $V_{IN} = 12V$, $V_{DD} = V_{CC} = V_{SECFB} = 5V$, $V_{REFIN2} = 1.0V$, $BYP = LDOREFIN = GND$, $ONLDO = IN$, $ON1 = ON2 = V_{CC}$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LINEAR REGULATOR (LDO)						
LDO Output-Voltage Accuracy	V_{LDO}	$V_{IN} = 24V$, $LDOREFIN = BYP = GND$, $0mA < I_{LDO} < 100mA$	4.85		5.15	V
		$V_{IN} = 24V$, $LDOREFIN = V_{CC}$, $BYP = GND$, $0mA < I_{LDO} < 100mA$	3.20		3.40	
		$V_{IN} = 24V$, $BYP = GND$, $V_{LDOREFIN} = 0.5V$, $0mA < I_{LDO} < 100mA$	0.960		1.040	
LDOREFIN Input Range	$V_{LDOREFIN}$	$V_{LDO} = 2 \times V_{LDOREFIN}$	0.3		2.0	V
LDOREFIN Dual-Mode Threshold Voltage		LDOREFIN low threshold	0.10		0.25	V
		LDOREFIN high threshold	$V_{CC} - 2V$		$V_{CC} - 0.9V$	
LDO Short-Circuit Current	$I_{LIM}(LDO)$	LDO = GND			260	mA
LDO Regulation Reduction/ Bypass Switchover Threshold		Falling edge of BYP	-12		-5	%
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO}(V_{CC})$	Falling edge of V_{CC} , PWM disabled below this threshold	3.8		4.3	V
3.3V ALWAYS-ON LINEAR REGULATOR (RTC)						
RTC Output-Voltage Accuracy	V_{RTC}	$ON1 = ON2 = GND$, $V_{IN} = 6V$ to $24V$, $0 < I_{RTC} < 5mA$	3.18		3.45	V
		$ON1 = ON2 = ONLDO = GND$, $V_{IN} = 6V$ to $24V$, $0 < I_{RTC} < 5mA$	3.16		3.50	
RTC Short-Circuit Current	$I_{LIM}(RTC)$	RTC = GND	5		30	mA
REFERENCE (REF)						
Reference Voltage	V_{REF}	$V_{CC} = 4.5V$ to $5.5V$, $I_{REF} = 0$	1.975		2.025	V
Reference Load-Regulation Error	V_{REF}	$I_{REF} = -20\mu A$ to $50\mu A$	-10		+10	mV
OUT1 FAULT DETECTION						
OUT1 Overvoltage Trip Threshold	$V_{OVP}(OUT1)$	With respect to error-comparator threshold	12		20	%
OUT1 Undervoltage-Protection Trip Threshold	$V_{UVP}(OUT1)$	With respect to error-comparator threshold	63		77	%
PGOOD1 Lower Trip Threshold		With respect to error-comparator threshold, falling edge, hysteresis = 1%	-20		-12	%
PGOOD1 Output-Low Voltage		$V_{FB1} = 0.56V$ (PGOOD1 low impedance), $I_{SINK} = 4mA$			0.4	V
OUT2 FAULT DETECTION						
OUT2 Overvoltage Trip Threshold	$V_{OVP}(OUT2)$	Preset mode ($REFIN2 = RTC$ or V_{CC}): with respect to error-comparator threshold	12		20	%
		Tracking mode: with respect to $REFIN2$ voltage	160		240	mV

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

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ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO, RTC, OUT1, OUT2, and REF, $V_{IN} = 12V$, $V_{DD} = V_{CC} = V_{SECFB} = 5V$, $V_{REFIN2} = 1.0V$, $BYP = LDOREFIN = GND$, $ONLDO = IN$, $ON1 = ON2 = V_{CC}$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OUT2 Undervoltage-Protection Trip Threshold	$V_{UVP(OUT2)}$	Preset mode: with respect to error-comparator threshold		63		77	%
		Tracking mode: with respect to REFIN2 voltage		-230		-370	mV
PGOOD2 Lower Trip Threshold		Preset mode: with respect to error-comparator threshold, falling edge, hysteresis = 1%		-20		-12	%
		Tracking mode: with respect to REFIN2 voltage, falling edge, hysteresis = 12mV		-185		-115	mV
PGOOD2 Output-Low Voltage		$V_{OUT2} = V_{REFIN2} - 150mV$ (PGOOD2 low impedance), $I_{SINK} = 4mA$				0.4	V
CURRENT LIMIT							
ILIM_ Adjustment Range	V_{ILIM}			0.2		2.0	V
Valley Current-Limit Threshold (Adjustable)	V_{VALLEY}	$V_{AGND} - V_{LX}$	$R_{ILIM_} = 100k\Omega$	40		60	mV
			$R_{ILIM_} = 200k\Omega$	85		115	
			$R_{ILIM_} = 400k\Omega$	164		236	
GATE DRIVERS							
DH_ Gate Driver On-Resistance	R_{DH}	BST1 - LX1 and BST2 - LX2 forced to 5V				3.5	Ω
DL_ Gate Driver On-Resistance	R_{DL}	DL1, DL2; high state				4.5	Ω
		DL1, DL2; low state				1.5	
INPUTS AND OUTPUTS							
TON Input Logic Levels		High		$V_{CC} - 0.4V$			V
		REF or open		1.6	3.0		
		Low			0.4		
\overline{SKIP} Input Logic Levels		High (forced-PWM)		$V_{CC} - 0.4V$			V
		Open (ultrasonic)		1.6	3.0		
		Low (skip)			0.4		
ON_ Input Logic Levels		High (SMPS on)		2.4			V
		Low (SMPS off)			0.8		
ONLDO Input Logic Levels		High (LDO on)		2.4			V
		Low (LDO off)			0.8		

Note 1: DC output accuracy specifications refer to the threshold of the error comparator. When the inductor is in continuous conduction, the MAX17020 regulates the valley of the output ripple, so the actual DC output voltage is higher than the trip level by 50% of the output ripple voltage. In discontinuous conduction ($I_{OUT} < I_{LOAD(SKIP)}$), the output voltage has a DC regulation level higher than the error-comparator threshold by approximately 1.5% due to slope compensation.

Note 2: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with $LX = PGND$, $V_{BST} = 5V$, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times might be different due to MOSFET switching speeds.

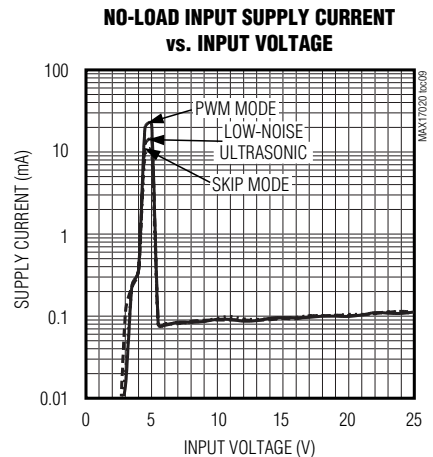
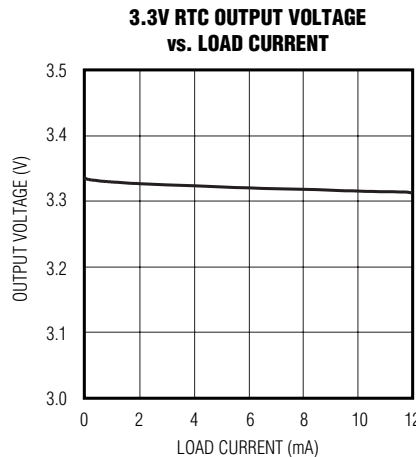
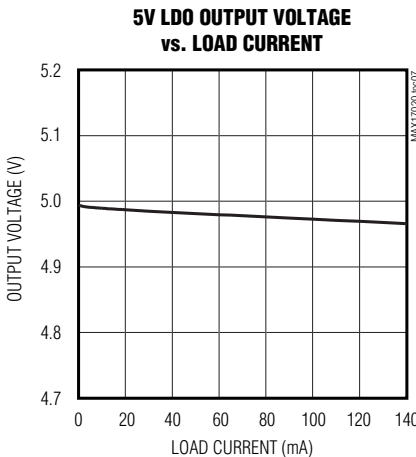
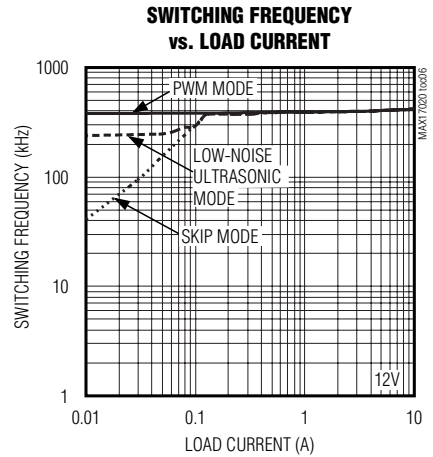
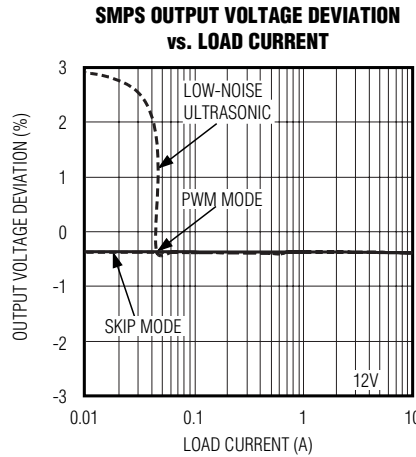
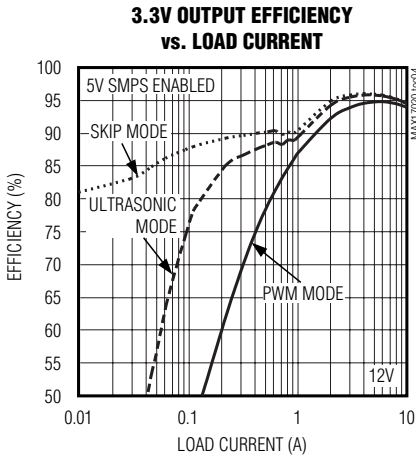
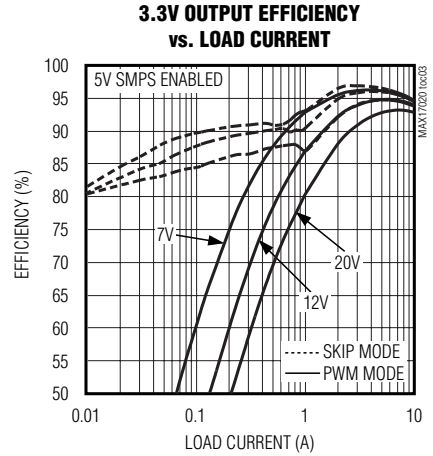
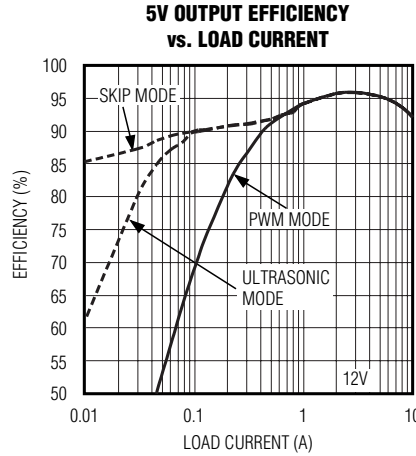
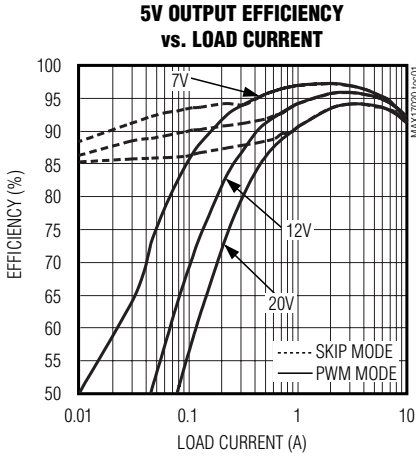
Note 3: Limits are 100% production tested at $T_A = +25^{\circ}C$. Maximum and minimum limits over temperature are guaranteed by design and characterization.

Note 4: Specifications increased by 1 Ω to account for test measurement error.

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

Typical Operating Characteristics

(Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = V_{CC} = 5V$, $T_{ON} = REF$, $T_A = +25^\circ C$, unless otherwise noted.)

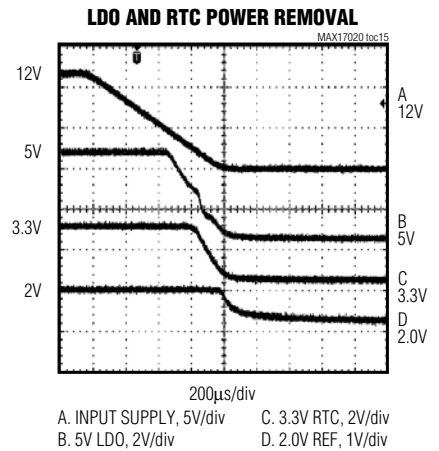
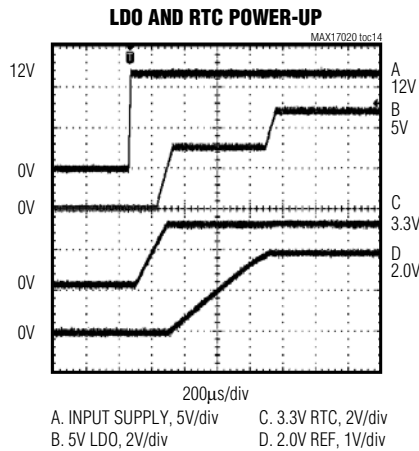
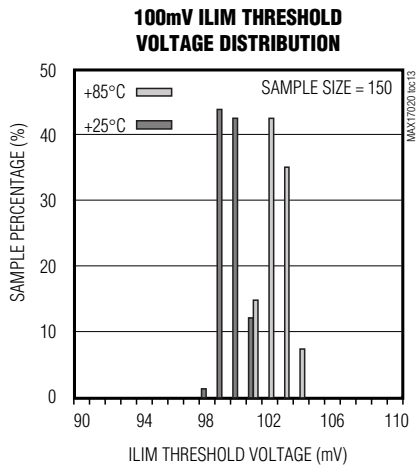
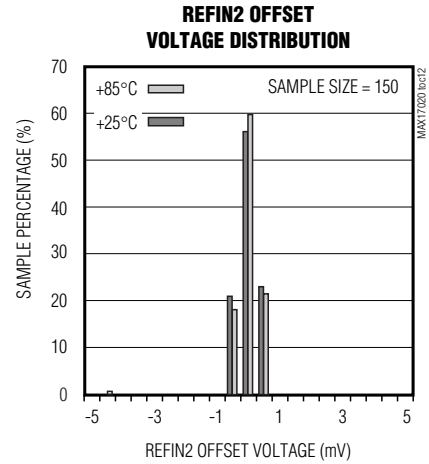
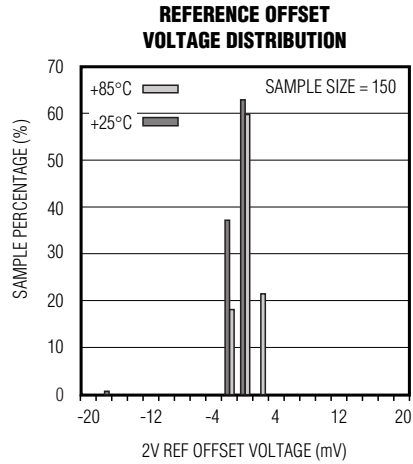
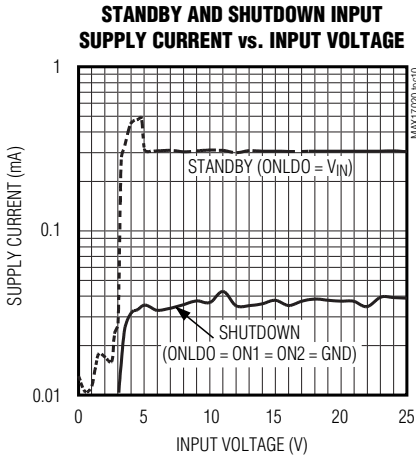


Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

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Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = V_{CC} = 5V$, $T_{ON} = REF$, $T_A = +25^\circ C$, unless otherwise noted.)

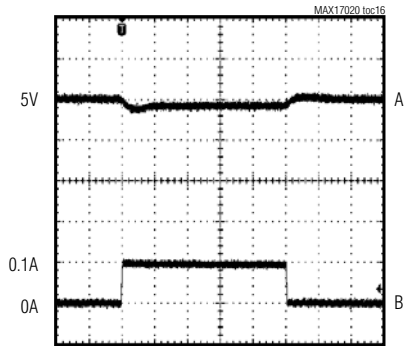


Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

Typical Operating Characteristics (continued)

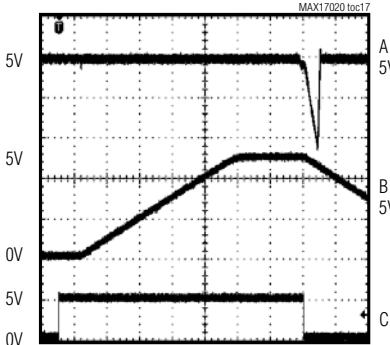
(Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = V_{CC} = 5V$, $T_{ON} = REF$, $T_A = +25^\circ C$, unless otherwise noted.)

5V LDO LOAD TRANSIENT



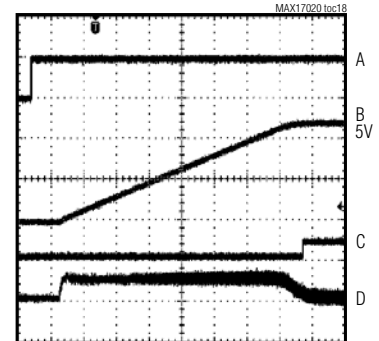
A. LDO OUTPUT, 100mV/div
B. LOAD CURRENT, 100mA/div

5V SMPS STARTUP AND SHUTDOWN



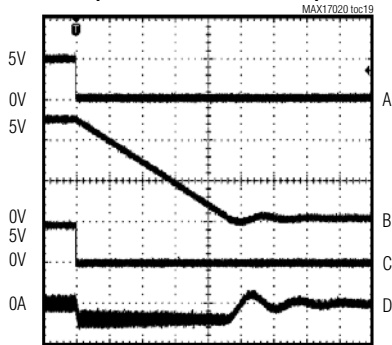
A. 5V LDO OUTPUT, 0.2V/div
B. 5V SMPS OUTPUT, 2V/div
C. ON1, 5V/div

STARTUP WAVEFORMS (SWITCHING REGULATORS)



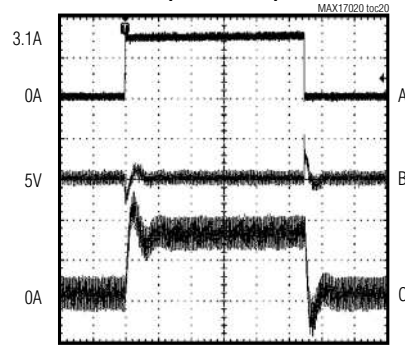
A. ON1, 2V/div
B. 5V SMPS OUTPUT, 2V/div
C. PGOOD1, 5V/div
D. INDUCTOR CURRENT, 5A/div

SHUTDOWN WAVEFORMS (SWITCHING REGULATORS)



A. ON1, 5V/div
B. 5V SMPS OUTPUT, 2V/div
C. PGOOD1, 2V/div
D. INDUCTOR CURRENT, 5A/div

5V SMPS LOAD TRANSIENT (PWM MODE)



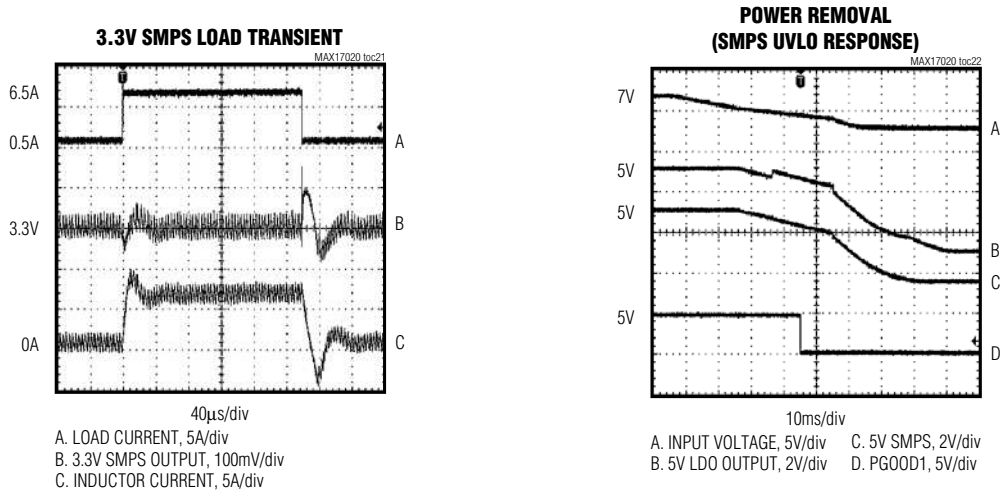
A. LOAD CURRENT, 2A/div
B. 5V SMPS OUTPUT, 100mV/div
C. INDUCTOR CURRENT, 2A/div

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

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Typical Operating Characteristics (continued)

(Circuit of Figure 1, $V_{IN} = 12V$, $V_{DD} = V_{CC} = 5V$, $T_{ON} = REF$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	REF	2V Reference-Voltage Output. Bypass REF to AGND with a 0.1µF or greater ceramic capacitor. The reference can source up to 50µA for external loads. Loading REF degrades output-voltage accuracy according to the REF load-regulation error. The reference shuts down when ON1, ON2, and ONLDO are all pulled low.
2	TON	Switching-Frequency Setting Input. Select the OUT1/OUT2 switching frequencies by connecting TON as follows for: High (V_{CC}) = 200kHz/300kHz Open (REF) = 400kHz/300kHz GND = 400kHz/500kHz
3	V_{CC}	Analog Supply Voltage Input. Connect V_{CC} to the system supply voltage with a series 50Ω resistor, and bypass to analog ground using a 1µF or greater ceramic capacitor.
4	ONLDO	Enable Input for LDO. Drive ONLDO high to enable the linear regulator (LDO) output. Drive ONLDO low to shut down the linear regulator output.
5	RTC	3.3V Always-On Linear Regulator Output for RTC Power. Bypass RTC with a 1µF or greater ceramic capacitor to analog ground. RTC can source at least 5mA for external load support. RTC power-up is required for controller operation.
6	IN	Power-Input Supply. IN powers the linear regulators (RTC and LDO) and senses the input voltage for the Quick-PWM on-time one-shot timers. The high-side MOSFET's on-time is inversely proportional to the input voltage. Bypass IN with a 0.1µF or greater ceramic capacitor to PGND close to the MAX17020.
7	LDO	Linear Regulator Output. Bypass LDO with a 4.7µF or greater ceramic capacitor. LDO can source at least 100mA for external load support. LDO is powered from IN and its regulation threshold is set by LDOREFIN. For preset 5V operation, connect LDOREFIN directly to GND. For preset 3.3V operation, connect LDOREFIN directly to V_{CC} . When LDO is used for 5V operation, LDO must supply V_{CC} and V_{DD} .

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

Pin Description (continued)

PIN	NAME	FUNCTION
8	LDOREFIN	External Reference Input for the Linear Regulator. LDOREFIN sets the LDO regulation voltage ($V_{LDO} = 2 \times V_{LDOREFIN}$) for a 0.3V to 2V LDOREFIN range. Connect LDOREFIN to GND for a fixed 5V linear-regulator output voltage, or connect LDOREFIN to V_{CC} for a fixed 3.3V linear-regulator output voltage. When LDO is set to 5V and is enabled, LDO must supply V_{CC} and V_{DD} .
9	BYP	Linear Regulator Bypass Input. When BYP voltage exceeds 93.5% of the LDO voltage, the controller bypasses the LDO output to the BYP input. The bypass switch is disabled if the LDO voltage drops by 8.5% from its nominal regulation threshold. When not being used, connect BYP to GND.
10	OUT1	Output Voltage-Sense Input for SMPS1. OUT1 is an input to the Quick-PWM on-time one-shot timer. OUT1 also serves as the feedback input for the preset 5V (FB1 = GND) and 1.5V (FB1 = V_{CC}) output voltage settings.
11	FB1	Adjustable Feedback Voltage-Sense Connection for SMPS1. Connect FB1 to GND for fixed 5V operation. Connect FB1 to V_{CC} for fixed 1.5V operation. Connect FB1 to an external resistive voltage-divider from OUT1 to analog ground to adjust the output voltage between 0.7V and 5.5V.
12	ILIM1	Valley Current-Limit Adjustment for SMPS1. The GND - LX1 current-limit threshold is 1/10 the voltage present on ILIM1 over a 0.2V to 2V range. An internal 5 μ A current source allows this voltage to be set with a single resistor between ILIM1 and analog ground.
13	PGOOD1	Open-Drain Power-Good Output for SMPS1. PGOOD1 is low when the output voltage is more than 16% (typ) below the nominal regulation threshold, during soft-start, in shutdown, and after the fault latch has been tripped. After the soft-start circuit has terminated, PGOOD1 becomes high impedance if the output is in regulation.
14	ON1	Enable Input for SMPS1. Drive ON1 high to enable SMPS1. Drive ON1 low to shut down SMPS1.
15	DH1	High-Side Gate-Driver Output for SMPS1. DH1 swings from LX1 to BST1.
16	LX1	Inductor Connection for SMPS1. Connect LX1 to the switched side of the inductor. LX1 is the lower supply rail for the DH1 high-side gate driver.
17	BST1	Boost Flying-Capacitor Connection for SMPS1. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST1 allows the DH1 turn-on current to be adjusted.
18	DL1	Low-Side Gate-Driver Output for SMPS1. DL1 swings from PGND to V_{DD} .
19	V_{DD}	Supply-Voltage Input for the DL_ Gate Drivers. Connect to a 5V supply. Also connect to the drain of the BST diode switch.
20	SECFB	Secondary Feedback Input. The secondary feedback input forces the SMPS1 output into ultrasonic mode when the SECFB voltage drops below its 2V threshold voltage. This forces DL1 and DH1 to switch, allowing the system to refresh an external low-power charge pump being driven by DL1 (see Figure 1). Connect SECFB to V_{CC} to the 5V bias supply to disable secondary feedback.
21	AGND	Analog Ground. Connect the backside exposed pad to AGND.
22	PGND	Power Ground
23	DL2	Low-Side Gate-Driver Output for SMPS2. DL2 swings from PGND to V_{DD} .
24	BST2	Boost Flying-Capacitor Connection for SMPS2. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST2 allows the DH2 turn-on current to be adjusted.
25	LX2	Inductor Connection for SMPS2. Connect LX2 to the switched side of the inductor. LX2 is the lower supply rail for the DH2 high-side gate driver.

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

Pin Description (continued)

PIN	NAME	FUNCTION
26	DH2	High-Side Gate-Driver Output for SMPS2. DH2 swings from LX2 to BST2.
27	ON2	Enable Input for SMPS2. Drive ON2 high to enable SMPS2. Drive ON2 low to shut down SMPS2.
28	PGOOD2	Open-Drain Power-Good Output for SMPS2. PGOOD2 is low when the output voltage is more than 150mV (typ) below the REFIN2 voltage or more than 16% below the preset voltage, during soft-start, in shutdown, and when the fault latch has been tripped. After the soft-start circuit has terminated, PGOOD2 becomes high impedance if the output is in regulation. PGOOD2 is blanked—forced high-impedance state—when a dynamic REFIN transition is detected.
29	$\overline{\text{SKIP}}$	Pulse-skipping Control Input. This three-level input determines the operating mode for the switching regulators: High (V_{CC}) = Forced-PWM operation Open/REF (2V) = Ultrasonic mode GND = Pulse-skipping mode
30	OUT2	Output Voltage-Sense Input for SMPS2. OUT2 is an input to the Quick-PWM on-time one-shot timer. OUT2 also serves as the feedback input for the preset 3.3V (REFIN2 = V_{CC}) and 1.05V (REFIN2 = RTC).
31	ILIM2	Valley Current-Limit Adjustment for SMPS2. The GND - LX2 current-limit threshold is 1/10 the voltage present on ILIM2 over a 0.2V to 2V range. An internal 5 μ A current source allows this voltage to be set with a single resistor between ILIM2 and analog ground.
32	REFIN2	External Reference Input for SMPS2. REFIN2 sets the feedback-regulation voltage ($V_{OUT2} = V_{REFIN2}$). The MAX17020 includes an internal window comparator to detect when the REFIN2 voltage changes, allowing the controller to blank PGOOD2 and the fault protection. Connect REFIN2 to RTC for fixed 1.05V operation. Connect REFIN2 to V_{CC} for fixed 3.3V operation.
—	EP	Exposed Pad. Connect the backside exposed pad to AGND.

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Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

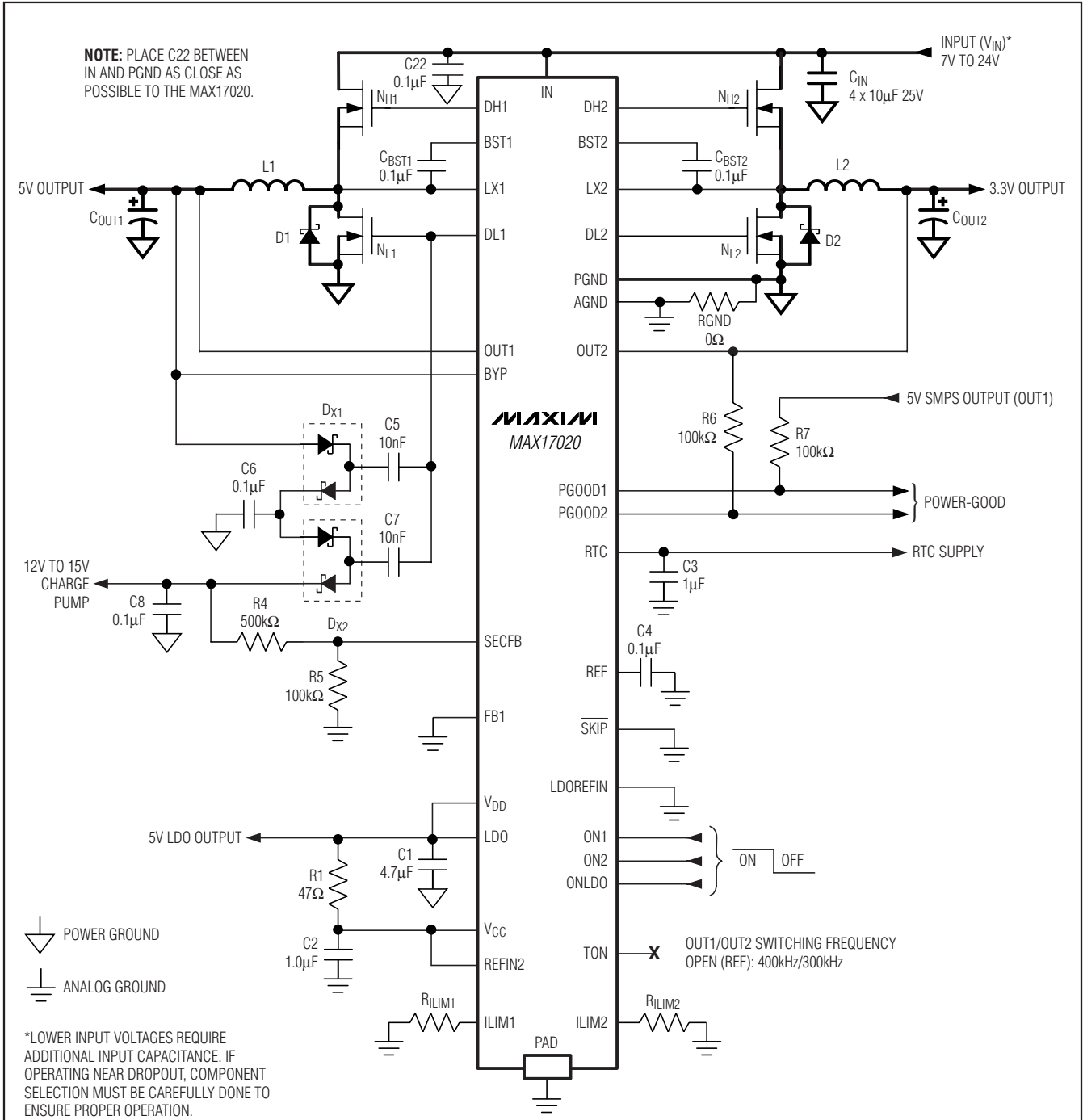


Figure 1. Standard Application Circuit—Main Supply

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

MAX17020

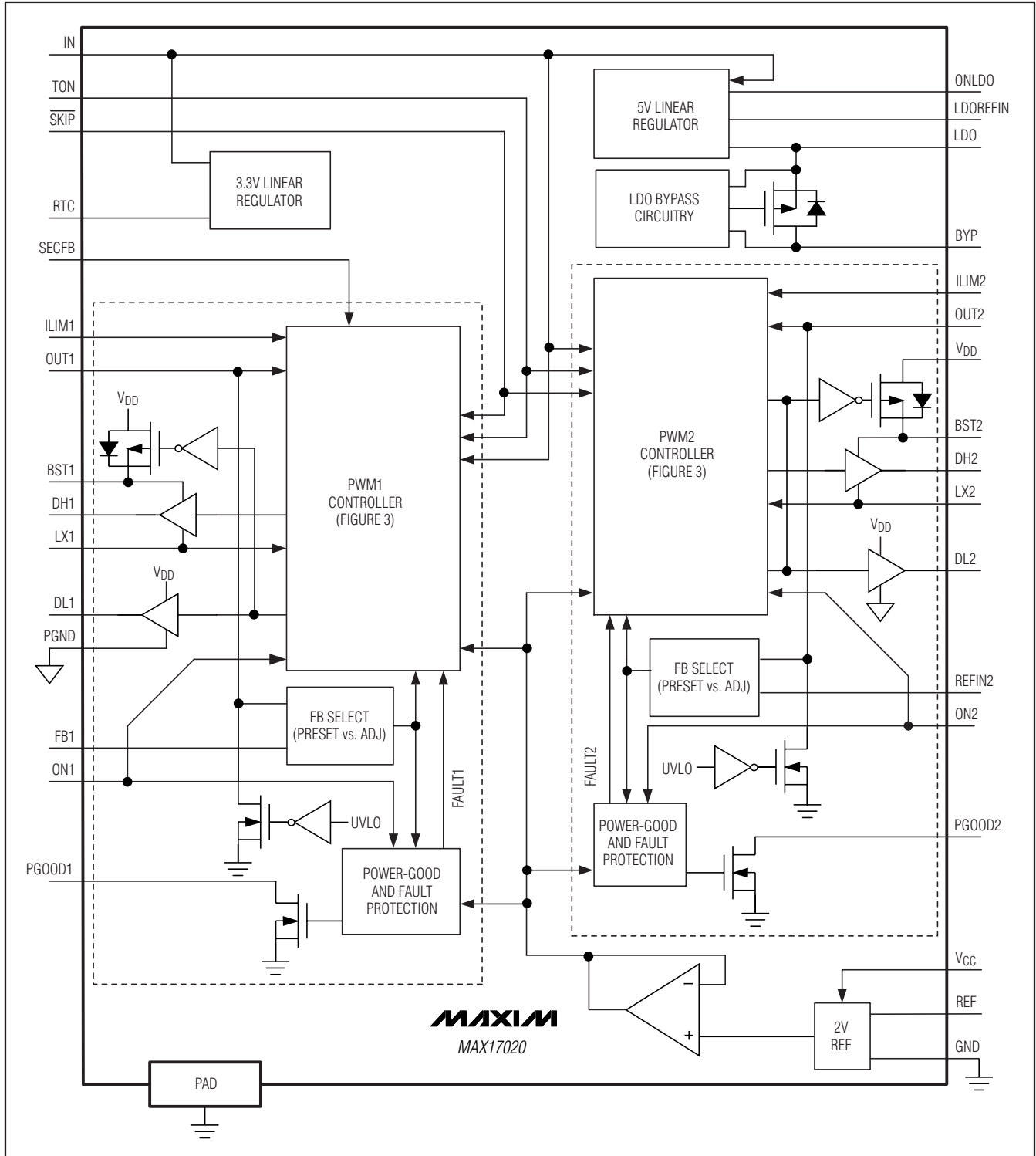


Figure 2. Functional Diagram Overview

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

Table 1. Component Selection for Standard Applications

COMPONENT	400kHz/300kHz SMPS 1: 5V AT 5A SMPS 2: 3.3V AT 8A	400kHz/500kHz SMPS 1: 5V AT 3A SMPS 2: 3.3V AT 5A	400kHz/300kHz SMPS 1: 1.5V AT 8A SMPS 2: 1.05V AT 5A
Input Voltage	$V_{IN} = 7V$ to 24V	$V_{IN} = 7V$ to 24V	$V_{IN} = 7V$ to 24V
Input Capacitor (C_{IN})	(4x) 10 μ F, 25V Taiyo Yuden TMK432BJ106KM	(2x) 10 μ F, 25V Taiyo Yuden TMK432BJ106KM	(4x) 10 μ F, 25V Taiyo Yuden TMK432BJ106KM
SMPS 1			
Output Capacitor (C_{OUT1})	330 μ F, 6V, 18m Ω SANYO 6TPE330MIL	330 μ F, 6V, 18m Ω SANYO 6TPE330MIL	(2x) 330 μ F, 2V, 7m Ω SANYO 2TPF330M7
Inductor (L_1)	4.3 μ H, 11.4m Ω , 11A Sumida CEP125U	4.7 μ H, 9.8m Ω , 7A Sumida CDRH10D68	1.5 μ H, 12A, 7m Ω NEC/Tokin MPLC1040L1R5
High-Side MOSFET (N_{H1})	Fairchild Semiconductor FDS6612A 26m Ω /30m Ω , 30V	Vishay Siliconix Si4814DY Dual 30V MOSFET	Fairchild Semiconductor FDS8690 8.6m Ω /11.4m Ω , 30V
Low-Side MOSFET (N_{L1})	Fairchild Semiconductor FDS6670S 9m Ω /11.5m Ω , 30V	High side: 19m Ω /23m Ω Low side: 18m Ω /22m Ω	Fairchild Semiconductor FDMS8660S 2.6m Ω /3.5m Ω , 30V
Current-Limit Resistor (R_{ILIM1})	200k Ω	150k Ω	49.9k Ω
SMPS 2			
Output Capacitor (C_{OUT2})	470 μ F, 4V, 15m Ω SANYO 4TPE470MFL	330 μ F, 6V, 18m Ω SANYO 6TPE330MIL	330 μ F, 2V, 7m Ω SANYO 2TPF330M7
Inductor (L_2)	4.3 μ H, 11.4m Ω , 11A Sumida CEP125U	4.7 μ H, 9.8m Ω , 7A Sumida CDRH10D68	1.5 μ H, 12A, 7m Ω NEC/Tokin MPLC1040L1R5
High-Side MOSFET (N_{H2})	Fairchild Semiconductor FDS8690 8.6m Ω /11.4m Ω , 30V	Vishay Siliconix Si4814DY Dual 30V MOSFET	Fairchild Semiconductor FDS8690 8.6m Ω /11.4m Ω , 30V
Low-Side MOSFET (N_{L2})	Fairchild Semiconductor FDMS8660S 2.6m Ω /3.5m Ω , 30V	High side: 19m Ω /23m Ω Low side: 18m Ω /22m Ω	Fairchild Semiconductor FDMS8660S 2.6m Ω /3.5m Ω , 30V
Current-Limit Resistor (R_{ILIM2})	200k Ω	200k Ω	49.9k Ω

Table 2. Component Suppliers

SUPPLIER	WEBSITE
AVX Corp.	www.avxcorp.com
Central Semiconductor Corp.	www.centalsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp	www.kemet.com
NEC/Tokin America, Inc.	www.nec-tokinamerica.com
Panasonic Corp.	www.panasonic.com
Philips/nxp Semiconductor	www.semiconductors.philips.com
Pulse Engineering	www.pulseeng.com

SUPPLIER	WEBSITE
Renesas Technology Corp.	www.renesas.com
SANYO Electric Co., Ltd.	www.sanyodevice.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Vishay (Dale, Siliconix)	www.vishay.com
Würth Elektronik GmbH & Co. KG	www.we-online.com

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

Detailed Description

The MAX17020 step-down controller is ideal for high-voltage, low-power supplies for notebook computers. Maxim's Quick-PWM pulse-width modulator in the MAX17020 is specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs, while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes. Figure 2 is a functional diagram overview. Figure 3 is the functional diagram—Quick-PWM core.

The MAX17020 includes several features for multipurpose notebook functionality, allowing this controller to be used two or three times in a single notebook—main, I/O chipset, and graphics. The MAX17020 includes a 100mA LDO that can be configured for preset 5V operation—ideal for initial power-up of the notebook and main supply—or can be adjusted for lower voltage operation—ideal for low-power I/O or graphics supply requirements. Additionally, the MAX17020 includes a 3.3V, 5mA RTC supply that remains always enabled, which can be used to power the RTC supply and system pullups when the notebook shuts down. The MAX17020 also includes an optional secondary feedback input that allows an unregulated charge pump or secondary winding to be included on a supply—ideal for generating the low-power 12V to 15V load switch supply. Finally, the MAX17020 includes a reference input on SMPS 2 that allows dynamic voltage transitions when driven by an adjustable resistive voltage-divider or DAC—ideal for the dynamic graphics core requirements.

3.3V RTC Power

The MAX17020 includes a low-current (5mA) linear regulator that remains active as long as the input supply (IN) exceeds 2V (typ). The main purpose of this “always-enabled” linear regulator is to power the real-time clock (RTC) when all other notebook regulators are disabled. RTC also serves as the main bias supply of the MAX17020 so it powers up before the LDO and switching regulators. The RTC regulator sources at least 5mA for external loads.

Adjustable 100mA Linear Regulator

The MAX17020 includes a high-current (100mA) linear regulator that can be configured for preset 5V or 3.3V operation or adjusted between 0.6V to 4V. When the MAX17020 is configured as a main supply, this LDO is required to generate the 5V bias supply necessary to power up the switching regulators. Once the switching regulators are enabled, the LDO can be bypassed using the dedicated BYP input. The adjustable linear regulator allows generation of the 3.3V suspend supply or buffered low-power chipset and GPU reference supplies. The MAX17020 LDO sources at least 100mA of supply current.

Bypass Switch

The MAX17020 includes an independent LDO bypass input that allows the LDO to be bypassed by either switching regulator output or from a different regulator all together. When the bypass voltage (BYP) exceeds 93.5% of the LDO output voltage for 500μs, the MAX17020 reduces the LDO regulation threshold and turns on an internal p-channel MOSFET to short BYP to LDO. Instead of disabling the LDO when the MAX17020 enables the bypass switch, the controller reduces the LDO regulation voltage, which effectively places the linear regulator in a standby state while switched over, yet allows a fast recovery if the bypass supply drops.

Connect BYP to GND when not used to avoid unintentional conduction through the body diode (BYP to LDO) of the p-channel MOSFET.

5V Bias Supply (VCC/VDD)

The MAX17020 requires an external 5V bias supply (VDD and VCC) in addition to the battery. Typically, this 5V bias supply is generated by either the internal 100mA LDO (when configured for a main supply) or from the notebook's 95%-efficient 5V main supply (when configured for an I/O chipset, DDR, or graphics). Keeping these bias supply inputs independent improves the overall efficiency and allows the internal linear regulator to be used for other applications as well.

The VDD bias supply input powers the internal gate drivers and the VCC bias supply input powers the analog control blocks. The maximum current required is dominated by the switching losses of the drivers and can be estimated as follows:

$$I_{\text{BIAS(MAX)}} = I_{\text{CC(MAX)}} + f_{\text{sw}}Q_{\text{G}} \approx 30\text{mA to } 60\text{mA (typ)}$$

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

Free-Running Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant on-time, current-mode regulator with voltage feed-forward. This architecture relies on the output filter capacitor's ESR to act as a current-sense resistor, so the feedback ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. Another one-shot sets a minimum off-time (400ns typ). The on-time one-shot is triggered if the error comparator is low, the low-side switch current is below the valley current-limit threshold, and the minimum off-time one-shot has timed out.

On-Time One-Shot

The heart of the PWM core is the one-shot that sets the high-side switch on-time. This fast, low-jitter, adjustable one-shot includes circuitry that varies the on-time in response to battery and output voltage. The high-side switch on-time is inversely proportional to the battery voltage as sensed by the IN input, and proportional to the output voltage:

$$\text{On-Time} = K (V_{\text{OUT}}/V_{\text{IN}})$$

where K (switching period) is set by the tri-level TON input (see the *Pin Description* section). High-frequency (400kHz/500kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This might be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (200kHz/300kHz) operation offers the best overall efficiency at the expense of component size and board space.

For continuous conduction operation, the actual switching frequency can be estimated by:

$$f_{\text{SW}} = \frac{V_{\text{OUT}} + V_{\text{DROP1}}}{t_{\text{ON}}(V_{\text{IN}} + V_{\text{DROP1}} - V_{\text{DROP2}})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; V_{DROP2} is the sum of the voltage drops in the charging path, including the high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time calculated by the MAX17020.

Table 3. Approximate K-Factor Errors

SWITCHING REGULATOR	TON SETTING (kHz)	TYPICAL K-FACTOR (μs)	K-FACTOR ERROR (%)	COMMENTS
SMPS 1	200kHz TON = V _{CC}	5.0	±10	Use for absolute best efficiency.
	400kHz TON = REF or GND	2.5	±12.5	Useful in 3-cell systems for lighter loads than the CPU core or where size is key.
SMPS 2	300kHz TON = REF or V _{CC}	3.3	±10	Considered mainstream by current standards.
	500kHz TON = GND	2.0	±12.5	Good operating point for compound buck designs or desktop circuits.

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

MAX17020

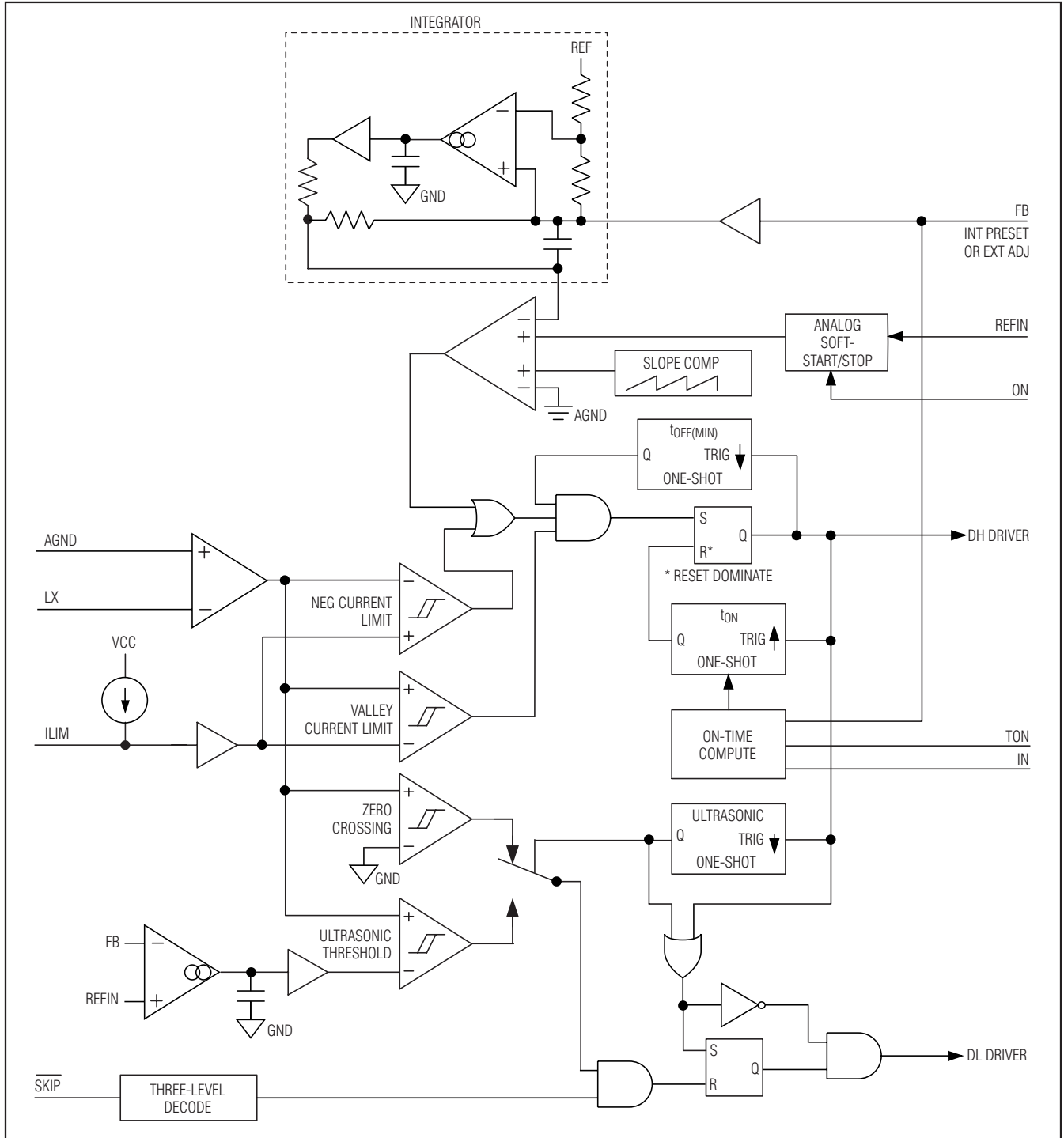


Figure 3. Functional Diagram—Quick-PWM Core

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

Modes of Operation

Forced-PWM Mode ($\overline{\text{SKIP}} = \text{VCC}$)

The low-noise forced-PWM mode ($\overline{\text{SKIP}} = \text{VCC}$) disables the zero-crossing comparator, which controls the low-side switch on-time. This forces the low-side gate-drive waveform to constantly be the complement of the high-side gate-drive waveform, so the inductor current reverses at light loads while DH maintains a duty factor of $V_{\text{OUT}}/V_{\text{IN}}$. The benefit of forced-PWM mode is to keep the switching frequency fairly constant. However, forced-PWM operation comes at a cost: the no-load 5V bias current remains between 20mA to 60mA depending on the switching frequency and MOSFET selection.

The MAX17020 automatically uses forced-PWM operation during all transitions—dynamic REFIN, startup, and shutdown—regardless of the $\overline{\text{SKIP}}$ configuration.

Automatic Pulse-Skipping Mode ($\overline{\text{SKIP}} = \text{GND}$)

In skip mode ($\overline{\text{SKIP}} = \text{GND}$), an inherent automatic switchover to PFM takes place at light loads. This switchover is affected by a comparator that truncates the low-side switch on-time at the inductor current's zero crossing. The zero-crossing comparator threshold is set by the differential across LX and AGND.

DC output-accuracy specifications refer to the integrated threshold of the error comparator. When the inductor is in continuous conduction, the MAX17020 regulates the valley of the output ripple and the internal integrator removes the actual DC output-voltage error caused by the output-ripple voltage and internal slope compensation. In discontinuous conduction ($\overline{\text{SKIP}} = \text{GND}$ and $I_{\text{OUT}} < I_{\text{LOAD}}(\overline{\text{SKIP}})$), the integrator cannot correct for the low-frequency output ripple error, so the output voltage has a DC regulation level higher than the error comparator threshold by approximately 1.5% due to slope compensation and output ripple voltage.

Ultrasonic Mode ($\overline{\text{SKIP}} = \text{Open or REF}$)

Leaving $\overline{\text{SKIP}}$ unconnected or connecting $\overline{\text{SKIP}}$ to REF (2V) activates a unique pulse-skipping mode with a guaranteed minimum switching frequency of 20kHz. This ultrasonic pulse-skipping mode eliminates audio-frequency modulation that would otherwise be present when a lightly loaded controller automatically skips pulses. In ultrasonic mode, the controller automatically transitions to fixed-frequency PWM operation when the load reaches the same critical conduction point ($I_{\text{LOAD}}(\overline{\text{SKIP}})$) that occurs when normally pulse skipping.

An ultrasonic pulse occurs (Figure 4) when the controller detects that no switching has occurred within the last 37 μs or when SECFB drops below its feedback threshold. Once triggered, the ultrasonic circuitry pulls

DL high, turning on the low-side MOSFET to induce a negative inductor current. After the inductor current reaches the negative ultrasonic current threshold, the controller turns off the low-side MOSFET (DL pulled low) and triggers a constant on-time (DH driven high). When the on-time has expired, the controller reenables the low-side MOSFET until the inductor current drops below the zero-crossing threshold. Starting with a DL pulse greatly reduces the peak output voltage when compared to starting with a DH pulse.

The output voltage at the beginning of the ultrasonic pulse determines the negative ultrasonic current threshold, resulting in the following equation:

$$V_{\text{NEG(US)}} = I_{\text{LRCS}} = (V_{\text{NOM}} - V_{\text{FB}}) \times 0.385\text{V}$$

where V_{NOM} is the nominal feedback-regulation voltage, and V_{FB} is the actual feedback voltage ($V_{\text{FB}} > V_{\text{NOM}}$), and R_{CS} is the current-sense resistance seen across LX to AGND.

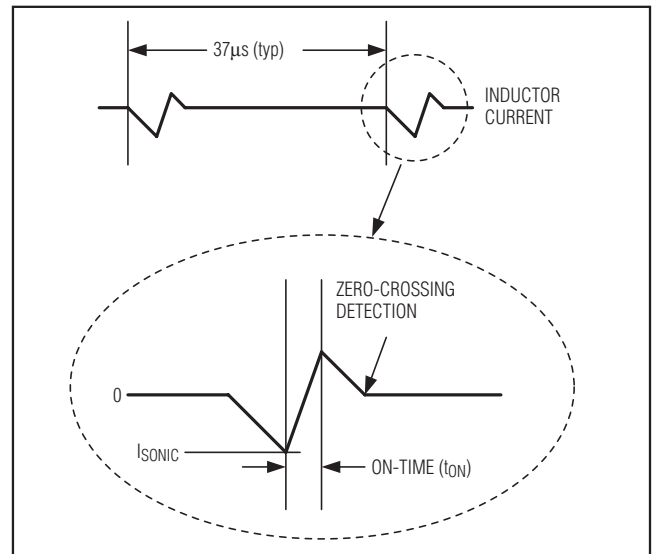


Figure 4. Ultrasonic Waveforms

Secondary Feedback: SECFB—OUT1 ONLY

When the controller skips pulses ($\overline{\text{SKIP}} = \text{GND or REF}$), the long time between pulses (especially if the output is sinking current) allows the external charge-pump voltage or transformer secondary winding voltage to drop. When the SECFB voltage drops below its 2V feedback threshold, the MAX17020 issues an ultrasonic pulse (regardless of the ultrasonic one-shot state). This forces a switching cycle, allowing the external unregulated charge pump (or transformer secondary winding) to be refreshed. See the *Ultrasonic Mode ($\overline{\text{SKIP}} = \text{Open or REF}$)* section for switching cycle sequence/specifications.

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

Dynamic Output Voltage—OUT2 Only

The MAX17020 regulates OUT2 to the voltage set at REFIN2, so the MAX17020 supports applications that require dynamic output-voltage changes between two set points by adjusting the REFIN2 voltage. For a step-voltage change at REFIN2, the rate of change of the output voltage is limited either by the internal slew-rate circuit, by the REFIN2 slew rate, or by the component selection—inductor current ramp, the total output capacitance, the current limit, and the load during the transition—whichever is the slowest. The total output capacitance determines how much current is needed to change the output voltage, while the inductor limits the current ramp rate. Additional load current slows down the output voltage change during a positive REFIN2 voltage change, and speeds up the output voltage change during a negative REFIN2 voltage change. Figure 5 is the dynamic REFIN transition.

Automatic Fault Blanking

When the MAX17020 automatically detects that the internal target and REFIN2 are more than $\pm 25\text{mV}$ (typ) apart, the controller automatically blanks PGOOD2, blanks the UVP protection, and sets the OVP threshold to REF + 200mV. The blanking remains until 1) the internal target and REFIN2 are within $\pm 20\text{mV}$ of each other and 2) an edge is detected on the error amplifier signifying that the output is in regulation. This prevents the system or internal fault protection from shutting down the controller during transitions.

Valley Current-Limit Protection

The current-limit circuit employs a unique “valley” current-sensing algorithm that senses the inductor current through the low-side MOSFET—across LX to AGND. If the current through the low-side MOSFET exceeds the valley current-limit threshold, the PWM controller is not allowed to initiate a new cycle. The actual peak current is greater than the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the inductor value and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

In forced-PWM mode, the MAX17020 also implements a negative current limit to prevent excessive reverse inductor currents when V_{OUT} is sinking current. The negative current-limit threshold is set to approximately 120% of the positive current limit.

POR, UVLO

When V_{CC} rises above the power-on reset (POR) threshold, the MAX17020 clears the fault latches, forces the low-side MOSFET to turn on (DL high), and resets the soft-start circuit, preparing the controller for power-up. However, the V_{CC} undervoltage lockout (UVLO) circuitry inhibits switching until V_{CC} reaches 4.2V (typ). When V_{CC} rises above 4.2V and the controller has been enabled (ON_ pulled high), the controller activates the enabled PWM controllers and initializes soft-start.

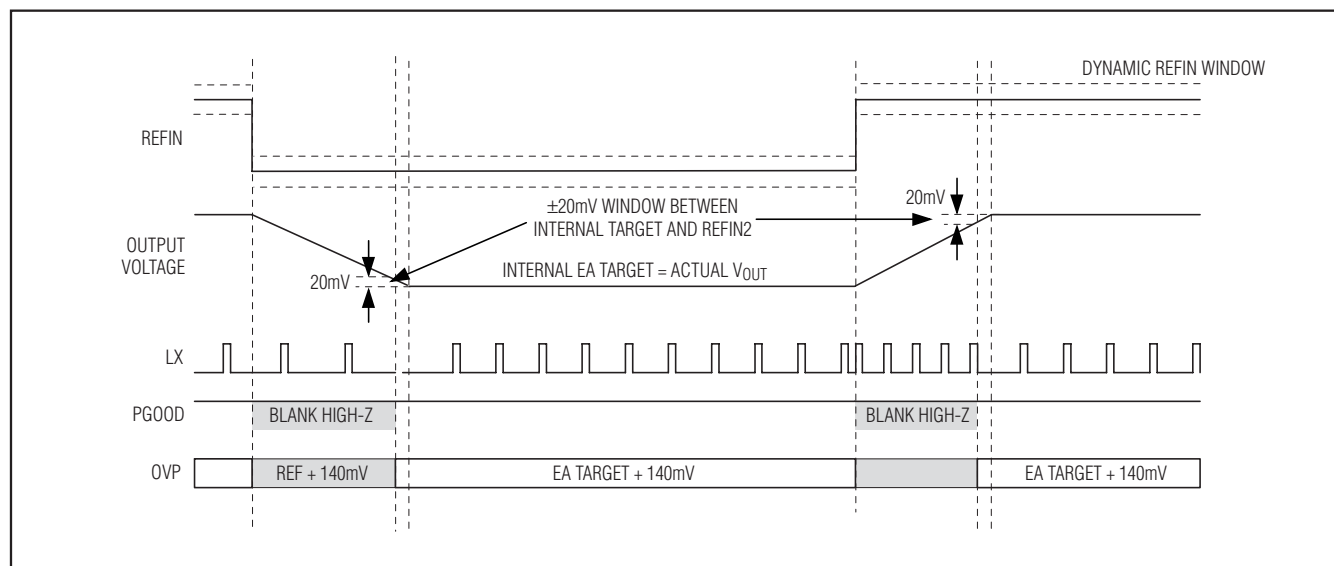


Figure 5. Dynamic REFIN Transition

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

When V_{CC} drops below the UVLO threshold (falling edge), the controller stops switching, and DH and DL are pulled low and a 10Ω switch discharges the outputs. When the 2V POR falling-edge threshold is reached, the DL state no longer matters since there is not enough voltage to force the switching MOSFETs into a low on-resistance state, so the controller pulls DL high, allowing a soft discharge of the output capacitors (damped response). However, if the V_{CC} recovers before reaching the falling POR threshold, DL remains low until the error comparator has been properly powered up and triggers an on-time. Only one enable input needs to be toggled to clear the fault latches and activate both outputs.

Soft-Start and Soft-Shutdown

The MAX17020 includes voltage soft-start and soft-shutdown—slowly ramping up and down the target voltage. During startup, the slew-rate control softly slews the preset/fixed target voltage over a 1ms startup period or its tracking voltage ($REFIN2 < 2V$) with a $1mV/\mu s$ slew rate. This long startup period reduces the inrush current during startup.

When ON1 or ON2 is pulled low or the output undervoltage fault latch is set, the respective output automatically enters soft-shutdown—the regulator enters PWM mode and ramps down its preset/fixed output voltage over a 1ms period or its tracking voltage ($REFIN2 < 2V$) with a $1mV/\mu s$ slew rate. After the output voltage drops below 0.1V, the MAX17020 pulls DL high, clamping the output and LX switching node to ground, preventing leakage currents from pulling up the output and minimizing the negative output voltage undershoot during shutdown.

Output Voltage

DC output-accuracy specifications in the *Electrical Characteristics* table refer to the error comparator's threshold. When the inductor continuously conducts, the MAX17020 regulates the valley of the output ripple, so the actual DC output voltage is lower than the slope-compensated trip level by 50% of the output ripple voltage. For PWM operation (continuous conduction), the output voltage is accurately defined by the following equation:

$$V_{OUT(PWM)} = V_{NOM} + \left(\frac{V_{RIPPLE}}{2ACC_V} \right)$$

where V_{NOM} is the nominal feedback voltage, ACC_V is the integrator's gain, and V_{RIPPLE} is the output ripple voltage ($V_{RIPPLE} = ESR \times \Delta I_{INDUCTOR}$, as described in the *Output Capacitor Selection* section).

In discontinuous conduction ($I_{OUT} < I_{LOAD(SKIP)}$), the longer off-times allow the slope compensation to increase the threshold voltage by as much as 1%, so

the output voltage regulates slightly higher than it would in PWM operation.

Internal Integrator

The internal integrator improves the output accuracy by removing any output accuracy errors caused by the slope compensation, output ripple voltage, and error-amplifier offset. Therefore, the DC accuracy (in forced-PWM mode) depends on the integrator's gain, the integrator's offset, and the accuracy of the integrator's reference input.

Adjustable/Fixed Output Voltages

Connect FB1 to GND for fixed 5V operation. Connect FB1 to V_{CC} for fixed 1.5V operation. Connect FB1 to an external resistive voltage-divider from OUT1 to analog ground to adjust the output voltage between 0.7V and 5.5V. During soft-shutdown, application circuits configured for adjustable feedback briefly switch modes when FB1 drops below the 110mV dual-mode threshold.

Choose R_{FBL} (resistance from FB1 to AGND) to be approximately $49.9k\Omega$ and solve for R_{FBH} (resistance from OUT1 to FB1) using the following equation:

$$R_{FBH} = R_{FBL} \times \left(\frac{V_{OUT1}}{0.7V} - 1 \right)$$

Connect REFIN2 to V_{CC} for fixed 3.3V operation. Connect REFIN2 to RTC (3.3V) for fixed 1.05V operation. Connect REFIN2 to an external resistive voltage-divider from REF to analog ground to adjust the output voltage between 0V and 2V.

Choose R_{REFINL} (resistance from REFIN2 to GND) to be approximately $49.9k\Omega$ and solve for R_{REFINH} (resistance from REF to REFIN2) using the equation:

$$R_{REFINH} = R_{REFINL} \times \left(\frac{V_{REF}}{V_{OUT2}} - 1 \right)$$

Power-Good Outputs (PGOOD) and Fault Protection

PGOOD is the open-drain output that continuously monitors the output voltage for undervoltage and over-voltage conditions. PGOOD_ is actively held low in shutdown ($ON_ = GND$), during soft-start or soft-shutdown. Approximately $20\mu s$ (typ) after the soft-start terminates, PGOOD_ becomes high impedance as long as the feedback voltage exceeds 85% of the nominal fixed-regulation voltage or within 150mV of the REFIN2 input voltage. PGOOD_ goes low if the feedback voltage drops 16% below the fixed target voltage, or if the output voltage drops 150mV below the dynamic REFIN2 voltage, or if the SMPS controller is shut down. For a

Dual Quick-PWM Step-Down Controller with Low-Power LDO, RTC Regulator

logic-level PGOOD_ output voltage, connect an external pullup resistor between PGOOD_ and V_{DD}. A 100kΩ pullup resistor works well in most applications.

Overvoltage Protection (OVP)

When the output voltage rises 16% above the fixed-regulation voltage or has risen 200mV above the dynamic REFIN2 input voltage, the controller immediately pulls the respective PGOOD_ low, sets the overvoltage fault latch, and immediately pulls the respective DL_ high—clamping the output to GND. Toggle either ON1 or ON2 input, or cycle V_{CC} power below its POR threshold to clear the fault latch and restart the controller.

Undervoltage Protection (UVP)

When the output voltage drops 30% below the fixed-regulation voltage or has dropped 300mV below the dynamic REFIN2 input voltage, the controller immediately pulls the respective PGOOD_ low, sets the undervoltage fault latch, and begins the shutdown sequence. After the output voltage drops below 0.1V, the synchronous rectifier turns on, clamping the output to GND. Toggle either ON1 or ON2 input, or cycle V_{CC} power below its POR threshold to clear the fault latch and restart the controller.

Thermal-Fault Protection (TSHDN)

The MAX17020 features a thermal-fault protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD1 and PGOOD2 low, enables the 10Ω discharge circuit, and disables the controller—DH and DL are pulled low. Toggle ONLDO or cycle IN power to reactivate the controller after the junction temperature cools by 15°C.

Design Procedure

Firmly establish the input-voltage range and maximum load current before choosing a switching frequency and inductor operating point (ripple-current ratio). The primary

design trade-off lies in choosing a good switching frequency and inductor operating point, and the following four factors dictate the rest of the design:

- **Input Voltage Range:** The maximum value (V_{IN(MAX)}) must accommodate the worst-case, high AC-adaptor voltage. The minimum value (V_{IN(MIN)}) must account for the lowest battery voltage after drops due to connectors, fuses, and battery-selector switches. If there is a choice at all, lower input voltages result in better efficiency.
- **Maximum Load Current:** There are two values to consider. The peak load current (I_{LOAD(MAX)}) determines the instantaneous component stresses and filtering requirements and thus drives output capacitor selection, inductor saturation rating, and the design of the current-limit circuit. The continuous load current (I_{LOAD}) determines the thermal stresses and thus drives the selection of input capacitors, MOSFETs, and other critical heat-contributing components.
- **Switching Frequency:** This choice determines the basic trade-off between size and efficiency. The optimal frequency is largely a function of maximum input voltage due to MOSFET switching losses that are proportional to frequency and V_{IN}². The optimum frequency is also a moving target due to rapid improvements in MOSFET technology that are making higher frequencies more practical.
- **Inductor Operating Point:** This choice provides trade-offs between size vs. efficiency and transient response vs. output ripple. Low inductor values provide better transient response and smaller physical size, but also result in lower efficiency and higher output ripple due to increased ripple currents. The minimum practical inductor value is one that causes the circuit to operate at the edge of critical conduction (where the inductor current just touches zero with every cycle at maximum load). Inductor values

Table 4. Fault Protection and Shutdown Operation Table

MODE	CONTROLLER STATE	DRIVER STATE
Shutdown (ON_ = High to Low); Output UVP (Latched)	Voltage soft-shutdown initiated. Internal error-amplifier target slowly ramped down to GND and output actively discharged (automatically enters forced-PWM mode).	DL driven high and DH pulled low after soft-shutdown completed (output < 0.1V).
Output OVP (Latched)	Controller shuts down and EA target internally slewed down. Controller remains off until ON_ toggled or V _{CC} power cycled.	DL immediately driven high, DH pulled low.
V _{CC} UVLO Falling-Edge Thermal Fault (Latched)	SMPS controller disabled (assuming ON_ pulled high), 10Ω output discharge active.	DL and DH pulled low.
V _{CC} UVLO Rising Edge	SMPS controller enabled (assuming ON_ pulled high).	DL driven high, DH pulled low.
V _{CC} POR	SMPS inactive, 10Ω output discharge active.	DL driven high, DH pulled low.