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19-4577; Rev 1; 8/09

EVALUATION KIT AVAILABLE

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

General Description

The MAX17030/MAX17036 are 3/2-phase interleaved Quick-PWM™ step-down VID power-supply controllers for IMVP-6.5 notebook CPUs. Two integrated drivers and the option to drive a third phase using an external driver such as the MAX8791 allow for a flexible 3/2-phase configuration depending on the CPU being supported.

True out-of-phase operation reduces input ripple-current requirements and output-voltage ripple while easing component selection and layout difficulties. The Quick-PWM control provides instantaneous response to fast load-current steps. Active voltage positioning reduces power dissipation and bulk output capacitance requirements and allows ideal positioning compensation for tantalum, polymer, or ceramic bulk output capacitors.

The MAX17030/MAX17036 are intended for bucking down the battery directly to create the core voltage. The single-stage conversion method allows this device to directly step down high-voltage batteries for the highest possible efficiency.

A slew-rate controller allows controlled transitions between VID codes. A thermistor-based temperature sensor provides programmable thermal protection. An output current monitor provides an analog current output proportional to the sum of the inductor currents, which in steady state is the same as the current consumed by the CPU.

Applications

IMVP-6.5 SV and XE Core Power Supplies

High-Current Voltage-Positioned Step-Down Converters

3 to 4 Li+ Cells Battery to CPU Core Supply Converters

Notebooks/Desktops/Servers

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17030GTL+	-40°C to +105°C	40 TQFN-EP*
MAX17036GTL+	-40°C to +105°C	40 TQFN-EP*

+Denotes a lead-free(Pb)/RoHS-compliant package.

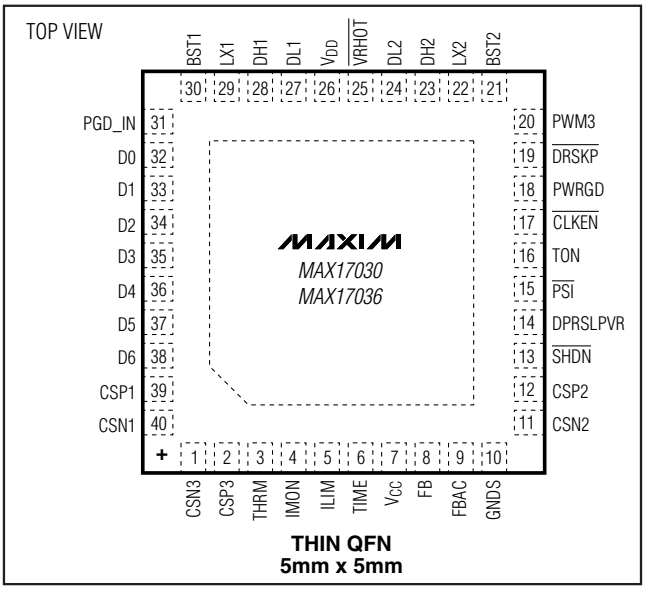
**EP = Exposed pad.*

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Features

- **Triple/Dual-Phase Quick-PWM Controllers**
- **2 Internal Drivers + 1 External Driver**
- **±0.5% V_{OUT} Accuracy Over Line, Load, and Temperature**
- **7-Bit IMVP-6.5 DAC**
- **Dynamic Phase Selection Optimizes Active/Sleep Efficiency**
- **Transient Phase Overlap Reduces Output Capacitance**
- **Transient Suppression Feature (MAX17036 Only)**
- **Integrated Boost Switches**
- **Active Voltage Positioning with Adjustable Gain**
- **Accurate Lossless Current Balance and Current Limit**
- **Remote Output and Ground Sense**
- **Adjustable Output Slew-Rate Control**
- **Power-Good (IMVPOK), Clock Enable ($\overline{CLKEN}$), and Thermal-Fault (VRHOT) Outputs**
- **IMVP-6.5 Power Sequencing and Timing Compliant**
- **Output Current Monitor (IMON)**
- **Drives Large Synchronous Rectifier FETs**
- **7V to 26V Battery Input Range**
- **Adjustable Switching Frequency (600kHz max)**
- **Undervoltage, Overvoltage, and Thermal-Fault Protection**

Pin Configuration



THIN QFN
5mm x 5mm

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC}, V_{DD} to GND .....-0.3V to +6V
D0–D6, PGD_IN, $\overline{PSI}$, DPRSLPVR to GND .....-0.3V to +6V
CSP_, CSN_, THRM, ILIM to GND.....-0.3V to +6V
PWRGD, $\overline{CLKEN}$, $\overline{VR\_HOT}$ to GND.....-0.3V to +6V
FB, FBAC, IMON, TIME to GND .....-0.3V to (V_{CC} + 0.3V)
$\overline{SHDN}$ to GND (Note 2).....-0.3V to +30V
TON to GND .....-0.3V to +30V
GNDS to GND .....-0.3V to +0.3V
DL1, DL2, PWM3, $\overline{DRSKP}$ to GND .....-0.3V to (V_{DD} + 0.3V)
BST1, BST2 to GND .....-0.3V to +36V
BST1, BST2 to V_{DD}.....-0.3V to +30V
LX1 to BST1.....-6V to +0.3V
LX2 to BST2.....-6V to +0.3V
DH1 to LX1 .....-0.3V to (V_{BST1} + 0.3V)
DH2 to LX2 .....-0.3V to (V_{BST2} + 0.3V)
Continuous Power Dissipation (40-pin, 5mm x 5mm TQFN)
Up to +70°C 1778mW
Derating above +70°C .....22.2mW/°C
Operating Temperature Range .....-40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Absolute Maximum Ratings valid using 20MHz bandwidth limit.

Note 2: $\overline{SHDN}$ might be forced to 12V for the purpose of debugging prototype breadboards using the no-fault test mode. Internal BST switches are disabled as well. Use external BST diodes when $\overline{SHDN}$ is forced to 12V.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
		V_{IN}		7		26	
FB Output Voltage Accuracy	V_{FB}	Measured at FB with respect to GNDS; includes load-regulation error (Note 3)	DAC codes from 0.8125V to 1.5000V	-0.5		+0.5	%
			DAC codes from 0.3750V to 0.8000V	-7		+7	mV
			DAC codes from 0 to 0.3625V	-20		+20	
Boot Voltage	V_{BOOT}			1.094	1.100	1.106	V
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 26V			0.1		%
FB Input Bias Current		T_A = +25°C		-0.1		+0.1	µA
GNDS Input Range				-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97	1.00	1.03	V/V
GNDS Input Bias Current	I_{GNDS}	T_A = +25°C		-0.5		+0.5	µA
TIME Regulation Voltage	V_{TIME}	R_{TIME} = 147kΩ		1.985	2.000	2.015	V
TIME Slew-Rate Accuracy		R_{TIME} = 147kΩ (6.08mV/µs nominal)		-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)		-15		+15	
		Soft-start and soft-shutdown: R_{TIME} = 35.7kΩ (6.25mV/µs nominal) to 178kΩ (1.25mV/µs nominal)		-20		+20	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Time Accuracy	t_{ON}	V_{IN} = 10V, V_{FB} = 1.0V, measured at DH1, DH2, and PWM3 (Note 4)	R_{TON} = 96.75kΩ (600kHz per phase), 167ns nominal	-15		+15	%
			R_{TON} = 200kΩ (300kHz per phase), 333ns nominal	-10		+10	
			R_{TON} = 303.25kΩ (200kHz per phase), 500ns nominal	-15		+15	
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH1, DH2, and PWM3 (Note 4)			300	375	ns
TON Shutdown Input Current	$I_{TON,SDN}$	$\overline{SHDN}$ = GND, V_{IN} = 26V, V_{CC} = V_{DD} = 0 or 5V, T_A = +25°C			0.01	0.1	µA
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, $V_{DPRSLPVR}$ = 5V, FB forced above the regulation point			3.5	7	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, $V_{DPRSLPVR}$ = 0, FB forced above the regulation point, T_A = +25°C			0.02	1	µA
Shutdown Supply Current (V_{CC})	$I_{CC,SDN}$	Measured at V_{CC}, $\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
Shutdown Supply Current (V_{DD})	$I_{DD,SDN}$	Measured at V_{DD}, $\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
FAULT PROTECTION							
Output Overvoltage-Protection Threshold	V_{OVP}	Skip mode after output reaches the regulation voltage or PWM mode; measured at FB with respect to the voltage target set by the VID code (see Table 4)		250	300	350	mV
		Soft-start, soft-shutdown, skip mode, and output have not reached the regulation voltage; measured at FB		1.45	1.50	1.55	V
		Minimum OVP threshold; measured at FB			0.8		
Output Overvoltage-Propagation Delay	t_{OVP}	FB forced 25mV above trip threshold			10		µs
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to the voltage target set by the VID code (see Table 4)		-450	-400	-350	mV
Output Undervoltage-Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold			10		µs
$\overline{CLKEN}$ Startup Delay and Boot Time Period	t_{BOOT}	Measured from the time when FB reaches the boot target voltage (Note 3)		20	60	100	µs

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWRGD Startup Delay		Measured at startup from the time when $\overline{CLKEN}$ goes low		3	6.5	10	ms
$\overline{CLKEN}$ and PWRGD Threshold		Measured at FB with respect to the voltage target set by the VID code (see Table 4), 20mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350	-300	-250	mV
			Upper threshold, rising edge (overvoltage)	+150	+200	+250	
$\overline{CLKEN}$ and PWRGD Delay		FB forced 25mV outside the PWRGD trip thresholds			10		µs
$\overline{CLKEN}$ and PWRGD Transition Blanking Time (VID Transitions)	t_{BLANK}	Measured from the time when FB reaches the target voltage (Note 3)			20		µs
$\overline{CLKEN}$, PWRGD Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
$\overline{CLKEN}$, PWRGD Leakage Current		High-Z state, pin forced to 5V, T_A = +25°C				1	µA
CSN1 Pulldown Resistance in UVLO and Shutdown		$\overline{SHDN}$ = GND, measured after soft-shutdown completed (DL = low)			8		Ω
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level		4.05	4.27	4.48	V
THERMAL PROTECTION							
$\overline{VRHOT}$ Trip Threshold		Measured at THRM with respect to V_{CC}; falling edge, typical hysteresis = 75mV		29	30	31	%
$\overline{VRHOT}$ Delay	$t_{\overline{VRHOT}}$	THRM forced 25mV below the $\overline{VRHOT}$ trip threshold, falling edge			10		µs
$\overline{VRHOT}$ Output On-Resistance	$R_{ON(\overline{VRHOT})}$	Low state			2	8	Ω
$\overline{VRHOT}$ Leakage Current		High-Z state, $\overline{VRHOT}$ forced to 5V, T_A = +25°C				1	µA
THRM Input Leakage	I_{THRM}	V_{THRM} = 0 to 5V, T_A = +25°C		-0.1		+0.1	µA
Thermal-Shutdown Threshold	T_{SHDN}	Typical hysteresis = 15°C			+160		°C
VALLEY CURRENT LIMIT, DROOP, CURRENT BALANCE, AND CURRENT MONITOR							
Current-Limit Threshold Voltage (Positive)	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$	V_{TIME} - V_{ILIM} = 100mV	7	10	13	mV
			V_{TIME} - V_{ILIM} = 500mV	45	50	55	
			ILIM = V_{CC}	20	22.5	25	
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	$V_{CSP\_}$ - $V_{CSN\_}$, nominally -125% of V_{LIMIT}		-4		+4	mV
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZX}	V_{GND} - $V_{LX\_}$, $V_{DPRSLPVR}$ = 5V			0		mV
CSP_, CSN_ Common-Mode Input Range				0		2	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Phases 2, 3 Disable Threshold		Measured at CSP2, CSP3		3	V_{CC} - 1	V_{CC} - 0.4	V
CSP_, CSN_ Input Current	I_{CSP}, I_{CSN}	T_A = +25°C		-0.2		+0.2	µA
ILIM Input Current	I_{ILIM}	T_A = +25°C		-0.1		+0.1	µA
Droop Amplifier Offset		(1/N) x Σ($V_{CSP\_}$ - $V_{CSN\_}$) at I_{FBAC} = 0; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3	T_A = +25°C	-0.5		+0.5	mV/ phase
			T_A = 0°C to +85°C	-0.75		+0.75	
Droop Amplifier Transconductance	$G_{m(FBAC)}$	$\Delta I_{FBAC}/\Delta[\Sigma(V_{CSP\_} - V_{CSN\_})]$; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3, V_{FBAC} = $V_{CSN\_}$ = 0.45V to 1.5V		393	400	406	µS
Current-Monitor Offset		(1/N) x Σ($V_{CSP\_}$ - $V_{CSN\_}$) at I_{IMON} = 0, Σ indicates summation over all power-up enabled phases from 1 to N, N = 3		-1.1		+1	mV/ phase
Current-Monitor Transconductance	$G_{m(IMON)}$	$\Delta I_{IMON}/\Delta[\Sigma(V_{CSP\_} - V_{CSN\_})]$; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3, $V_{CSN\_}$ = 0.45V to 1.5V		1.552	1.6	1.648	mS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V	High state (pullup)		0.9	2.5	Ω
			Low state (pulldown)		0.7	2	
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$		High state (pullup)		0.7	2	Ω
			Low state (pulldown)		0.25	0.7	
DH_ Gate-Driver Source Current	$I_{DH(SOURCE)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.2		A
DH_ Gate-Driver Sink Current	$I_{DH(SINK)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.7		A
DL_ Gate-Driver Source Current	$I_{DL(SOURCE)}$	DL_ forced to 2.5V			2.7		A
DL_ Gate-Driver Sink Current	$I_{DL(SINK)}$	DL_ forced to 2.5V			8		A
DL_ Transition Time		DL_ falling, $C_{DL\_}$ = 3nF			20		ns
		DL rising, $C_{DL\_}$ = 3nF			20		
DH_ Transition Time		DH_ falling, $C_{DH\_}$ = 3nF			20		ns
		DH_ rising, $C_{DH\_}$ = 3nF			20		
Internal BST_ Switch On-Resistance	$R_{ON(BST)}$	$I_{BST\_}$ = 10mA			10	20	Ω

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PWM3, $\overline{DRSKP}$ OUTPUTS						
PWM3, $\overline{DRSKP}$ Output High Voltages		I_{SOURCE} = 3mA	V_{DD} - 0.4V			V
PWM3, $\overline{DRSKP}$ Output Low Voltages		I_{SINK} = 3mA			0.4	V
LOGIC AND I/O						
Logic-Input High Voltage	V_{IH}	$\overline{SHDN}$, PGD_IN	2.3			V
Logic-Input Low Voltage	V_{IL}	$\overline{SHDN}$, PGD_IN			1.0	V
Low-Voltage Logic-Input High Voltage	V_{IHLV}	$\overline{PSI}$, D0–D6, DPRSLPVR	0.67			V
Low-Voltage Logic-Input Low Voltage	V_{ILLV}	$\overline{PSI}$, D0–D6, DPRSLPVR			0.33	V
Logic Input Current		T_A = +25°C; $\overline{SHDN}$, DPRSLPVR, PGD_IN, $\overline{PSI}$, D0–D6 = 0 or 5V	-1		+1	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = -40ºC to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
		V_{IN}		7		26	
FB Output-Voltage Accuracy	V_{FB}	Measured at FB with respect to GNDS, includes load-regulation error (Note 3)	DAC codes from 0.8125V to 1.5000V	-0.75		+0.75	%
			DAC codes from 0.3750V to 0.8000V	-10		+10	mV
			DAC codes from 0 to 0.3625V	-25		+25	
Boot Voltage	V_{BOOT}			1.085		1.115	V
GNDS Input Range				-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.95		1.05	V/V
TIME Regulation Voltage	V_{TIME}	R_{TIME} = 147kΩ		1.985		2.015	V
TIME Slew-Rate Accuracy		R_{TIME} = 147kΩ (6.08mV/µs nominal)		-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)		-15		+15	
		Soft-start and soft-shutdown: R_{TIME} = 35.7kΩ (6.25mV/µs nominal) to 178kΩ (1.25mV/µs nominal)		-20		+20	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Time Accuracy	t_{ON}	V_{IN} = 10V, V_{FB} = 1.0V, measured at DH1, DH2, and PWM3 (Note 4)	R_{TON} = 96.75kΩ (600kHz per phase), 167ns nominal	-15		+15	%
			R_{TON} = 200kΩ (300kHz per phase), 333ns nominal	-10		+10	
			R_{TON} = 303.25kΩ (200kHz per phase), 500ns nominal	-15		+15	
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH1, DH2, and PWM3 (Note 4)				400	ns
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, DPRSLPVR = 5V, FB forced above the regulation point				7	mA
FAULT PROTECTION							
Output Overvoltage-Protection Threshold	V_{OVP}	Skip mode after output reaches the regulation voltage or PWM mode; measured at FB with respect to the voltage target set by the VID code (see Table 4)		250		350	mV
		Soft-start, soft-shutdown, skip mode, and output have not reached the regulation voltage; measured at FB		1.45		1.55	V
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to the voltage target set by the VID code (see Table 4)		-450		-350	mV
$\overline{CLKEN}$ Startup Delay and Boot Time Period	t_{BOOT}	Measured from the time when FB reaches the boot target voltage (Note 3)		20		100	µs
PWRGD Startup Delay		Measured at startup from the time when $\overline{CLKEN}$ goes low		3		10	ms
$\overline{CLKEN}$ and PWRGD Threshold		Measured at FB with respect to the voltage target set by the VID code (see Table 4), 20mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350		-250	mV
			Upper threshold, rising edge (overvoltage)	+150		+250	
$\overline{CLKEN}$, PWRGD Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level		4.05		4.5	V
THERMAL PROTECTION							
$\overline{VRHOT}$ Trip Threshold		Measured at THRM with respect to V_{CC}, falling edge, typical hysteresis = 75mV		29		31	%
$\overline{VRHOT}$ Output On-Resistance	$R_{ON(\overline{VRHOT})}$	Low state				8	Ω

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGD_IN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, $V_{DPRSLPVR}$ = V_{GNDS} = 0, $V_{CSP\_}$ = $V_{CSN\_}$ = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN_, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VALLEY CURRENT LIMIT, DROOP, CURRENT BALANCE, AND CURRENT MONITOR							
Current-Limit Threshold Voltage (Positive)	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$	V_{TIME} - V_{ILIM} = 100mV	7		13	mV
			V_{TIME} - V_{ILIM} = 500mV	45		55	
			ILIM = V_{CC}	20		25	
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	$V_{CSP\_}$ - $V_{CSN\_}$, nominally -125% of V_{LIMIT}		-4		+4	mV
CSP_, CSN_ Common-Mode Input Range				0		2	V
Phases 2, 3 Disable Threshold		Measured at CSP2, CSP3		3		V_{CC} - 0.4	V
Droop Amplifier Offset		(1/N) x Σ($V_{CSP\_}$ - $V_{CSN\_}$) at I_{FBAC} = 0; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3		-1		+1	mV/ phase
Droop Amplifier Transconductance	$G_{m(FBAC)}$	$\Delta I_{FBAC}/\Delta[\Sigma(V_{CSP\_} - V_{CSN\_})]$; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3, V_{FBAC} = $V_{CSN\_}$ = 0.45V to 1.5V		390		407	µS
Current-Monitor Offset		(1/N) x Σ($V_{CSP\_}$ - $V_{CSN\_}$) at I_{FBAC} = 0; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3		-1.5		+1.5	mV/ phase
Current-Monitor Transconductance	$G_{m(IMON)}$	$\Delta I_{IMON}/\Delta[\Sigma(V_{CSP\_} - V_{CSN\_})]$; Σ indicates summation over all power-up enabled phases from 1 to N, N = 3, $V_{CSN\_}$ = 0.45V to 1.5V		1.536		1.664	mS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ – LX_ forced to 5V	High state (pullup)			2.5	Ω
			Low state (pulldown)			2	
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)				2	Ω
		Low state (pulldown)				0.7	
Internal BST_ Switch On-Resistance	$R_{ON(BST)}$	I_{BST-} = 10mA				20	Ω
PWM3, $\overline{DRSKP}$ OUTPUTS							
PWM3, $\overline{DRSKP}$ Output High Voltages		I_{SOURCE} = 3mA		V_{DD} - 0.4V			V
PWM3, $\overline{DRSKP}$ Output Low Voltages		I_{SINK} = 3mA				0.4	V
LOGIC AND I/O							
Logic-Input High Voltage	V_{IH}	$\overline{SHDN}$, PGD_IN		2.3			V
Logic-Input Low Voltage	V_{IL}	$\overline{SHDN}$, PGD_IN				1.0	V
Low-Voltage Logic-Input High Voltage	V_{IHLV}	$\overline{PSI}$, D0–D6, DPRSLPVR		0.67			V
Low-Voltage Logic-Input Low Voltage	V_{ILLV}	$\overline{PSI}$, D0–D6, DPRSLPVR				0.33	V

ELECTRICAL CHARACTERISTICS (continued)

Note 3: The equation for the target voltage V_{TARGET} is:
V_{TARGET} = The slew-rate-controlled version of V_{DAC}, where V_{DAC} = 0 for shutdown
$V_{DAC} = V_{BOOT}$ during IMVP-6.5 startup
$V_{DAC} = V_{VID}$ otherwise (the V_{VID} voltages for all possible VID codes are given in Table 4).
In pulse-skipping mode, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

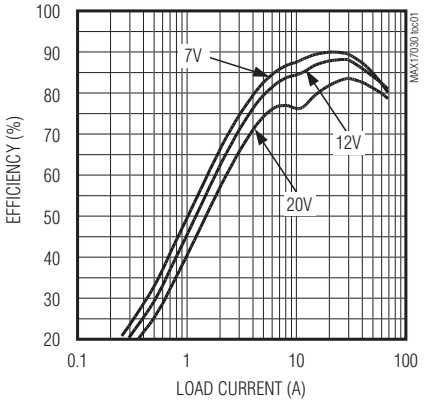
Note 4: On-time and minimum off-time specifications are measured from 50% to 50% at the DH_ pin, with LX_ forced to 0V, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times might be different due to MOSFET switching speeds.

Note 5: Specifications to -40°C and +105°C are guaranteed by design, not production tested.

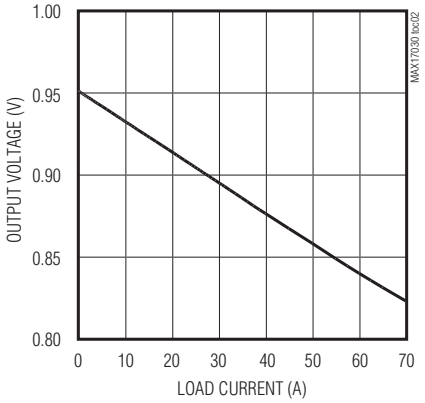
Typical Operating Characteristics

(Circuit of Figure 1. V_{IN} = 12V, $V_{CC} = V_{DD}$ = 5V, $\overline{SHDN} = V_{CC}$, D0–D6 set for 0.95V, T_A = +25°C, unless otherwise specified.)

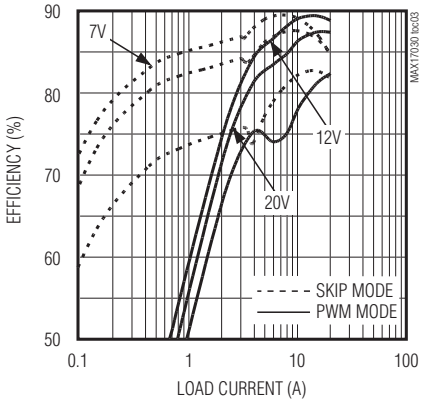
EFFICIENCY vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 0.95V)



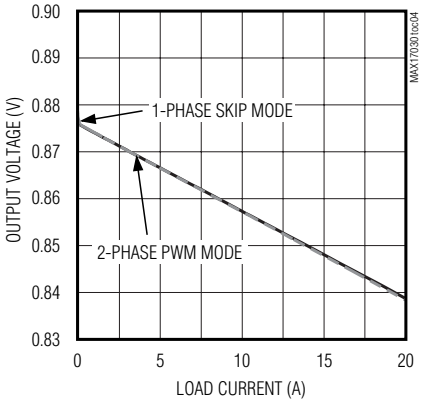
OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 0.95V)



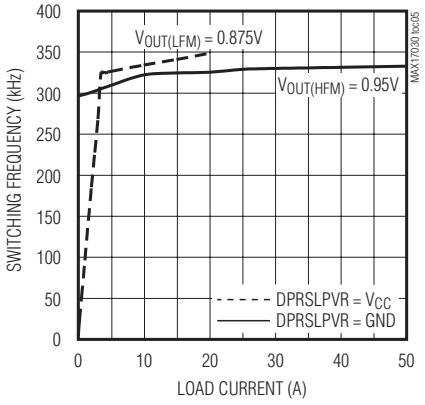
EFFICIENCY vs. LOAD CURRENT ($V_{OUT(LFM)}$ = 0.875V)



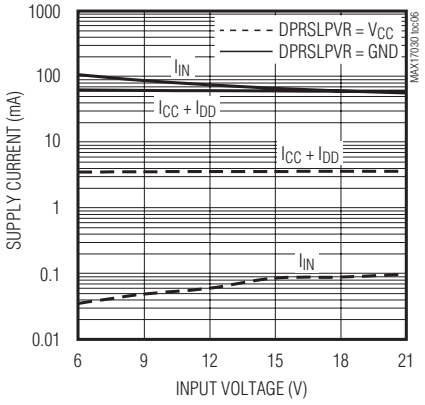
OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(LFM)}$ = 0.875V)



SWITCHING FREQUENCY vs. LOAD CURRENT



$V_{OUT(HFM)}$ = 0.95V NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE

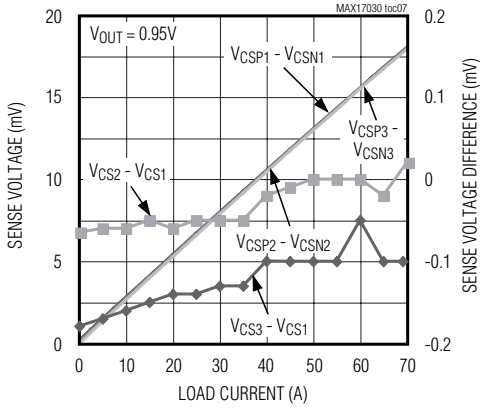


1/2/3-Phase-Quick-PWM IMVP-6.5 VID Controllers

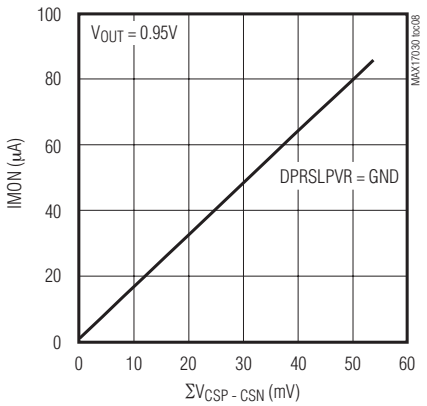
Typical Operating Characteristics (continued)

(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 0.95V, T_A = +25°C, unless otherwise specified.)

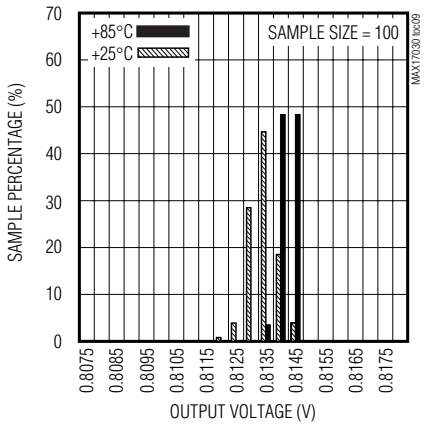
CURRENT BALANCE vs. LOAD CURRENT



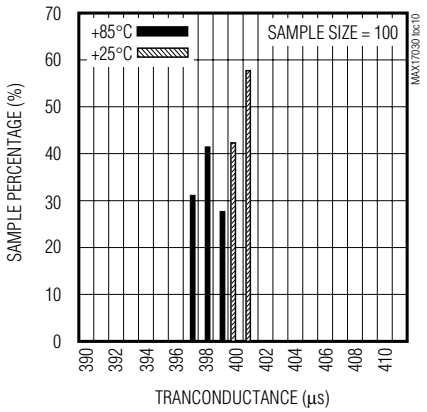
I_{IMON} vs. LOAD CURRENT



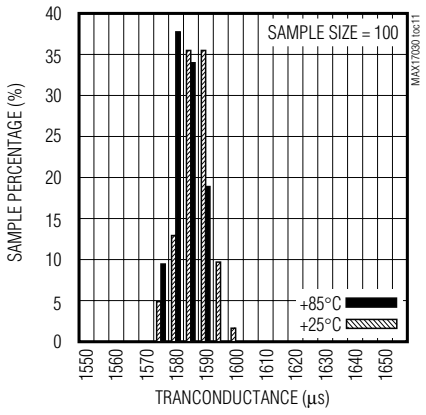
0.8125V OUTPUT VOLTAGE DISTRIBUTION



$G_{m(FB)}$ TRANSCONDUCTANCE DISTRIBUTION



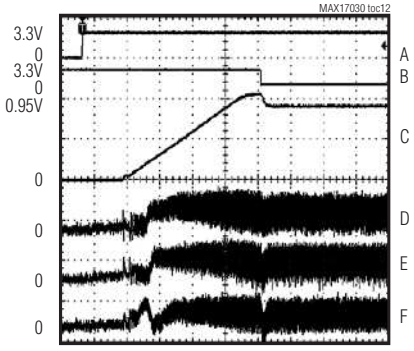
$G_{m(IMON)}$ TRANSCONDUCTANCE DISTRIBUTION



Typical Operating Characteristics (continued)

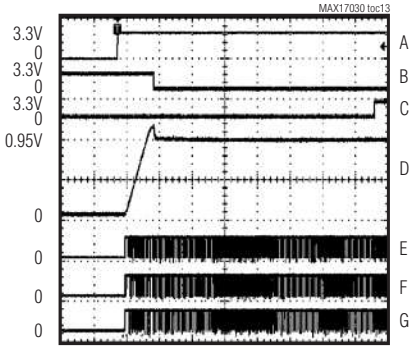
(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 0.95V, T_A = +25°C, unless otherwise specified.)

SOFT-START WAVEFORM (UP TO $\overline{CLKEN}$)



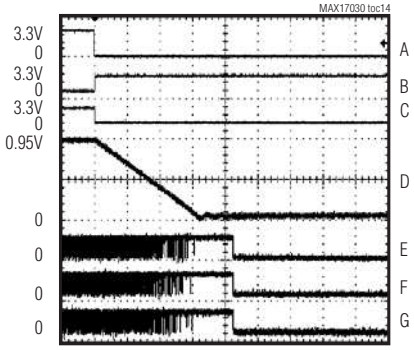
A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 10V/div
C. V_{OUT}, 500mV/div
D. I_{LX1}, 10A/div
E. I_{LX2}, 10A/div
F. I_{LX3}, 10A/div
I_{OUT}, 15A

SOFT-START WAVEFORM (UP TO PWRGD)



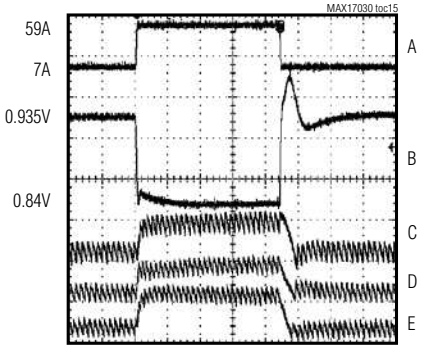
A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 6.6V/div
C. PWRGD, 10V/div
D. V_{OUT}, 1V/div
E. DL1, 10V/div
F. DL2, 10V/div
G. DL3, 10V/div
I_{OUT}, 15A

SHUTDOWN WAVEFORM



A. $\overline{SHDN}$, 5V/div
B. PWRGD, 10V/div
C. $\overline{CLKEN}$, 10V/div
D. V_{OUT}, 500mV/div
E. DL1, 10V/div
F. DL2, 10V/div
G. DL3, 10V/div

LOAD-TRANSIENT RESPONSE (HFM MODE)



A. I_{OUT} = 7A - 59A
B. V_{OUT}, 50mV/div
C. I_{LX1}, 20A/div
D. I_{LX2}, 20A/div
E. I_{LX3}, 20A/div

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

Pin Description

PIN	NAME	FUNCTION
1	CSN3	Negative Input of the Output Current Sense of Phase 3. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
2	CSP3	Positive Input of the Output Current Sense of Phase 3. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. To disable phase 3, connect CSP3 to V_{CC} and CSN3 to GND.
3	THRM	Input of Internal Comparator. Connect the output of a resistor- and thermistor-divider (between V_{CC} and GND) to THRM. Select the components such that the voltage at THRM falls below 1.5V (30% of V_{CC}) at the desired high temperature.
4	IMON	Current Monitor Output Pin. The output current at this pin is: $I_{IMON} = G_{M(IMON)} \times \Sigma V(CSP\_,CSN\_)$ where $G_{M(IMON)}$ = 1.6mS typical and Σ denotes summation over all enabled phases. An external resistor R_{IMON} between IMON and GNDS sets the current-monitor output voltage: $V_{IMON} = I_{LOAD} \times R_{SENSE} \times G_{M(IMON)} \times R_{IMON}$ where R_{SENSE} is the value of the effective current-sense resistance. Choose R_{IMON} such that V_{IMON} does not exceed 900mV at the maximum expected load current I_{MAX}. IMON is high impedance when the MAX17030/MAX17036 are in shutdown.
5	ILIM	Current-Limit Adjust Input. The valley positive current-limit threshold voltages at V(CSP_,CSN_) are precisely 1/10 the differential voltage V(TIME,ILIM) over a 0.1V to 0.5V range of V(TIME,ILIM). The valley negative current-limit thresholds are typically -125% of the corresponding valley positive current-limit thresholds. Connect ILIM to V_{CC} to get the default current-limit threshold setting of 22.5mV typ.
6	TIME	Slew-Rate Adjustment Pin. The total resistance R_{TIME} from TIME to GND sets the internal slew rate: Slew rate = (12.5mV/µs) x (71.5kΩ/R_{TIME}) where R_{TIME} is between 35.7kΩ and 178kΩ. This “normal” slew rate applies to transitions into and out of the low-power pulse-skipping modes and to the transition from boot mode to VID. The slew rate for startup and for entering shutdown is always 1/4 of normal. If the VID DAC inputs are clocked, the slew rate for all other VID transitions is set by the rate at which they are clocked, up to a maximum slew rate equal to the normal slew rate defined above.
7	V_{CC}	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with 1µF minimum.
8	FB	Feedback Voltage Input. The voltage at the FB pin is compared with the slew-rate-controlled target voltage by the error comparator (fast regulation loop), as well as by the internal voltage integrator (slow, accurate regulation loop). Having sufficient ripple signal at FB that is in phase with the sum of the inductor currents is essential for cycle-by-cycle stability. The external connections and compensation at FB depend on the desired DC and transient (AC) droop values. If DC droop = AC droop, then short FB to FBAC. To disable DC droop, connect FB to the remote-sensed output voltage through a resistor R and feed forward the FBAC ripple to FB through capacitor C, where the R x C time constant should be at least 3x the switching period per phase.

Pin Description (continued)

PIN	NAME	FUNCTION
9	FBAC	Output of the Voltage-Positioning Transconductance Amplifier. Connect a resistor R_{FBAC} between FBAC and the positive side of the feedback remote sense to set the transient (AC) droop based on the stability, load-transient response, and voltage-positioning gain requirements: $R_{FBAC} = R_{DROOP,AC}/[R_{SENSE} \times G_{m(FBAC)}]$ where $R_{DROOP,AC}$ is the transient (AC) voltage-positioning slope that provides an acceptable tradeoff between stability and load-transient response, $G_{m(FBAC)}$ = 400µS typ, and R_{SENSE} is the effective current-sense resistance that is used to provide the (CSP_, CSN_) current-sense voltages. A minimum $R_{DROOP,AC}$ value is required for stability, but if there are no ceramic output capacitors used, then the minimum requirement applies to $R_{ESR} + R_{DROOP,AC}$, where R_{ESR} is the effective ESR of the output capacitors. If lossless sensing (inductor DCR sensing) is used, use a thermistor-resistor network to minimize the temperature dependence of the voltage-positioning slope. FBAC is high impedance in shutdown.
10	GNDS	Feedback Remote-Sense Input, Negative Side. Normally connected to GND directly at the load. GNDS internally connects to a transconductance amplifier that fine tunes the output voltage compensating for voltage drops from the regulator ground to the load ground.
11	CSN2	Negative Input of the Output Current Sense of Phase 2. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
12	CSP2	Positive Input of the Output Current Sense of Phase 2. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. To disable phase 2, connect CSP2 to V_{CC} and CSN2 to GND.
13	$\overline{SHDN}$	Shutdown Control Input. Connect to V_{CC} for normal operation. Connect to ground to put the IC into the 1µA (max at T_A = +25°C) shutdown state. During startup, the output voltage is ramped up at 1/4 the slew rate set by the TIME resistor to the boot voltage or to the target voltage. During the transition from normal operation to shutdown, the output voltage is ramped down at 1/4 the slew rate set by the TIME resistor. Forcing $\overline{SHDN}$ to 11V~13V to enter no-fault test mode clears the fault latches, disables transient phase overlap, and turns off the internal BST_-to-V_{DD} switches. However, internal diodes still exist between BST_ and V_{DD} in this state.
14	DPRSLPVR	Deeper Sleep VR Control Input. This low-voltage logic input indicates power usage and sets the operating mode together with $\overline{PSI}$ as shown in the truth table below. When DPRSLPVR is forced high, the controller is immediately set to 1-phase automatic pulse-skipping mode. The controller returns to forced-PWM mode when DPRSLPVR is forced low and the output is in regulation. The PWRGD upper threshold is blanked during any downward output-voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete and the output reaches regulation. During this blanking period, the overvoltage fault threshold is changed from a tracking [VID + 300mV] threshold to a fixed 1.5V threshold. The controller is in N-phase skip mode during startup including boot mode, but is in N-phase forced-PWM mode during the transition from boot mode to VID mode, during soft-shutdown, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. However, if phases 2 and 3 are disabled by connecting CSP2, CSP3 to V_{CC}, then only phase 1 is active in the above modes.

DPRSLPVR	$\overline{PSI}$	MODE
1	X	Very low current (1-phase skip)
0	0	Intermediate power potential (N-1-phase PWM)
0	1	Max power potential (full-phase PWM: N-phase or 1 phase as set by user at CSP2, CSP3)

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

Pin Description (continued)

PIN	NAME	FUNCTION
15	$\overline{PSI}$	This low-voltage logic input indicates power usage and sets the operating mode together with DPRSLPVR as shown in the truth table below. While DPRSLPVR is low, if $\overline{PSI}$ is forced low, the controller is immediately set to (N-1)-phase forced-PWM mode. The controller returns to N-phase forced-PWM mode when $\overline{PSI}$ is forced high. The controller is in N-phase skip mode during startup including boot mode, but is in N-phase forced-PWM mode during the transition from boot mode to VID mode, during soft-shutdown, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. However, if phases 2 and 3 are disabled by connecting CSP2, CSP3 to VCC, then only phase 1 is active in the above modes.
		DPRSLPVR / **$\overline{PSI}$** / **MODE** 1 / X / Very low current (1-phase skip) 0 / 0 / Intermediate power potential (N-1-phase PWM) 0 / 1 / Max power potential (full-phase PWM: N-phase or 1 phase as set by user at CSP2, CSP3)
16	TON	Switching Frequency Setting Input. An external resistor between the input power source and this pin sets the switching frequency according to the following equation: $f_{SW} = 1/(C_{TON} \times (R_{TON} + 6.5k\Omega))$ where C_{TON} = 16.26pF. The external resistor must also satisfy the requirement $[V_{IN(MIN)}/R_{TON}] \geq 10\mu A$ where $V_{IN(MIN)}$ is the minimum V_{IN} value expected in the application. TON is high impedance in shutdown.
17	$\overline{CLKEN}$	Clock Enable Open-Drain Logic Output Powered by V_{3P3}. This inverted logic output indicates when the output voltage sensed at FB is in regulation. $\overline{CLKEN}$ is forced high in shutdown and during soft-start and soft-stop transitions. $\overline{CLKEN}$ is forced low during dynamic VID transitions and for an additional 20µs after the transition is completed. $\overline{CLKEN}$ is the inverse of PWRGD, except for the 5ms PWRGD startup delay period after $\overline{CLKEN}$ is pulled low. See the startup timing diagram (Figure 9). The $\overline{CLKEN}$ upper threshold is blanked during any downward output-voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete and the output reaches regulation.
18	PWRGD	Open-Drain Power-Good Output. After output-voltage transitions, except during power-up and power-down, if FB is in regulation, then PWRGD is high impedance. PWRGD is low during startup, continues to be low while the output is at the boot voltage, and stays low until 5ms (typ) after $\overline{CLKEN}$ goes low, after which it starts monitoring the FB voltage and goes high if FB is within the PWRGD threshold window. PWRGD is forced low during soft-shutdown and while in shutdown. PWRGD is forced high impedance whenever the slew-rate controller is active (output-voltage transitions), and continues to be forced high impedance for an additional 20µs after the transition is completed. The PWRGD upper threshold is blanked during any downward output-voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete and the output reaches regulation. A pullup resistor on PWRGD causes additional finite shutdown current.
19	$\overline{DRSKP}$	Driver Skip Control Output. Push/pull logic output that controls the operating mode of the skip-mode driver IC. $\overline{DRSKP}$ swings from V_{DD} to GND. When $\overline{DRSKP}$ is high, the driver ICs operate in forced-PWM mode. When $\overline{DRSKP}$ is low, the driver ICs enable their zero-crossing comparators and operate in pulse-skipping mode. $\overline{DRSKP}$ goes low at the end of the soft-shutdown sequence, instructing the external drivers to shut down.

Pin Description (continued)

PIN	NAME	FUNCTION
20	PWM3	PWM Signal Output for Phase 3. Swings from GND to V_{DD}. Three-state whenever phase 3 is disabled (in shutdown, when CSP3 is connected to V_{CC}, and when operating with fewer than all phases).
21	BST2	Phase 2 Boost Flying Capacitor Connection. BST2 is the internal upper supply rail for the DH2 high-side gate driver. An internal switch between V_{DD} and BST2 charges the BST2-LX2 flying capacitor while the low-side MOSFET is on (DL2 pulled high).
22	LX2	Phase 2 Inductor Connection. LX2 is the internal lower supply rail for the DH2 high-side gate driver. Also used as an input to phase 2's zero-crossing comparator.
23	DH2	Phase 2 High-Side Gate-Driver Output. DH2 swings from LX2 to BST2. Low in shutdown.
24	DL2	Phase 2 Low-Side Gate-Driver Output. DL2 swings from GND to V_{DD}. DL2 is forced low in shutdown. DL2 is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DL2 is forced low in skip mode after detecting an inductor current zero crossing.
25	$\overline{VRHOT}$	Open-Drain Output of Internal Comparator. $\overline{VRHOT}$ is pulled low when the voltage at THRM goes below 1.5V (30% of V_{CC}). $\overline{VRHOT}$ is high impedance in shutdown.
26	V_{DD}	Supply Voltage Input for the DL_ Drivers. V_{DD} is also the supply voltage used to internally recharge the BST_-LX_ flying capacitor during the times the respective DL_s are high. Connect V_{DD} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD} to GND with a 1µF or greater ceramic capacitor.
27	DL1	Phase 1 Low-Side Gate-Driver Output. DL1 swings from GND to V_{DD}. DL1 is forced low in shutdown. DL1 is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DL1 is forced low in skip mode after detecting an inductor current zero crossing.
28	DH1	Phase 1 High-Side Gate-Driver Output. DH1 swings from LX1 to BST1. Low in shutdown.
29	LX1	Phase 1 Inductor Connection. LX1 is the internal lower supply rail for the DH1 high-side gate driver. Also used as an input to phase 1's zero-crossing comparator.
30	BST1	Phase 1 Boost Flying Capacitor Connection. BST1 is the internal upper supply rail for the DH1 high-side gate driver. An internal switch between V_{DD} and BST1 charges the BST1-LX1 flying capacitor while the low-side MOSFET is on (DL1 pulled high).
31	PGD_IN	Power-Good Logic Input Pin that Indicates the Power Status of Other System Rails and Used for Supply Sequencing. During startup, after soft-starting to the boot voltage, the output voltage remains at V_{BOOT}, and the $\overline{CLKEN}$ and PWRGD outputs remain high and low, respectively, as long as the PGD_IN input stays low. When PGD_IN later goes high, the output is allowed to transition to the voltage set by the VID code, and $\overline{CLKEN}$ is allowed to go low. During normal operation, if PGD_IN goes low, the controller immediately forces $\overline{CLKEN}$ high and PWRGD low, and slews the output to the boot voltage while in skip mode at 1/4 the normal slew rate set by the TIME resistor. The output then stays at the boot voltage until the controller is turned off or power cycled, or until PGD_IN goes high again.
32–38	D0–D6	Low-Voltage (1.0V Logic) VID DAC Code Inputs. The D0–D6 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. The output voltage is set by the VID code indicated by the logic-level voltages on D0–D6 (see Table 4). The 1111111 code corresponds to a shutdown mode. When this code is detected, The MAX17030/MAX17036 initiate a soft-shutdown transition identical to the shutdown transition for a $\overline{SHDN}$ falling edge. After slewing the output to 0V, it forces DH_, DL_, and $\overline{DRSKP}$ low, and three-states PWM3. The IC remains active and its V_{CC} quiescent current consumption stays the same as in normal operation. If D6–D0 is changed from 1111111 to a different code, the MAX17030/MAX17036 initiate a startup sequence identical to the startup sequence for a $\overline{SHDN}$ rising edge.
39	CSP1	Positive Input of the Output Current Sense of Phase 1. This pin should be connected to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

Pin Description (continued)

PIN	NAME	FUNCTION
40	CSN1	Negative Input of the Output Current Sense of Phase 1. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. A 10Ω discharge FET is turned on in UVLO event or thermal shutdown, or at the end of soft-shutdown.
—	PAD (GND)	Exposed Backplate (Pad) of Package. Internally connected to both analog ground and power (driver) grounds. Connect to the ground plane through a thermally enhanced via.

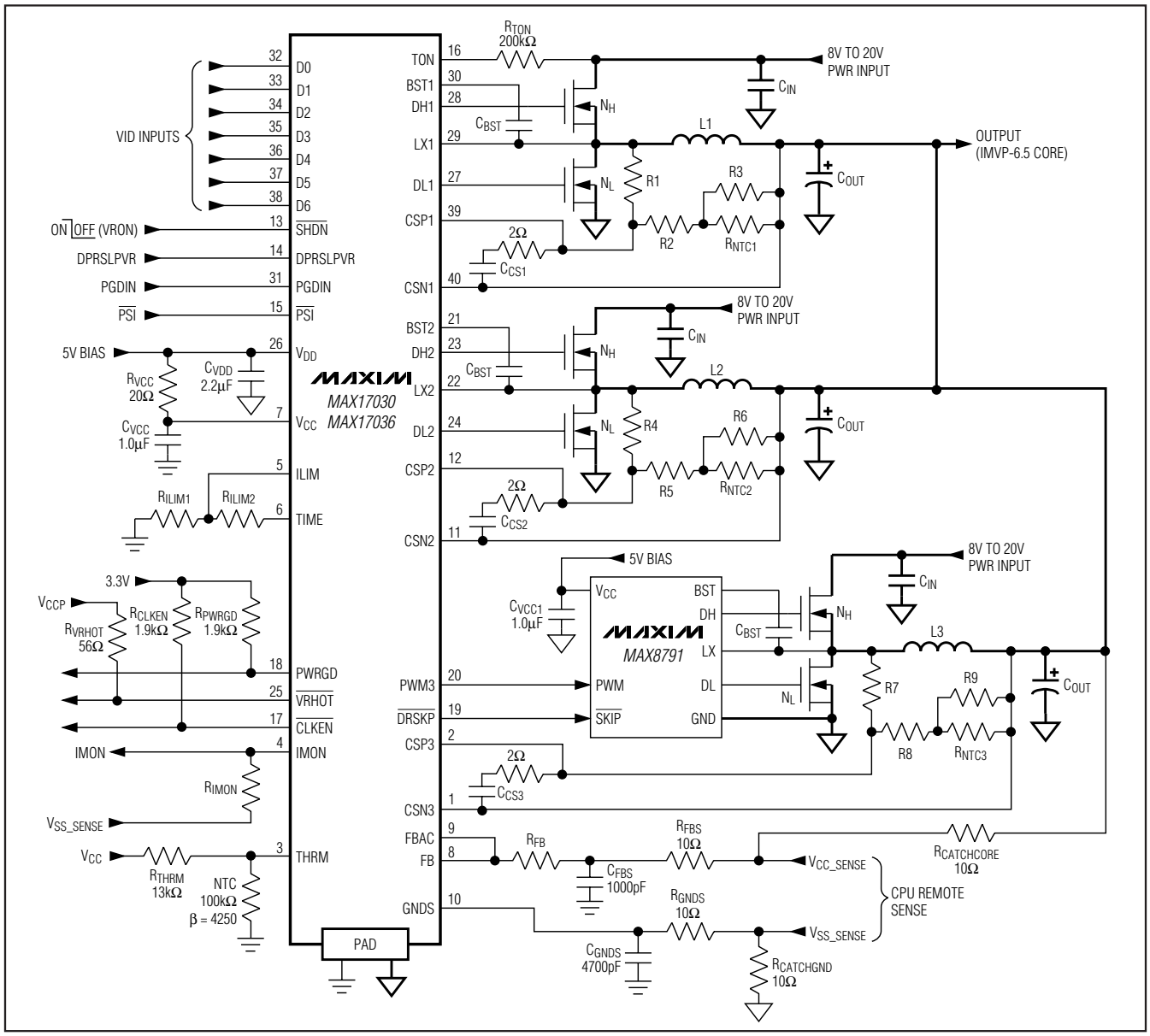


Figure 1. Standard 3-Phase IMVP-6.5 Application Circuit

Table 1. Component Selection for Standard Applications

DESIGN PARAMETERS	IMVP-6.5 XE CORE 3-PHASE	IMVP-6.5 SV CORE 3-PHASE	IMVP-6.5 SV CORE 2-PHASE
Circuit	Figure 1	Figure 1	Figure 2
Input Voltage Range	8V to 20V	8V to 20V	8V to 20V
Maximum Load Current	65A (48A TDC)	52A (38A TDC)	52A (38A TDC)
Transient Load Current	49A (100A/µs)	39A (100A/µs)	39A (100A/µs)
Load Line	-1.9mV/A	-1.9mV/A	-1.9mV/A
POC Setting	110	101	101
TON Resistance (R_{TON})	200kΩ (f_{SW} = 300kHz)	200kΩ (f_{SW} = 300kHz)	200kΩ (f_{SW} = 300kHz)
Inductance (L)	0.36µH, 36A, 0.82mΩ (10mm x 10mm) Panasonic ETQP4LR36ZFC	0.42µH, 20A, 1.55mΩ (7mm x 7mm) NEC/TOKIN MPC0740LR42C	0.36µH, 36A, 0.82mΩ (10mm x 10mm) Panasonic ETQP4LR36ZFC
High-Side MOSFET (N_H)	Fairchildsemi 1x FDS6298 9.4mΩ/12mΩ (typ/max) Toshiba 1x TPCA8030-H 9.6mΩ/13.4mΩ (typ/max)	Fairchildsemi 1x FDS6298 9.4mΩ/12mΩ (typ/max) Toshiba 1x TPCA8030-H 9.6mΩ/13.4mΩ (typ/max	Fairchildsemi 1x FDS6298 9.4mΩ/12mΩ (typ/max) Toshiba 1x TPCA8030-H 9.6mΩ/13.4mΩ (typ/max)
Low-Side MOSFET (N_L)	Fairchildsemi 2x FDS8670 4.2mΩ/5mΩ (typ/max) Toshiba 2x TPCA8019-H	Fairchildsemi 1x FDS8670 4.2mΩ/5mΩ (typ/max) Toshiba 1x TPCA8019-H	Fairchildsemi 2x FDS8670 4.2mΩ/5mΩ (typ/max) Toshiba 2x TPCA8019-H
Output Capacitors (C_{OUT}) (MAX17030 Only) **Contact Maxim for MAX17036 reference design**	4x 330µF, 2V, 4.5mΩ Panasonic EEFSXOD331E4 or NEC/Tokin PSGVOE337M4.5 27x 22µF, 6.3V X5R ceramic capacitor (0805)	3x 330µF, 2V, 4.5mΩ Panasonic EEFSXOD331E4 or NEC/Tokin PSGVOE337M4.5 27x 22µF, 6.3V X5R ceramic capacitor (0805)	4x 330µF, 6mΩ, 2.5V Panasonic EEFSX0D0D331XR 28x 10µF, 6V ceramic (0805)
Input Capacitors (C_{IN})	6x 10µF 25V ceramic (1210)	4x 10µF 25V ceramic (1210)	4x 10µF 25V ceramic (1210)
TIME-ILIM Resistance (R_{ILIM2})	14kΩ	14kΩ	16.9kΩ
ILIM-GND Resistance (R_{ILIM1})	137kΩ	137kΩ	133kΩ
FB Resistance (R_{FB})	6.04kΩ	453kΩ	6.04kΩ
IMON Resistance (R_{IMON})	12.1kΩ	10.2kΩ	14kΩ
LX-CSP Resistance	2.21kΩ (R1, R4, R7)	1.4kΩ (R1, R4, R7)	2.21kΩ (R1, R7)
CSP-CSN Resistance	3.24kΩ (R2, R5, R8) 40.2kΩ (R3, R6, R9)	2kΩ (R2, R5, R8) 40.2kΩ (R3, R6, R9)	3.24kΩ (R2, R8) 40.2kΩ (R3, R9)
DCR Sense NTC (R_{NTC})	10kΩ NTC B = 3380 TDK NTCG163JH103F	10kΩ NTC B = 3380 TDK NTCG163JH103F	10kΩ NTC B = 3380 TDK NTCG163JH103F
DCR Sense Capacitance (C_{SENSE})	0.22µF, 6V ceramic (0805)	0.22µF, 6V ceramic (0805)	0.22µF, 6V ceramic (0805)

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
AVX Corp.	www.avxcorp.com
Fairchild Semiconductor	www.fairchildsemi.com
NEC/TOKIN America, Inc.	www.nec-tokinamerica.com
Panasonic Corp.	www.panasonic.com
SANYO Electric Co., Ltd.	www.sanyodevice.com

MANUFACTURER	WEBSITE
Siliconix (Vishay)	www.vishay.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Toshiba America Electronic Components, Inc.	www.toshiba.com/taec

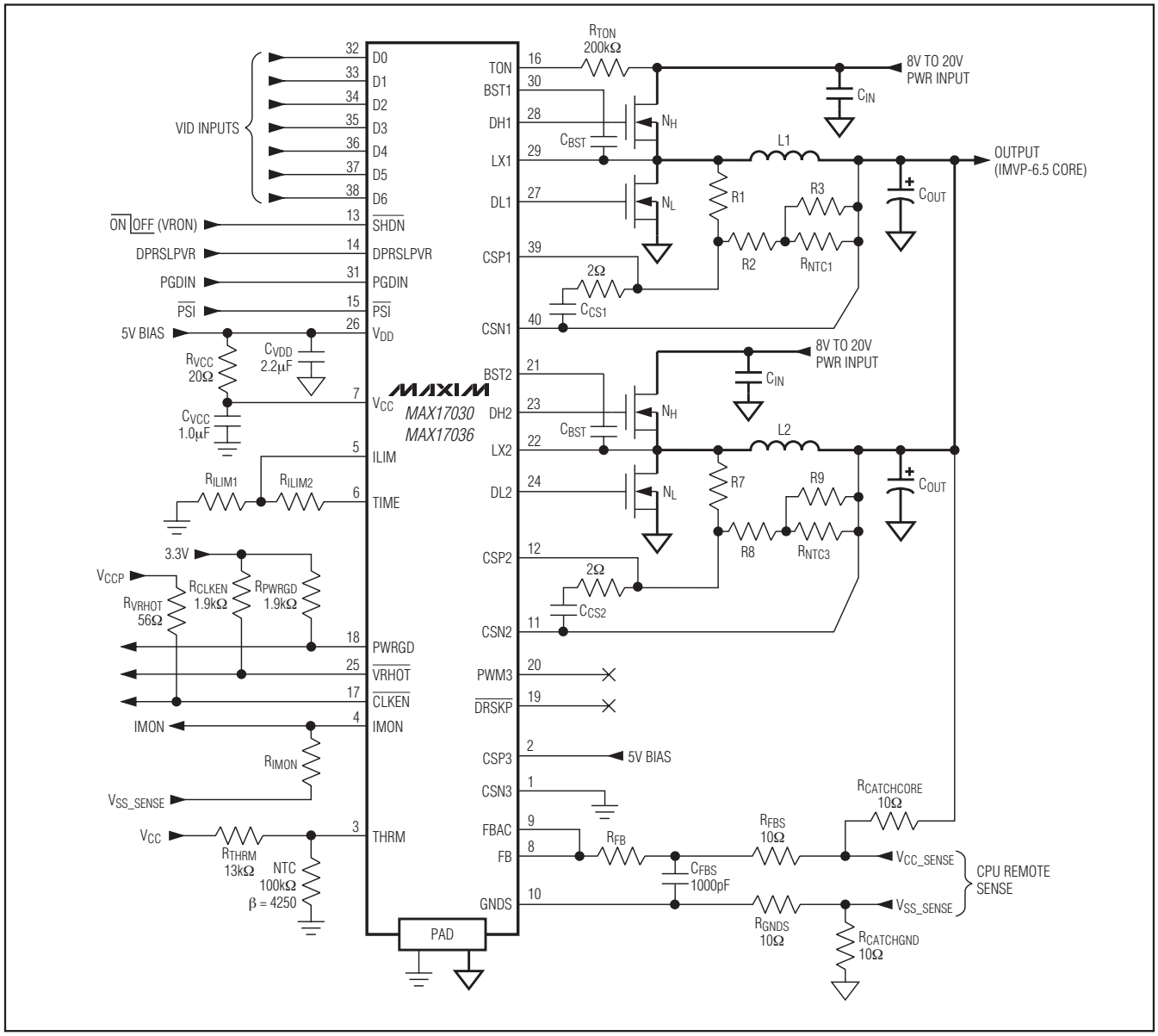


Figure 2. Standard 2-Phase IMVP-6.5 Application Circuit

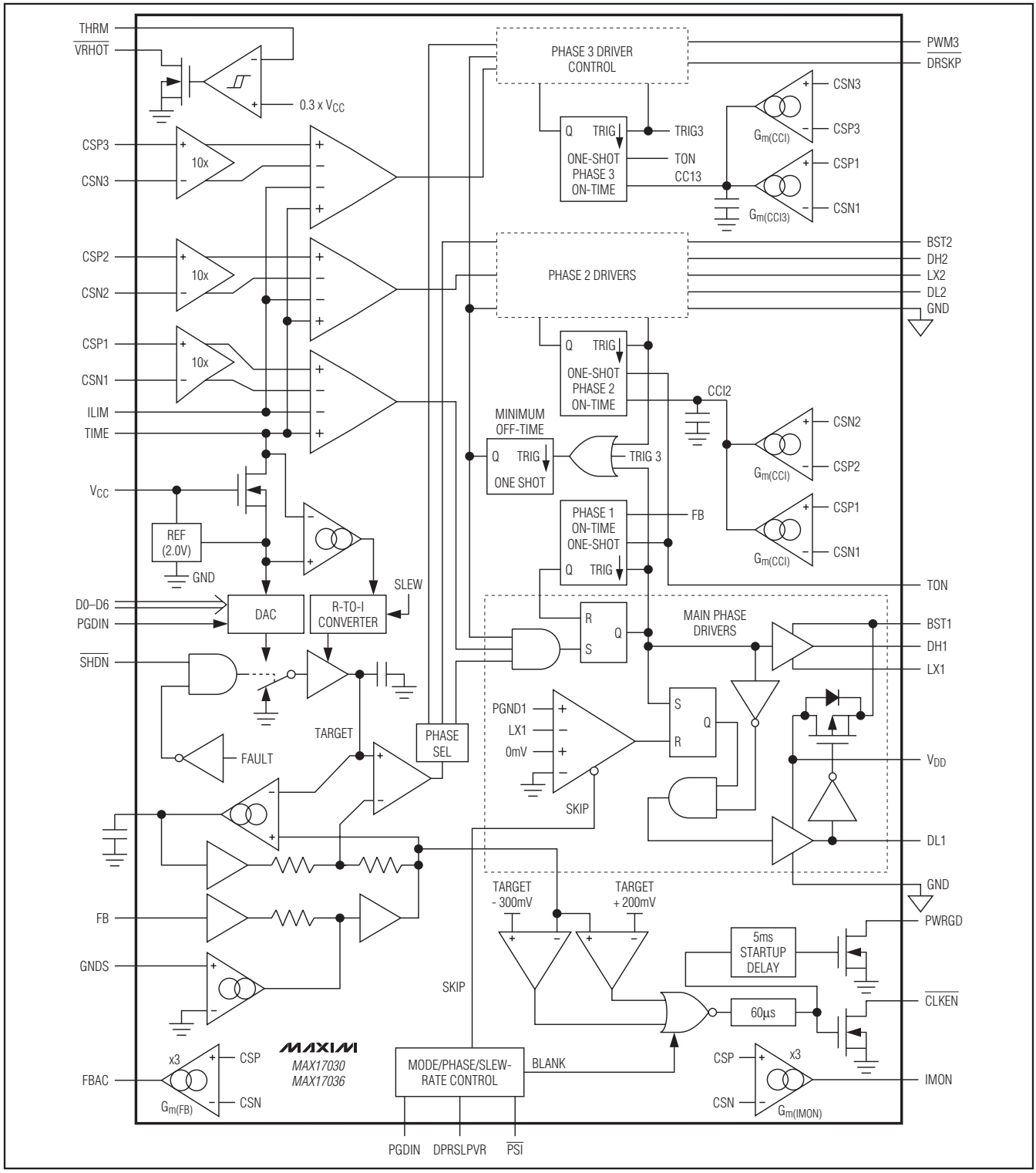


Figure 3. Functional Diagram

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

Detailed Description

Free-Running, Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward (Figure 3). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage, and directly proportional to output voltage or the difference between the main and secondary inductor currents (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low, the inductor current of the selected phase is below the valley current-limit threshold, and the minimum off-time one-shot times out. The controller maintains 120° out-of-phase operation by alternately triggering the three phases after the error comparator drops below the output-voltage set point.

Triple 120° Out-of-Phase Operation

The three phases in the MAX17030/MAX17036 operate 120° out-of-phase to minimize input and output filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making the MAX17030/MAX17036 ideal for high-power, cost-sensitive applications.

The MAX17030/MAX17036 share the current between three phases that operate 120° out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of each phase is effectively reduced, resulting in reduced input voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). Therefore, the same performance can be achieved with fewer or less-expensive input capacitors.

+5V Bias Supply (V_{CC} and V_{DD})

The Quick-PWM controller requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient +5V system supply. The +5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW}\left(Q_{G(LOW)} + Q_{G(HIGH)}\right)$$

where I_{CC} is provided in the *Electrical Characteristics* table, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V_{IN} and V_{DD} can be connected together if the input power source is a fixed +4.5V to +5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (TON)

Connect a resistor (R_{TON}) between TON and V_{IN} to set the switching period $T_{SW} = 1/f_{SW}$, per phase:

$$T_{SW} = 16.26pF \times (R_{TON} + 6.5k\Omega)$$

A 96.75kΩ to 303.25kΩ corresponds to switching periods of 167ns (600kHz) to 500ns (200kHz), respectively. High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

TON Open-Circuit Protection

The TON input includes open-circuit protection to avoid long, uncontrolled on-times that could result in an overvoltage condition on the output. The MAX17030/MAX17036 detect an open-circuit fault if the TON current drops below 10µA for any reason—the TON resistor (R_{TON}) is unpopulated, a high resistance value is used, the input voltage is low, etc. Under these conditions, the MAX17030/MAX17036 stop switching (DH and DL pulled low) and immediately set the fault latch. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

On-Time One-Shot

The MAX17030/MAX17036 contain a fast, low-jitter, adjustable one-shot that sets the high-side MOSFETs on-time. It is shared among the three phases. The one-shot for the main phase varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the V+ input, and proportional to the feedback voltage (V_{FB}):

$$t_{ON} = \frac{T_{SW}\left(V_{FB} + 0.075V\right)}{V_{IN}}$$

The one-shot for the second phase and third phase varies the on-time in response to the input voltage and the difference between the main and the other inductor currents. Two identical transconductance amplifiers integrate the difference between the master and each slave's current-sense signals. The summed output is connected to an internal integrator for each master-slave pair, which serves as the input to the respective slave's high-side MOSFET TON timer.

When the main and other phase current-sense signals ($V_{CM} = V_{CMP} - V_{CMN}$ and $V_{CS} = V_{CSP} - V_{CSM}$) become unbalanced, the transconductance amplifiers adjust the other phase's on-time, which increases or decreases the phase inductor current until the current-sense signals are properly balanced:

$$t_{ON(SEC)} = T_{SW}\left(\frac{V_{CCI} + 0.075V}{V_{IN}}\right)$$
$$= T_{SW}\left(\frac{V_{FB} + 0.075V}{V_{IN}}\right) + T_{SW}\left(\frac{I_{CCI}Z_{CCI}}{V_{IN}}\right)$$
$$= (\text{Main On-time}) + (\text{Secondary Current Balance Correction})$$

where V_{CCI} is the internal integrator node for each slave's current-balance integrator, and Z_{CCI} is the effective impedance at that node.

During phase overlap, t_{ON} is calculated based on phase 1's on-time requirements, but reduced by 33% when operating with three phases.

For a 3-phase regulator, each phase cannot be enabled until the other 2 phases have completed their on-time and the minimum off-times have expired. As such, the minimum period is limited by 3 x (t_{ON} + $t_{OFF(MIN)}$). Maximum t_{ON} is dependent on minimum V_{IN} and maximum output voltage:

$$T_{SW(MIN)} = N_{PH} \times (t_{ON(MAX)} + t_{OFF(MIN)})$$

where:

$$t_{ON(MAX)} = V_{FB(MAX)}/V_{IN(MIN} \times T_{SW(MIN)}$$

so:

$$T_{SW(MIN)} = t_{OFF(MIN)}/[1/N_{PH} - V_{IN(MAX)}/V_{IN(MIN)}]$$

Hence, for a 7V input and 1.1V output, 500kHz is the maximum switching frequency. Running at this limit is not desirable as there is no room to allow the regulator to make adjustments without triggering phase overlap. For a 3-phase, high-current application with minimum 8V input, the practical switching frequency is 300kHz.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* are influenced by parasitics in the conduction paths and propagation delays. For loads above the critical conduction point, where the dead-time effect (LX flying high and conducting through the high-side FET body diode) is no longer a factor, the actual switching frequency (per phase) is:

$$f_{SW} = \frac{(V_{OUT} + V_{DIS})}{t_{ON}(V_{IN} + V_{DIS} - V_{CHG})}$$

where V_{DIS} and V_{CHG} are the sum of the parasitic voltage drops in the inductor discharge and charge paths, including MOSFET, inductor, and PCB resistances; V_{CHG} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time as determined above.

Current Sense

The MAX17030/MAX17036 sense the output current of each phase allowing the use of current-sense resistors on inductor DCR as the current-sense element. Low-offset amplifiers are used for current balance, voltage-positioning gain, and current limit.

Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. The initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and current monitor. This current-sense method uses an RC filtering network to extract the current information from the output inductor (see Figure 4). The RC network should match the inductor's time constant (L/R_{DCR}):

$$R_{CS} = \left(\frac{R2}{R1 + R2}\right)R_{DCR}$$

and:

$$R_{CS} = \frac{L}{C_{EQ}}\left[\frac{1}{R1} + \frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance, and R_{DCR} is the inductor's series DC resistance. Use the typical inductance and R_{DCR} values provided by the inductor manufacturer. To minimize the current-sense error due to the current-sense inputs' bias current ($I_{CSP\_}$ and $I_{CSN\_}$), choose R1//R2 to be less than 2kΩ and use the above equation to determine the sense capacitance (C_{EQ}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage Positioning and Loop Compensation* section for detailed information.

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 4). The ESL induced voltage step might affect the average current-sense voltage. The RC filter's time constant should match the L_{ESL}/R_{SENSE} time constant formed by the current-sense resistor's parasitic inductance:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R_{EQ}$$

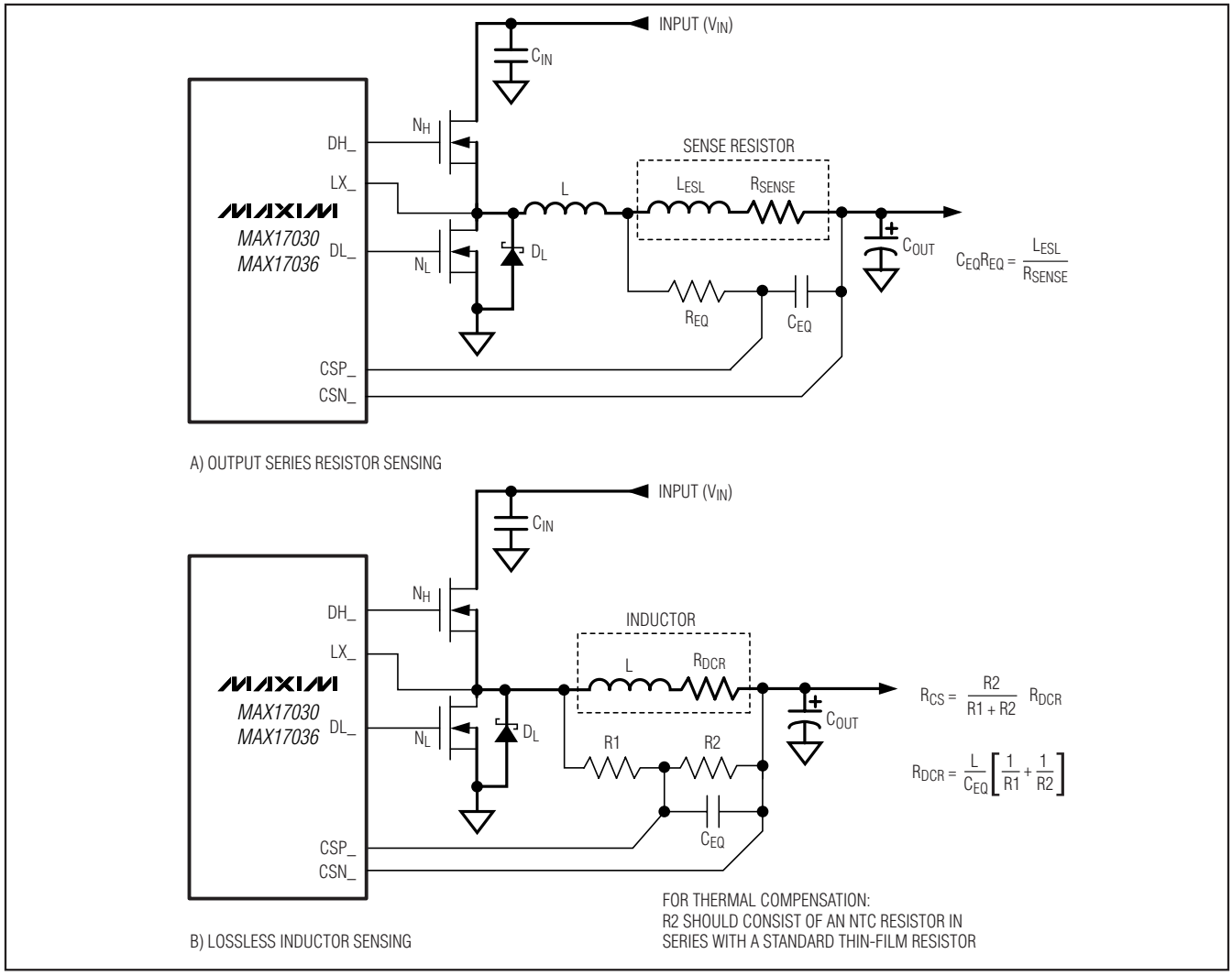


Figure 4. Current-Sense Methods

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is current-sense resistance value, and C_{EQ} and R_{EQ} are the time-constant matching components.

Current Balance

The MAX17030/MAX17036 integrate the difference between the current-sense voltages and adjust the on-time of the secondary phase to maintain current balance. The current balance relies on the accuracy of the current-sense signals across the current-sense resistor or inductor DCR. With active current balancing, the current mismatch is determined by the current-sense resistor or inductor DCR values and the offset voltage of the transconductance amplifiers:

$$I_{OS(IBAL)} = I_{LMAIN} - I_{LSEC} = \frac{V_{OS(IBAL)}}{R_{SENSE}}$$

where $R_{SENSE} = R_{CM} = R_{CS}$ and $V_{OS(IBAL)}$ is the current balance offset specification in the *Electrical Characteristics* table.

The worst-case current mismatch occurs immediately after a load transient due to inductor value mismatches resulting in different di/dt for the two phases. The time it takes the current-balance loop to correct the transient imbalance depends on the mismatch between the inductor values and switching frequency.

Current Limit

The current-limit circuit employs a unique "valley" current-sensing algorithm that senses the voltage across the current-sense resistors or inductor DCR at the current-sense inputs (CSP_ to CSN_). If the current-sense signal of the selected phase is above the current-limit threshold, the PWM controller does not initiate a new cycle until the inductor current of the selected phase drops below the valley current-limit threshold. When any one phase exceeds the current limit, all phases are effectively current limited since the interleaved controller does not initiate a cycle with the next phase.

Since only the valley current is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage.

The positive valley current-limit threshold voltage at CSP to CSN equals precisely 1/10 of the differential TIME to ILIM voltage over a 0.1V to 0.5V range (10mV to 50mV current-sense range). Connect ILIM directly to V_{CC} to set the default current-limit threshold setting of 22.5mV (typ).

The negative current-limit threshold (forced-PWM mode only) is nominally -125% of the corresponding valley current-limit threshold. When the inductor current drops below the negative current limit, the controller immediately activates an on-time pulse—DL turns off, and DH turns on—allowing the inductor current to remain above the negative current threshold.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (CSP_, CSN_).

Feedback Adjustment Amplifiers

Voltage-Positioning Amplifier (Steady-State Droop)

The MAX17030/MAX17036 include a transconductance amplifier for adding gain to the voltage-positioning sense path. The amplifier's input is generated by summing the current-sense inputs, which differentially sense the voltage across either current-sense resistors or the inductor's DCR. The amplifier's output connects directly to the regulator's voltage-positioned feedback input (FB), so the resistance between FB and the output-voltage sense point determines the voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FB}I_{FB}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output Voltage Selection* section, and the FB amplifier's output current (I_{FB}) is determined by the sum of the current-sense voltages:

$$I_{FB} = G_{m(FB)} \sum_{X=1}^{\eta_{PH}} V_{CSX}$$

where $V_{CSX} = V_{CSP} - V_{CSN}$ is the differential current-sense voltage, and $G_{m(FB)}$ is typically 400µS as defined in the *Electrical Characteristics*.

Differential Remote Sense

The MAX17030/MAX17036 include differential, remote-sense inputs to eliminate the effects of voltage drops along the PCB traces and through the processor's power pins. The feedback-sense node connects to the voltage-positioning resistor (R_{FB}). The ground-sense (GNDS) input connects to an amplifier that adds an offset directly to the target voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the voltage-positioning resistor (R_{FB}) and ground sense (GNDS) input directly to the processor's remote sense outputs as shown in Figure 1.

Integrator Amplifier

An internal integrator amplifier forces the DC average of the FB voltage to equal the target voltage, allowing accurate DC output-voltage regulation regardless of the output ripple voltage.

The MAX17030/MAX17036 disable the integrator by connecting the amplifier inputs together at the beginning of all VID transitions done in pulse-skipping mode (DPRSLPVR = high). The integrator remains disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Transient Overlap Operation

When a transient occurs, the response time of the controller depends on how quickly it can slew the inductor current. Multiphase controllers that remain 120° out-of-phase when a transient occurs actually respond slower than an equivalent single-phase controller. In order to provide fast transient response, the MAX17030/MAX17036 support a phase overlap mode, which allows the triple regulators to operate in-phase when heavy load transients are detected, effectively reducing the response time. After any high-side MOSFET turns off, if the output voltage does not exceed the regulation voltage when the minimum off-time expires, the controller simultaneously turns on all high-side MOSFETs with the same on-time during the next on-time cycle. The phases remain overlapped until the output voltage exceeds the regulation voltage after the minimum

1/2/3-Phase Quick-PWM IMVP-6.5 VID Controllers

off-time expires. The on-time for each phase is based on the input voltage to FB ratio (i.e., follows the master on-time), but reduced by 33% in a 3-phase configuration, and not reduced in a 2-phase configuration. This maximizes the total inductor current slew rate.

After the phase-overlap mode ends, the controller automatically begins with the next phase. For example, if phase 2 provided the last on-time pulse before overlap operation began, the controller starts switching with phase 3 when overlap operation ends.

Nominal Output Voltage Selection

The nominal no-load output voltage (V_{TARGET}) is defined by the selected voltage reference (VID DAC) plus the remote ground-sense adjustment (V_{GNDS}) as defined in the following equation:

$$V_{TARGET} = V_{FB} = V_{DAC} + V_{GNDS}$$

where V_{DAC} is the selected VID voltage. On startup, the MAX17030/MAX17036 slew the target voltage from ground to the preset boot voltage. Table 3 is the operating mode truth table.

DAC Inputs (D0–D6)

The digital-to-analog converter (DAC) programs the output voltage using the D0–D6 inputs. D0–D6 are low-voltage (1.0V) logic inputs, designed to interface directly with the CPU. Do not leave D0–D6 unconnected. Changing D0–D6 initiates a transition to a new output-voltage level. Change D0–D6 together, avoiding greater than 20ns skew between bits. Otherwise, incorrect DAC readings might cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages are compatible with the IMVP-6.5 (Table 4) specifications.

OFF Code

VID = 1111111 is defined as an OFF code. When the OFF code is set, the MAX17030/MAX17036 go through the same shutdown sequence as though $\overline{SHDN}$ has been pulled low—output discharged to zero, $\overline{CLKEN}$ high, and PWRGD low. Only the IC supply currents remain at the operating levels rather than the shutdown level. When exiting from the OFF code, the MAX17030/MAX17036 go through the boot sequence, similar to the sequence when $\overline{SHDN}$ is first pulled high.

Table 3. Operating Mode Truth Table

INPUTS			PHASE OPERATION*	OPERATING MODE
$\overline{SHDN}$	DPRSLPVR	$\overline{PSI}$		
GND	X	X	Disabled	Low-Power Shutdown Mode. DL1 and DL2 forced low, and the controller is disabled. The supply current drops to 1µA (max).
Rising	X	X	Multiphase Pulse Skipping 1/4 R_{TIME} Slew Rate	Startup/Boot. When $\overline{SHDN}$ is pulled high, the MAX17030/MAX17036 begin the startup sequence. Once the REF is above 1.84V, the controller enables the PWM controller and ramps the output voltage up to the boot voltage. See Figure 9.
High	Low	High	Multiphase Forced-PWM Nominal R_{TIME} Slew Rate	Full Power. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4).
High	Low	Low	(N-1)-Phase Forced-PWM Nominal R_{TIME} Slew Rate	Intermediate Power. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4). When $\overline{PSI}$ is pulled low, the MAX17030/MAX17036 immediately disable phase 3, PWM3 is three-state, and $\overline{DRSKP}$ is low.
High	High	X	1-Phase Pulse Skipping Nominal R_{TIME} Slew Rate	Deeper Sleep Mode. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4). When DPRSLPVR is pulled high, the MAX17030/MAX17036 immediately enter 1-phase pulse-skipping operation allowing automatic PWM/PFM switchover under light loads. The PWRGD and $\overline{CLKEN}$ upper thresholds are blanked. DH2 and DL2 are pulled low, PWM3 is three-state and $\overline{DRSKP}$ is low.

**Multiphase operation = All enabled phases active.*

Table 3. Operating Mode Truth Table (continued)

INPUTS			PHASE OPERATION*	OPERATING MODE
$\overline{SHDN}$	DPRSLPVR	$\overline{PSI}$		
Falling	X	X	Multiphase Forced-PWM 1/4 R_{TIME} Slew Rate	Shutdown. When $\overline{SHDN}$ is pulled low, the MAX17030/MAX17036 immediately pull PWRGD low, $\overline{CLKEN}$ becomes high impedance, all enabled phases are activated, and the output voltage is ramped down to 12.5mV; then DH and DL are pulled low and CSN1 discharge FET is turned on.
High	X	X	Disabled	Fault Mode. The fault latch has been set by the MAX17030/MAX17036 UVP or thermal-shutdown protection, or by the OVP protection. The controller remains in fault mode until V_{CC} power is cycled or $\overline{SHDN}$ toggled.

**Multiphase operation = All enabled phases active.*

Table 4. IMVP-6.5 Output Voltage VID DAC Codes

D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)	D6	D5	D4	D3	D2	D1	D0	OUTPUT VOLTAGE (V)
0	0	0	0	0	0	0	1.5000	1	0	0	0	0	0	0	0.7000
0	0	0	0	0	0	1	1.4875	1	0	0	0	0	0	1	0.6875
0	0	0	0	0	1	0	1.4750	1	0	0	0	0	1	0	0.6750
0	0	0	0	0	1	1	1.4625	1	0	0	0	0	1	1	0.6625
0	0	0	0	1	0	0	1.4500	1	0	0	0	1	0	0	0.6500
0	0	0	0	1	0	1	1.4375	1	0	0	0	1	0	1	0.6375
0	0	0	0	1	1	0	1.4250	1	0	0	0	1	1	0	0.6250
0	0	0	0	1	1	1	1.4125	1	0	0	0	1	1	1	0.6125
0	0	0	1	0	0	0	1.4000	1	0	0	1	0	0	0	0.6000
0	0	0	1	0	0	1	1.3875	1	0	0	1	0	0	1	0.5875
0	0	0	1	0	1	0	1.3750	1	0	0	1	0	1	0	0.5750
0	0	0	1	0	1	1	1.3625	1	0	0	1	0	1	1	0.5625
0	0	0	1	1	0	0	1.3500	1	0	0	1	1	0	0	0.5500
0	0	0	1	1	0	1	1.3375	1	0	0	1	1	0	1	0.5375
0	0	0	1	1	1	0	1.3250	1	0	0	1	1	1	0	0.5250
0	0	0	1	1	1	1	1.3125	1	0	0	1	1	1	1	0.5125
0	0	1	0	0	0	0	1.3000	1	0	1	0	0	0	0	0.5000
0	0	1	0	0	0	1	1.2875	1	0	1	0	0	0	1	0.4875
0	0	1	0	0	1	0	1.2750	1	0	1	0	0	1	0	0.4750
0	0	1	0	0	1	1	1.2625	1	0	1	0	0	1	1	0.4625
0	0	1	0	1	0	0	1.2500	1	0	1	0	1	0	0	0.4500
0	0	1	0	1	0	1	1.2375	1	0	1	0	1	0	1	0.4375
0	0	1	0	1	1	0	1.2250	1	0	1	0	1	1	0	0.4250
0	0	1	0	1	1	1	1.2125	1	0	1	0	1	1	1	0.4125
0	0	1	1	0	0	0	1.2000	1	0	1	1	0	0	0	0.4000
0	0	1	1	0	0	1	1.1875	1	0	1	1	0	0	1	0.3875