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EVALUATION KIT AVAILABLE

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

MAX17085B

General Description

The MAX17085B is an all-in-one notebook power solution integrating a multichemistry battery charger, dual fixed-output Quick-PWM™ step-down controllers, and dual keep-alive linear regulators:

Charger: The high-frequency (~1.4MHz) multichemistry battery charger uses a current-mode, fixed inductor current ripple architecture that significantly reduces component size and cost. Low-offset sense amplifiers allow the use of low-value sense resistors for charging and input current limit.

The charger uses n-channel switching MOSFETs. Adjustable charge current, charge voltage, and cell selection allow for flexible use with different battery packs. Charge current is set by an analog control input, or a PWM input. High-accuracy current-sense amplifiers provide fast cycle-by-cycle current-mode control to protect against short circuits to the battery and respond quickly to system load transients. Additionally, the charger provides a high-accuracy analog output that is proportional to the adapter current.

An integrated charge pump controls an n-channel adapter selector switch. The charge pump remains active even when the charger is off. When the adapter is absent, a p-channel MOSFET selects the battery.

Main SMPS: The dual Quick-PWM step-down controllers with synchronous rectification generate the 5V and 3.3V main power in a notebook. Low-side MOSFET sensing provides a simple low-cost, highly efficient valley current-limit protection. The MAX17085B also includes output undervoltage, output overvoltage, and thermal-fault protection.

Separate enable inputs for each SMPS and a combined open-drain power-good output allow flexible power sequencing. Voltage soft-start reduces inrush current, while passive shutdown discharges the output through an internal switch. Fast transient response, with an extended on-time feature reduces output capacitance requirements. Selectable pulse-skipping mode and ultrasonic mode improve light-load efficiency. Ultrasonic mode operation maintains a minimum switching frequency at light loads, minimizing audible noise effects.

Dual LDO Regulators: An internal 5V/100mA LDO5 with switchover can be used to either generate the 5V bias needed for power-up or other lower power "always-on" suspend supplies. Another 3.3V/50mA LDO3 provides "always-on" power to a system microcontroller.

Features

- **All-in-One Charger Plus Dual Main Step-Down Controllers**
- **5V/100mA and 3.3V/50mA LDO Regulators**
- **Main**
  Dual Quick-PWM with Fast Transient Response and Extended On-Time
  300kHz to 800kHz Switching Frequency
  Fixed 5V and 3.3V SMPS Outputs
  Low-Noise Ultrasonic Mode
  Autoretry Fault Protection
- **Charger**
  High Switching Frequency (1.4MHz)
  Selectable 2-, 3-, and 4-Cell Battery Voltage
  Automatic Selection of System Power Source
  Internal Charge-Pump for Adapter n-Channel MOSFETs Drive
  ±0.4% Accurate Charge Voltage
  ±2.5% Accurate Input Current Limiting
  ±3% Accurate Charge Current
- **Monitor Outputs for**
  AC Adapter Current (±2% Accuracy)
  Battery Discharge Current (±2% Accuracy)
  AC Adapter OK
- **Analog/PWM (100Hz to 500kHz) Adjustable Charge Current Setting**
- **AC Adapter Overvoltage and Overcurrent Protection**

Applications

Notebook Computers

PDAs and Mobile Communicators

5V and 3.3V Supplies

2-to-4, Li+-Cell, Battery-Powered Devices

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17085BETL+	-40°C to +85°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

ABSOLUTE MAXIMUM RATINGS (Note 1)

TON, DCIN, CSSP, BATT, CSIP to GND, LX_ to GND ..... -0.3V to +28V
CSIP to CSIN, CSSP to CSSN ..... -0.3V to +0.3V
LDO3, LDO5, VCC to GND (Note 2) ..... -0.3V to +6V
ISET, VCTL, ACIN, $\overline{ACOK}$ to GND ..... -0.3V to +6V
OUT3, OUT5 to GND (Note 2) ..... -0.3V to +6V
ON3, ON5, PGOOD to GND ..... -0.3V to +6V
ILIM3, ILIM5, SKIP, REF to GND ..... -0.3V to (V_{CC} + 0.3V)
GND to EP ..... -0.3V to +0.3V
DL_ to EP ..... -0.3V to (V_{LDO5} + 0.3V)
BST_ to GND ..... -0.3V to +34V
BST_ to LDO5 ..... -0.3V to +28V
DH3 to LX3 ..... -0.3V to (V_{BST3} + 0.3V)
BST3 to LX3 ..... -0.3V to +6V
DH5 to LX5 ..... -0.3V to (V_{BST5} + 0.3V)
BST5 to LX5 ..... -0.3V to +6V
DHC to LXC ..... -0.3V to (V_{BSTC} + 0.3V)
PDSL to GND ..... -0.3V to + 36V
BSTC to LXC ..... -0.3V to +6V
CELLS, CC, IINP to GND ..... -0.3V to (V_{LDO5} + 0.3V)
LDO_ Short Circuit to GND ..... Momentary
LDO5 Current (Internal Regulator) Continuous ..... +100mA
LDO3 Current (Internal Regulator) Continuous ..... +50mA
LDO_ Current (Switched Over) Continuous ..... +200mA
Continuous Power Dissipation (T_A = +70°C)
40-Pin Thin QFN (derate 34.5mW/°C above +70°C) 2857mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Note 1: Absolute Maximum Ratings valid using 20MHz bandwidth limit.

Note 2: LDO5 has a weak leakage to V_{CC} when LDO5 is more than 0.5V above V_{CC}. OUT5 has a weak leakage to V_{CC} when OUT5 is more than 0.5V above V_{CC}.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLIES							
Adapter Present Quiescent Current		I_{DCIN} + I_{CSSP} + I_{CSSN}, ON3 = ON5 = SKIP = V_{CC}, V_{OUT3} = 3.5V, V_{OUT5} = 5.3V	Charging enabled		3	6	mA
			Charging disabled		1.5	2.5	
Adapter Absent Quiescent Current		I_{DCIN} + I_{CSSP} + I_{CSSN}, ON3 = ON5 = SKIP = V_{CC}, V_{OUT3} = 3.5V, V_{OUT5} = 5.3V	V_{ISET} = 2.4V, IINP ON		1.5	2.5	mA
			ISET = GND		1.2	2.2	
CSSN Input Current		V_{CSSP} = V_{CSSN} = 24V, T_A = +25°C			0.1	2	µA
BATT + CSIP + CSIN + LXC Input Current		V_{BATT} = 16.8V, adapter absent, T_A = +25°C				4	µA
		V_{BATT} = 2V to 19V, adapter present			200	650	
DCIN Input Current	I_{DCIN}	ON3 = ON5 = SKIP = V_{CC}, charger disabled; V_{OUT3} = 3.5V, V_{OUT5} = 5.3V			0.1	0.2	mA
DCIN Standby Supply Current		V_{DCIN} = 5V to 24V, ON3 = ON5 = GND			130	270	µA
V_{CC} Supply Current	I_{CC}	ON3 = ON5 = SKIP = V_{CC}, charger disabled; V_{OUT3} = 3.5V, V_{OUT5} = 5.3V			1.0	1.5	mA
DCIN Input Voltage Range		**Note:** LDO5 is NOT guaranteed to be in regulation until DCIN is above 6V.		4.5		24	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DCIN Undervoltage-Lockout Trip Point for Charger	$V_{DCIN(UVLO)}$	V_{DCIN} falling		7.0	7.2		V
		V_{DCIN} rising			7.7	7.9	
DCIN POR Threshold	$V_{DCIN(POR)}$	Falling edge of V_{DCIN}			2.0		V
V_{CC} Undervoltage Lockout Threshold	$V_{CC(UVLO)}$	Falling edge of V_{CC}, PWM disabled below this threshold		3.8	4.0	4.3	V
		Rising edge of V_{CC}			4.2		
V_{CC} POR Threshold		Falling edge of V_{CC}			1.5		V
LINEAR REGULATORS							
LDO_ Output-Voltage Accuracy	V_{LDO5}	V_{DCIN} = 6V to 24V, ON5 = ON3 = GND 0mA < I_{LDO5} < 100mA, ON5 = GND		4.90	5.00	5.10	V
	V_{LDO3}	V_{LDO5} = 5V, I_{LDO5} = 0A 0mA < I_{LDO3} < 50mA, ON3 = GND		3.23	3.30	3.37	
Internal LDO Voltage After Switchover	V_{LDO5}	Not production tested		4.4	4.5	4.6	V
	V_{LDO3}	Not production tested		2.7	2.8	2.9	
LDO3 Short-Circuit Current		LDO3 = GND		50		130	mA
LDO5 Short-Circuit Current		LDO5 = GND		100		260	mA
LDO5 Bootstrap Switch Resistance		LDO5 to OUT5, V_{OUT5} = 5V, I_{LDO5} = 50mA			1.0	2.5	Ω
LDO3 Bootstrap Switch Resistance		LDO3 to OUT3, V_{OUT3} = 3.3V, I_{LDO3} = 50mA			1.5	3	Ω
Thermal-Shutdown Threshold	t_{SHDN}	Hysteresis = 50°C			+160		°C
REFERENCE							
REF Output Voltage	V_{REF}	I_{REF} = 50µA		2.09	2.10	2.11	V
REF Undervoltage-Lockout Threshold	V_{REF_UVLO}	V_{REF} falling			2.0		V
MAIN SMPS							
OUT5 Output Voltage Accuracy	V_{OUT5}	V_{IN} = 6V to 28V, SKIP = REF		5.033	5.083	5.135	V
OUT3 Output Voltage Accuracy	V_{OUT3}	V_{IN} = 6V to 28V, SKIP = REF		3.267	3.300	3.333	V
Load Regulation Error		Either SMPS, V_{SKIP} = 2V, I_{LOAD} = 0 to 5A			-0.1		%
		Either SMPS, SKIP = GND, I_{LOAD} = 0 to 5A			-1.7		
		Either SMPS, SKIP = V_{CC}, I_{LOAD} = 0 to 5A			-1.5		
Line Regulation Error		Either SMPS, V_{IN} = 6V to 28V			0.005		%/V
DH5 On-Time	t_{ON5}	V_{IN} = 12V, V_{OUT5} = 5.0V (Note 3)	R_{TON} = 549kΩ (300kHz + 10%)	1073	1263	1452	ns
			R_{TON} = 202kΩ (800kHz + 10%)	402	473	545	

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DH3 On-Time	t_{ON3}	V_{IN} = 12V, V_{OUT3} = 3.3V (Note 3)	R_{TON} = 549kΩ (300kHz - 10%)	866	1019	1171	ns
			R_{TON} = 202kΩ (800kHz - 10%)	325	382	439	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)		210	270	330	ns
Extended On-Time Blanking		Duty cycle > 50%; not for production test			300	360	ns
Soft-Start Time	t_{SS}	Rising edge on ON_			2		ms
Ultrasonic Operating Frequency	$f_{SW(USONIC)}$	SKIP = GND		15	22		kHz
MAIN SMPS FAULT DETECTION							
OUT_ Overvoltage Trip Threshold (PGOOD Pulled Low Above This Level)		With respect to error comparator threshold		13	16	19	%
OUT_Overvoltage Fault Propagation Delay	t_{OVP}	$V_{FB\_}$ forced 50mV above trip threshold			10		µs
OUT_ Undervoltage Protection Trip Threshold		With respect to error comparator threshold		65	70	75	%
OUT_ Output Undervoltage Fault Propagation Delay	t_{UVP}				10		µs
PGOOD Lower Trip Threshold		With respect to error comparator threshold, falling edge, hysteresis = 15mV		-350	-250	-150	mV
PGOOD Propagation Delay	t_{PGOOD}	OUT5 or OUT3 forced 50mV beyond PGOOD trip threshold, falling edge			10		µs
PGOOD Output Low Voltage		PGOOD low impedance, ON5 = ON3 = GND, I_{SINK} = 4mA				0.3	V
PGOOD Leakage Current	I_{PGOOD}	PGOOD high impedance, SMPS in regulation, PGOOD forced to 5.5V, T_A = +25°C				1	µA
Fault Reset Timer				7	10		ms
MAIN SMPS CURRENT LIMIT							
ILIM_ Adjustment Range				0.2		2.1	V
ILIM_ Leakage Current		T_A = +25°C		-0.1		+0.1	µA
Valley Current-Limit Threshold (Adjustable)	$V_{LIM\_(VAL)}$	V_{AGND} - $V_{LX\_}$	$V_{ILIM\_}$ = 0.5V	40	50	60	mV
			$V_{ILIM\_}$ = 1.00V	87	100	113	
			$V_{ILIM\_}$ = 2.10V	184	210	236	
Ultrasonic Negative Current-Limit Threshold	$I_{NEG(US)}$				72		mV
Current-Limit Threshold (Zero Crossing)	V_{ZX}	V_{AGND} - $V_{LX\_}$, SKIP = V_{CC} or GND, V_{ILIM} = 1V			1.5		mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MAIN SMPS INPUTS AND OUTPUTS						
SKIP Threshold Voltage	V_{SKIP}	High = SKIP	2.3		V_{CC}	V
		Mid = PWM	1.5		1.9	
		Low = ultrasonic	0		0.8	
SKIP Leakage Current		V_{SKIP} = 0 or 5V, T_A = +25°C	-2		+2	µA
ON_ Input Logic Levels		High (SMPS on)	2.4			V
		Low (SMPS off)			0.8	
ON_ Leakage Current		V_{ON3} = V_{ON5} = 0 or 5V, T_A = +25°C	-2		+2	µA
OUT_ Discharge-Mode On-Resistance	R_{DSCHG}	ON_ = GND	7.5	20	50	Ω
SMPS GATE DRIVERS						
DH3, DH5 Gate Driver On-Resistance	R_{DH3}, R_{DH5}	BST3 - LX3 and BST5 - LX5 forced to 5V; high state		1.6	3.8	Ω
		BST3 - LX3 and BST5 - LX5 forced to 5V; low state		1.6	3.8	
DL3, DL5 Gate Driver On-Resistance	R_{DL3}, R_{DL5}	DL3, DL5; high state		1.5	3.5	Ω
		DL3, DL5; low state		0.6	1.5	
DH3, DH5 Gate Driver Source/ Sink Current	I_{DH}	DH3, DH5 forced to 2.5V, BST3 - LX3 and BST5 - LX5 forced to 5V		2		A
DL3, DL5 Gate Driver Source Current	$I_{DL(SOURCE)}$	DL3, DL5 forced to 2.5V		1.7		A
DL3, DL5 Gate Driver Sink Current	$I_{DL(SINK)}$	DL3, DL5 forced to 2.5V		3.3		A
DHC Gate Driver On-Resistance	R_{DHC}	High state, I_{DHC} = 10mA		1.5	3	Ω
		Low state, I_{DHC} = -10mA		0.8	2.1	
DLC Gate Driver On-Resistance	R_{DLC}	High state, I_{DLC} = 10mA		3	6	Ω
		Low state, I_{DLC} = -10mA		3	6	
Internal BST_ Switch On-Resistance	R_{BST}	$I_{BST\_}$ = 10mA, V_{DD} = 5V		5		Ω
BST_ Leakage Current	I_{BST}	$V_{BST\_}$ = 24V, OUT3 and OUT5 above regulation threshold, T_A = +25°C		2	20	µA
CHARGER SMPS						
DHC Off-Time K Factor		V_{DCIN} = 19V, V_{BATT} = 10V	30	35	40	ns/V
Sense Voltage for Minimum Discontinuous Mode Ripple Current		V_{CSIP} - V_{CSIN}		5		mV
Zero Crossing Comparator Threshold		V_{CSIP} - V_{CSIN}		10		mV
Cycle-by-Cycle Current- Limit Sense Voltage		V_{CSIP} - V_{CSIN}	120	125	130	mV

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CHARGE-VOLTAGE REGULATION							
Battery-Regulation Voltage Accuracy	V_{BATT}	CELLS = open, VCTL = REF, 2 cells		-0.5		+0.5	%
		CELLS = GND, VCTL = REF, 3 cells		-0.5		+0.5	
		CELLS = LDO3, VCTL = REF, 4 cells		-0.5		+0.5	
VCTL Range		CELLS = open, 2 cells		1.0		3.5	V
VCTL Input Bias Current		VCTL = GND or VCTL = REF, T_A = +25°C		-1		+1	µA
CELLS 3-Cell Threshold						0.8	V
CELLS 2-Cell Level		CELLS = open		1.9	2.1	2.3	V
CELLS 4-Cell Threshold				2.8			V
CELLS Input Bias Current		CELLS = GND or V_{CELLS} = 3.6V, T_A = +25°C		-2		+2	µA
CHARGE-CURRENT REGULATION							
ISET Range		Charging current, analog setting		0		REF	V
Full-Charge-Current Accuracy (CSIP to CSIN)	V_{CSI}	V_{BATT} = 4V to 16.8V	V_{ISET} = V_{REF}, or PWM = 100%	97	100	103	mV
			V_{ISET} = 0.6 x V_{REF}, or PWM = 60%	57.6	60.0	62.4	
Trickle Charge-Current Accuracy	V_{CSI}	V_{BATT} = 4V to 16.8V, V_{ISET} = V_{REF}/36 or PWM = 2.7%		1.25	2.70	4.30	mV
Charge-Current Gain Error				-1.5		+1.5	%
Charge-Current Offset Error		Based on V_{ISET} = V_{REF} and V_{ISET} = 0.6 x V_{REF}		-1.4		+1.4	mV
CSIP/CSIN/BATT Input-Voltage Range				0		24	V
CSIP Leakage Current		V_{CSIP} = V_{CSIN} = 24V, T_A = +25°C		-0.2		+0.2	µA
CSIN Leakage Current		V_{CSIP} = V_{CSIN} = 24V, T_A = +25°C		1		4	µA
ISET Power-Down Mode Threshold	$V_{ISET-SDN}$	ISET falling		20	26	32	mV
		ISET rising		32	38	46	
ISET Input Bias Current		V_{ISET} = V_{REF}/2 and V_{ISET} = V_{REF}, T_A = +25°C		-0.15		+0.15	µA
ISET PWM Threshold		ISET rising				2.4	V
		ISET falling		0.8			
ISET Frequency	f_{ISET}			0.128		500	kHz
ISET Effective Resolution		f_{ISET} = 100kHz			8		Bit
INPUT SOURCE-CURRENT REGULATION							
Input Source Current-Limit Threshold	V_{CSS}	V_{CSSP} - V_{CSSN}		58.5	60.0	61.5	mV
				-2.5		+2.5	%
CSSP/CSSN Input-Voltage Range				5		26	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IINP Current-Sense Amplifier Voltage Gain	G_{IINP}		59.1	60.0	60.9	V/V
IINP Output-Voltage Range			0		4	V
IINP Accuracy		V_{CSSP} - V_{CSSN} = 60mV	-2		+2	%
		V_{CSSP} - V_{CSSN} = 40mV	-3		+3	
		V_{CSSP} - V_{CSSN} = 20mV	-4		+4	
IINP Gain Error		Measured at V_{CSSP} - V_{CSSN} = 60mV and V_{CSSP} - V_{CSSN} = 20mV	-1.25		+1.25	%
IINP Offset Error		Measured at V_{CSSP} - V_{CSSN} = 60mV and V_{CSSP} - V_{CSSN} = 20mV	-0.6		+0.6	mV
ADAPTER OVERCURRENT (ACOC) DETECTION						
ACOCP Threshold	$V_{CSIN-OCP}$	With respect to V_{CSSP} _V_{CSSN}		78		mV
				130		%
ACOCP Blanking Time				16		ms
ACOCP Waiting Time		When ACOCP comparator is high and at the time the blanking time expires		0.6		s
ACIN, $\overline{ACOK}$, AND ACOV						
ACIN Rising Debounce				44		ms
ACIN Falling Delay				10		µs
ACIN Input Bias Current		T_A = +25°C	-1		+1	µA
$\overline{ACOK}$ Detect Threshold	V_{ACINOK}	Measured at ACIN rising, hysteresis = 40mV (typ)	1.47	1.50	1.53	V
			-2		+2	%
ACOV Detect Threshold	V_{ACINOV}	Measured at ACIN rising, hysteresis = 40mV (typ)	2.05	2.10	2.15	V
			-2.38		+2.38	%
$\overline{ACOK}$ Sink Current		$V_{\overline{ACOK}}$ = 0.4V, V_{ACIN} = 1.7V	1			mA
$\overline{ACOK}$ Leakage Current		$V_{\overline{ACOK}}$ = 5.5V, V_{ACIN} = 1.3V, T_A = +25°C			1	µA
ADAPTER PRESENT DETECTION						
Adapter Absence Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} falling	0	100	200	mV
Adapter Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} rising	300	440	600	mV
CHARGE-PUMP MOSFET DRIVER						
PDSL Gate-Driver Source Current	$I_{PDSL-SRC}$	V_{PDSL} - V_{DCIN} = 3V, V_{DCIN} = 19V		60		µA
PDSL Gate-Driver Output Voltage High	V_{PDSL-H}	V_{DCIN} = 19V	V_{DCIN} + 5.3	V_{DCIN} + 8		V
PDSL SWITCH CONTROL						
PDSL Turn-Off Resistance	R_{PDSL}	Measured from PDSL to GND		2.5		kΩ
BATTERY OVERVOLTAGE						
BATT Overvoltage Threshold	$V_{CELL(OV)}$	V_{BATT} rising, hysteresis = 20mV (typ)		+100		mV/cell

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLIES							
Adapter Present Quiescent Current		I_{DCIN} + I_{CSSP} + I_{CSSN}, ON3 = ON5 = SKIP = V_{CC}, V_{OUT3} = 3.5V, V_{OUT5} = 5.3V	Charging enabled			6	mA
			Charging disabled			2.5	
Adapter Absent Quiescent Current		I_{DCIN} + I_{CSSP} + I_{CSSN}, ON3 = ON5 = SKIP = V_{CC}, V_{OUT3} = 3.5V, V_{OUT5} = 5.3V	V_{ISET} = 2.4V, IINP ON			2.5	mA
			ISET = GND			2.2	
CSSN Input Current		V_{CSSP} = V_{CSSN} = 24V				2	µA
BATT + CSIP + CSIN + LXC Input Current		V_{BATT} = 16.8V, adapter absent				4	µA
		V_{BATT} = 2V to 19V, adapter present				650	
DCIN Input Current	I_{DCIN}	ON3 = ON5 = SKIP = V_{CC}, charger disabled; V_{OUT3} = 3.5V, V_{OUT5} = 5.3V				0.2	mA
DCIN Standby Supply Current		V_{DCIN} = 5V to 24V, ON3 = ON5 = GND				300	µA
V_{CC} Supply Current	I_{CC}	ON3 = ON5 = SKIP = V_{CC}, charger disabled; V_{OUT3} = 3.5V, V_{OUT5} = 5.3V				1.5	mA
DCIN Input-Voltage Range		**Note:** LDO5 is NOT guaranteed to be regulation until DCIN is above 6V		4.5		24	V
DCIN Undervoltage-Lockout Trip Point for Charger	$V_{DCIN(UVLO)}$	V_{DCIN} falling		6.9			V
		V_{DCIN} rising				7.9	
V_{CC} UndervoltageLockout Threshold	$V_{CC(UVLO)}$	Falling edge of V_{CC}, PWM disabled below this threshold		3.8		4.3	V
LINEAR REGULATORS							
LDO_ Output-Voltage Accuracy	V_{LDO5}	V_{DCIN} = 6V to 24V, ON5 = ON3 = GND, 0mA < I_{LDO5} < 100mA, ON5 = GND		4.85		5.15	V
	V_{LDO3}	V_{LDO5} = 5V, I_{LDO5} = 0A, 0mA < I_{LDO3} < 50mA, ON3 = GND		3.20		3.40	
LDO3 Short-Circuit Current		LDO3 = GND				130	mA
LDO5 Short-Circuit Current		LDO5 = GND				260	mA
REFERENCE							
REF Output Voltage	V_{REF}	I_{REF} = 50µA		2.08		2.12	V
MAIN SMPS							
OUT5 Output-Voltage Accuracy	V_{OUT5}	V_{IN} = 6V to 28V, SKIP = REF		5.008		5.160	V
OUT3 Output-Voltage Accuracy	V_{OUT3}	V_{IN} = 6V to 28V, SKIP = REF		3.25		3.35	V
DH5 On-Time	t_{ON5}	V_{IN} = 12V, V_{OUT5} = 5.0V (Note 3)	R_{TON} = 549kΩ (300kHz + 10%)	1073		1452	ns
			R_{TON} = 202kΩ (800kHz + 10%)	402		545	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DH3 On-Time	t_{ON3}	V_{IN} = 12V, V_{OUT3} = 3.3V (Note 3)	R_{TON} = 549kΩ (300kHz - 10%)	866		1171	ns
			R_{TON} = 202kΩ (800kHz - 10%)	325		439	
Minimum Off-Time	$t_{OFF(MIN)}$	(Note 3)				330	ns
Extended On-Time Blanking		Duty cycle > 50%; not for production test				360	ns
Ultrasonic Operating Frequency	$f_{SW(USONIC)}$	SKIP = GND		13			kHz
MAIN SMPS FAULT DETECTION							
OUT_ Overvoltage Trip Threshold (PGOOD Pulled Low Above this Level)		With respect to error comparator threshold		12		20	%
OUT_ Undervoltage Protection Trip Threshold		With respect to error comparator threshold		63		77	%
PGOOD Lower Trip Threshold		With respect to error comparator threshold, falling edge, hysteresis = 15mV		-350		-150	mV
PGOOD Output Low Voltage		PGOOD low impedance, ON5 = ON3 = GND, I_{SINK} = 4mA				0.4	V
Fault Reset Timer		Not for production test		7			ms
MAIN SMPS CURRENT LIMIT							
ILIM_ Adjustment Range				0.2		2.1	V
Valley Current-Limit Threshold (Adjustable)	$V_{LIM\_(VAL)}$	V_{AGND} - $V_{LX\_}$	$V_{ILIM\_}$ = 0.5V	40		60	mV
			$V_{ILIM\_}$ = 1.00V	85		115	
			$V_{ILIM\_}$ = 2.10V	174		246	
MAIN SMPS INPUTS AND OUTPUTS							
SKIP Threshold Voltage	V_{SKIP}	High = SKIP		2.3		V_{CC}	V
		Mid = PWM		1.5		1.9	
		Low = ultrasonic		0		0.8	
SKIP Leakage Current		V_{SKIP} = 0 or 5V, T_A = +25°C		-2		+2	µA
ON_ Input Logic Levels		High (SMPS on)		2.4			V
		Low (SMPS off)				0.8	
SMPS GATE DRIVERS							
DH3, DH5 Gate Driver On-Resistance	R_{DH3}, R_{DH5}	BST3 - LX3 and BST5 - LX5 forced to 5V; high state				3.8	Ω
		BST3 - LX3 and BST5 - LX5 forced to 5V; low state				3.8	
DL3, DL5 Gate-Driver On-Resistance	R_{DL3}, R_{DL5}	DL3, DL5; high state				3.5	Ω
		DL3, DL5; low state				1.5	
DHC Gate-Driver On-Resistance	R_{DHC}	High state, I_{DHC} = 10mA				3	Ω
		Low state, I_{DHC} = -10mA				2.1	

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DLC Gate-Driver On-Resistance	R_{DLC}	High state, I_{DLC} = 10mA			6	Ω
		Low state, I_{DLC} = -10mA			6	
CHARGER SMPS						
DHC Off-Time K Factor		V_{DCIN} = 19V, V_{BATT} = 10V	30		40	ns/V
Cycle-by-Cycle Current-Limit Sense Voltage		V_{CSIP} - V_{CSIN}	120		130	mV
CHARGE-VOLTAGE REGULATION						
Battery-Regulation Voltage Accuracy	V_{BATT}	CELLS = open, VCTL = REF, 2 cells	-0.5		+0.5	%
		CELLS = GND, VCTL = REF, 3 cells	-0.5		+0.5	
		CELLS = LDO3, VCTL = REF, 4 cells	-0.5		+0.5	
VCTL Range			0		2.4	V
CELLS 3-Cell Threshold					0.8	V
CELLS 2-Cell Level		CELLS = open	1.9		2.3	V
CELLS 4-Cell Threshold			2.8			V
CHARGE-CURRENT REGULATION						
ISET Range		Charging current, analog setting	0.0		REF	V
Full-Charge-Current Accuracy (CSIP to CSIN)	V_{CSI}	V_{BATT} = 4V to 16.8V, V_{ISET} = V_{REF}, or PWM = 100%	97		103	mV
		V_{BATT} = 4V to 16.8V, V_{ISET} = 0.6 x V_{REF}, or PWM = 60%	57.6		62.4	
Trickle Charge-Current Accuracy	V_{CSI}	V_{BATT} = 4V to 16.8V, V_{ISET} = V_{REF}/36 or PWM = 2.7%	1.2		4.3	mV
Charge-Current Gain Error			-1.5		+1.5	%
Charge-Current Offset Error		Based on V_{ISET} = V_{REF} and V_{ISET} = 0.6 x V_{REF}	-1.4		+1.4	mV
CSIP/CSIN/BATT Input Voltage Range			0		24	V
ISET Power-Down Mode Threshold	$V_{ISET-SDN}$	ISET falling	20		32	mV
		ISET rising	32		46	
ISET PWM Threshold		ISET rising			2.4	V
		ISET falling	0.8			
ISET Frequency	f_{ISET}		0.128		500	kHz

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, no load on LDO5, LDO3, OUT5, OUT3, and REF, V_{CC} = 5V, ON3 = ON5 = V_{CC}, V_{DCIN} = V_{LXC} = V_{CSSP} = V_{CSSN} = 19V, V_{BSTC} - V_{LXC} = 5V, V_{BATT} = V_{CSIP} = V_{CSIN} = 12.6V, V_{VCTL} = V_{ISET} = 1.8V, CELLS = open, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SOURCE-CURRENT REGULATION						
Input Source-Current Limit Threshold	V_{CSS}	V_{CSSP} - V_{CSSN}	58.5		61.5	mV
			-2.5		+2.5	%
CSSP/CSSN Input-Voltage Range			5		26	V
IINP Current-Sense Amplifier Voltage Gain	G_{IINP}		59.9		60.1	V/V
IINP Output-Voltage Range			0		4	V
IINP Accuracy		V_{CSSP} - V_{CSSN} = 60mV	-2		+2	%
		V_{CSSP} - V_{CSSN} = 40mV	-3		+3	
		V_{CSSP} - V_{CSSN} = 20mV	-4		+4	
IINP Gain Error		Measured at V_{CSSP} - V_{CSSN} = 60mV and V_{CSSP} - V_{CSSN} = 20mV	-1.5		+1.5	%
IINP Offset Error		Measured at V_{CSSP} - V_{CSSN} = 60mV and V_{CSSP} - V_{CSSN} = 20mV	-0.65		+0.65	mV
ACIN, $\overline{ACOK}$, AND ACOV						
$\overline{ACOK}$ Detect Threshold	V_{ACINOK}	Measured at ACIN rising, hysteresis = 40mV (typ)	1.47		1.53	V
			-2		+2	%
ACOV Detect Threshold	V_{ACINOV}	Measured at ACIN rising, hysteresis = 40mV (typ)	2.05		2.15	V
			-2.38		+2.38	%
$\overline{ACOK}$ Sink Current		$V_{\overline{ACOK}}$ = 0.4V, V_{ACIN} = 1.7V	1			mA
ADAPTER PRESENT DETECTION						
Adapter Absence Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} falling	0		200	mV
Adapter Detect Threshold		V_{DCIN} - V_{BATT}, V_{DCIN} rising	300		600	mV
CHARGE-PUMP MOSFET DRIVER						
PDSL Gate-Driver Output Voltage High	V_{PDSL_H}	V_{DCIN} = 19V	V_{DCIN} + 5.3			V

Note 3: On-time and off-time specifications are measured from 50% point to 50% point at the DH pin with LX = PGND, V_{BST} = 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

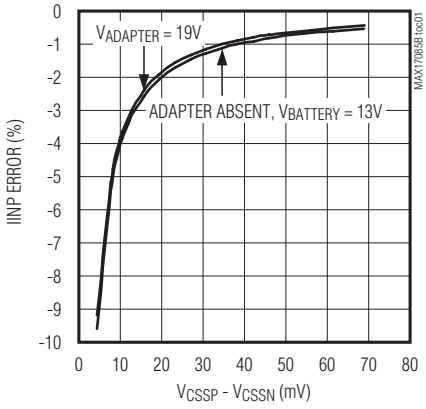
Note 4: Specifications to T_A = -40°C are guaranteed by design and not production tested.

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

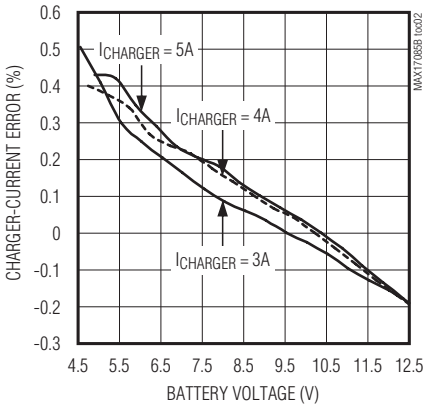
Typical Operating Characteristics

(Circuit of Figure 1, V_{ADP} = V_{SYS} = 20V, V_{BATT} = 16.8V, V_{LDO5} = V_{CC} = 5V, V_{LDO3} = 3.3V, T_A = +25°C, unless otherwise noted.)

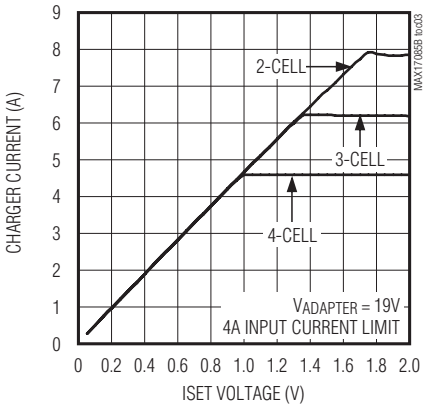
IINP ERROR vs. SYSTEM CURRENT (DC SWEEP)



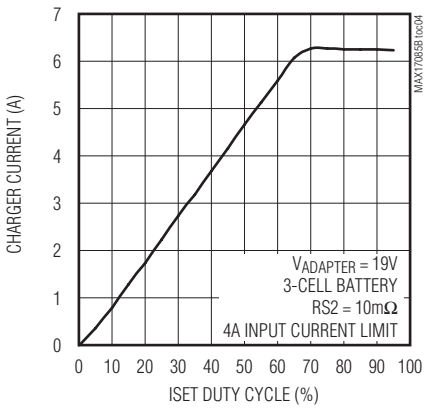
CHARGER-CURRENT ERROR vs. BATTERY VOLTAGE



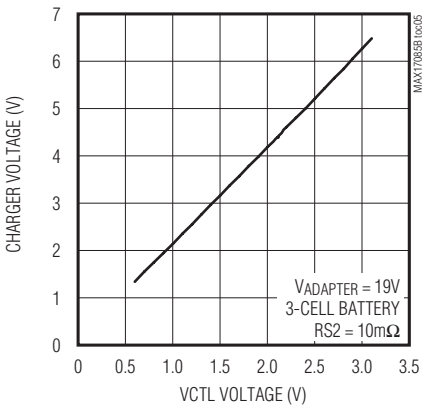
CHARGER CURRENT vs. ISET SETTING (ANALOG)



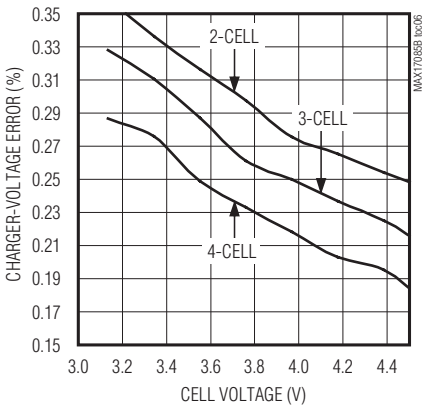
CHARGER CURRENT vs. ISET SETTING (PWM)



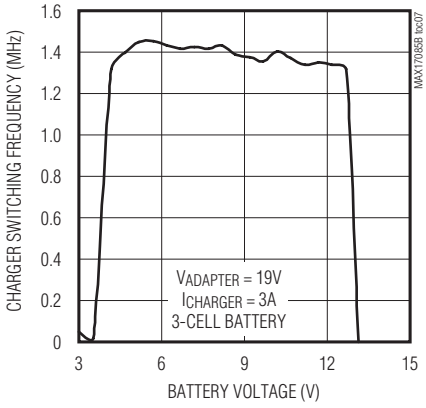
CHARGER-VOLTAGE PER CELL vs. VCTL VOLTAGE



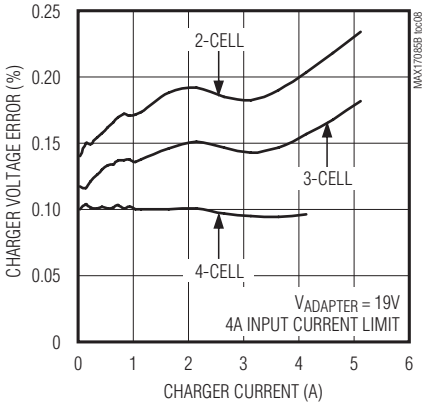
CHARGER-VOLTAGE ERROR vs. CELL VOLTAGE



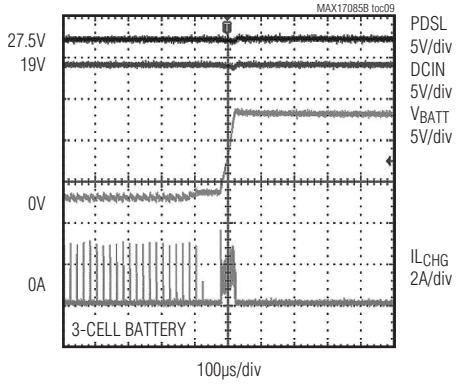
CHARGER SWITCHING FREQUENCY vs. BATTERY VOLTAGE



CHARGER VOLTAGE ERROR vs. CHARGER CURRENT



BATTERY REMOVAL (V_{BATT} = 3V)

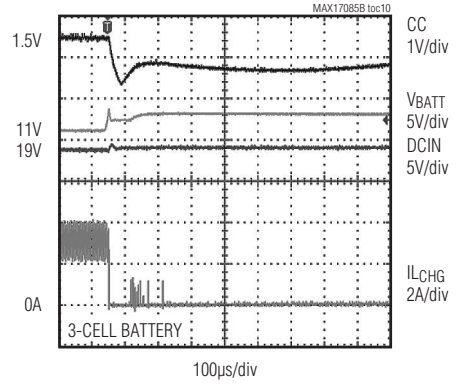


Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

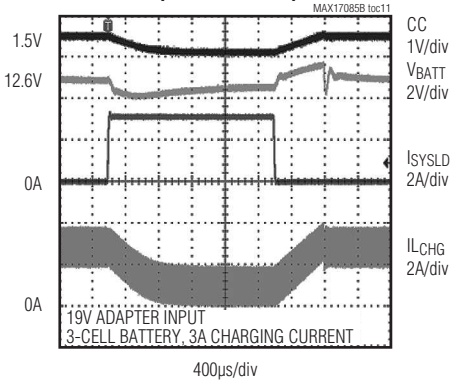
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{ADP} = V_{SYS} = 20V, V_{BATT} = 16.8V, V_{LDO5} = V_{CC} = 5V, V_{LDO3} = 3.3V, T_A = +25°C, unless otherwise noted.)

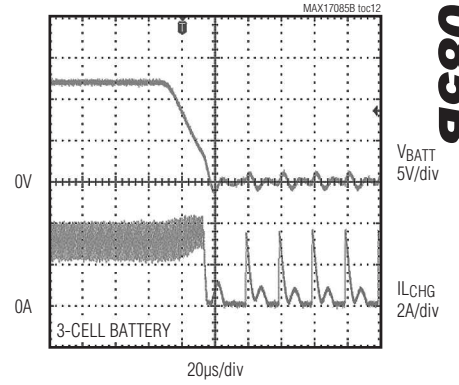
BATTERY REMOVAL (V_{BATT} = 11V)



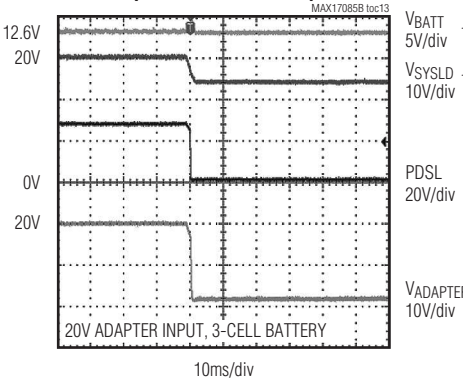
SYSTEM LOAD TRANSIENT (0A→3A→0A)



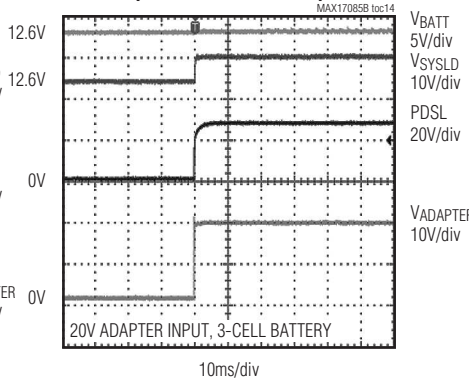
CHARGER OUTPUT SHORT CIRCUIT



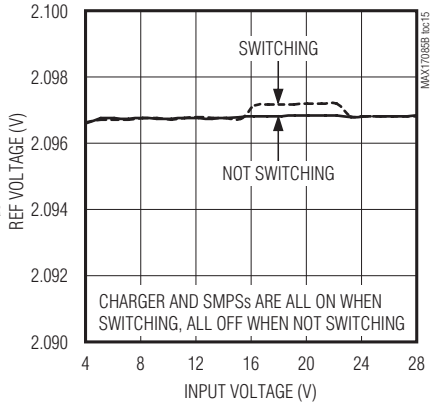
POWER-SOURCE SELECTOR SCHEME WHEN BATTERY IS PRESENT (ADAPTER REMOVAL)



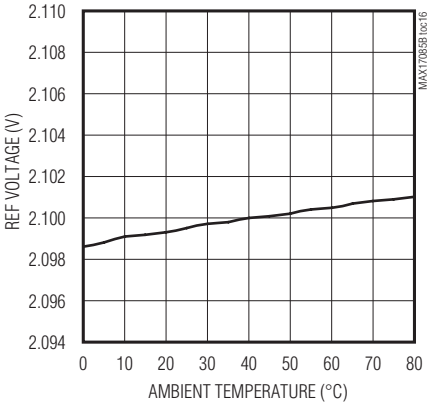
POWER-SOURCE SELECTOR SCHEME WHEN BATTERY IS PRESENT (ADAPTER INSERTION)



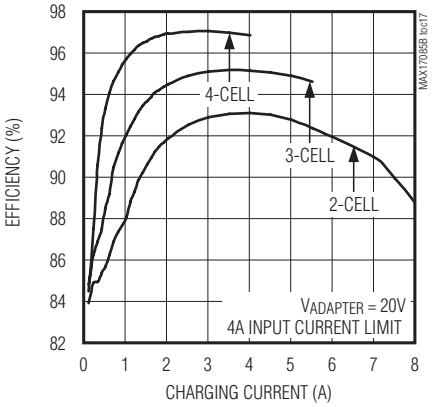
VREF LINE REGULATION (SWITCHING AND NOT SWITCHING)



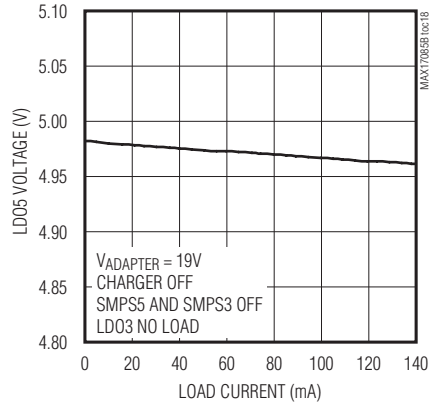
VREF vs. AMBIENT TEMPERATURE



CHARGER EFFICIENCY vs. CHARGING CURRENT



LDO5 LOAD REGULATION

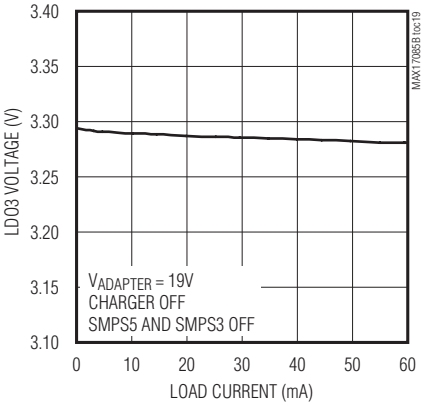


Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

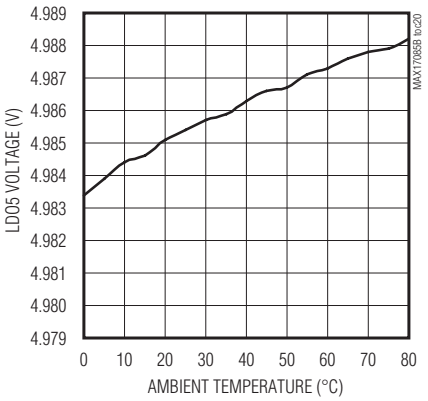
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{ADP} = V_{SYS} = 20V, V_{BATT} = 16.8V, V_{LDO5} = V_{CC} = 5V, V_{LDO3} = 3.3V, T_A = +25°C, unless otherwise noted.)

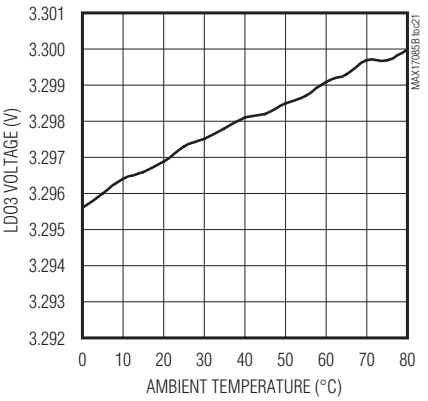
LDO3 LOAD REGULATION



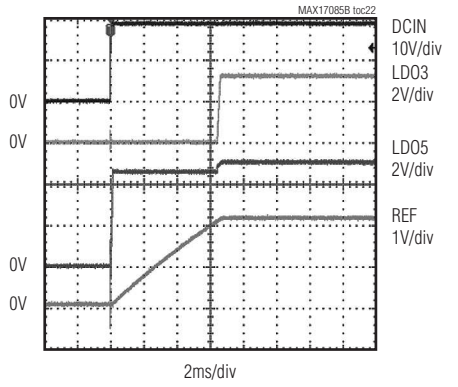
LDO5 vs. AMBIENT TEMPERATURE



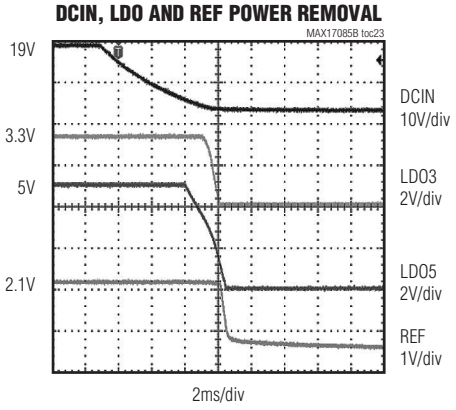
LDO3 vs. AMBIENT TEMPERATURE



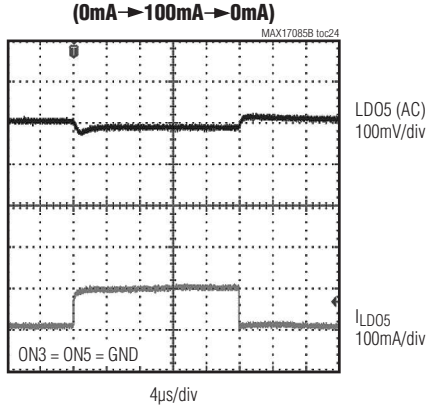
LDO AND REF POWER-UP



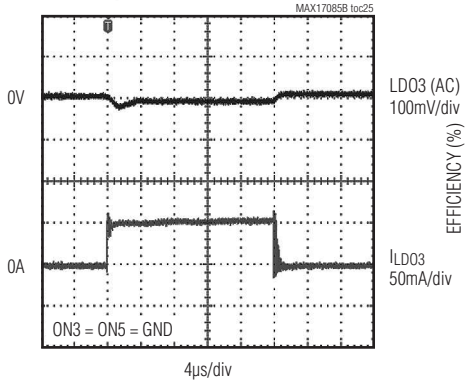
DCIN, LDO AND REF POWER REMOVAL



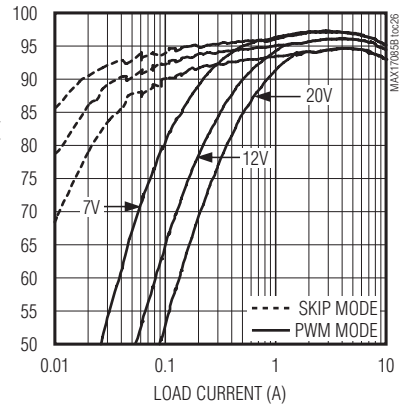
LDO5 LOAD TRANSIENT (0mA→100mA→0mA)



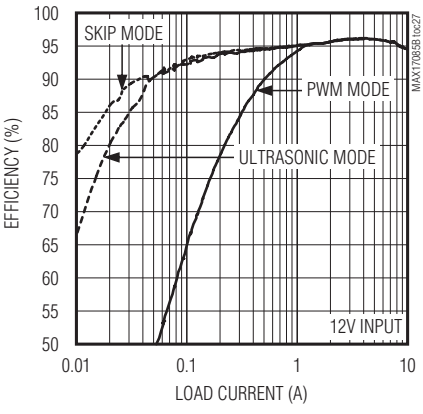
LDO3 LOAD TRANSIENT (0mA→50mA→0mA)



SMPS5 EFFICIENCY vs. LOAD CURRENT (CHARGER AND SMPS3 ARE OFF)



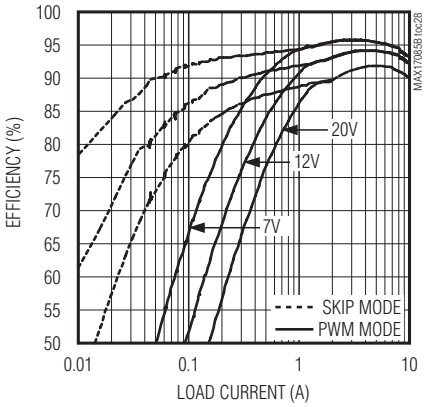
SMPS5 EFFICIENCY vs. LOAD CURRENT (CHARGER AND SMPS3 ARE OFF)



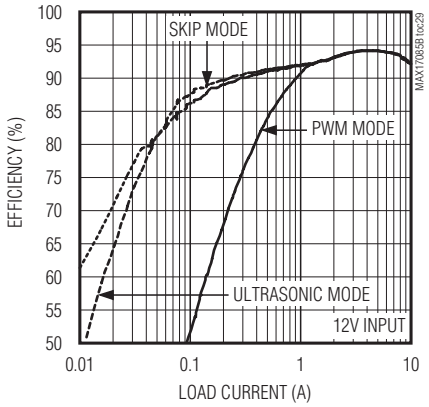
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{ADP} = V_{SYS} = 20V, V_{BATT} = 16.8V, V_{LDO5} = V_{CC} = 5V, V_{LDO3} = 3.3V, T_A = +25°C, unless otherwise noted.)

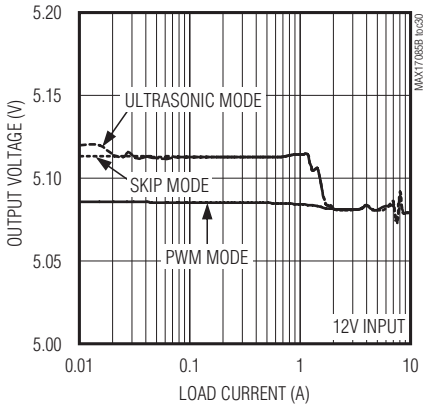
SMPS3 EFFICIENCY vs. LOAD CURRENT (CHARGER AND SMPS5 ARE OFF)



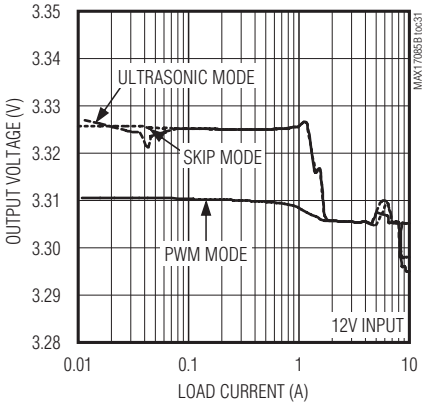
SMPS3 EFFICIENCY vs. LOAD CURRENT (CHARGER AND SMPS5 ARE OFF)



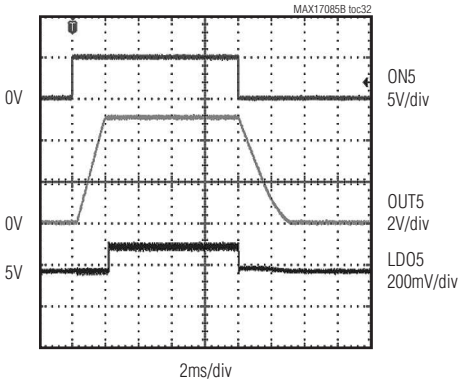
SMPS5 OUTPUT vs. LOAD CURRENT



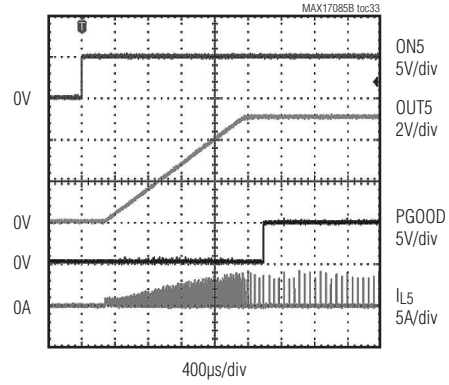
SMPS3 OUTPUT vs. LOAD CURRENT



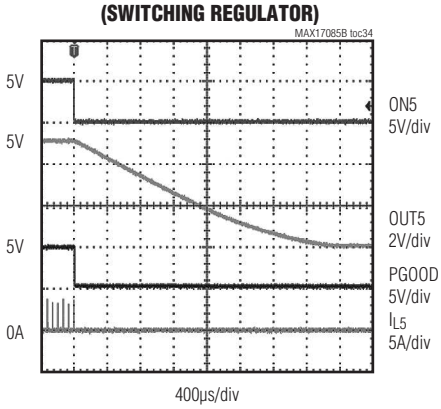
SMPS5 STARTUP AND SHUTDOWN LOAD



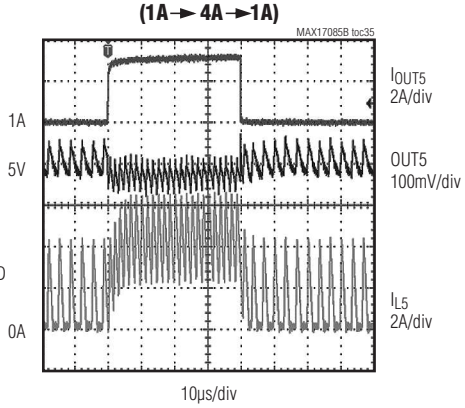
SMPS5 STARTUP WAVEFORMS (SWITCHING REGULATOR)



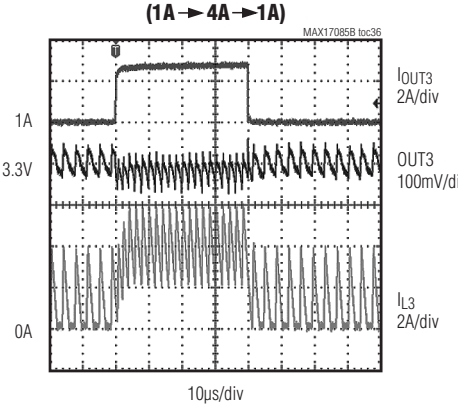
SMPS5 SHUTDOWN WAVEFORMS (SWITCHING REGULATOR)



SMPS5 LOAD TRANSIENT (1A→4A→1A)



SMPS3 LOAD TRANSIENT (1A→4A→1A)



Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

Pin Description

PIN	NAME	FUNCTION
1	LX3	Inductor Connection for SMPS3. Connect LX3 to the switched side of the inductor. LX3 is the lower supply rail for the DH3 high-side gate driver.
2	BST3	Boost Flying Capacitor Connection for SMPS3. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST3 allows the DH3 turn-on current to be adjusted. A 4.7Ω resistor is recommended to improve crosstalk between SMPSs.
3	DL3	Low-Side Gate-Driver Output for SMPS3. DL3 swings from PGND to LDO5.
4	OUT3	Output Voltage-Sense Input for SMPS3. OUT3 is an input to the Quick-PWM on-time one-shot timer. OUT3 also serves as the feedback input for the preset 3.3V, and the discharge path when in shutdown. When OUT3 is in regulation, LDO3 is internally set to a lower level, and a bypass switch between OUT3 and LDO3 is enabled.
5	LDO3	3.3V Linear Regulator Output. LDO3 is the output of the 3.3V linear regulator supplied from LDO5. LDO3 is switched over to OUT3 when SMPS3 is in regulation plus 200µs. Bypass LDO3 to PGND with a 4.7µF or greater ceramic capacitor.
6	DCIN	LDO5 Supply Input. Bypass DCIN with a 1µF capacitor to PGND.
7	LDO5	5V Linear Regulator Output. LDO5 provides the power to the MOSFET drivers. LDO5 is the output of the 5V linear regulator supplied from DCIN. LDO5 is switched over to OUT5 when SMPS5 is in regulation plus 200µs. Bypass LDO5 to PGND with a 4.7µF or greater ceramic capacitor.
8	OUT5	Output Voltage-Sense Input for SMPS5. OUT5 is an input to the Quick-PWM on-time one-shot timer. OUT5 also serves as the feedback input for the preset 5V, and the discharge path when in shutdown. When OUT5 is in regulation, LDO5 is internally set to a lower level, and a bypass switch between OUT5 and LDO5 is enabled.
9	DL5	Low-Side Gate-Driver Output for SMPS5. DL5 swings from PGND to LDO5.
10	BST5	Boost Flying Capacitor Connection for SMPS5. Connect to an external capacitor as shown in Figure 1. An optional resistor in series with BST5 allows the DH5 turn-on current to be adjusted. A 4.7Ω resistor is recommended to improve crosstalk between SMPSs.
11	LX5	Inductor Connection for SMPS5. Connect LX5 to the switched side of the inductor. LX5 is the lower supply rail for the DH5 high-side gate driver.
12	DH5	High-Side Gate-Driver Output for SMPS5. DH5 swings from LX5 to BST5.
13	DLC	Low-Side Power MOSFET Driver Output for Charger. Connect to the low-side n-channel MOSFET gate.
14	BSTC	Boost Flying Capacitor Connection for Charger. Connect a 0.1µF capacitor from BSTC to LXC, and a Schottky diode from LDO5 to BSTC.
15	LXC	High-Side Driver Source Connection. Connect a 0.1µF capacitor from BSTC to LXC.
16	DHC	High-Side Power MOSFET Driver Output for Charger. Connect to high-side n-channel MOSFET gate.
17	PGOOD	Open-Drain Power-Good Output for SMPS3 and SMPS5. PGOOD is low when either SMPS3 or SMPS5 output voltage is more than 250mV (typ) below the nominal regulation threshold, during soft-start, in shutdown (ON3 = ON5 = GND), and after either fault latch has been tripped. After the soft-start circuit has terminated, PGOOD becomes high impedance if the output is in regulation plus 200µs. When only one SMPS is active, PGOOD monitors the active SMPS output. When the 2nd SMPS is started, PGOOD is blanked high-Z during the 2nd SMPS soft-start plus 200µs, then PGOOD monitors both SMPS outputs.

Pin Description (continued)

PIN	NAME	FUNCTION
18	$\overline{ACOK}$	AC-Detect Output. This open-drain output is low impedance when ACIN is greater than 1.5V, with a delay of 44ms. The $\overline{ACOK}$ output remains high impedance when the MAX17085B is powered down. Connect a 100kΩ pullup resistor from LDO3 or LDO5 to $\overline{ACOK}$.
19	CSIN	Output Current-Sense Negative Input
20	CSIP	Output Current-Sense Positive Input. Connect a current-sense resistor from CSIP to CSIN.
21	BATT	Battery Voltage Feedback Input
22	PDSL	Power Source Switch Driver Output. When the adapter is not present or an overvoltage and overcurrent event is detected, the PDSL output is pulled to GND. Leave PDSL unconnected when it is not used.
23	CSSN	Input Current-Sense Negative Input
24	CSSP	Input Current Sense for Positive Input. Connect a current-sense resistor from CSSP to CSSN.
25	IINP	Input Current Monitor Output. IINP sources the current proportional to the current sensed across CSSP and CSSN. The gain from (CSSP - CSSN) to IINP is 60V/V: $V_{IINP} = 60 \times (V_{CSSP} - V_{CSSN})$ IINP also monitors the battery-discharge current when the adapter is absent. To monitor the discharge current, set ISET above the PWM threshold. Pull ISET to GND to disable the IINP battery-discharge current mode.
26	CELLS	Trilevel Input for Setting Number of Cells: • CELLS = open; charge with 2 times the cell voltage programmed at VCTL. • CELLS = GND; charge with 3 times the cell voltage programmed at VCTL. • CELLS > 2.8V; charge with 4 times the cell voltage programmed at VCTL.
27	CC	Charger Loop-Compensation Point. External compensation node for the charge voltage and input current-limit loops. Connect a 4.7nF to 47nF capacitor to GND. Typically a 10nF capacitor works for most applications.
28	ACIN	AC Adapter Detect Input. ACIN is the input to an uncommitted comparator. The $\overline{ACOK}$ detect threshold is typically 1.5V. The ACOVP detect threshold is typically 2.1V. When ACIN is above the $\overline{ACOK}$ detect threshold and below the ACOVP detect threshold, PDSL is enabled.
29	VCTL	Cell Charge Voltage-Control Input. VCTL range is from GND to LDO5. For 4.375V/cell setting, connect VCTL to REF: $V_{CELL} = 2.083 \times V_{VCTL}$
30	V_{CC}	Analog Supply Voltage Input. Connect V_{CC} to the system supply voltage with a series 47Ω resistor, and bypass to analog ground using a 1µF or greater ceramic capacitor.
31	ISET	Dual-Mode Input for Setting Maximum Charge Current. In PWM mode, use input frequencies from 128Hz to 500kHz for charge-current setting. If there are no **two edges** within 20ms, ISET is directly used as an analog input. In analog mode, charge current is set as follows: $I_{CHG} = \frac{100mV}{RS2} \times \frac{V_{ISET}}{V_{REF}}$ Pull ISET to GND to shut down the charger.
32	REF	2.1V Voltage Reference and Device Power-Supply Input. Bypass REF with a 1µF capacitor to GND.
33	GND	Analog Ground
34	ILIM3	Valley Current-Limit Adjustment for SMPS3. The GND - LX3 current-limit threshold is 1/10 the voltage present on ILIM3 over a 0.2V to 2.1V range.
35	ILIM5	Valley Current-Limit Adjustment for SMPS5. The GND - LX5 current-limit threshold is 1/10 the voltage present on ILIM5 over a 0.2V to 2.1V range.

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

Pin Description (continued)

PIN	NAME	FUNCTION
36	SKIP	Pulse-Skipping Control Input. This tri-level input determines the operating mode for the switching regulators. High (V_{CC}) = pulse-skipping mode Mid (1.8V) = forced-PWM operation GND = ultrasonic mode
37	TON	Switching Frequency Setting Input. An external resistor between the input power source and this pin sets the nominal switching frequency according to the following equation: $f_{SW(NOM)} = 1/(C_{TON} \times (R_{TON} + 6.5k\Omega))$ where C_{TON} = 6pF. SMPS5 has a switching frequency that is 10% higher than nominal, and SMPS3 has a switching frequency 10% lower than nominal. R_{TON} is high impedance when ON3 = ON5 = GND.
38	ON3	Enable Input for SMPS3. Drive ON3 high to enable SMPS3. Drive ON3 low to shut down SMPS3.
39	ON5	Enable Input for SMPS5. Drive ON5 high to enable SMPS5. Drive ON5 low to shut down SMPS5.
40	DH3	High-Side Gate-Driver Output for SMPS3. DH3 swings from LX3 to BST3.
—	EP	Exposed Pad. Internally connected to power ground (PGND). Connect the backside exposed pad to the system power ground as well.

Standard Application Circuit

The MAX17085B standard application circuit (Figure 1) features a 4A charger, 8A outputs on SMPS5 and SMPS3, and a 100mA LDO5 and 50mA LDO3 typical of most notebook CPU applications. See Table 1 for component selections. Table 2 lists the component suppliers.

Table 1. Component Selection for Standard Applications

COMPONENT	SMPS3: 3.3V, 8A, 500kHZ	SMPS5: 5V, 8A, 600kHZ	CHARGER, 16.8V, 4A, 1.2MHZ
Input Voltage	**V_{SYS} = 7V to 24V**	**V_{SYS} = 7V to 24V**	**V_{ADP} = 18V to 20V**
Input Capacitor	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM Murata GRM31CR61E106K	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM Murata GRM31CR61E106K	(2) 4.7µF, 25V Taiyo Yuden TMK432BJ475KM Murata GRM31CR71E475M
Output Capacitor	C_{OUT3} (1) 100µF, 6V, 18mΩ SANYO 6TPE100MI	C_{OUT5} (1) 100µF, 6V, 18mΩ SANYO 6TPE100MI	$C_{OUT(CHG)}$ (1) 4.7µF, 25V Taiyo Yuden TMK432BJ475KM Murata GRM31CR71E475M
Inductor	L3 1.5µH, 2.1mΩ, 11.8A Sumida CEP125S-1R5	L5 1.5µH, 2.1mΩ, 11.8A Sumida CEP125S-1R5	L_{CHG} 2µH, 19mΩ, 4.5A Sumida CDR7D28MN-2R0
High-Side MOSFET	N_{H3} 13A, 9.4mΩ/12mΩ, 30V Fairchild FDS6298	N_{H5} 13A, 9.4mΩ/12mΩ, 30V Fairchild FDS6298	N_{HC} 6.6A, 17mΩ/25mΩ, 30V International Rectifier IRF7807D1PBF
Low-Side MOSFET	N_{L3} 13A, 7.2mΩ/10mΩ, 30V Fairchild FDS6670A	N_{L5} 13A, 7.2mΩ/10mΩ, 30V Fairchild FDS6670A	N_{LC} 6.6A, 17mΩ/25mΩ, 30V International Rectifier IRF7807D1PBF
Current-Limit Setting	1.16V (1.16V limit) R_{ILIM3A} = 66.5kΩ R_{ILIM3B} = 82.5kΩ	1.16V (1.16V limit) R_{ILIM5A} = 66.5kΩ R_{ILIM5B} = 82.5kΩ	—

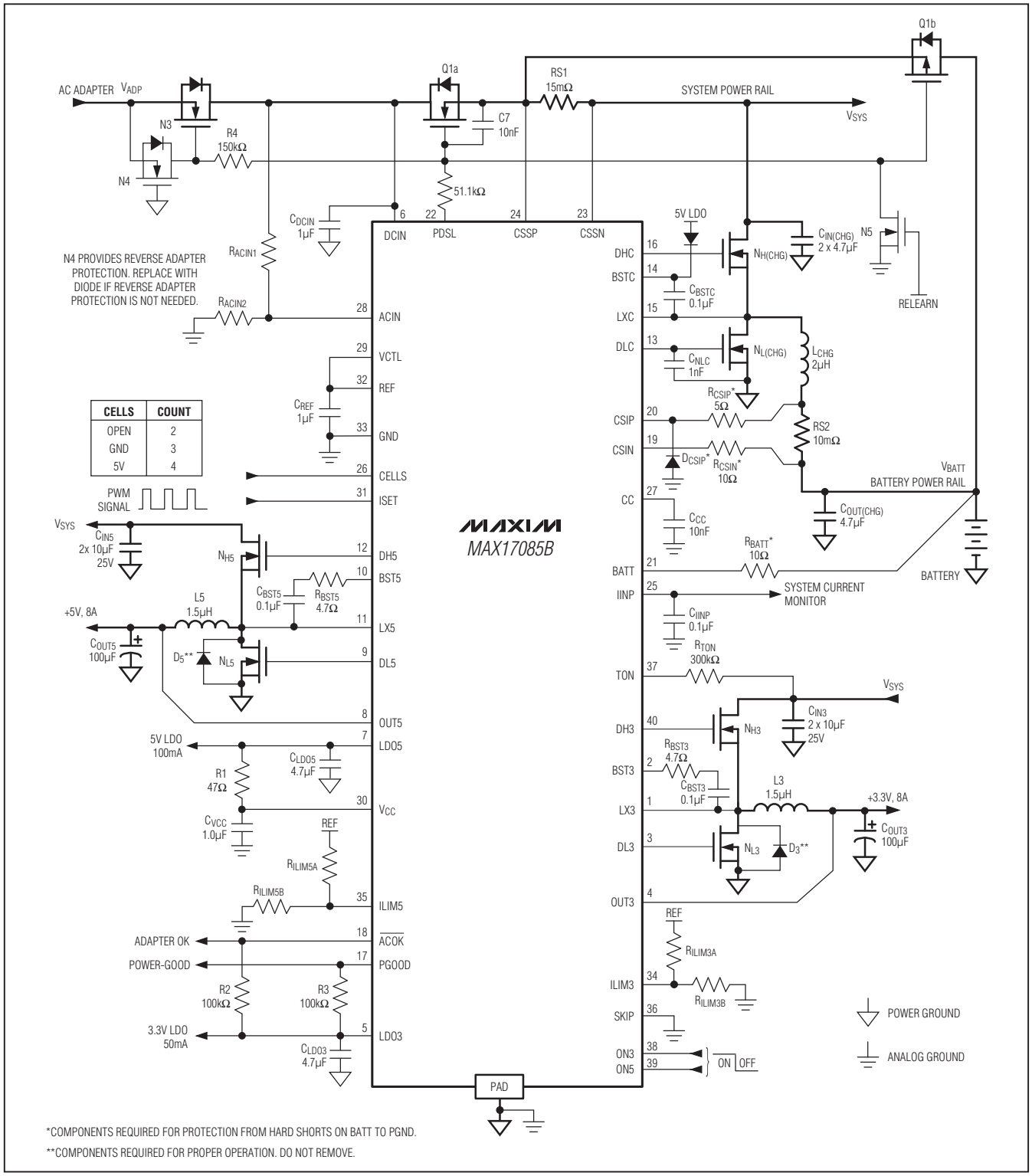


Figure 1. Standard Application Circuit

Table 2. Component Suppliers

SUPPLIER	WEBSITE
AVX Corp.	www.avxcorp.com
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp.	www.kemet.com
NEC/TOKIN America	www.nec-tokinamerica.com
Panasonic Corp.	www.panasonic.com/industrial
Philips/nxp Semiconductor	www.semiconductors.philips.com
Pulse Engineering	www.pulseeng.com
Renesas Technology Corp.	www.renesas.com
SANYO Electric Co., Ltd.	www.sanyodevice.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Vishay (Dale, Siliconix)	www.vishay.com
Würth Elektronik GmbH & Co. KG	www.we-online.com

Detailed Description

The MAX17085B integrated charger and main step-down controllers are ideal for notebook applications where board space and solution cost are key requirements. Together with the integrated, always-on 100mA LDO5 and 50mA LDO3, the MAX17085B provides a complete power solution for the notebook in the off-state, standby-state, and full active state. A functional diagram of the MAX17085B is shown in Figure 2.

Charger

The MAX17085B uses a new thermally optimized high-frequency architecture that reduces the output capacitance and inductance, resulting in smaller PCB area and lower cost. The MAX17085B charger includes all the necessary functions to charge Li+, NiMH, and NiCd batteries. An all n-channel synchronous-rectified step-down DC-DC converter is used to implement a precision constant-current, constant-voltage charger. The charge current and input current-limit sense amplifiers have low-input offset errors (200µV typ), allowing the use of small-valued sense resistors.

Main SMPS

The 5V and 3.3V main SMPSs in the MAX17085B use Maxim's Quick-PWM pulse-width modulator, specifically designed for handling fast load steps while maintaining a relatively constant operating frequency and inductor operating point over a wide range of input voltages. The Quick-PWM architecture circumvents the poor load-transient timing problems of fixed-frequency current-mode PWMs while also avoiding the problems caused by widely varying switching frequencies in conventional constant-on-time and constant-off-time PWM schemes.

100mA 5V Linear Regulator (LDO5) and Bias Supply (VCC)

The MAX17085B includes a high-current (100mA), always-on fixed 5V linear regulator (LDO5). LDO5 is required to generate the 5V bias supply necessary to power up the switching regulators, and as the input supply to the 3.3V linear regulator (LDO3). Once the 5V switching regulator (SMPS5) is enabled and in regulation, LDO5 is bypassed by an internal switch from OUT5 to LDO5. After switchover, the LDO5 pin can source 200mA. LDO5 starts up as soon as DCIN has valid voltage (around 2.5V), and regulates to ~ 4.5V using an internal crude reference. REF starts at the same time, and once REF is in regulation, LDO5 switches over to use the accurate REF, and regulates up to 5V.

The MAX17085B requires a low-noise 5V bias supply (V_{CC}) for its internal circuitry. Typically, this 5V bias is supplied by LDO5 through a lowpass filter. The total supply current required for the MAX17085B is:

$$I_{BIAS(MAX)} = I_{CC(MAX)} + f_{SW5}Q_{G5} + f_{SW3}Q_{G3} + f_{SWC}Q_{GC} \approx 45mA \text{ to } 90mA \text{ (typ)}$$

50mA, 3.3V Linear Regulator (LDO3)

A lower current (50mA), always-on fixed 3.3V linear regulator, is also included in the MAX17085B. Once the 3.3V switching regulator (SMPS3) is enabled and in regulation, LDO3 is bypassed by an internal switch from OUT3 to LDO3. After switchover, the LDO3 pin can source more than 200mA. LDO3 starts up as soon as REF is in regulation. This limits the inrush current by sequencing LDO5 to start before LDO3.

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

Thermal-Fault Protection (t_{SHDN})

The MAX17085B features a thermal fault-protection circuit. When the junction temperature rises above +160°C, a thermal sensor activates the fault latch, pulls PGOOD low, enables the 20Ω discharge circuit, and disables the controller—DH and DL pulled low. After the junction temperature cools by 50°C, the controller automatically restarts. This protects the internal LDO when a sustained overcurrent or output short circuit occurs.

POR, UVLO

When V_{CC} rises above the power-on reset (POR) threshold, the MAX17085B clears the fault latches and resets the soft-start circuit, preparing the controller for power-up. However, the V_{CC} undervoltage-lockout (UVLO) circuitry inhibits switching until V_{CC} reaches its 4.2V (typ) UVLO threshold.

When V_{CC} drops below the UVLO threshold (falling edge), the controller stops switching, pulling DH and DL low. When the 1.5V POR falling edge threshold is reached, the DL state no longer matters since there is not enough voltage to force the switching MOSFETs into a low on-resistance state, so the controller pulls DL high, allowing a soft discharge of the output capacitors (damped response). However, if the V_{CC} recovers before reaching the falling POR threshold, DL remains low until the error comparator has been properly powered up and triggers an on-time.

When DCIN is high enough for LDO5 to be in regulation and VCC to be above its UVLO, the main SMPS can begin running. Charger operation requires DCIN to be above its 7.7V UVLO threshold.

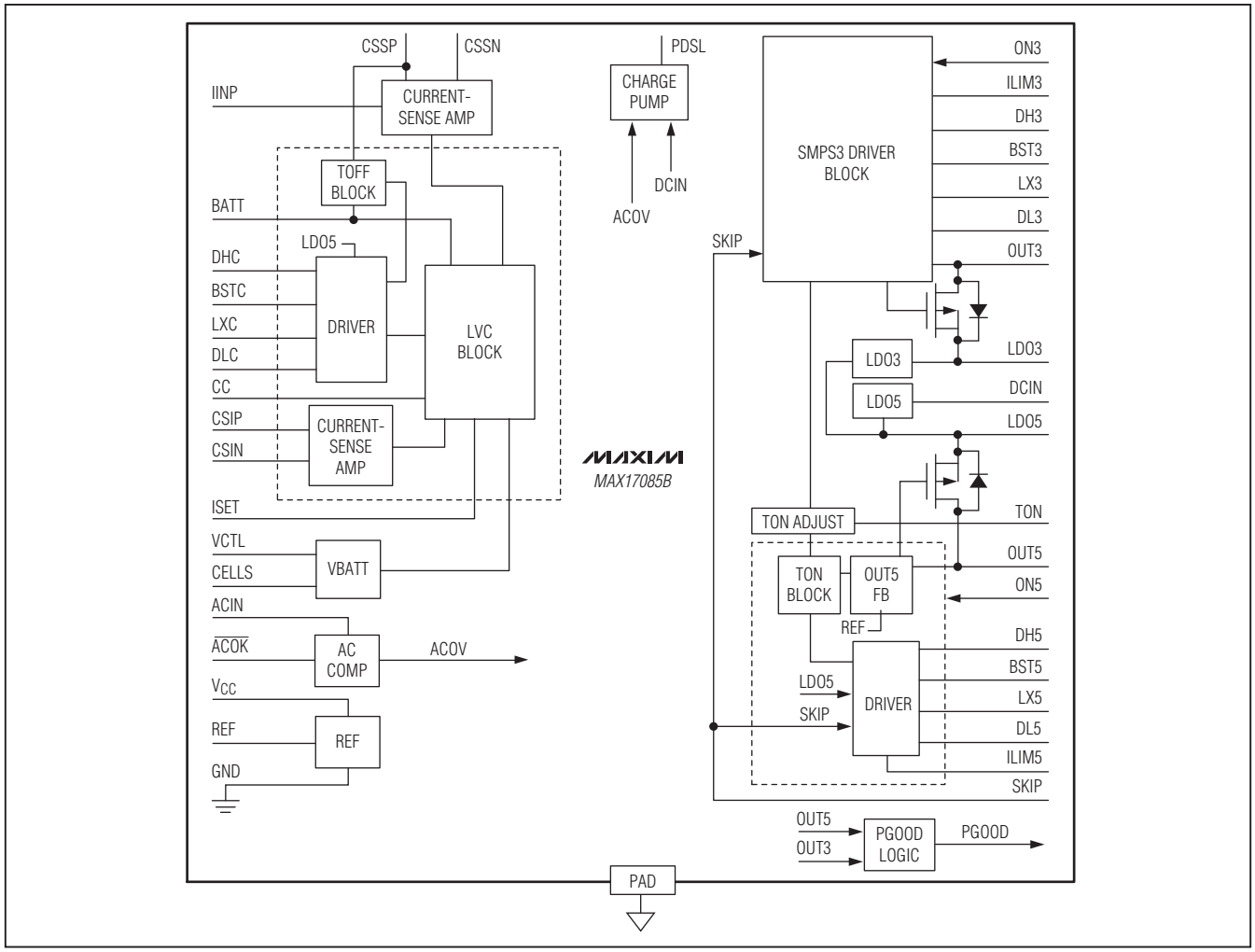


Figure 2. Functional Diagram

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

Charger Detailed Description

The MAX17085B charger has three regulations loops: a voltage-regulation loop (CCV) and two current-regulation loops (CCI and CCS). The loops operate independently of each other. The CCV voltage-regulation loop monitors BATT to ensure that its voltage never exceeds the voltage set by VCTL and CELLS. The CCI battery charge current-regulation loop monitors current delivered to BATT to ensure that it never exceeds the current limit set by ISET. The charge current-regulation loop is in control as long as the battery voltage is below the set point. When the battery voltage reaches its set point, the voltage-regulation loop takes control and maintains the battery voltage at the set point. A third loop (CCS) takes control and reduces the charge current when the adapter current exceeds the input current limit. The CCI current loop is internally compensated while the CCS and CCV loops are externally compensated with a capacitor at the CC pin.

The new thermally optimized high-frequency architecture controls the power dissipation in the high-side MOSFET, resulting in reduced output capacitance and inductance.

Setting the Charge Voltage

The MAX17085B features separate control inputs to set the per-cell voltage and the number of cells in series. The VCTL input sets the per-cell voltage, while the CELLS input sets the total number of cells in series. Together, these two inputs set the charge voltage at the BATT input, providing a flexible way to support different cell types and different battery-pack configurations.

Setting the Per-Cell Charge Voltage (VCTL)

The MAX17085B supports charge voltages of 4.0V/cell to 4.4V/cell based on the following equation:

$$V_{BATT}/Cell = 2.083 \times V_{VCTL}$$

The dynamic range of the VCTL input is limited, so it is possible to achieve ±0.5% charge voltage accuracy using resistive voltage-dividers composed of 1% accurate resistors.

Figure 3 shows a simple method to set two different CELL voltages using a logic output from the embedded controller.

Connecting V_{VCTL} to V_{REF} = 2.10V, which gives 4.375V/cell.

Setting the Number of Cells (CELLS)

The trilevel CELLS input allows simple switching between 2, 3, and 4 cells in series.

Setting Charge Current (ISET)

The ISET input controls the voltage across current-sense resistor RS2. ISET can accept either analog or digital inputs. The full-scale differential voltage between CSIP and CSIN is 100mV (5A for RS2 = 20mΩ).

Important: Keep ISET low during the initial power-up of the MAX17085B. Wait 10ms to allow PDSL to reach its final voltage before enabling the battery charger.

Analog ISET

When the MAX17085B powers up and the charger is ready, if there are no two clock edges within 20ms, the circuit assumes ISET is an analog input, and disables the PWM filter block. For ISET analog input, set ISET according to the following equation:

$$I_{CHG} = \frac{100mV}{RS2} \times \frac{V_{ISET}}{V_{REF}}$$

The input range for ISET is from 0 to REF. To shut down the charger, pull ISET below 26mV.

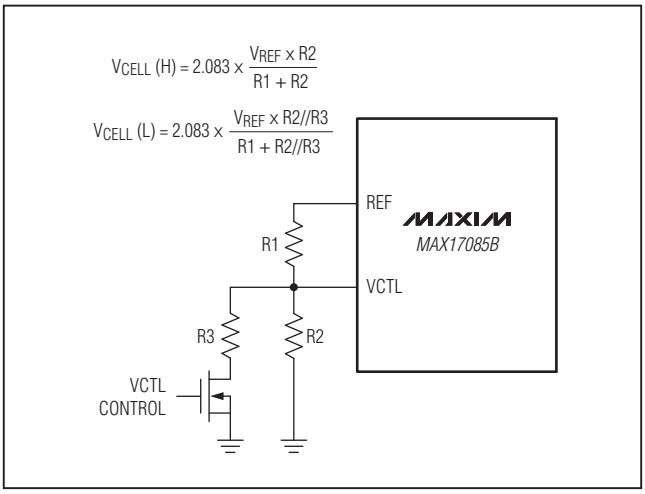


Figure 3. VCTL Setting

Table 3. CELLS Pin Setting

CELLS PIN VOLTAGE	CELLS COUNT	SETTING
OPEN	2	Charge with 2 times the cell voltage programmed at VCTL
GND	3	Charge with 3 times the cell voltage programmed at VCTL
> 2.8V	4	Charge with 4 times the cell voltage programmed at VCTL

Digital ISET

If there are two clock edges on ISET within 20ms, the PWM filter is enabled and ISET accepts digital PWM input. The PWM filter accepts the digital signal with a frequency from 128Hz to 500kHz. Zero duty cycle shuts down the MAX17085B, and the 99% duty cycle corresponds to full scale (100mV) across CSIP and CSIN. The PWM filter has a DAC with 8-bit resolution that corresponds to equivalent V_{CSIP} - V_{CSIN} steps. Each step is:

$$V_{STEP} = \frac{V_{REF}}{256 \cdot 21} = 0.391mV\ (7.8mA\ with\ RS2 = 20m\Omega)$$

Choose a current-sense resistor (RS2) to have a sufficient power dissipation rating to handle the full-charge current. The current-sense voltage may be reduced to minimize the power dissipation period. However, this may degrade accuracy due to the current-sense amplifier's input offset (200µV). See the *Typical Operating Characteristics* to estimate the charge-current accuracy at various set points.

Input Source Current

Setting Input Current Limit

The total input current, from a wall adapter or other DC source, is the sum of the system supply current and the current required by the charger. When the input current exceeds the set input current limit, the controller decreases the charge current to provide priority to system load current. System current normally fluctuates as portions of the system are powered up or down. The input-current-limit circuit reduces the power requirement of the AC wall adapter, which reduces adapter cost. As the system supply rises, the available charge current drops linearly to zero. Thereafter, the total input current can increase without limit. The total input current can be estimated as follows:

$$I_{INPUT} = I_{LOAD} + \frac{I_{CHG} \times V_{BATT}}{V_{ADP} \times \eta}$$

where η is the efficiency of the DC-to-DC converter (typically 85% to 95%).

In the MAX17085B, the voltage across CSSP and CSSN is constant at 60mV. Choose the current-sense resistor, RS1, to set the input current limit. For example, for 4A input current limit choose RS1 = 15mΩ. For the input current-limit settings, which cannot be achievable with standard sense resistor values, use a resistive voltage-divider between CSSP and CSSN to tune the setting.

AC Adapter Overcurrent (ACOC)

When the input current is 1.3 times the input current-limit setting, PDSL is pulled to GND after a 16ms blanking time. This turns off the adapter switch and enables the battery selector switch. After 0.6s, PDSL is reenabled. If the fault condition persists, the cycle is repeated, until the third time when the charger is latched off. To clear the fault latch, remove the adapter and allow DCIN to fall below its UVLO threshold before reinserting the adapter.

Analog Input Current-Monitor Output

IINP monitors the system-input current, which is sensed across CSSP and CSSN. The voltage at IINP is proportional to the input current:

$$V_{IINP} = G_{IINP} \times I_{ADP} \times RS1$$
$$V_{IINP} = 60 \times (V_{CSSP} - V_{CSSN})$$

where I_{ADP} is the DC current supplied by the AC adapter, G_{IINP} is the transconductance of the sense amplifier (60V/V typ), and RS1 is the resistor connected between CSSP and CSSN.

When the adapter is absent, drive ISET above 2.1V to enable IINP during battery discharge.

AC Adapter Detection (ACIN, $\overline{ACOK}$, ACOV)

The ACIN input goes to two internal comparators, one for adapter detection ($\overline{ACOK}$) and another for adapter overvoltage detection (ACOV). When ACIN is above 1.5V, the open-drain $\overline{ACOK}$ output becomes low impedance after 44ms.

When ACIN rises above 2.1V, the MAX17085B detects an ACOV condition and immediately pulls PDSL to GND, turning off the adapter selection switch and enabling the battery selector switch. This protects the system rail from excessively high voltages that might violate the absolute maximum ratings of the downstream components. Note that $\overline{ACOK}$ remains low even when ACIN is above the ACOV threshold.

Use a resistive voltage-divider from the adapter's output to the ACIN pin to set the appropriate detection threshold. Connect a 100kΩ pullup resistor between LDO3 or LDO5 and $\overline{ACOK}$.

Automatic Power-Source Selection (PDSL)

The MAX17085B integrates a charge pump to drive the gate of n-channel adapter selector switches (N3 and Q1a) and the p-channel battery-selector switch (Q1b). When the adapter is present, PDSL is driven 8V above V_{DCIN} so that N3 and Q1a are on, and Q1b is off. See the *Operating Conditions* section for the definition of adapter present.

Integrated Charger, Dual Main Step-Down Controllers, and Dual LDO Regulators

Table 4. Charger Operating Mode Truth Table

DCIN	ADAPTER PRESENT (NOTE 5)	INPUT CURRENT V_{CSSP} - V_{CSSN}	ACIN	ISET	PDSL	CHARGER STATE	IINP	COMMENTS
X	No	X	X	< 1V	GND	OFF	OFF	—
X	No	X	X	> 1V	GND	OFF	ON	—
< UVLO	Yes	> OCP threshold	X	X	GND	OFF	ON	—
< UVLO	Yes	X	V_{ACIN} > V_{ACINOV}	X	GND	OFF	ON	—
< UVLO	Yes	< OCP threshold	V_{ACINOK} < V_{ACIN} and V_{ACIN} < V_{ACINOV}	X	V_{DCIN} + 8V	OFF	ON	—
> UVLO	Yes	X	V_{ACINOK} < V_{ACIN} and V_{ACIN} < V_{ACINOV}	X	GND	OFF	ON	Adapter overvoltage fault
> UVLO	Yes	> OCP threshold	X	X	GND	OFF	ON	Adapter overcurrent fault
> UVLO	Yes	< OCP threshold	V_{ACINOK} < V_{ACIN} and V_{ACIN} < V_{ACINOV}	< ISET shutdown threshold	V_{DCIN} + 8V	OFF	ON	ISET shutdown
> UVLO	Yes	< OCP threshold	< ACOV threshold	> ISET shutdown threshold	V_{DCIN} + 8V	ON (ISET control)	ON	—

Note 5: Adapter is present when V_{DCIN} - V_{CSIN} > 420mV with V_{DCIN} rising, and absent when V_{DCIN} - V_{CSIN} < 120mV with V_{DCIN} falling.

When the adapter voltage is removed and the adapter is absent, the charger is disabled and PDSL is pulled to GND. N3 and Q1a turn off, and Q1b turns on to supply power to the system from the battery.

Operating Conditions

Table 4 defines the MAX17085B charger operating conditions.

Charger SMPS

The MAX17085B employs a synchronous step-down DC-DC converter with an n-channel high-side MOSFET switch and an n-channel low-side synchronous rectifier. The charger features a controlled inductor current ripple architecture, current-mode control scheme with cycle-by-cycle current limit. The controller's off-time (t_{OFF}) is adjusted to keep the high-side MOSFET junction temperature constant. In this way, the controller switches faster when the high-side MOSFET has available thermal capacity. This allows the inductor current ripple and the output voltage ripple to decrease so that smaller and cheaper components can be used. The controller can also operate in discontinuous conduction mode for improved light-load efficiency.

The operation of the DC-to-DC controller is determined by the following five comparators as shown in the functional diagram in Figures 2 and 4:

- The **IMIN** comparator triggers a pulse in discontinuous mode when the accumulated error is too high. IMIN compares the control signal (LVC) against 5mV (typ) (referred at V_{CSIP} - V_{CSIN}). When LVC is less than 5mV, DHC and DLC are both forced low. Indirectly, IMIN sets the peak inductor current in discontinuous mode.
- The **CCMP** comparator is used for current-mode regulation in continuous conduction mode. CCMP compares LVC against the inductor current. The high-side MOSFET on-time is terminated when the CSI voltage is higher than LVC.
- The **IMAX** comparator provides a secondary cycle-by-cycle current limit. IMAX compares CSI to the current limit programmed at ISET. The high-side MOSFET on-time is terminated when the current-sense signal exceeds the programmed limit. A new

cycle cannot start until the IMAX comparator's output goes low.

- The **ZCMP** comparator provides zero-crossing detection during discontinuous conduction. ZCMP compares the current-sense feedback signal to 10mV. When the current-sense signal is lower than the 10mV threshold, the comparator output is high and DLC is turned off.
- The **OV** comparator is used to prevent overvoltage at the output due to battery removal. OV compares BATT against the VCTL and CELLS settings. When BATT is 40mV/cell above the set value, the OV comparator output goes high and the high-side MOSFET on-time is terminated. DHC and DLC remain off until the OV condition is removed.

CCV, CCI, CCS, and LVC Control Blocks

The MAX17085B controls input current (CCS control loop), charge current (CCI control loop), or charge voltage (CCV control loop), depending on the operating condition. The three control loops—CCV, CCI, and CCS—are brought together internally at the lowest voltage clamp (LVC) amplifier. The output of the LVC amplifier is the feedback control signal for the DC-DC controller. The minimum voltage at the CCV, CCI, or CCS appears at the output of the LVC amplifier and clamps the other control loops to within 0.3V above the control point. Clamping the other two control loops close to the lowest control loop ensures fast transition with minimal overshoot when switching between different control loops (see the *Compensation* section). The CCI loop is compensated internally, while the CCS and CCV loops are compensated externally using a shared capacitor on the CC pin.

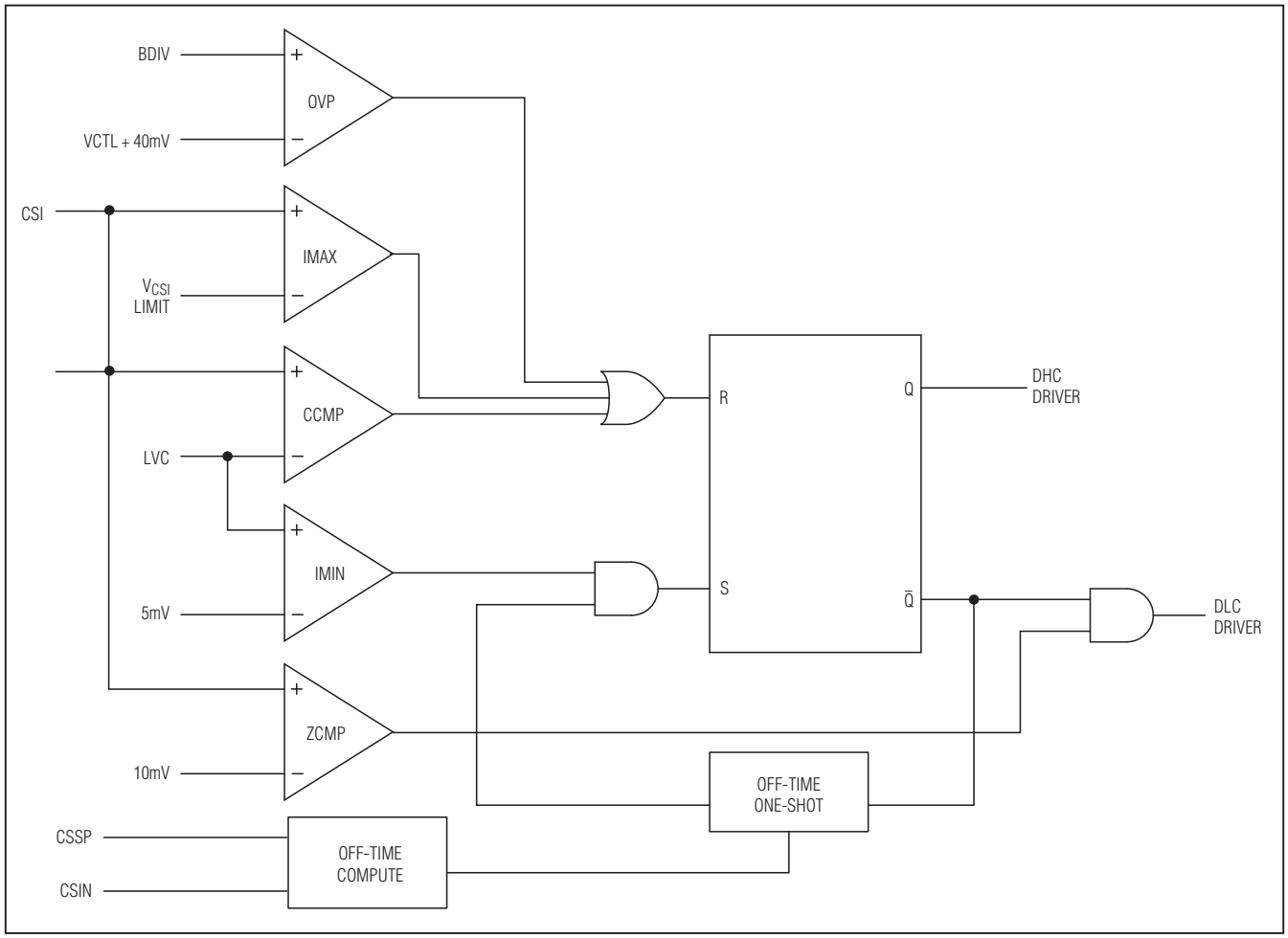


Figure 4. Charger Functional Diagram