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19-5241; Rev 0; 4/10

EVALUATION KIT AVAILABLE

Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

General Description

The MAX17117 includes a high-performance step-up regulator, a 350mA low-dropout (LDO) linear regulator, a high-speed operational amplifier, and a high-voltage level-shifting scan driver with gate-shading control. The device is optimized for thin-film transistor (TFT) liquid-crystal display (LCD) applications.

The step-up DC-DC converter provides the regulated supply voltage for panel source-driver ICs. The high 1.2MHz switching frequency allows the use of ultra-small inductors and ceramic capacitors. The current-mode control architecture provides a fast-transient response to pulsed loads typical of source driver loads. The step-up regulator features an adjustable soft-start and an adjustable cycle-by-cycle current limit.

The high-current operational amplifier is designed to drive the LCD backplane (VCOM). The amplifier features high output current (±200mA typ), fast slew rate (40V/µs typ), wide bandwidth (16MHz typ), and rail-to-rail inputs and outputs.

The low-voltage LDO linear regulator has an integrated 0.8Ω pass element and can provide at least 350mA. The output voltage is accurate within ±1%.

The high-voltage, level-shifting scan driver with gate-shading control is designed to drive the TFT panel gate drivers. Its seven outputs swing 40V (maximum) between +35V (maximum) and -15V (minimum) and can swiftly drive capacitive loads.

The MAX17117 is available in a 32-pin, 5mm x 5mm, thin QFN package with a maximum thickness of 0.8mm for thin LCD panels.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17117ETJ+	-40°C to +85°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

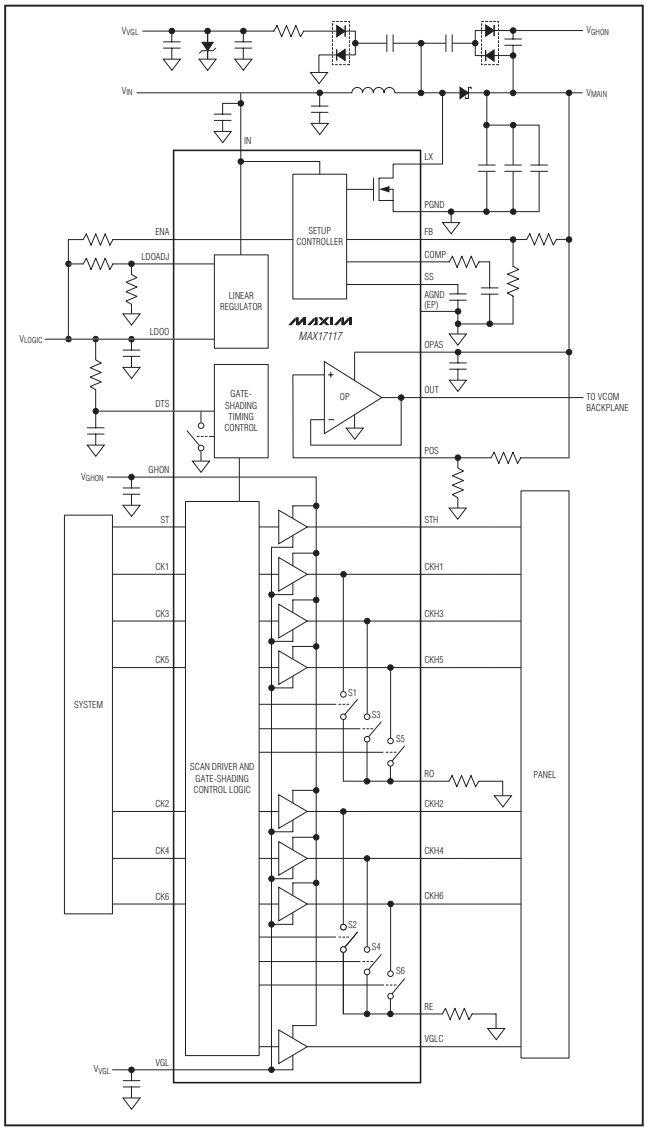
Applications

Notebook Computer Displays

Features

- **2.3V to 5.5V IN Supply-Voltage Range**
- **1.2MHz Current-Mode Step-Up Regulator**
  - **Fast-Transient Response**
  - **High-Accuracy Reference (1%)**
  - **Integrated 16V, 2A, 200mΩ MOSFET**
  - **High Efficiency (> 85%)**
  - **Adjustable Cycle-by-Cycle Current Limit**
- **High-Performance Operational Amplifier**
  - **200mA Output Short-Circuit Current**
  - **40V/µs Slew Rate**
  - **16MHz, -3dB Bandwidth**
  - **Low-Dropout Linear Regulator**
  - **High-Accuracy Output Voltage (1.0%)**
- **High-Voltage Drivers with Scan Logic**
  - **+35V to -15V Outputs**
  - **40V Maximum Voltage Swing**
  - **Gate-Shading Control**
- **Thermal-Overload Protection**
- **32-Pin, 5mm x 5mm, Thin QFN Package**

Simplified Operating Circuit



Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

ABSOLUTE MAXIMUM RATINGS

IN, ENA, FB, COMP, SS, DTS, LDOADJ, ST, CK1–CK6, LDOO to AGND ..... -0.3V to +7.5V
PGND to AGND ..... -0.3V to +0.3V
LX, OPAS to PGND ..... -0.3V to +18V
GHON to PGND ..... -0.3V to +45V
VGL to PGND ..... -20V to +0.3V
GHON to VGL ..... +45V
STH, CKH1–CKH6, VGLC, RO, RE to VGL ..... -0.3V to (V_{GHON} + 0.3V)
OUT, POS to PGND ..... -0.3V to (V_{OPAS} + 0.3V)
GHON and VGL RMS Current Rating 0.8A
VGLC, STH, and CKH1–CKH6 RMS Current Rating 0.8A
LX, PGND RMS Current Rating 1.6A
Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 24.9mW/°C above +70°C) 1990mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, V_{GHON} = +24V, V_{VGL} = -6.2V, V_{ST} = $V_{CK\_}$ = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input Voltage Range		2.3		5.5	V
IN Undervoltage-Lockout Threshold	V_{IN} rising, typical hysteresis = 150mV	1.80	2.00	2.20	V
IN Quiescent Current	V_{FB} = 1.3V, LX not switching		1.0	2.5	mA
	V_{FB} = 1.2V, LX switching		2.5	5	
IN Standby Current	V_{ENA} = V_{VGL} = 0V, V_{IN} = 5.5V, V_{GHON} = 4V		0.7	2	mA
GHON Standby Current	V_{ENA} = V_{VGL} = 0V, V_{IN} = 5.5V, V_{GHON} = 4V		100	200	µA
OPAS Standby Current	V_{ENA} = V_{VGL} = 0V, V_{IN} = 5.5V, V_{GHON} = 4V		20	50	µA
Thermal Shutdown	Temperature rising	145	170		°C
STEP-UP REGULATOR					
Output Voltage Range		V_{IN}		15	V
OPAS Overvoltage Threshold	OPAS rising	16.5	17	18	V
Operating Frequency		1000	1200	1400	kHz
Oscillator Maximum Duty Cycle		91	94	97	%
FB Regulation Voltage	No load	1.227	1.240	1.252	V
FB Fault-Trip Level	Falling edge	1.05	1.10	1.15	V
Fault-Trigger Delay			160		ms
FB Load Regulation	0 < I_{LOAD} < full load		-0.2		%
FB Line Regulation	V_{IN} = 2.5V to 5.5V, T_A = +25°C		0.1	0.25	%/V
FB Input-Bias Current	V_{FB} = 1.24V, T_A = +25°C		65	200	nA
FB Transconductance	ΔI_{COMP} = ±2.5µA, FB = COMP	75	160	280	µS
LX Current Limit	R_{ENA} = 10kΩ, duty cycle = 60%	1.6	2	2.4	A
LX On-Resistance	I_{LX} = 1A		200	500	mΩ
LX Input-Bias Current	V_{LX} = 13.5V, T_A = +25°C		10	20	µA
Current-Sense Transresistance		0.10	0.20	0.30	V/A
Soft-Start Pullup Current		2	4	6	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, V_{GHON} = +24V, V_{VGL} = -6.2V, V_{ST} = $V_{CK\_}$ = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCOM BUFFER					
OPAS Voltage Range		5		15	V
OPAS Supply Current	V_{POS} = V_{OPAS}/2, no load		0.8	1.2	mA
OUT Voltage Swing High	I_{OUT} = 5mA	V_{OPAS} - 100	V_{OPAS} - 50		mV
OUT Voltage Swing Low	I_{OUT} = 5mA		50	100	mV
OUT Short-Circuit Current	Sourcing, short to V_{OPAS}/2 - 1V	100	200		mA
	Sinking, short to V_{OPAS}/2 + 1V	100	200		
POS Input-Bias Current	V_{POS} = V_{OPAS}/2, T_A = +25°C	-50		+50	nA
POS Input-Offset Voltage	V_{OUT} = V_{OPAS}/2	-15		+15	mV
Gain-Bandwidth Product			8		MHz
-3dB Bandwidth	R_{LOAD} = 10kΩ, C_{LOAD} = 10pF		16		MHz
Slew Rate	5V pulse applied to POS, OUT measured from 10% to 90%	10	40		V/µs
HIGH-VOLTAGE SCAN DRIVER					
GHON Voltage Range		12		35	V
VGL Voltage Range		-15		-3	V
GHON-to-VGL Voltage Range	V_{GHON} - V_{VGL}			40	V
GHON Supply Current	CK1 through CK6 and ST low		350	550	µA
VGL Supply Current	CK1 through CK6 and ST low	-500	-300		µA
Output Impedance Low	STH, CKH_, VGLC, I_{OUT} = -20mA			80	Ω
Output Impedance High	STH, CKH_, VGLC, I_{OUT} = +20mA			80	Ω
Gate-Shading Switch Resistance	CKH1, CKH3, CKH5, I_{RE} = 10mA			100	Ω
	CKH2, CKH4, CKH6, I_{RO} = 10mA			100	
RO, RE Resistance Range		100			Ω
Propagation Delay from ST Rising Edge to STH Rising Edge	C_{LOAD} = 100pF, R_{LOAD} = 0Ω		100	200	ns
Propagation Delay from ST Falling Edge to STH Falling Edge	C_{LOAD} = 100pF, R_{LOAD} = 0Ω		100	200	ns
Propagation Delay from CK_ Rising Edge to CKH_ Rising Edge	C_{LOAD} = 100pF, R_{LOAD} = 0Ω		100	200	ns
Propagation Delay from CK_ Falling Edge to CKH_ Falling Edge	C_{LOAD} = 100pF, R_{LOAD} = 0Ω		100	200	ns
STH, VGLC, CKH_ Rise Time	C_{LOAD} = 5nF, R_{LOAD} = 0Ω; V_{GHON} = 30V, V_{VGL} = -10V; measured from 10% to 90%		0.5	1	µs
STH, VGLC, CKH_ Fall Time	C_{LOAD} = 5nF, R_{LOAD} = 0Ω; V_{GHON} = 30V, V_{VGL} = -10V; measured from 10% to 90%		0.5	1	µs
STH, CKH_ Operating Frequency Range	C_{LOAD} = 5nF, R_{LOAD} = 0Ω			100	kHz

Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, V_{GHON} = +24V, V_{VGL} = -6.2V, V_{ST} = $V_{CK\_}$ = 0V, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GATE-SHADING TIMING CONTROL					
Gate-Shading Detection Threshold	DTS falling		100	150	mV
Gate-Shading Detection Current	V_{DTS} = 0.5V	5	10	15	µA
DTS Switch Resistance	V_{DTS} = 1.3V, I_{DTS} = 1mA		10	50	Ω
DTS Rising Edge Threshold		1.215	1.240	1.265	V
DTS Falling Edge Threshold			100	150	mV
LDO					
LDOO Output Voltage Range		1.8		V_{IN}	V
Dropout Voltage	V_{IN} = 3.3V, V_{LDOADJ} = 1.1V, I_{LDOO} = 350mA		300	500	mV
LDOO Line Regulation	V_{IN} = 2.8V to 5.5V, V_{LDOO} = 2.5V, I_{LDOO} = 100mA		0.1	0.3	%/V
LDOO Load Regulation	V_{LDOO} = 2.5V, I_{LDOO} = 1mA to 300mA		0.2	0.5	%/V
LDOO Current Limit	V_{LDOADJ} = 1.0V	0.4	0.62	0.8	A
LDOADJ Feedback Voltage		1.227	1.240	1.252	V
LDOADJ Input-Bias Current	V_{LDOADJ} = 1.3V, T_A = +25°C		100	200	nA
DIGITAL INPUTS					
ST, CK_ Input High Level	1.8V < V_{LDOO} < 5.5V	0.7 x V_{LDOO}			V
ST, CK_ Input Low Level	1.8V < V_{LDOO} < 5.5V			0.3 x V_{LDOO}	V
ENA Input Logic-High Level	1.8V < V_{LDOO} < 3.0V	0.7 x V_{LDOO}			V
	V_{LDOO} > 3.0V	2.1			V
ENA Input Logic-Low Level	1.8V < V_{LDOO} < 3.0V			0.3 x V_{LDOO}	V
	V_{LDOO} > 3.0V			0.8	V
ENA Resistor Range		0		200	kΩ

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, V_{GHON} = +24V, V_{VGL} = -6.2V, V_{ST} = $V_{CK\_}$ = 0V, **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IN Input Voltage Range		2.3		5.5	V
IN Undervoltage-Lockout Threshold	V_{IN} rising, typical hysteresis = 150mV	1.80		2.20	V
IN Quiescent Current	V_{FB} = 1.3V, LX not switching			2.5	mA
	V_{FB} = 1.2V, LX switching			5	
IN Standby Current	V_{ENA} = V_{VGL} = 0V, V_{IN} = 5.5V, V_{GHON} = 4V			2	mA
GHON Standby Current	V_{ENA} = V_{VGL} = 0V, V_{IN} = 5.5V, V_{GHON} = 4V			160	µA
OPAS Standby Current	V_{ENA} = V_{VGL} = 0V, V_{IN} = 5.5V, V_{GHON} = 4V			50	µA
Thermal Shutdown	Temperature rising	145			°C

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, V_{GHON} = +24V, V_{VGL} = -6.2V, V_{ST} = $V_{CK\_}$ = 0V, **T_A = -40°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STEP-UP REGULATOR					
Output Voltage Range		V_{IN}		15	V
OPAS Overvoltage Threshold	OPAS rising	16.5		18	V
Operating Frequency		1000		1400	kHz
Oscillator Maximum Duty Cycle		91		97	%
FB Regulation Voltage	No load	1.227		1.252	V
FB Fault-Trip Level	Falling edge	1.05		1.15	V
FB Line Regulation	V_{IN} = 2.5V to 5.5V, T_A = +25°C			0.3	%/V
FB Input-Bias Current	V_{FB} = 1.3V, T_A = +25°C			200	nA
FB Transconductance	ΔI_{COMP} = ±2.5µA, FB = COMP	75		280	µS
LX Current Limit	V_{FB} = 1.2V, duty cycle = 60%	1.6		2.4	A
LX On-Resistance	I_{LX} = 1A			500	mΩ
LX Input-Bias Current	V_{LX} = 13.5V, T_A = +25°C			20	µA
Current-Sense Transresistance		0.10		0.30	V/A
Soft-Start Pullup Current		2		6	µA
VCOM BUFFER					
OPAS Voltage Range		5		15	V
OPAS Supply Current	V_{POS} = V_{OPAS}/2, no load			1.2	mA
OUT Voltage Swing High	I_{OUT} = 5mA	V_{OPAS} - 100			mV
OUT Voltage Swing Low	I_{OUT} = 5mA			100	mV
OUT Short-Circuit Current	Sourcing, short to V_{OPAS}/2 - 1V	100			mA
	Sinking, short to V_{OPAS}/2 + 1V	100			
POS Input-Bias Current	V_{POS} = V_{OPAS}/2, T_A = +25°C	-50		+50	nA
POS Input-Offset Voltage	V_{OUT} = V_{OPAS}/2	-15		+15	mV
Slew Rate	5V pulse applied to POS, OUT measured from 10% to 90%	10			V/µs
HIGH-VOLTAGE SCAN DRIVER					
GHON Voltage Range		12		35	V
VGL Voltage Range		-15		-3	V
GHON-to-VGL Voltage Range	V_{GHON} - V_{VGL}			40	V
GHON Supply Current	CK1 through CK6 and ST low			550	µA
VGL Supply Current	CK1 through CK6 and ST low	-500			µA
Output Impedance Low	STH, CKH_, VGLC, I_{OUT} = -20mA			80	Ω
Output Impedance High	STH, CKH_, VGLC, I_{OUT} = +20mA			80	Ω
Gate-Shading Switch Resistance	CKH1, CKH3, CKH5, I_{RE} = 10mA			100	Ω
	CKH2, CKH4, CKH6, I_{RO} = 10mA			100	
RO, RE Resistance Range		100			Ω
Propagation Delay from ST Rising Edge to STH Rising Edge	C_{LOAD} = 100pF, R_{LOAD} = 0Ω			200	ns

Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3V, Circuit of Figure 1, V_{OPAS} = +8.5V, V_{GHON} = +24V, V_{VGL} = -6.2V, V_{ST} = $V_{CK\_}$ = 0V, **T_A = -40°C to +85°C**, unless otherwise noted.)

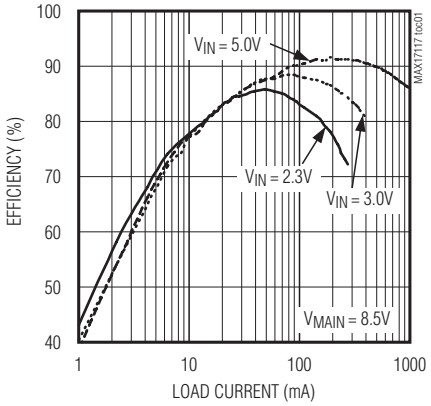
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from ST Falling Edge to STH Falling Edge	C_{LOAD} = 100pF, R_{LOAD} = 0Ω			200	ns
Propagation Delay from CK_ Rising Edge to CKH_ Rising Edge	C_{LOAD} = 100pF, R_{LOAD} = 0Ω			200	ns
Propagation Delay from CK_ Falling Edge to CKH_ Falling Edge	C_{LOAD} = 100pF, R_{LOAD} = 0Ω			200	ns
STH, VGLC, CKH_ Rise Time	C_{LOAD} = 5nF, R_{LOAD} = 0Ω; V_{GHON} = 30V, V_{VGL} = -10V; measured from 10% to 90%			1	µs
STH, VGLC, CKH_ Fall Time	C_{LOAD} = 5nF, R_{LOAD} = 0Ω; V_{GHON} = 30V, V_{VGL} = -10V; measured from 10% to 90%			1	µs
STH, CKH_ Operating Frequency Range	C_{LOAD} = 5nF, R_{LOAD} = 0Ω			100	kHz
GATE-SHADING TIMING CONTROL					
Gate-Shutdown Detection Threshold	DTS falling		100	150	mV
Gate-Shutdown Detection Current	V_{DTS} = 0.5V	5	10	15	µA
DTS Switch Resistance	V_{DTS} = 1.3V, I_{DTS} = 1mA			50	Ω
DTS Rising Edge Threshold		1.210		1.265	V
DTS Falling Edge Threshold				150	mV
LDO					
LDOO Output Voltage Range		1.8		V_{IN}	V
Dropout Voltage	V_{IN} = 3.3V, V_{LDOADJ} = 1.1V, I_{LDOO} = 350mA			500	mV
LDOO Line Regulation	V_{IN} = 2.8V to 5.5V, V_{LDOO} = 2.5V, I_{LDOO} = 100mA			0.3	%/V
LDOO Load Regulation	V_{LDOO} = 2.5V, I_{LDOO} = 1mA to 300mA			0.5	%/V
LDOO Current Limit	V_{LDOADJ} = 1.0V	0.4		0.8	A
LDOADJ Feedback Voltage		1.227		1.252	V
LDOADJ Input-Bias Current	V_{LDOADJ} = 1.3V, T_A = +25°C			200	nA
DIGITAL INPUTS					
ST, CK_ Input High Level	1.8V < V_{LDOO} < 5.5V	0.7 x V_{LDOO}			V
ST, CK_ Input Low Level	1.8V < V_{LDOO} < 5.5V			0.3 x V_{LDOO}	V
ENA Input Logic-High Level	1.8V < V_{LDOO} < 3.0V	0.7 x V_{LDOO}			V
	V_{LDOO} > 3.0V	2.1			
ENA Input Logic-Low Level	1.8V < V_{LDOO} < 3.0V			0.3 x V_{LDOO}	V
	V_{LDOO} > 3.0V			0.8	
ENA Resistor Range		0		200	kΩ

Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

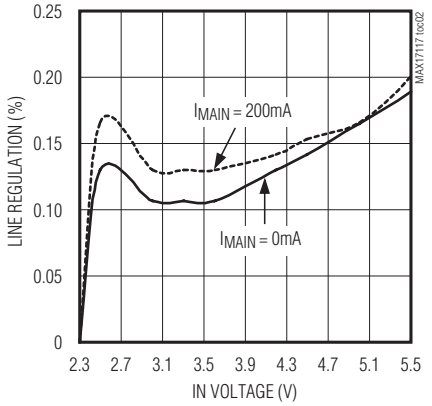
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

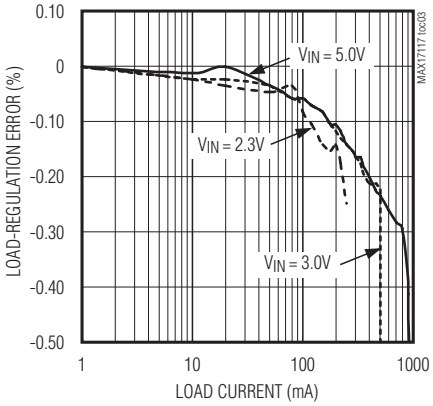
STEP-UP REGULATOR EFFICIENCY vs. LOAD CURRENT



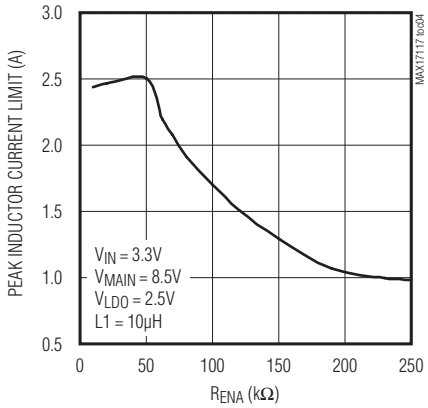
STEP-UP REGULATOR LINE REGULATION vs. INPUT VOLTAGE



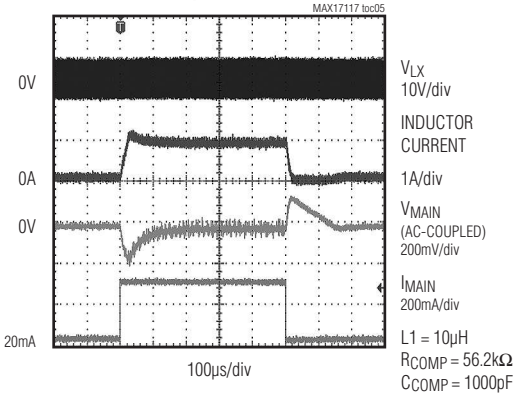
STEP-UP REGULATOR OUTPUT LOAD REGULATION vs. LOAD CURRENT



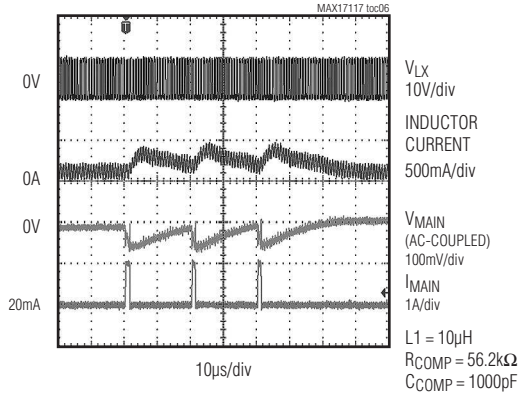
STEP-UP CONVERTER PEAK INDUCTOR CURRENT LIMIT vs. RENA



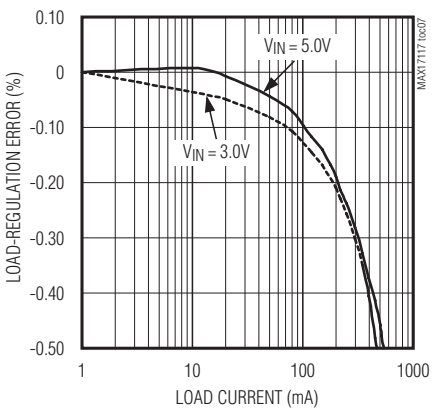
STEP-UP REGULATOR LOAD-TRANSIENT RESPONSE (20mA TO 300mA)



STEP-UP REGULATOR PULSED LOAD-TRANSIENT RESPONSE (20mA TO 1A)



LDO OUTPUT LOAD REGULATION vs. LOAD CURRENT

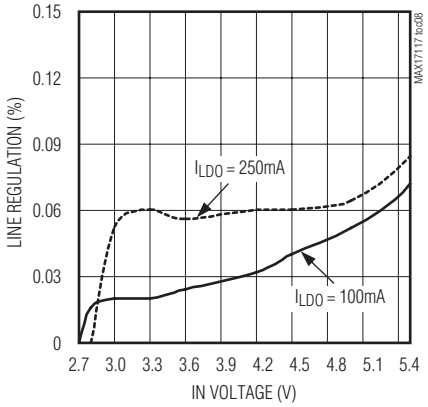


Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

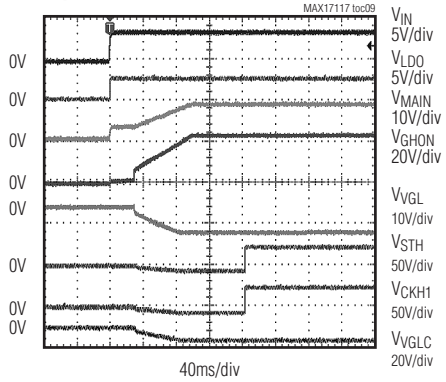
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

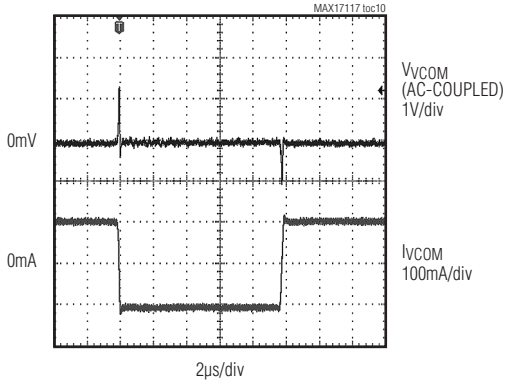
LDO LINE REGULATION vs. INPUT VOLTAGE



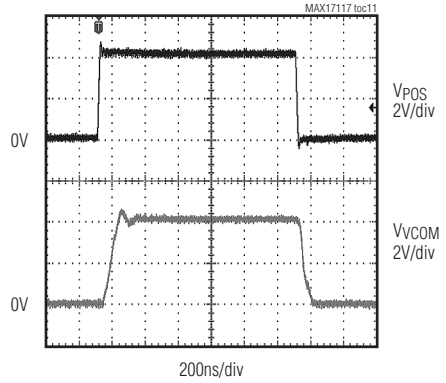
POWER-UP SEQUENCE (CK1 AND ST CONNECTED TO V_{LDO})



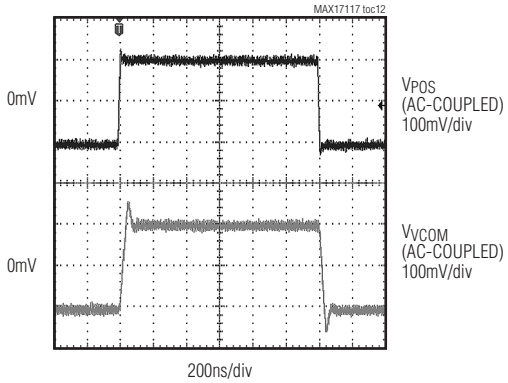
OPERATIONAL AMPLIFIER LOAD-TRANSIENT RESPONSE



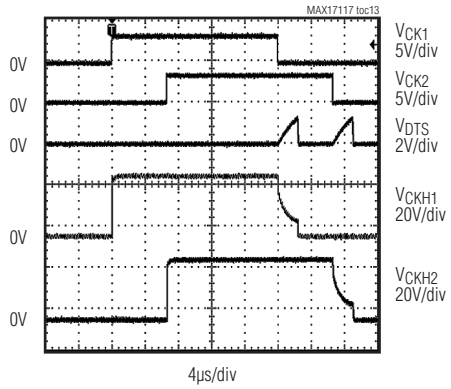
OPERATIONAL AMPLIFIER LARGE-SIGNAL STEP RESPONSE



OPERATIONAL AMPLIFIER SMALL-SIGNAL STEP RESPONSE

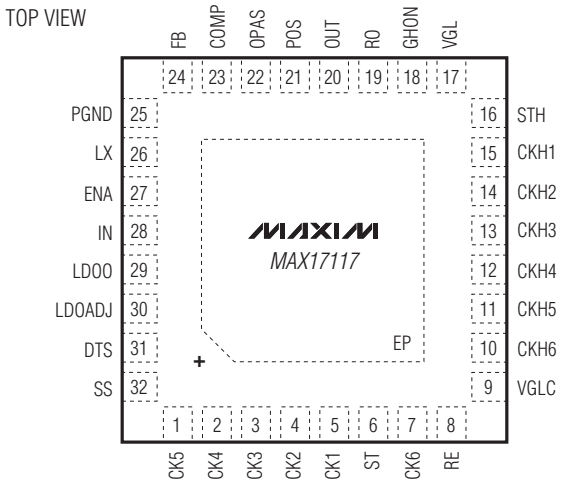


CKH_ OUTPUT WAVEFORMS WITH LOGIC INPUT AND GATE-SHADING CONTROL



Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

Pin Configuration



THIN QFN

Pin Description

PIN	NAME	FUNCTION
1–5, 7	CK5–CK1, CK6	Level-Shifter Logic-Level Inputs
6	ST	Start-Pulse, Level-Shifter Logic-Level Input
8	RE	Gate-Shading Discharge for CKH2, CKH4, and CKH6
9	VGLC	VGL Voltage Output
10–15	CKH6–CKH1	Level-Shifter Outputs
16	STH	Start-Pulse Level-Shifter Output
17	VGL	Gate-Off Supply. VGL is the negative supply voltage for the STH, CKH1–CKH6, and VGLC high-voltage driver outputs. Bypass to PGND with a minimum of 0.1µF ceramic capacitor.
18	GHON	Gate-On Supply. GHON is the positive supply voltage for the STH, CKH1–CKH6, and VGLC high-voltage scan-driver outputs. Bypass to PGND with a minimum of 0.1µF ceramic capacitor.
19	RO	Gate-Shading Discharge for CKH1, CKH3, and CKH5
20	OUT	Operational Amplifier Output
21	POS	Operational Amplifier Noninverting Input
22	OPAS	Operational Amplifier Supply Input. Connect to V_{MAIN} (Figure 1) and bypass to AGND with a 0.1µF or greater ceramic capacitor.
23	COMP	Compensation for Error Amplifier. Connect a series RC from this pin to AGND. Typical values are 56kΩ and 1000pF.
24	FB	Step-Up Regulator Feedback. Reference voltage is 1.24V nominal. Connect the midpoint of an external resistor-divider to FB and minimize trace area. Set V_{MAIN} according to V_{MAIN} = 1.24V (1 + R1/R2).

Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

Pin Description (continued)

PIN	NAME	FUNCTION
25	PGND	Power Ground. Source connection of the internal step-up regulator power switch.
26	LX	Switching Node. Connect inductor/catch diode here and minimize trace area for lowest EMI.
27	ENA	Chip-Enable Control and OCP Set Input. When ENA = low, the step-up converter and op amp are disabled, the LDO remains active, and the level-shifter outputs are high impedance.
28	IN	Step-Up Regulator and Low-Dropout Regulator Supply. Bypass IN to AGND with a 1µF or greater ceramic capacitor.
29	LDOO	Internal Linear Regulator Output. Bypass LDOO to AGND with a 1µF capacitor.
30	LDOADJ	Linear Regulator Feedback Input. Reference voltage is 1.24V nominal.
31	DTS	Gate-Shading Discharge Time Adjust
32	SS	Step-Up Regulator Soft-Start Control
—	EP	Exposed Backside Pad. Connect to the analog ground plane for proper electrical and thermal performance.

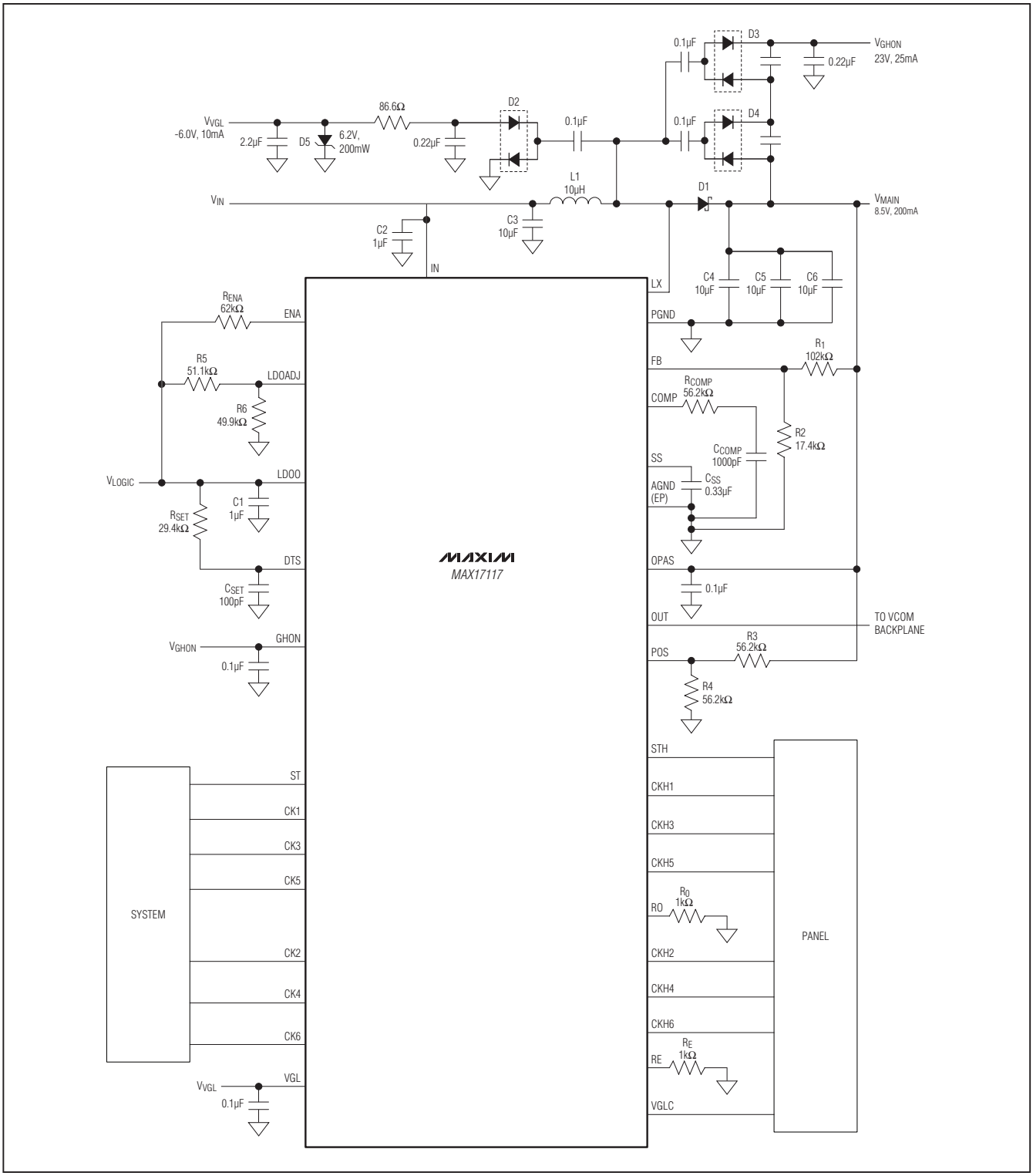


Figure 1. Typical Application Circuit

Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

Table 1. Component List

DESIGNATION	DESCRIPTION
C1, C2	1µF ±10%, 16V X5R ceramic capacitors (0603) Murata GRM188R61C105K TDK C1608X5R1C105K
C3	10µF ±10%, 10V X5R ceramic capacitor (0805) TDK C2012X5R1A106K Murata GRM21BR61A106K
C4, C5, C6	10µF ±10%, 16V X5R ceramic capacitors (1206) Murata GRM31CR61C106K TDK C3216X5R1C106K
D1	1A, 30V Schottky diode (S-Flat) Central CMMSH1-40 LEAD FREE Nihon EP10QY03 Toshiba CRS02 (TE85L, Q, M)
D2, D3, D4	200mA, 100V dual diodes (SOT23) Fairchild MMBD4148SE (Top Mark: D4) Central CMPD7000+ (Top Mark: C5C)
D5	6.2V, 200mW zener diode (SOD-323) ROHM UDZSTE-176.2B Fairchild MM3Z6V2B
L1	10µH, 1.85A, 74.4mΩ inductor (6mm x 6mm x 3mm) Sumida CDRH5D28RHPNP-100M

Typical Application Circuit

The MAX17117 typical application circuit (Figure 1) generates a +8.5V source-driver supply and approximately +23V and -6V gate-driver supplies for TFT displays. The input voltage range for the IC is from +2.3V to +5.5V, but the circuit in Figure 1 is designed to run from 2.5V to 3.6V. Table 1 lists the recommended components and Table 2 lists the component suppliers.

Detailed Description

The MAX17117 includes a high-performance step-up regulator, a 350mA low-dropout (LDO) linear regulator, a high-speed operational amplifier, and a high-voltage, level-shifting scan driver with gate-shading control. Figure 2 shows the functional diagram.

Step-Up Regulator

The step-up regulator employs a peak current-mode control architecture with a fixed 1.2MHz switching frequency that maximizes loop bandwidth and provides a fast-transient response to pulsed loads found in source drivers of TFT LCD panels. The high switching frequency allows the use of low-profile inductors and ceramic capacitors to minimize the thickness of LCD panel designs. The integrated high-efficiency MOSFET reduces the number of external components required. The output voltage can be set from V_{IN} to 15V with an external resistive voltage-divider.

Table 2. Component Suppliers

SUPPLIER	WEBSITE
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
Murata Electronics North America, Inc.	www.murata-northamerica.com
Nihon Inter Electronics Corp.	www.niec.co.jp
ROHM Co., Ltd.	www.rohm.com
Sumida Corp.	www.sumida.com
TDK Corp.	www.component.tdk.com
Toshiba America Electronic Components, Inc.	www.toshiba.com/taec

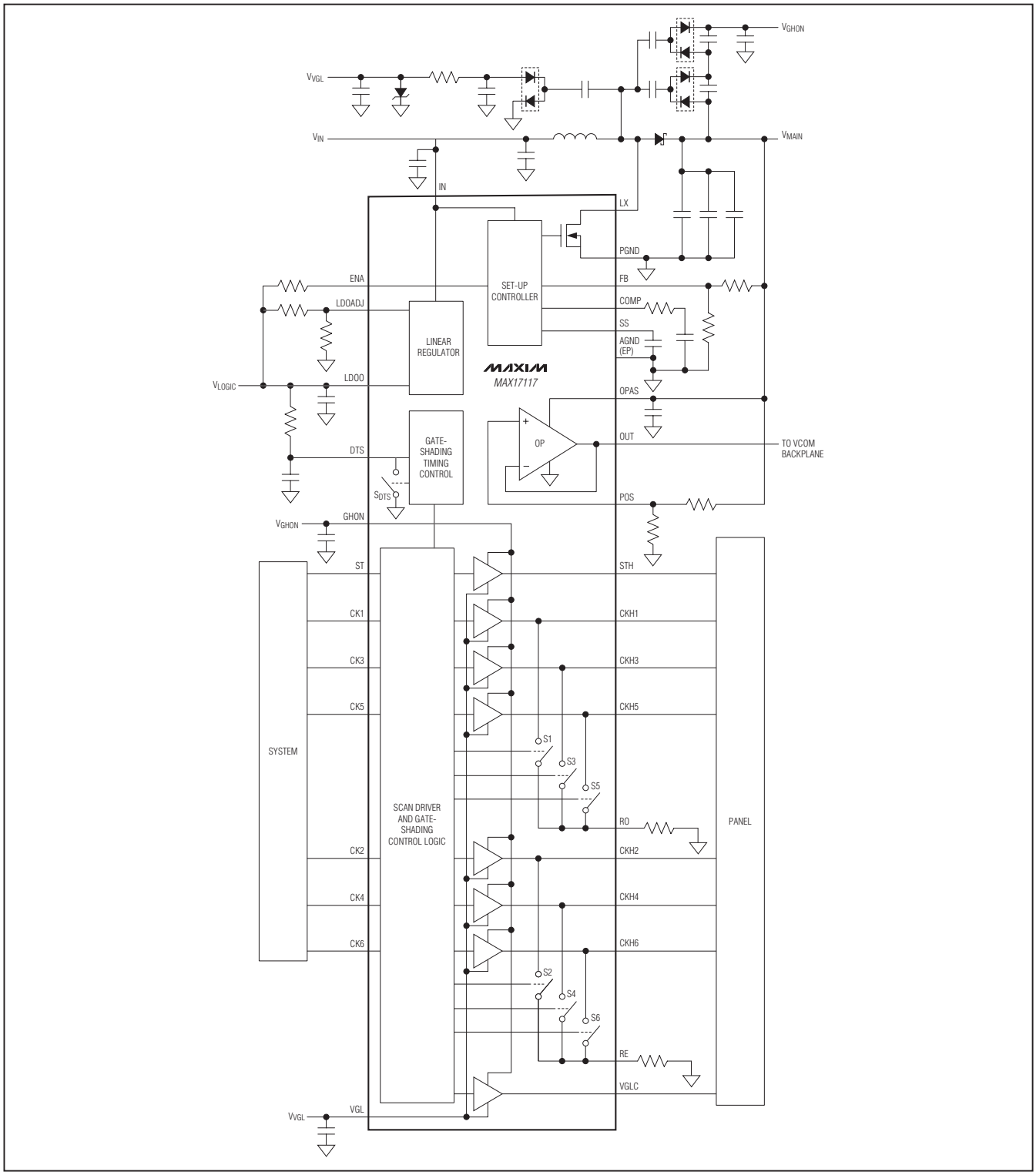


Figure 2. Functional Diagram

Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

The regulator controls the output voltage and the power delivered to the output by modulating the duty cycle (D) of the internal power MOSFET in each switching cycle. The duty cycle of the MOSFET is approximated by:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

Figure 3 shows the step-up regulator block diagram. An error amplifier compares the signal at FB to 1.24V and changes the COMP output. The voltage at COMP determines the current trip point each time the internal MOSFET turns on. As the load varies, the error amplifier sources or sinks current to the COMP output accordingly to produce the inductor peak current necessary to service the load. To maintain stability at high duty cycles, a slope compensation signal is summed with the current-sense signal.

On the rising edge of the internal clock, the controller sets a flip-flop, turning on the n-channel MOSFET and applying the input voltage across the inductor. The current through the inductor ramps up linearly, storing energy in its magnetic field. Once the sum of the current-feedback signal and the slope compensation exceed the COMP voltage, the controller resets the flip-flop and turns off the MOSFET. Since the inductor current is continuous, a transverse potential develops across the inductor that turns on the diode (D1). The voltage across the inductor then becomes the difference between the output voltage and the input voltage. This discharge condition forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and the load. The MOSFET remains off for the rest of the clock cycle.

Undervoltage Lockout (UVLO)

The UVLO circuit compares the input voltage at IN with the UVLO threshold (2.0V typ) to ensure that the input voltage is high enough for reliable operation. The 150mV (typ) hysteresis prevents supply transients from causing a restart. Once the input voltage exceeds the UVLO rising threshold, startup begins. When the input voltage falls below the UVLO falling threshold, the controller turns off the main step-up regulator.

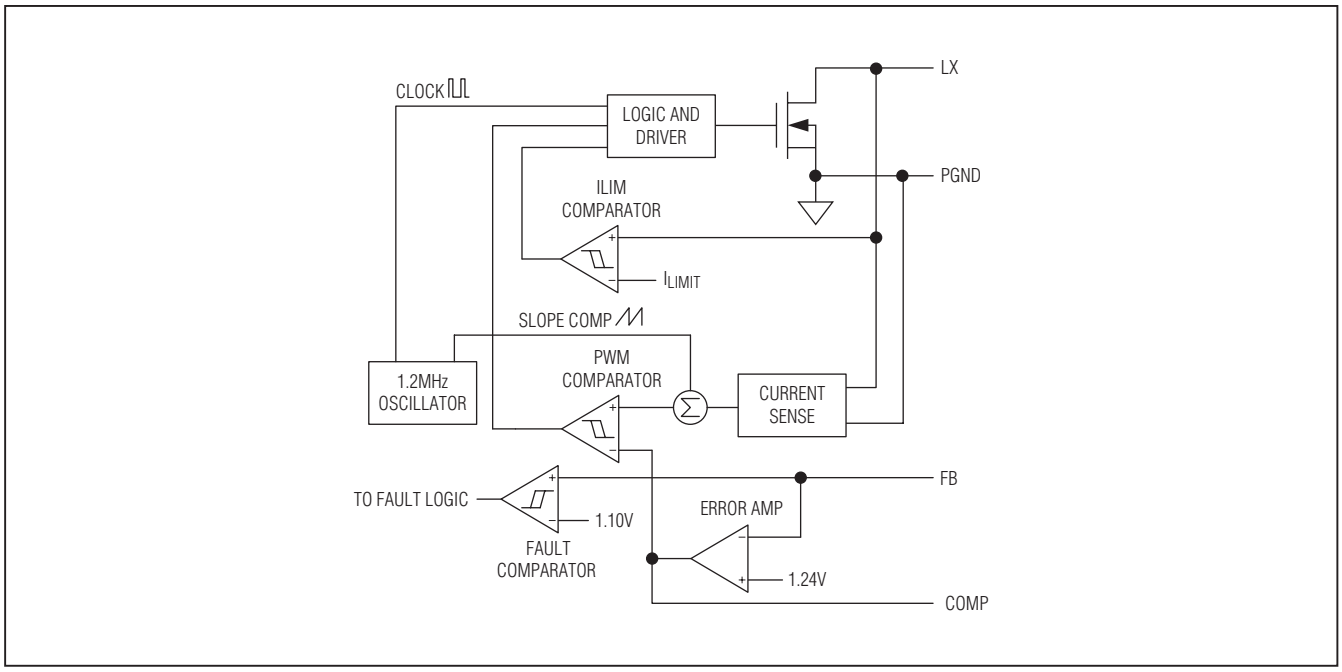


Figure 3. Step-Up Regulator Block Diagram

Overvoltage Protection

The MAX17117 monitors OPAS for an overvoltage condition. If the OPAS voltage is above 17V (typ), the MAX17117 disables the gate driver of the step-up regulator and prevents the internal MOSFET from switching. The OPAS overvoltage condition does not set the fault latch.

Overcurrent Protection

The step-up regulator features an adjustable cycle-by-cycle current limit. The inductor current is sensed through the LX switch during the LX switch on-time. If the peak inductor current rises above the current-limit threshold set by R_{ENA}, the LX switch immediately turns off until the next switching cycle, effectively limiting the peak-inductor current each cycle.

Soft-Start

The soft-start feature effectively limits the inrush current at startup by slowly raising the regulation voltage of the step-up converter's feedback pin (V_{FB}) at a rate determined by the selection of the soft-start capacitor (C_{SS}).

At startup, once ENA is pulled high through R_{ENA}, an internal 4µA (typ) current source begins to charge the soft-start capacitor (C_{SS}), slowly bringing up the voltage at the soft-start pin (V_{SS}). V_{FB} follows V_{SS} for V_{SS} < 1.24V. Once V_{SS} exceeds 1.24V, V_{FB} remains at 1.24V, allowing V_{MAIN} to reach its full regulation voltage.

Fault Protection

During steady-state operation, the MAX17117 monitors the FB voltage. If the FB voltage falls below 1.1V (typ), the MAX17117 activates an internal fault timer. If there is a continuous fault more than 160ms (typ), the MAX17117 sets the fault latch, turning off all outputs except LDOO. Once the fault condition is removed, cycle the input voltage to clear the fault latch and reactivate the device. The fault-detection circuit is disabled during the soft-start time.

Operational Amplifier

The MAX17117 has an operational amplifier that is typically used to drive the LCD backplane (VCOM) or the gamma-correction-divider string. The operational amplifier features ±200mA (typ) output short-circuit current, 40V/µs (typ) slew rate, and 16MHz (typ) bandwidth. While the op amp is a rail-to-rail input and output design, its accuracy is significantly degraded for input voltages within 1V of its supply rails (OPAS and AGND).

Short-Circuit Current Limit

The operational amplifier limits short-circuit current to approximately ±200mA (typ) if the output is directly shorted to OPAS or to AGND. If the short-circuit condition persists, the junction temperature of the IC rises until it reaches the thermal-shutdown threshold (+170°C typ). Once the junction temperature reaches the thermal-shutdown threshold, an internal thermal sensor immediately shuts down all outputs until the input voltage is cycled off, then on again.

Driving Pure Capacitive Loads

The operational amplifier is typically used to drive the LCD backplane (VOUT) or the gamma-correction-divider string. The LCD backplane consists of a distributed series capacitance and resistance, a load that can be easily driven by the operational amplifier. However, if the operational amplifier is used in an application with a pure capacitive load, steps must be taken to ensure stable operation. As the operational amplifier's capacitive load increases, the amplifier's bandwidth decreases and gain peaking increases. A 5Ω to 50Ω small resistor placed between VOUT and the capacitive load reduces peaking, but also reduces the gain. An alternative method of reducing peaking is to place a series RC network (snubber) in parallel with the capacitive load. The RC network does not continuously load the output or reduce the gain. Typical values of the resistor are between 100Ω and 200Ω and the typical value of the capacitor is 10pF.

High-Voltage Scan Driver

The high-voltage, level-shifting scan driver with gate-shading control is designed to drive the TFT panel gate drivers. Its seven outputs swing 40V (maximum) between +35V (maximum) and -15V (minimum) and can swiftly drive capacitive loads. The driver outputs (STH, CKH_) swing between their power-supply rails (GHON and VGL), according to the input logic levels on their corresponding inputs (ST, CK_) except during a gate-shading period. During a gate-shading period, a CKH_ output driver becomes high impedance and an internal switch connected between the CKH_ output's capacitive load and either RO or RE closes (S1–S6) whenever the state of its corresponding CK_ input is logic-low. This allows part of an output's GHON-to-VGL transition to be completed by partially discharging its capacitive load through an external resistor attached to either RO or RE for a duration set by the gate-shading period. See Figure 4.

Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

If the gate-shading control is enabled, a gate-shading period is initiated by a falling edge of a CK_ input whenever V_{DTS} is less than 100mV. Once the gate-shading period is initiated, a switch across C_{SET} (S_{DTS}) opens, allowing C_{SET} to be charged through R_{SET}. Once V_{DTS} reaches 1.24V, S_{DTS} closes to discharge C_{SET}, the gate-shading period is terminated, and the CKH_ output states are directly determined by their corresponding CK_ input logic states again. Once a gate-shading period is initiated, V_{DTS} must charge to 1.24V and subsequently discharge back below 100mV, before the next CK_ falling can activate a new gate-shading period.

By configuring R_{SET} and C_{SET} as shown in Figure 1, the gate-shading period time duration is determined by R_{SET} and C_{SET} and V_{LDOO} (see the *Setting the Gate-Shading Period Time Duration* section). The gate-shading control can be disabled by removing R_{SET}. If R_{SET} is removed, the states of the CKH_ outputs are always determined by their corresponding CK_ input logic states. See Figure 5.

Low-Dropout Linear Regulator (LDO)

The MAX17117 has an integrated 0.8Ω pass element and can provide at least 350mA. The output voltage is accurate within ±1%.

Thermal-Overload Protection

When the junction temperature exceeds T_J = +170°C (typ), a thermal sensor activates a fault-protection latch, which shuts down all outputs, allowing the IC to cool down. All outputs remain off until the IC cools and the input voltage is cycled below, then back above the IN UVLO threshold.

The thermal-overload protection protects the IC in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of T_J = +150°C.

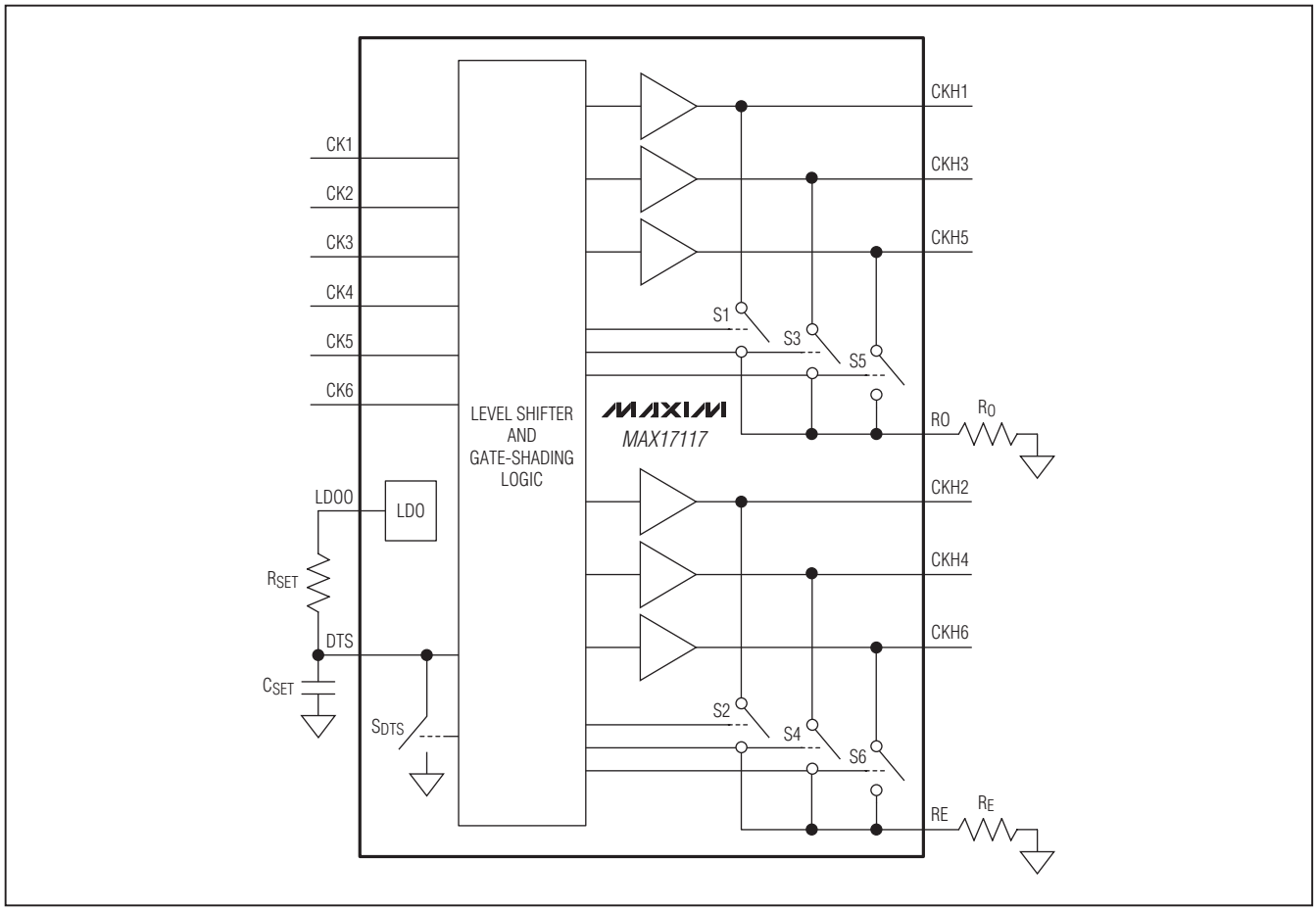


Figure 4. Scan-Driver Block Diagram

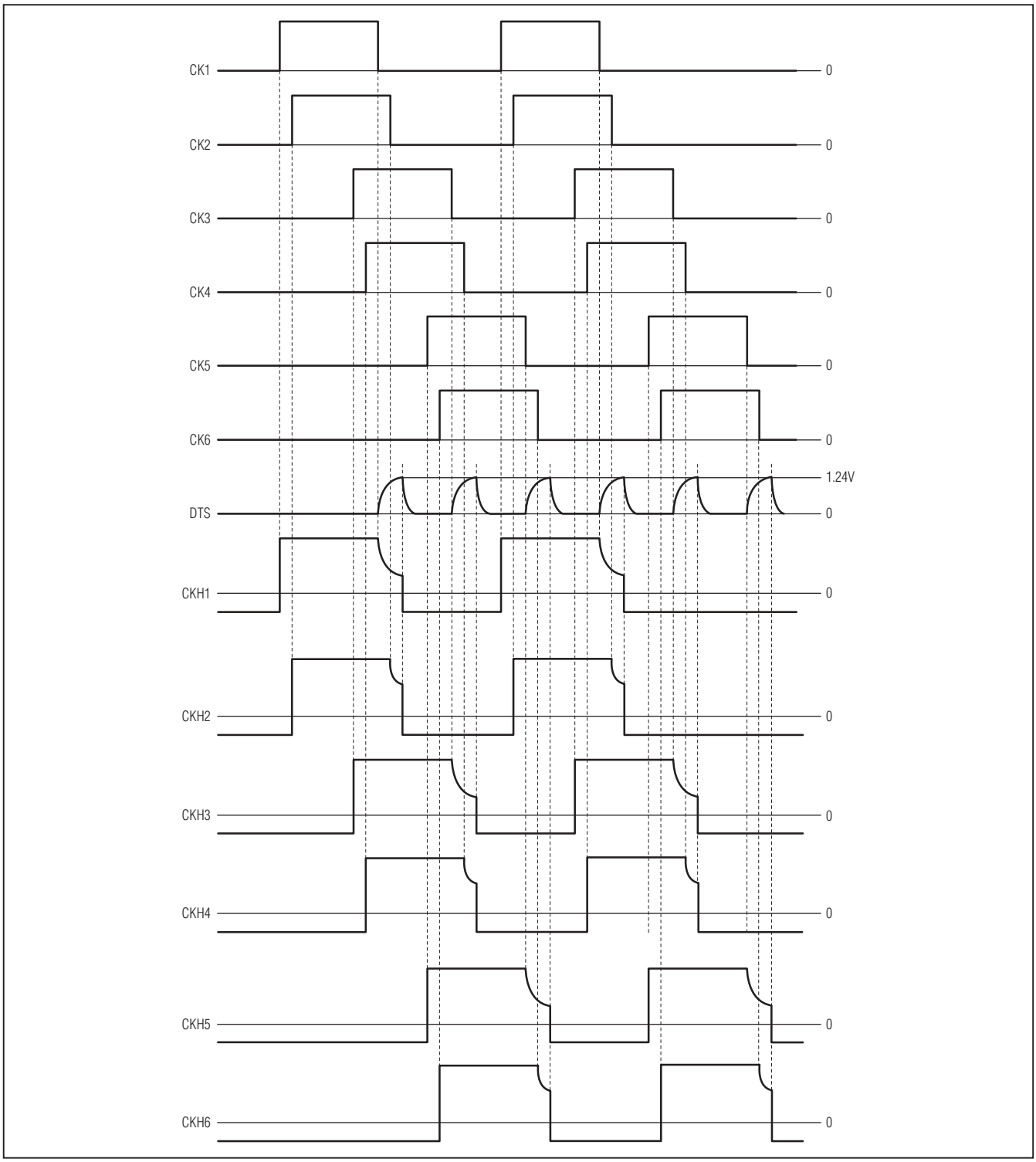


Figure 5. Scan-Driver Operation with Gate-Shading Control Enabled

Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

Design Procedure

Main Step-Up Regulator

Inductor Selection

The minimum inductance value, peak current rating, and series resistance are factors to consider when selecting the inductor. These factors influence the converter's efficiency, maximum output-load capability, transient-response time, and output-voltage ripple. Physical size and cost are also important factors to be considered.

The maximum output current, input voltage, output voltage, and switching frequency determine the inductor value. Very high-inductance values minimize the current ripple and therefore reduce the peak current, which decreases core losses in the inductor and I^2R losses in the entire power path. However, large inductor values also require more energy storage and more turns of wire, which increase physical size and can increase I^2R losses in the inductor. Low-inductance values decrease the physical size but increase the current ripple and peak current. Finding the best inductor involves choosing the best compromise among circuit efficiency, inductor size, and cost.

The equations used here include a constant called LIR, which is the ratio of the inductor peak-to-peak ripple current to the average DC inductor current at the full-load current. The best trade-off between inductor size and circuit efficiency for step-up regulators generally has an LIR between 0.3 and 0.5. However, depending on the AC characteristics of the inductor core material and ratio of inductor resistance to other power-path resistances, the best LIR can shift up or down. If the inductor resistance is relatively high, more ripple can be accepted to reduce the number of turns required and increase the wire diameter. If the inductor resistance is relatively low, increasing inductance to lower the peak current can decrease losses throughout the power path. If extremely thin high-resistance inductors are used, as is common for LCD panel applications, the best LIR can increase to between 0.5 and 1.0.

Once a physical inductor is chosen, higher and lower values of the inductor should be evaluated for efficiency improvements in typical operating regions.

In Figure 1, the LCD's gate-on and gate-off supply voltages are generated from two unregulated charge pumps driven by the step-up regulator's LX node. The additional load on LX must therefore be considered in the inductance and current calculations. The effective maximum output current, $I_{MAIN(EFF)}$, becomes the sum of the maximum load current of the step-up regulator's output plus the contributions from the positive and negative charge pumps:

$$I_{MAIN(EFF)} = I_{MAIN(MAX)} + n_{VN} \times I_{VN} + (n_{VP} + 1) \times I_{VP}$$

where $I_{MAIN(MAX)}$ is the maximum step-up output current, n_{VN} is the number of negative charge-pump stages, n_{VP} is the number of positive charge-pump stages, I_{VN} is the negative charge-pump output current, and I_{VP} is the positive charge-pump output current, assuming the initial pump source for I_{VP} is V_{MAIN}.

Calculate the approximate inductor value using the typical input voltage (V_{IN}), the maximum output current ($I_{MAIN(EFF)}$), the expected efficiency (η_{TYP}) taken from an appropriate curve in the *Typical Operating Characteristics*, the desired switching frequency (f_{OSC}), and an estimate of LIR based on the above discussion:

$$L = \left(\frac{V_{IN}}{V_{MAIN}}\right)^2 \left(\frac{V_{MAIN} - V_{IN}}{I_{MAIN(EFF)} \times f_{OSC}}\right)\left(\frac{\eta_{TYP}}{LIR}\right)$$

Choose an available inductor value from an appropriate inductor family. Calculate the maximum DC input current at the minimum input voltage $V_{IN(MIN)}$ using conservation of energy and the expected efficiency at that operating point (η_{MIN}) taken from an appropriate curve in the *Typical Operating Characteristics*:

$$I_{IN(DC,MAX)} = \frac{I_{MAIN(EFF)} \times V_{MAIN}}{V_{IN(MIN)} \times \eta_{MIN}}$$

Calculate the ripple current at that operating point and the peak current required for the inductor:

$$I_{RIPPLE} = \frac{V_{IN(MIN)} \times \left(V_{MAIN} - V_{IN(MIN)}\right)}{L \times V_{MAIN} \times f_{OSC}}$$

$$I_{PEAK} = I_{IN(DC,MAX)} + \frac{I_{RIPPLE}}{2}$$

The inductor's saturation current rating and the MAX17117 LX current limit should exceed I_{PEAK} and the inductor's DC current rating should exceed $I_{IN(DC,MAX)}$. For good efficiency, choose an inductor with less than 0.1Ω series resistance.

Considering the typical application circuit, the maximum load current ($I_{MAIN(MAX)}$) is 200mA, with an 8.5V output and a typical input voltage of 3.3V. The effective full-load step-up current is:

$$I_{MAIN(EFF)} = 200mA + 1 \times 10mA + (2 + 1) \times 25mA = 285mA$$

Choosing an LIR of 0.2 and estimating efficiency of 85% at this operating point:

$$L = \left(\frac{3.3V}{8.5V}\right)^2 \left(\frac{8.5V - 3.3V}{0.285A \times 1.2MHz}\right)\left(\frac{0.85}{0.2}\right) \approx 9.7\mu H$$

A 10µH inductor is chosen. Then, using the circuit's minimum input voltage (3.0V) and estimating efficiency of 83% at that operating point:

$$I_{IN(DC,MAX)} = \frac{0.285A \times 8.5V}{3V \times 0.83} \approx 0.973A$$

The ripple current and the peak current at that input voltage are:

$$I_{RIPPLE} = \frac{3V \times (8.5V - 3V)}{10\mu H \times 8.5V \times 1.2MHz} \approx 0.162A$$

$$I_{PEAK} = 0.973A + \frac{0.162A}{2} = 1.05A$$

Peak Inductor Current-Limit Setting

Connecting R_{ENA} between the ENA pin and the LDOO output, as shown in Figure 1, allows the inductor peak current limit to be adjusted up to 2A max by choosing the appropriate R_{ENA} resistor with the following equation:

$$R_{ENA} \approx \frac{(V_{LDOO} - 1.25V)(80000)}{I_{OCP}}$$

The above threshold set by R_{ENA} varies depending on the step-up converter's input voltage, output voltage, and duty cycle. Place R_{ENA} close to the IC such that the connection between R_{ENA} and the ENA pin is as short as possible.

Output Capacitor Selection

The total output-voltage ripple has two components: the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{MAIN}}{C_{OUT}}\left(\frac{V_{MAIN} - V_{IN}}{V_{MAIN} f_{OSC}}\right)$$

and:

$$V_{RIPPLE(ESR)} \approx I_{PEAK} R_{ESR(COUT)}$$

where I_{PEAK} is the peak inductor current (see the *Inductor Selection* section). For ceramic capacitors, the output-voltage ripple is typically dominated by $V_{RIPPLE(C)}$. The voltage rating and temperature characteristics of the output capacitor must also be considered.

Input-Capacitor Selection

The input capacitor (C3) reduces the current peaks drawn from the input supply and reduces noise injection into the IC. A 10µF ceramic capacitor is used in the typical application circuit (Figure 1) because of the high source impedance seen in typical lab setups. Actual applications usually have much lower source impedance since the step-up regulator often runs directly from the output of another regulated supply.

Rectifier Diode

The MAX17117 high switching frequency demands a high-speed rectifier. Schottky diodes are recommended for most applications because of their fast recovery time and low forward voltage. In general, a 1A Schottky diode complements the internal MOSFET well.

Output-Voltage Selection

The output voltage of the main step-up regulator is adjusted by connecting a resistive voltage-divider from the output (V_{MAIN}) to AGND with the center tap connected to FB (see Figure 1). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equation:

$$R1 = R2 \times \left(\frac{V_{MAIN}}{V_{REF}} - 1\right)$$

Place R1 and R2 close to the IC such that the connections between these components and the FB pin are kept as short as possible.

Loop Compensation

Choose R_{COMP} to set the high-frequency integrator gain for fast-transient response. Choose C_{COMP} to set the integrator zero to maintain loop stability.

For low-ESR output capacitors, use the following equations to obtain stable performance and good transient response:

$$R_{COMP} \approx \frac{1.45k \times V_{IN} \times V_{MAIN} \times C_{OUT}}{L \times I_{MAIN(MAX)}}$$

$$C_{COMP} \approx \frac{40 \times V_{MAIN} \times L \times I_{MAIN(MAX)}}{(V_{IN})^2 \times R_{COMP}}$$

To further optimize transient response, vary R_{COMP} in 20% steps and C_{COMP} in 50% steps while observing transient-response waveforms.

Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

Operational Amplifier Output Voltage

Using the buffer configuration as shown in Figure 1, the output voltage of the operational amplifier is adjusted by connecting a resistive voltage-divider from the output (V_{MAIN}) to AGND with the center tap connected to POS (see Figure 1). Select R3 in the 10kΩ to 100kΩ range. Calculate R4 with the following equation:

$$R3 = R4 \times \left(1 - \frac{V_{MAIN}}{V_{OUT}}\right)$$

Place R3 and R4 close to the IC such that the connections between these components and the POS pin are kept as short as possible.

LDO Output Voltage

The output voltage of the LDO is adjusted by connecting a resistive voltage-divider from the output (V_{LDOO}) to AGND with the center tap connected to LDOADJ (see Figure 1). Select R6 in the 10kΩ to 50kΩ range. Calculate R5 with the following equation:

$$R5 = R6 \times \left(\frac{V_{LDOO}}{1.24V} - 1\right)$$

Place R5 and R6 close to the IC such that the connections between these components and the LDOADJ pin are kept as short as possible.

Connect a 1µF low ESR capacitor between LDOO and AGND to ensure stability and to provide good output-transient performance.

Scan Driver

Setting the Gate-Shading Period Time Duration

To set the gate-shading period time duration, configure R_{SET} and C_{SET} as shown in Figure 1. Choose a C_{SET} value greater than 35pF, then calculate the required R_{SET} value that gives the desired gate-shading period time duration with the following equation:

$$R_{SET} = \frac{-t}{\ln\left(1 - \frac{1.24V}{V_{LDOO}}\right) \times C_{SET}}$$

Increase or decrease C_{SET} as needed and repeat the above calculation to achieve the desired gate-shading period time duration, while ensuring C_{SET} remains greater than 35pF and R_{SET} is within the 8kΩ to 100kΩ range.

Place R_{SET} and C_{SET} close to the IC such that the connections between these components and the DTS pin are kept as short as possible.

Gate-Shading Discharge Resistors

For proper operation, choose R_O and R_E discharge resistors that are greater than 100Ω. Place R_O and R_E close to the IC such that the connections between these components and their respective pins are kept as short as possible.

Applications Information

Power Dissipation

An IC's maximum power dissipation depends on the thermal resistance from the die to the ambient environment and the ambient temperature. The thermal resistance depends on the IC package, PCB copper area, other thermal mass, and airflow.

The MAX17117, with its exposed backside paddle soldered to 1in² of PCB copper, can dissipate approximately 1990mW into +70°C still air. More PCB copper, cooler ambient air, and more airflow increase the possible dissipation, while less copper or warmer air decreases the IC's dissipation capability. The major components of power dissipation are the power dissipated in the step-up regulator and the power dissipated by the operational amplifiers.

The MAX17117's largest on-chip power dissipation occurs in the step-up switch, the VCOM amplifier, the CKH_ level shifters, and the LDO.

Step-Up Regulator

The largest portions of the power dissipated by the step-up regulator are the internal MOSFET, the inductor, and the output diode. If the step-up regulator with 3.3V input and 285mA output has approximately 85% efficiency, approximately 5% of the power is lost in the internal MOSFET, approximately 3% in the inductor, and approximately 5% in the output diode. The remaining few percent are distributed among the input and output capacitors and the PCB traces. If the input power is approximately 2.85W, the power lost in the internal MOSFET is approximately 143mW.

Operational Amplifier

The power dissipated in the operational amplifier depends on the output current, the output voltage, and the supply voltage:

$$PD_{SOURCE} = I_{VCOM\_SOURCE} \times (V_{AVDD} - V_{VCOM})$$

$$PD_{SINK} = I_{VCOM\_SINK} \times V_{VCOM}$$

where I_{VCOM_SOURCE} is the output current sourced by the operational amplifier, and I_{VCOM_SINK} is the output current that the operational amplifier sinks. In a typical

case where the supply voltage is 8.5V and the output voltage is 4.25V with an output source current of 30mA, the power dissipated is 128mW.

LDO

The power dissipated in the LDO depends on the LDO's output current, input voltage, and output voltage:

$$PD_{LDO} = I_{LDOO} \times (V_{IN} - V_{LDOO})$$

Scan-Driver Outputs

The power dissipated by the six CKH_ scan-driver outputs depends on the scan frequency, the capacitive load on each output, and the difference between the GHON and VGL supply voltages:

$$PD_{SCAN} = 6 \times f_{SCAN} \times C_{PANEL} \times (V_{GHON} - V_{VGL})^2$$

If the scan frequency is 50kHz, the load of the six CKH_ outputs is 3.4nF, and the supply voltage difference is 30V, then the power dissipated is 0.92W.

PCB Layout and Grounding

Careful PCB layout is important for proper operation. Use the following guidelines for good PCB layout:

- Minimize the area of high-current loops by placing the inductor, output diode, and output capacitors near the input capacitors and near LX and PGND. The high-current input loop goes from the positive terminal of the input capacitor to the inductor, to the IC's LX pin, out of PGND, and to the input capacitor's negative terminal. The high-current output loop is from the positive terminal of the input capacitor to the inductor, to the output diode (D1), to the positive terminal of the output capacitors, reconnecting between the output capacitor and input capacitor ground terminals. Connect these loop components with short, wide connections. Avoid using vias in the high-current paths. If vias are unavoidable, use many vias in parallel to reduce resistance and inductance.
- Create a power ground island (PGND) consisting of the input and output capacitor grounds, PGND pin, and any charge-pump components. Connect all these together with short, wide traces or a small ground plane. Maximizing the width of the power ground traces improves efficiency and reduces output-voltage ripple and noise spikes. Create an analog ground plane (AGND) consisting of all the feedback-divider ground connections; the operational-amplifier-divider ground connection; the OPAS bypass capacitor ground connection; the COMP, SS, and SET capacitor ground connections; and the device's exposed backside pad. Connect the AGND and PGND islands by connecting the PGND pin directly to the exposed backside pad. Make no other connections between these separate ground planes.
- Place the feedback voltage-divider resistors as close as possible to their respective feedback pins. The divider's center trace should be kept short. Placing the resistors far away causes the feedback trace to become an antenna that can pick up switching noise. Care should be taken to avoid running the feedback trace near LX or the switching nodes in the charge pumps.
- Place the IN pin bypass capacitor as close as possible to the device. The ground connections of the IN bypass capacitor should be connected directly to AGND at the backside pad of the IC.
- Minimize the length and maximize the width of the traces between the output capacitors and the load for best transient responses.
- Minimize the size of the LX node while keeping it wide and short. Keep the LX node away from the feedback node and analog ground. Use DC traces as a shield if necessary.

Refer to the MAX17117 Evaluation Kit for an example of proper board layout.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
32 TQFN-EP	T3255N+1	21-0140

Internal-Switch Boost Regulator with Integrated 7-Channel Scan Driver, Op Amp, and LDO

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/10	Initial release	—