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MAX17201/MAX17205/ MAX17211/MAX17215

Stand-Alone ModelGauge m5 Fuel Gauge with SHA-256 Authentication

General Description

The MAX1720x/MAX1721x are ultra-low power stand-alone fuel gauge ICs that implement the Maxim ModelGauge™ m5 algorithm without requiring host interaction for configuration. This feature makes the MAX1720x/MAX1721x excellent pack-side fuel gauges. The MAX17201/MAX17211 monitor a single cell pack. The MAX17205/MAX17215 monitor and balance a 2S or 3S pack or monitor a multiple-series cell pack.

To prevent battery pack cloning, the ICs integrate SHA-256 authentication with a 160-bit secret key. Each IC incorporates a unique 64-bit ID.

The ModelGauge™ m5 algorithm combines the short-term accuracy and linearity of a coulomb counter with the long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel gauge accuracy. The IC automatically compensates for cell aging, temperature, and discharge rate, and provides accurate state of charge (SOC) in milliampere-hours (mAh) or percentage (%) over a wide range of operating conditions. As the battery approaches the critical region near empty, the ModelGauge m5 algorithm invokes a special error correction mechanism that eliminates any error. The ICs provide accurate estimation of time-to-empty and time-to-full, Cycle+™ age forecast, and three methods for reporting the age of the battery: reduction in capacity, increase in battery resistance, and cycle odometer.

The ICs provide precision measurements of current, voltage, and temperature. Temperature of the battery pack is measured using an internal temperature measurement and up to two external thermistors supported by ratiometric measurements on auxiliary inputs. A Maxim 1-Wire® (MAX17211/MAX17215) or 2-wire I²C (MAX17201/MAX17205) interface provides access to data and control registers. The ICs are available in lead-free, 3mm x 3mm, 14-pin TDFN and 1.6mm x 2.4mm 15-bump WLP packages.

Applications

- Smartphones and Tablets
- Portable Game Players
- e-Readers
- Digital Still and Video Cameras
- Handheld Computers and Terminals
- Portable Medical Equipment
- Handheld Radios

Benefits and Features

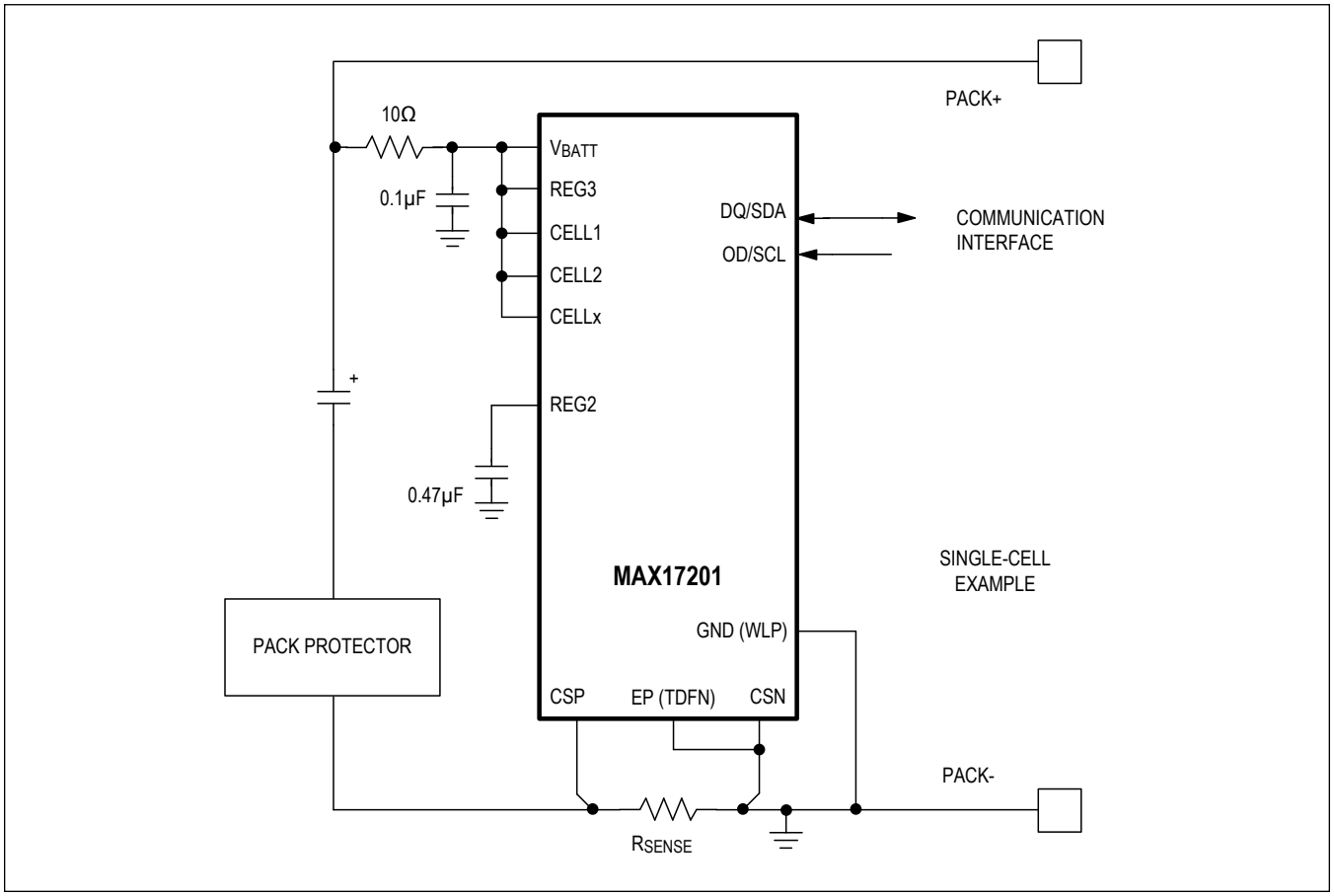
- ModelGauge m5 Algorithm
  - Eliminates Error when Approaching Empty Voltage
  - Eliminates Coulomb-Counter Drift
  - Current, Temperature, and Age Compensated
  - Does Not Require Empty, Full, or Idle States
  - No Characterization Required for EZ Performance (See the *ModelGauge m5 EZ Performance* Section)
  - Cycle+ Age Forecasting Observes Lifespan
- Nonvolatile Memory for Stand-Alone Operation
  - Learned Parameters and History Logging
  - Up to 75 Words Available for User Data
- Precision Measurement System
  - No Calibration Required
- Time-to-Empty and Time-to-Full Estimation
- Temperature Measurement
  - Die Temperature
  - Up to Two External Thermistors
- Multiple Series Cell Pack Operation
- Low Quiescent Current
  - MAX172x1: 18µA Active, 9µA Hibernate
  - MAX172x5: 25µA Active, 12µA Hibernate
- Alert Indicator for Voltage, SOC, Temperature, Current, and 1% SOC Change
- High-Speed Overcurrent Comparators
- Predicts Remaining Capacity Under Theoretical Load
- SHA-256 Authentication
- Maxim 1-Wire or 2-Wire (I²C) Interface
- SBS 1.1 Compatible Register Set

***Ordering Information* appears at end of data sheet.**

19-8424; Rev 2; 8/16

maxim integrated™

Simplified Block Diagram



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Absolute Maximum Ratings (TDFN)

V_{BATT} to CSN (MAX17201/MAX17211).....-0.3V to +6V
V_{BATT} to CSN (MAX17205/MAX17215).....-0.3V to +22V
ALRT1 to CSN.....-0.3V to +17V
CELL1 to CSN..... -0.3V to V_{CELL2} + 0.3V
CELL2 to CELL1 ..... -0.3V to V_{BATT} + 0.3V
REG3 to V_{BATT} (MAX17201/MAX17211) ..... 0V to 0V
REG3 to CSN (MAX17205/MAX17215).....-0.3V to +6V
AIN1, AIN2 to CSN.....-0.3V to +6V
THRM, CELLx to CSN ..... -0.3V to V_{REG3} + 0.3V
REG2 to CSN.....-0.3V to +2.2V
CSP to CSN .....-2V to +2V
DQ/SDA, OD/SCL to CSN.....-0.3V to +6V
Continuous Source Current for THRM.....20mA
Continuous Sink Current for DQ/SDA, ALRT1.....20mA
Continuous Sink Current for BATT, CELL1, CELL2.....50mA
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Absolute Maximum Ratings (WLP)

V_{BATT} to GND (MAX17201/MAX17211) .....-0.3V to +6V
V_{BATT} to GND (MAX17205/MAX17215).....-0.3V to +22V
ALRT1 to GND .....-0.3V to +17V
CELL1 to GND ..... -0.3V to V_{CELL2} + 0.3V
CELL2 to CELL1 ..... -0.3V to V_{BATT} + 0.3V
REG3 to V_{BATT} (MAX17201/MAX17211) ..... 0V to 0V
REG3 to GND (MAX17205/MAX17215) .....-0.3V to +6V
AIN1, AIN2 to GND .....-0.3V to +6V
THRM, CELLx to GND..... -0.3V to V_{REG3} + 0.3V
REG2 to GND.....-0.3V to +2.2V
CSP to GND .....-2V to +2V
DQ/SDA, OD/SCL to GND .....-0.3V to +6V
Continuous Source Current for THRM.....20mA
Continuous Sink Current for DQ/SDA, ALRT1.....20mA
Continuous Sink Current for BATT, CELL1, CELL2.....50mA
Operating Temperature Range..... -40°C to +85°C
Storage Temperature Range..... -55°C to +125°C
Lead Temperature (soldering 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

14 TDFN-EP

Package Code	T1433+2C
Outline Number	**21-0137**
Land Pattern Number	**90-0063**
Thermal Resistance, Single Layer Board:	
Junction-to-Ambient (θ_{JA})	54°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8°C/W

15 WLP

Package Code	W151F2+1
Outline Number	21-100072
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	62°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{BATT} = 2.3V to 4.9V (MAX17201/MAX17211) 4.2V to 20V (MAX17205/MAX17215), T_A = -40°C to 85°C, unless otherwise noted. Typical values are T_A = +25°C. See Figure 1, Figure 2, and Figure 3. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{BATT}	MAX17201/MAX17211 (Notes 1, 2)	2.3		4.9	V
		MAX17205/MAX17215 (Notes 1, 2)	4.2		20	
Startup Voltage	V_{BATT}	MAX17201/MAX17211 (Note 1)		2.85	3.0	V
Shutdown Supply Current	I_{DD0}	Single cell, shutdown mode (Note 3)		0.7	1.5	µA
		Multiple cell, shutdown mode (Note 3)		1.5	3.0	
Hibernate Supply Current	I_{DD1}	Hibernate mode average current, single cell (Note 3)		9	20	µA
		Hibernate mode average current, multiple cell (Note 3)		12	25	
Active Supply Current	I_{DD2}	MAX17201/MAX17211, not including thermistor measurement current (Note 3)		18	35	µA
		MAX17205/1MAX17215, not including thermistor measurement current (Note 3)		25	40	
Regulation Voltage	V_{REG2}			1.8		V
	V_{REG3}	MAX17205/MAX17215 only		3.4		
ANALOG-TO-DIGITAL CONVERSION						
Voltage Measurement Error	V_{GERR}	T_A = +25°C (Note 4)	-12.5		+12.5	mV
		(Note 4)	-25		+25	
		T_A = +25°C (Note 5)	-12.5		+12.5	
		(Note 5)	-25		+25	
	VB_{GERR}	T_A = +25°C (Note 6)	-30		+30	
		(Note 6)	-100		+100	
	VX_{GERR}	T_A = +25°C (Note 7)	-0.2		+0.2	% of Reading
		(Note 7)	-0.5		+0.5	
Voltage Measurement Resolution	V_{LSB}	Individual cell		78.125		µV
	VB_{LSB}	V_{BATT} pin		1.25		mV
	VX_{LSB}	CELLx pin		78.125		µV
Voltage Measurement Range	V_{FS}	Individual cell	2.3		4.9	V
	VB_{FS}	V_{BATT} pin	4.2		20.0	
	VX_{FS}	CELLx pin	0.92		2.0	
Current Measurement Offset Error	I_{OERR}	V_{CSP} = 0V, long-term average (Note 2)	-2.0	-0.7	+0.5	µV
Current Measurement Gain Error	I_{GERR}	CSP between -50mV and +50mV	-1		+1	% of reading
Current Measurement Resolution	I_{LSB}			1.5625		µV

Electrical Characteristics (continued)

(V_{BATT} = 2.3V to 4.9V (MAX17201/MAX17211) 4.2V to 20V (MAX17205/MAX17215), T_A = -40°C to 85°C, unless otherwise noted. Typical values are T_A = +25°C. See Figure 1, Figure 2, and Figure 3. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Current Measurement Range	I_{FS}			±51.2		mV
Internal Temperature Measurement Error	TI_{GERR}			±1		°C
Internal Temperature Measurement Resolution	TI_{LSB}	AIN1, AIN2 (Note 1)		0.00391		°C
Auxiliary Ratiometric Measurement Error	TE_{GERR}		-0.5		+0.5	% of reading
Auxiliary Ratiometric Measurement Resolution	TE_{LSB}			0.001526		%
INPUT/OUTPUT						
Output Drive High, THRM	V_{OH}	I_{OH} = -1mA, V_{REG3} = 2.3V	V_{REG3} - 0.1			V
Output Drive Low, ALRT1, SDA/DQ	V_{OL}	I_{OL} = 4mA, V_{REG3} = 2.3V			0.4	V
Input Logic-High, SCL/OD, SDA/DQ	V_{IH}		1.5			V
Input Logic-Low, SCL/OD, SDA/DQ	V_{IL}				0.44	V
Battery-Detach Detection Threshold	V_{DET}	AIN1 as a fraction of the voltage of THRM, AIN1 rising (Note 1)	91	95	99	%
Battery-Detach Detection Threshold Hysteresis	$V_{DET-HYS}$	AIN1 falling		1		%
Battery-Detach Comparator Delay	t_{TOFF}	AIN1 step from 70% to 100% of THRM voltage to ALRT1 falling, Config register AIrtp = 0, Ber = 1, FTHRM = 1			100	µs
COMPARATORS						
Overcurrent Threshold Offset Error	OC_{OE}	OD or SC comparator	-2.5		+2.5	mV
Overcurrent Threshold Gain Error	OC_{GE}	OD or SC comparator	-5.0		+5.0	% of threshold
Over Current Comparator Delay	OC_{DLY}	OD or SC comparator, 20mV minimum input overdrive, delay configured to minimum		2		µs
RESISTANCE AND LEAKAGE						
Leakage Current, AIN1, AIN2	I_{LEAK}	AIN1, AIN2 < REG3	-0.2		0.2	µA
Leakage Current, CELLx	I_{LEAK}	V_{CELLx} < 2.0V (Note 2)	-60	±5	+60	nA

Electrical Characteristics (continued)

(V_{BATT} = 2.3V to 4.9V (MAX17201/MAX17211) 4.2V to 20V (MAX17205/MAX17215), T_A = -40°C to 85°C, unless otherwise noted. Typical values are T_A = +25°C. See Figure 1, Figure 2, and Figure 3. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Leakage Current, CELL1, CELL2, CSN, CSP, ALRT1, THRM	I_{LEAK}	V_{ALRT1} < 15V, THRM < REG3	-1		+1	µA
Input Resistance, CELL2, CELL1, CSP	R_{VAD}	Resistance during voltage sampling (Note 15)		1		MΩ
Input Resistance, CELLx	R_{CELLx}			400		MΩ
Cell-Balancing Resistance	R_{BAL}	V_{BATT} = 12.6V, I_{BAL} = 50mA, between V_{BATT}-CELL2, CELL2-CELL1, and CELL1-CSN (TDFN) or CELL1-GND (WLP)	3	9	20	Ω
Input Pulldown Current	I_{PD}	V_{SDA}, V_{SCL} pins = 0.4V	0.05	0.2	0.4	µA
TIMING						
Time-Base Accuracy	t_{ERR}	T_A= +25°C	-1		+1	%
SHA Calculation Time	t_{SHA}			4.5	10	ms
THRM Precharge Time	t_{PRE}	Time between turning on the THRM pullup and AIN1 or AIN2 analog-to-digital conversions	8.48			ms
Power-on-Reset Time	t_{POR}	(Note 2)			10	ms
Task Period	t_{TP}			351.5		ms
NONVOLATILE MEMORY						
Nonvolatile Access Voltage	V_{NVM}	For block programming and recalling, applied on V_{BATT} (MAX17201/MAX17211)	3.0			V
		For block programming and recalling, applied on V_{BATT} (MAX17205/MAX17215)	4.2			
Programming Supply Current	I_{PROG}	Current from V_{BATT} for block programming		4	10	mA
Block Programming Time	t_{BLOCK}			368	7360	ms
Page Programming Time	t_{UPDATE}	SHA secret update or learned parameters update		64	1280	ms
Nonvolatile Memory Recall Time	t_{RECALL}				5	ms
Write Capacity, Configuration Memory	n_{CONFIG}	(Notes 2, 8, 9)		7		writes
Write Capacity, SHA Secret	n_{SECRET}	(Notes 2, 8, 9)		5		writes
Write Capacity, Learned Parameters	$n_{LEARNED}$	(Notes 2, 8, 9)		202		writes
Data Retention	t_{NV}	(Note 2)	10			years

Electrical Characteristics (continued)

(V_{BATT} = 2.3V to 4.9V (MAX17201/MAX17211) 4.2V to 20V (MAX17205/MAX17215), T_A = -40°C to 85°C, unless otherwise noted. Typical values are T_A = +25°C. See Figure 1, Figure 2, and Figure 3. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
1-WIRE INTERFACE, REGULAR SPEED						
Time Slot	t_{SLOT}		60		120	µs
Recovery Time	t_{REC}		1			µs
Write-0 Low Time	t_{LOW0}		60		120	µs
Write-1 Low Time	t_{LOW1}		1		15	µs
Read-Data Valid	t_{RDV}				15	µs
Reset-Time High	t_{RSTH}		480			µs
Reset-Time Low	t_{RSTL}		480			µs
Presence-Detect High	t_{PDH}		15		60	µs
Presence-Detect Low	t_{PDL}		60		240	µs
1-WIRE INTERFACE, OVERDRIVE SPEED						
Time Slot	t_{SLOT}		6		16	µs
Recovery Time	t_{REC}		1			µs
Write-0 Low Time	t_{LOW0}		6		16	µs
Write-1 Low Time	t_{LOW1}		1		2	µs
Read-Data Valid	t_{RDV}				2	µs
Reset-Time High	t_{RSTH}		48			µs
Reset-Time Low	t_{RSTL}		48			µs
Presence-Detect High	t_{PDH}		2		6	µs
Presence-Detect Low	t_{PDL}		8		24	µs
2-WIRE INTERFACE						
SCL Clock Frequency	f_{SCL}	(Note 10)	0		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(Note 11)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 12, 13)	0		0.9	us
Data Setup Time	$t_{SU:DAT}$	(Note 12)	100			ns
Rise Time of Both SDA and SCL Signals	t_R		5		300	ns

Electrical Characteristics (continued)

(V_{BATT} = 2.3V to 4.9V (MAX17201/MAX17211) 4.2V to 20V (MAX17205/MAX17215), T_A = -40°C to 85°C, unless otherwise noted. Typical values are T_A = +25°C. See Figure 1, Figure 2, and Figure 3. Limits are 100% tested at T_A = +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.)

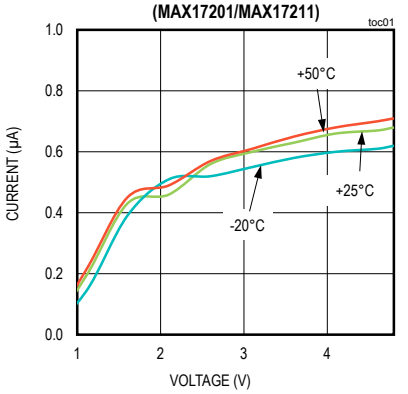
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Fall Time of Both SDA and SCL Signals	t_F		5		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Width Suppressed by Input Filter	t_{SP}	(Note 14)			50	ns
Capacitive Load for Each Bus Line	C_B				400	pF
SCL, SDA Input Capacitance	C_{BIN}			6		pF

Note 1: All voltages are referenced to CSN in the TDFN package. All voltages are referenced to GND in the WLP package.
Note 2: Specification is guaranteed by design (GBD), and not production tested.
Note 3: T_A < +50°C, V_{BATT} = 4.9V for single cell or 20V for multiple cell.
Note 4: Single cell, CELL1 to CSP cell voltage between 2.3V and 4.9V.
Note 5: Multiple cell, V_{BATT} to CELL2, CELL2 to CeLL1, or CELL1 to CSP, cell voltages between 2.3V and 4.9V; for voltages between 2.3V and 4.9V; for two cells, CELL2 must be shorted to CELL1.
Note 6: Multiple cell, total V_{BATT} voltage, V_{BATT} = 4.2V to 20V.
Note 7: The MAX17205/MAX17215 only CELLx to CSP, per cell voltage of 2.3V to 4.9V.
Note 8: Write capacity numbers shown have one write subtracted for the initial write performed during manufacturing test to set nonvolatile memory to a known value.
Note 9: Due to the nature of one-time programmable memory, write capacity cannot be production tested. Follow the nonvolatile memory and SHA secret update procedures detailed in the data sheet.
Note 10: Timing must be fast enough to prevent the IC from entering shutdown mode due to bus low for a period greater than the shutdown timer setting.
Note 11: f_{SCL} must meet the minimum clock low time plus the rise/fall times.
Note 12: The maximum $t_{HD:DAT}$ has only to be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.
Note 13: This device internally provides a hold time of at least 100ns for the SDA signal (referred to the minimum V_{IH} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
Note 14: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.
Note 15: Resistance is measured to CSN in the TDFN package. Resistance is measured to GND in the WLP package.

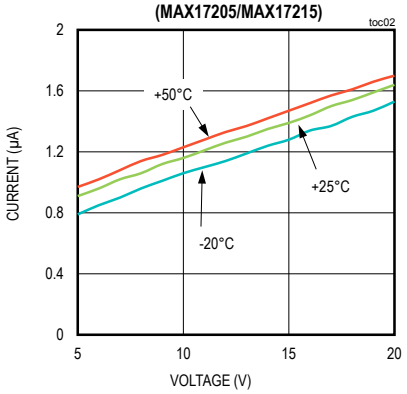
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

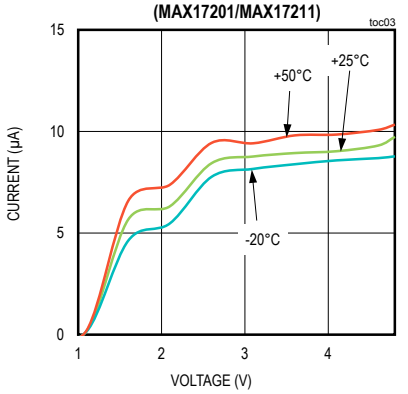
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE
(MAX17201/MAX17211)



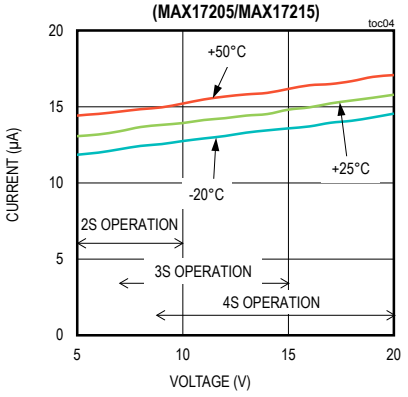
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE
(MAX17205/MAX17215)



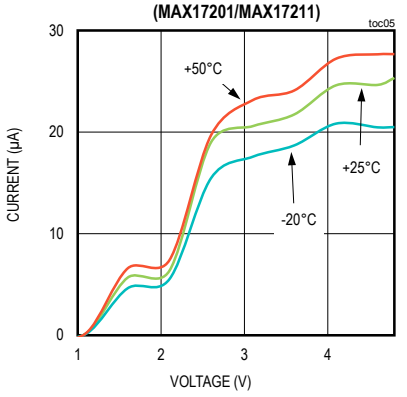
HIBERNATE CURRENT vs. SUPPLY VOLTAGE
(MAX17201/MAX17211)



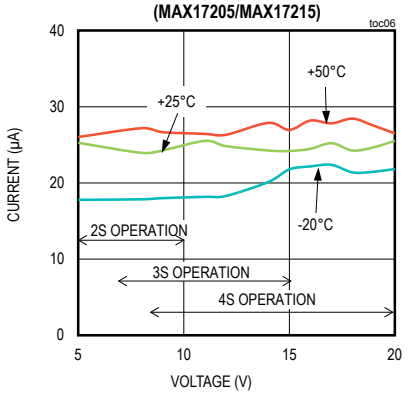
HIBERNATE CURRENT vs. SUPPLY VOLTAGE
(MAX17205/MAX17215)



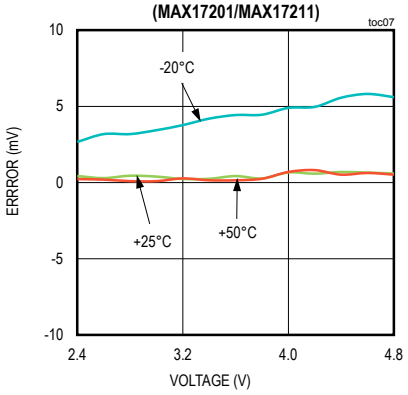
ACTIVE CURRENT vs. SUPPLY VOLTAGE
(MAX17201/MAX17211)



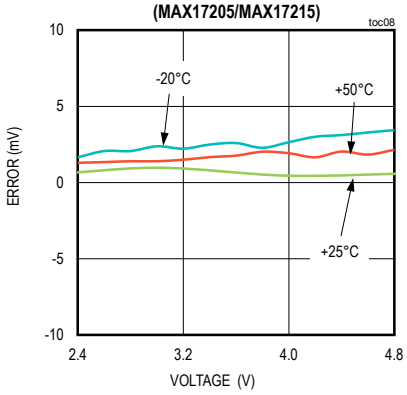
ACTIVE CURRENT vs. SUPPLY VOLTAGE
(MAX17205/MAX17215)



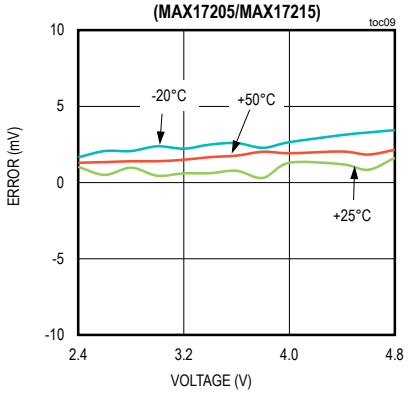
CELL1 VOLTAGE ADC ERROR
(MAX17201/MAX17211)



CELL1 VOLTAGE ADC ERROR
(MAX17205/MAX17215)



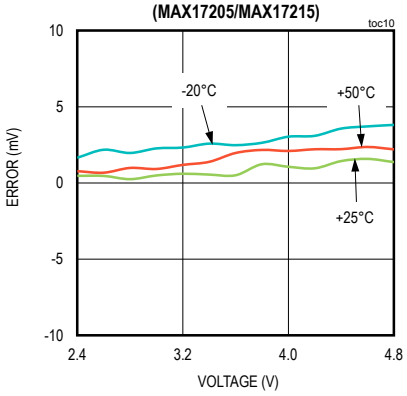
CELL2 VOLTAGE ADC ERROR
(MAX17205/MAX17215)



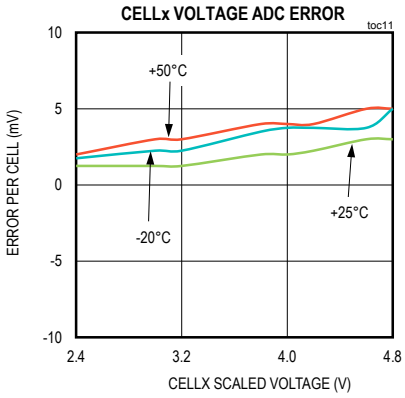
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

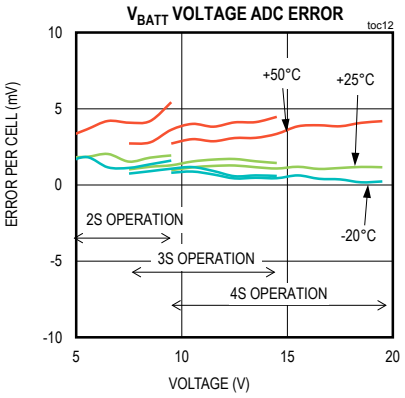
CELL3 VOLTAGE ADC ERROR
(MAX17205/MAX17215)



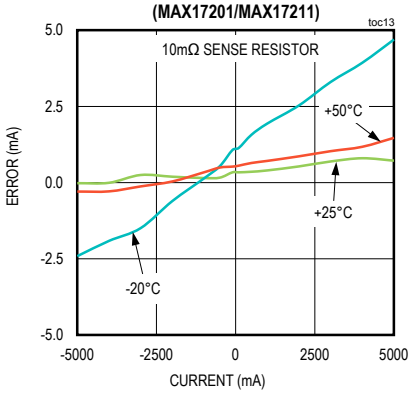
CELLx VOLTAGE ADC ERROR



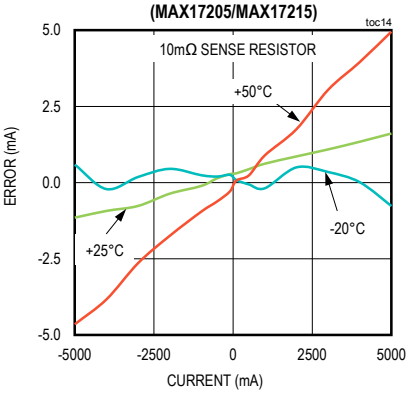
V_{BATT} VOLTAGE ADC ERROR



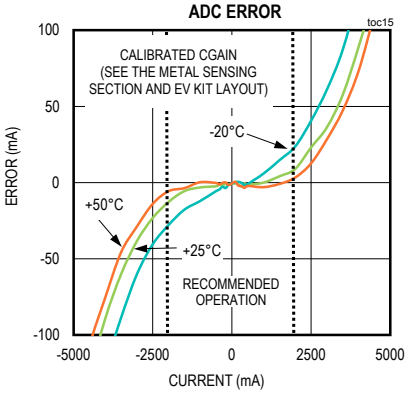
CURRENT ADC ERROR
(MAX17201/MAX17211)



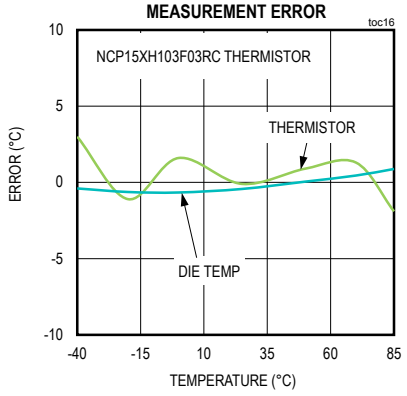
CURRENT ADC ERROR
(MAX17205/MAX17215)



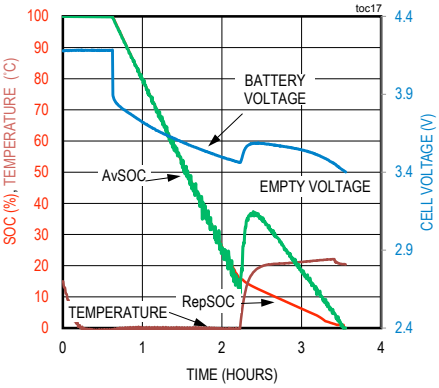
METAL TRACE CURRENT SENSE
ADC ERROR



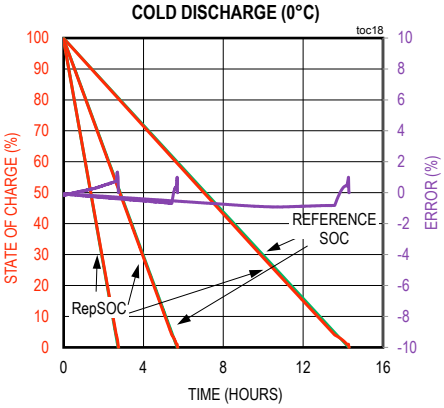
DIE TEMPERATURE AND THERMISTOR
MEASUREMENT ERROR



RESPONSE TO TEMPERATURE TRANSIENT
AT CONSTANT CURRENT LOAD



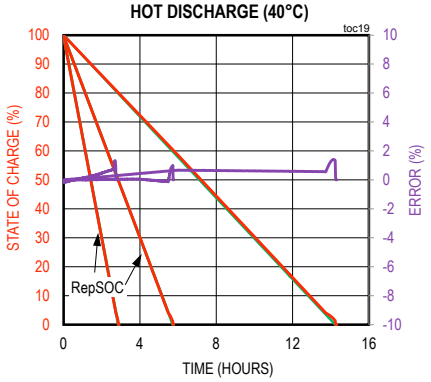
COLD DISCHARGE (0°C)



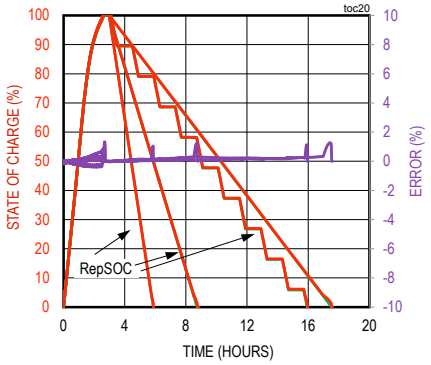
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

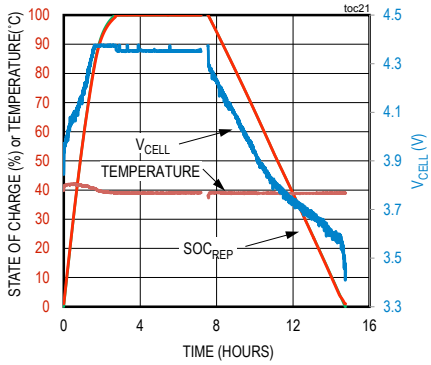
HOT DISCHARGE (40°C)



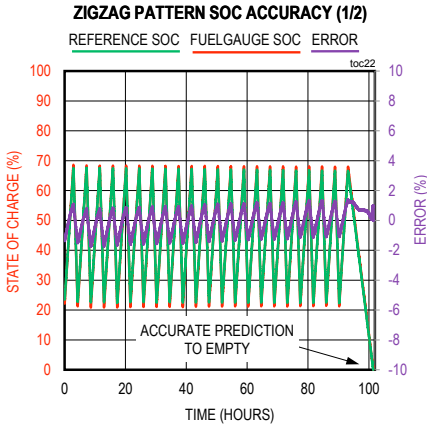
CHARGE AND DISCHARGE (+20°C)



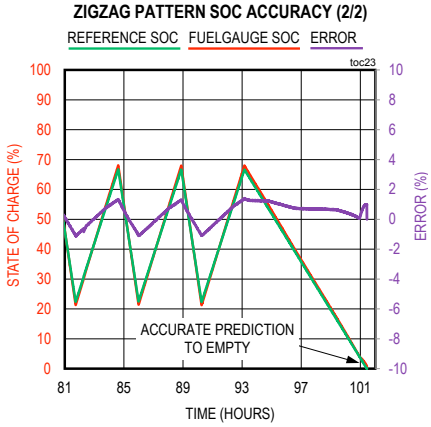
CHARGE AND DISCHARGE IN ACTUAL SYSTEM



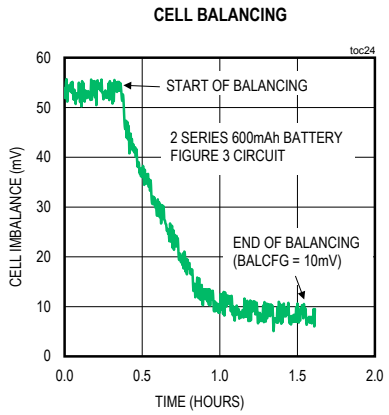
ZIGZAG PATTERN SOC ACCURACY (1/2)



ZIGZAG PATTERN SOC ACCURACY (2/2)



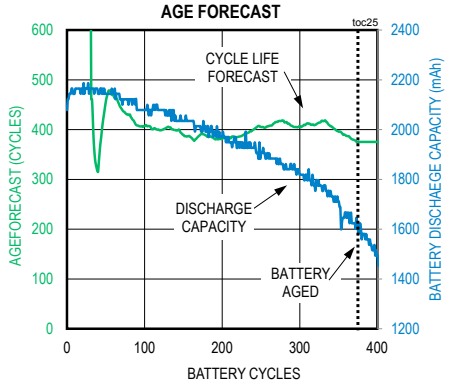
CELL BALANCING



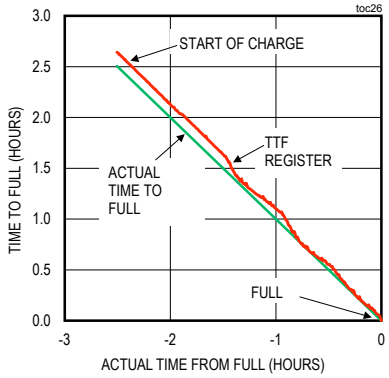
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

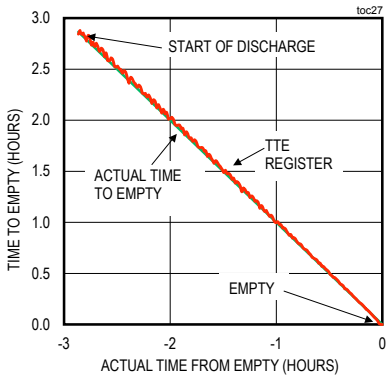
AGE FORECAST



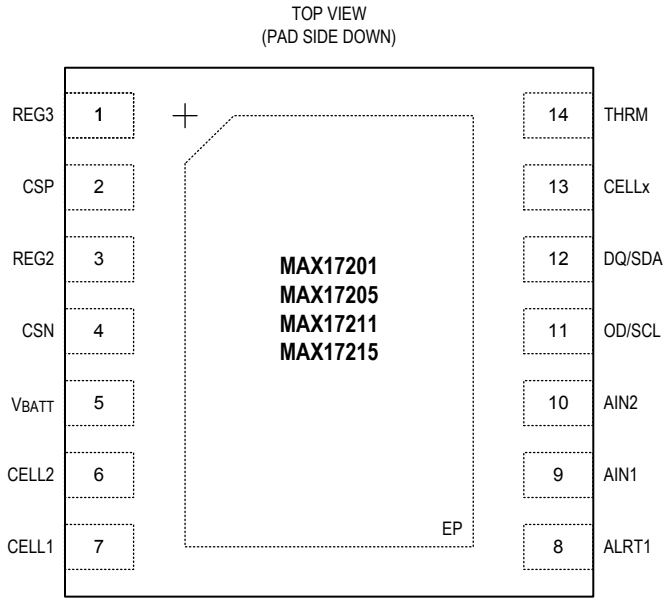
TIME TO FULL PERFORMANCE



TIME TO EMPTY PERFORMANCE



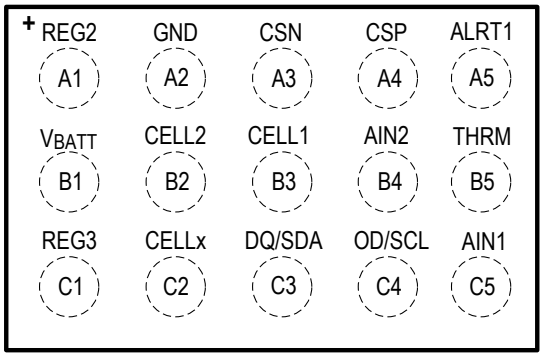
Pin Configurations



TDFN

TOP VIEW

MAX17201/MAX17205/MAX17211/MAX17215

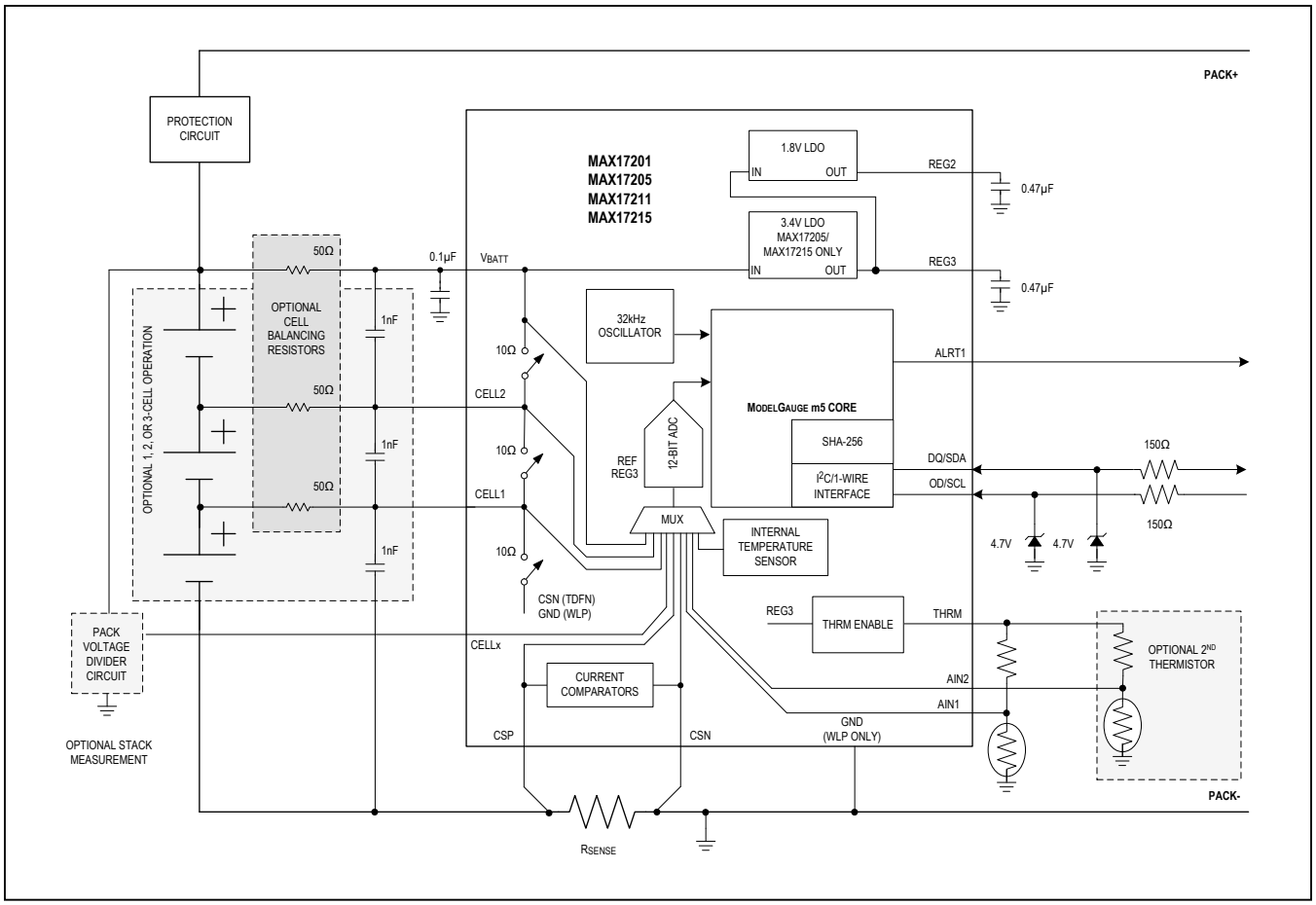


15 WLP

Pin/Bump Description

PIN/BUMP		NAME	FUNCTION
TDFN	WLP		
1	C1	REG3	Internal 3.4V Regulator Output. For the MAX17205/MAX17215, bypass with an external 0.47µF capacitor. For the MAX17201/MAX17211, connect REG3 to V_{BATT}.
2	A4	CSP	Current Measurement Positive Sense Point. Kelvin connect to cell side of sense resistor.
3	A1	REG2	Internal 1.8V Regulator Output. Bypass with an external 0.47µF capacitor to CSN (TDFN) or GND (WLP).
4	A3	CSN	Device Ground and Current Measurement Negative Sense Point. Kelvin connect to load side of sense resistor.
5	B1	V_{BATT}	Power-Supply and Battery Voltage Sense Input. Connect to positive terminal of cell stack. Bypass with RC filter to CSN (TDFN) or GND (WLP).
6	B2	CELL2	Voltage Sense Input for Measuring Cell Voltage of Second or Middle Cell. Series resistance determines balancing current. Also acts as the external divider gate drive when measuring pack voltage on CELLx pin.
7	B3	CELL1	Voltage Sense Input for Measuring Voltage of Bottom Cell. Series resistance determines balancing current.
8	A5	ALRT1	Programmable Alert Output
9	C5	AIN1	Auxiliary Voltage Input 1. Auxiliary voltage input from external thermal-measurement network.
10	B4	AIN2	Auxiliary Voltage Input 2. Auxiliary voltage input from external thermal-measurement network.
11	C4	OD/SCL	Serial Clock Input for I^2C Communication or Speed Selection for 1-Wire Communication. Input only. For I^2C communication, connect to the clock terminal of the battery pack. Connect to CSN for standard speed 1-wire communication. Connect to REG3 pin for overdrive 1-wire communication. OD/SCL has an internal pulldown (IPD) for sensing pack disconnection.
12	C3	DQ/SDA	Serial Data Input/Output for Both 1-Wire and I^2C communication modes. Open-drain output driver. Connect to the DATA terminal of the battery pack. DQ/SDA has an internal pulldown (IPD) for sensing pack disconnection.
13	C2	CELLx	High-Impedance Voltage Measurement Channel. Connect to an external voltage divider for measuring cell stacks larger than 4S.
14	B5	THRM	Thermistor Bias Connection. Connect to the high side of the thermistor resistor-divider circuit. THRM biases to REG3 voltage during AIN1 and AIN2 measurement.
—	A2	GND	IC Ground (WLP Only). Connect to PACK-. Keep isolated from CSN.
—	—	EP	Exposed Pad (TDFN Only). Connect directly to CSN.

Functional Diagram



Detailed Description

The MAX1720x/MAX1721x ultra-low power stand-alone fuel gauge ICs that implement the ModelGauge m5 algorithm without requiring host interaction for configuration. This feature makes the MAX1720x/MAX1721x an excellent pack-side fuel gauge. Voltage of the battery pack is measured at the BATT, CELL2, CELL1, CELLx, and CSP connections. Current is measured by an external sense resistor placed between the CSP and CSN pins. An external resistive voltage-divider network allows the IC to measure temperature of the battery pack by monitoring the AIN1 and AIN2 pins. The THRM pin provides a strong pullup for the resistor-divider that is disabled internally when temperature is not being measured. Internal die temperature of the ICs is also measured. The MAX17201/MAX17211 monitor a single-cell pack. The MAX17205/MAX17215 monitor individual cells of a 2S or 3S pack or the entire stack voltage of any number of multiple-series cells.

The ModelGauge m5 algorithm combines the short-term accuracy and linearity of a coulomb-counter with the long-term stability of a voltage-based fuel gauge, along with temperature compensation to provide industry-leading fuel gauge accuracy. Additionally, the algorithm does not suffer from abrupt corrections that normally occur in coulomb-counter algorithms, since tiny continual corrections are distributed over time. The MAX1720x automatically compensates for aging, temperature, and discharge rate and provides accurate state of charge (SOC) in milliampere-hours (mAh) or percentage (%) over a wide range of operating conditions. Fuel gauge error always converges to 0% as the cell approaches empty. The ICs provide accurate estimation of time-to-empty and time-to-full and provide three methods for reporting the age of the battery: reduction in capacity, increase in battery resistance, and cycle odometer. In addition, age forecasting allows the user to estimate the expected lifespan of the cell.