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EVALUATION KIT AVAILABLE

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

MAX17410

General Description

The MAX17410 is a 2-/1-phase interleaved Quick-PWM™ step-down VID power-supply controller for notebook IMVP6+ CPUs. True out-of-phase operation reduces input ripple current requirements and output voltage ripple while easing component selection and layout difficulties. The Quick-PWM control scheme provides instantaneous response to fast load current steps. Active voltage positioning reduces power dissipation and bulk output capacitance requirements and allows ideal positioning compensation for tantalum, polymer, or ceramic bulk output capacitors.

The MAX17410 is intended for two different CPU core applications: either bucking down the battery directly to create the core voltage, or bucking down the +5V system supply. The single-stage conversion method allows this device to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, 2-stage conversion (stepping down the +5V system supply instead of the battery) at higher switching frequency provides the minimum possible physical size.

A slew-rate controller allows controlled transitions between VID codes. A thermistor-based temperature sensor provides programmable thermal protection. A power monitor provides a buffered analog voltage output proportional to the power delivered to the load.

The MAX17410 is available in a 48-pin, 7mm x 7mm TQFN package.

Applications

IMVP6+ Core Supply

Multiphase CPU Core Supply

Voltage-Positioned, Step-Down Converters

Notebook/Desktop Computers

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17410GTM+	-40°C to +105°C	48 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

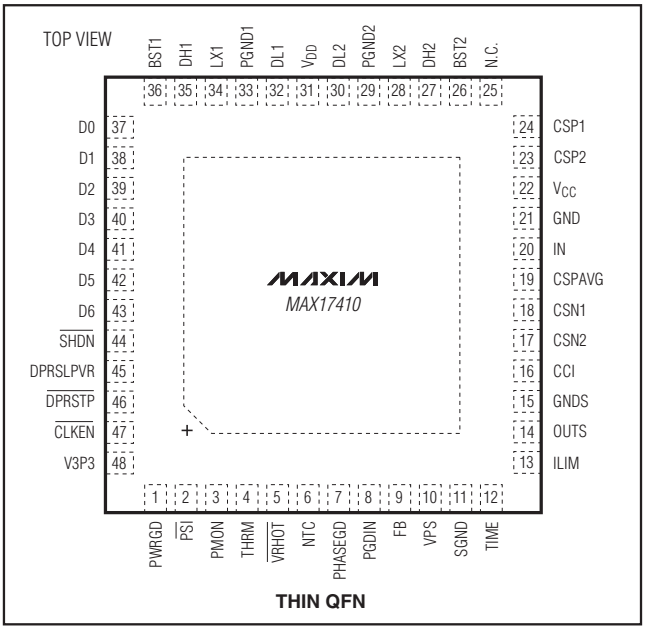
**EP = Exposed pad.*

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Features

- Dual-/Single-Phase Interleaved Quick-PWM Controller
- ±0.5% V_{OUT} Accuracy Over Line, Load, and Temperature
- 7-Bit IMVP6+ DAC
- Dynamic Phase Selection Optimizes Active/Sleep Efficiency
- Transient Phase Overlap Reduces Output Capacitance
- Active Voltage Positioning with Adjustable Gain
- Accurate Lossless Current Balance
- Accurate Droop and Current Limit
- Remote Output and Ground Sense
- Adjustable Output Slew-Rate Control
- Power-Good Window Comparator
- Power Monitor
- Programmable Thermal-Fault Protection
- Phase Fault Output (PHASEGD)
- Drives Large Synchronous Rectifier FETs
- 4.5V to 26V Battery Input Range
- Output Overvoltage and Undervoltage Protection
- Soft-Startup and Soft-Shutdown
- Integrated Boost Switches
- Low-Profile 7mm x 7mm, 48-Pin TQFN Package

Pin Configuration



Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{DD}, V3P3 to GND .....-0.3V to +6V
D0–D6, $\overline{PSI}$, DPRSLPVR, $\overline{DPRSTP}$ to GND .....-0.3V to +6V
CSPAVG, CSP_, CSN_, ILIM to GND .....-0.3V to +6V
PWRGD, PHASEGD, $\overline{VRHOT}$ to GND .....-0.3V to +6V
FB, OUTS, CCI, TIME, PMON to GND.....-0.3V to (V_{CC} + 0.3V)
PGDIN, NTC, THRM to GND .....-0.3V to (V_{CC} + 0.3V)
$\overline{CLKEN}$ to GND .....-0.3V to (V_{3P3} + 0.3V)
VPS to OUTS .....-0.3V to +0.3V
$\overline{SHDN}$ to GND (Note 1).....-0.3V to +30V
IN to GND .....-0.3V to +30V
GNDS, SGND, PGND_ to GND .....-0.3V to +0.3V
DL_ to GND .....-0.3V to (V_{DD} + 0.3V)
BST_ to V_{DD}.....-0.3V to +30V
LX_ to BST_ .....-6V to +0.3V
DH_ to LX_.....-0.3V to (V_{BST} - +0.3V)
Continuous Power Dissipation (48-pin, 7mm x 7mm TQFN)
Up to +70°C 2222mW
Derating Above +70°C .....27.8mW/°C
Operating Temperature Range .....-40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: $\overline{SHDN}$ may be forced to 12V for the purpose of debugging prototype breadboards using the no-fault test mode.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
		V3P3		3.0		3.6	
		IN		4.5		26	
DC Output Voltage Accuracy	V_{OUT}	Measured at FB with respect to GNDS, includes load regulation error (Note 2)	DAC codes from 0.8125V to 1.5000V	-0.5		+0.5	%
			DAC codes from 0.3750V to 0.8000V	-7		+7	mV
			DAC codes from 0 to 0.3625V	-20		+20	
Boot Voltage	V_{BOOT}			1.192	1.200	1.209	V
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 26V			0.1		%
OUTS Input Bias Current		VPS floating, T_A = +25°C		-0.1		+0.1	µA
OUTS-to-VPS Resistance				3.5	10	40	Ω
SGND-to-AGND Resistance					2.5		Ω
GNDS Input Range				-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97	1.00	1.03	V/V
GNDS Input Bias Current	I_{GNDS}	V(OUTS, GNDS) = 1.0V		-15	-10	-4	µA
TIME Regulation Voltage	V_{TIME}	R_{TIME} = 71.5kΩ		1.985	2.000	2.015	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIME Slew-Rate Accuracy		R_{TIME} = 71.5kΩ (12.5mV/µs nominal)	-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)	-15		+15	
		Soft-start and soft-shutdown: R_{TIME} = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal)	-16		+30	
		Slow: $V_{\overline{DPRSTP}}$ = $V_{DPRSLPVR}$ = 5V, 1/4 normal slew rate, R_{TIME} = 35.7kΩ (6.25mV/µs nominal) to 178kΩ (1.25mV/µs nominal)	-12		+25	
On-Time Accuracy	t_{ON}	V_{IN} = 10V, V_{FB} = 1.0V, V_{CCI} = (1.0V + V_{DIODE}), measured at DH_, 300kHz per phase nominal (Note 3)	300	333	366	ns
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH_ (Note 3)		300	375	ns
BIAS CURRENTS						
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, $V_{DPRSLPVR}$ = 5V, FB forced above the regulation point		3	6	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, $V_{DPRSLPVR}$ = 0, FB forced above the regulation point, T_A = +25°C		0.02	1	µA
Quiescent Supply Current (V3P3)	I_{3P3}	Measured at V3P3, FB forced within the $\overline{CLKEN}$ power-good window, T_A = +25°C		0.01	1	µA
Quiescent Supply Current (IN)	I_{IN}	Measured at IN, V_{IN} = 10V		15	25	µA
Shutdown Supply Current (V_{CC})	$I_{CC,SDN}$	Measured at V_{CC}, $\overline{SHDN}$ = GND, T_A = +25°C		0.01	1	µA
Shutdown Supply Current (V_{DD})	$I_{DD,SDN}$	Measured at V_{DD}, $\overline{SHDN}$ = GND, T_A = +25°C		0.01	1	µA
Shutdown Supply Current (V3P3)	$I_{3P3,SDN}$	Measured at V3P3, $\overline{SHDN}$ = GND, T_A = +25°C		0.01	1	µA
Shutdown Supply Current (IN)	$I_{IN,SDN}$	Measured at IN, V_{IN} = 26V, $\overline{SHDN}$ = GND, V_{CC} = 0V or 5V, T_A = +25°C		0.01	0.1	µA
FAULT PROTECTION						
Output Overvoltage-Protection Threshold	V_{OVP}	Skip mode after output reaches the regulation voltage or PWM mode, measured at FB with respect to the voltage target set by the VID code (see Table 4)	250	300	350	mV
		Soft-start, soft-shutdown, skip mode, and output has not reached the regulation voltage; measured at FB	1.75	1.80	1.85	V
		Minimum OVP threshold; measured at FB		0.8		
Output Overvoltage-Propagation Delay	t_{OVP}	FB forced 25mV above trip threshold		10		µs

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to the voltage target set by the VID code; see Table 4		-450	-400	-350	mV
Output Undervoltage-Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold			10		µs
$\overline{CLKEN}$ Startup Delay and Boot Time Period	t_{BOOT}	Measured from the time when FB reaches the boot target voltage (Note 2)		20	60	100	µs
PWRGD Startup Delay		Measured at startup from the time when $\overline{CLKEN}$ goes low		3	6.5	10	ms
$\overline{CLKEN}$ and PWRGD Threshold		Measured at FB with respect to the voltage target set by the VID code; see Table 4, 20mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350	-300	-250	mV
			Upper threshold, rising edge (overvoltage)	+150	+200	+250	
$\overline{CLKEN}$ and PWRGD Delay		FB forced 25mV outside the PWRGD trip thresholds			10		µs
PHASEGD Delay		V(CCI, FB) forced 25mV outside trip thresholds			10		µs
$\overline{CLKEN}$, PWRGD, and PHASEGD Transition Blanking Time (VID Transitions)	t_{BLANK}	Measured from the time when FB reaches the target voltage (Note 2)			20		µs
PHASEGD Transition Blanking Time (Phase 2 Enable Transitions)		Number of DH2 pulses for which PHASEGD is blanked after phase 2 is enabled			32		Pulses
$\overline{CLKEN}$ Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
$\overline{CLKEN}$ Output High Voltage		High state, I_{SOURCE} = 3mA		V3P3 - 0.4			V
PWRGD, PHASEGD Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
PWRGD, PHASEGD Leakage Current		High-impedance state; PWRGD, PHASEGD forced to 5V; T_A = +25°C				1	µA
CSN_ Pulldown Resistances in Shutdown		$\overline{SHDN}$ = 0, measured after soft-shutdown completed (DL = low)			10		Ω
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level		4.05	4.27	4.48	V
THERMAL PROTECTION							
THRM, NTC Pullup Current	I_{THRM}, I_{NTC}	V_{THRM} = V_{NTC} = 1V		40	50	60	µA
Ratio of NTC Pullup Current to THRM Pullup Current	I_{NTC}/I_{THRM}	V_{THRM} = V_{NTC} = 1V		0.995	1	1.025	µA/µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
$\overline{VRHOT}$ Trip Threshold		Measured at NTC with respect to THRM, V_{THRM} = 1V, falling edge; typical hysteresis = 100mV		-12		+12	mV
$\overline{VRHOT}$ Delay	$t_{\overline{VRHOT}}$	V_{NTC} forced 25mV below V_{THRM}, V_{THRM} = 1V, falling edge			10		µs
$\overline{VRHOT}$ Output On-Resistance	$R_{ON(\overline{VRHOT})}$	Low state			2	8	Ω
$\overline{VRHOT}$ Leakage Current		High-impedance state, $\overline{VRHOT}$ forced to 5V, T_A = +25°C				1	µA
Thermal-Shutdown Threshold	T_{SHDN}	Typical hysteresis = 15°C			+160		°C
VALLEY CURRENT LIMIT, DROOP, CURRENT BALANCE, AND CURRENT MONITOR							
Current-Limit Threshold Voltage (Positive)	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$	V_{TIME} - V_{ILIM} = 100mV	7	10	13	mV
			V_{TIME} - V_{ILIM} = 500mV	45	50	55	
			ILIM = V_{CC}	20	22.5	25	
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	$V_{CSP\_}$ - $V_{CSN\_}$, nominally -125% of V_{LIMIT}		-4		+4	mV
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZERO}	V_{AGND} - $V_{LX\_}$, DPRSLPVR = 5V			1		mV
CSPAVG, CSP_, CSN_ Common-Mode Input Range				0		2	V
Phase 2 Disable Threshold		Measured at CSP2		3	V_{CC} - 1	V_{CC} - 0.4	V
CSPAVG, CSP_, CSN_ Input Current	I_{CSPAVG}, $I_{CSP\_}$, $I_{CSN\_}$	T_A = +25°C		-0.2		+0.2	µA
ILIM Input Current	I_{ILIM}	T_A = +25°C		-0.1		+0.1	µA
Droop Amplifier Offset		[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] at I_{FB} = 0	T_A = +25°C	-0.5		+0.5	mV
			T_A = 0°C to +85°C	-0.75		+0.75	
Droop Amplifier Transconductance	$G_{m(FB)}$	$\Delta I_{FB}/\Delta$[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2], V_{FB} = $V_{CSN\_}$ = 0.45V to 1.5V		1.180	1.2	1.216	mS
Power Monitor Output Voltage for Typical HFM Conditions	V_{PMON}	V(OUTS, GNDS) = 1.200V, I_{PMON} = 0µA	[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 225mV	1.65	1.7	1.743	V
			[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 500mV	0.738	0.765	0.792	
Power Monitor Gain Referred to Output Voltage V(OUTS, GNDS)	A_{PMON}/V_{OUT}	[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 225mV, I_{PMON} = 0µA		1.375	1.4167	1.452	V/V
Power Monitor Gain Referred to [V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2]	A_{PMON}/V_{CS}	V(CSN, GNDS) = 1.200V, V(TIME, ILIM) = 225mV, I_{PMON} = 0µA		104	113.33	123	V/V

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power Monitor Load Regulation		Measured at PMON with respect to unloaded voltage	I_{PMON} = 0 to 500µA	-6			µV/µA
			I_{PMON} = -100µA		50		mV
Current Balance Amplifier Offset		(V_{CSP1} - V_{CSN1}) - (V_{CSP2} - V_{CSN2}) at I_{CCI} = 0		-1.0		+1.0	mV
Current Balance Amplifier Transconductance	$G_{m(CCI)}$	$\Delta I_{CCI}/\Delta[(V_{CSP1} - V_{CSN1}) - (V_{CSP2} - V_{CSN2})]$, $V_{CSN\_}$ = 0.45V to 1.5V			200		µS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V	High state (pullup)		0.9	2.5	Ω
			Low state (pulldown)		0.7	2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	High state (pullup)			0.7	2.0	Ω
		Low state (pulldown)			0.25	0.7	
DH_ Gate-Driver Source Current	$I_{DH\_(SOURCE)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.2		A
DH_ Gate-Driver Sink Current	$I_{DH\_(SINK)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.7		A
DL_ Gate-Driver Source Current	$I_{DL\_(SOURCE)}$	DL_ forced to 2.5V			2.7		A
DL_ Gate-Driver Sink Current	$I_{DL\_(SINK)}$	DL_ forced to 2.5V			8		A
Driver Propagation Delay	$t_{DH\_DL\_}$	DH_ low to DL_ high			20		ns
	$t_{DL\_DH\_}$	DL_ low to DH_ high			20		
DL_ Transition Time		DL_ falling, $C_{DL\_}$ = 3nF			20		ns
		DL_ rising, $C_{DL\_}$ = 3nF			20		
DH_ Transition Time		DH_ falling, $C_{DH\_}$ = 3nF			20		ns
		DH_ rising, $C_{DH\_}$ = 3nF			20		
Internal BST_ Switch On-Resistance	$R_{ON(BST\_)}$				10	20	Ω
LOGIC AND I/O							
Logic Input High Voltage	V_{IH}	$\overline{SHDN}$, PGDIN, DPRSLPVR		2.3			V
Logic Input Low Voltage	V_{IL}	$\overline{SHDN}$, PGDIN, DPRSLPVR				1.0	V
Low-Voltage Logic Input High Voltage	V_{IHLV}	$\overline{PSI}$, D0–D6, $\overline{DPRSTP}$		0.67			V
Low-Voltage Logic Input Low Voltage	V_{ILLV}	$\overline{PSI}$, D0–D6, $\overline{DPRSTP}$				0.33	V
Logic Input Current		T_A = +25°C, PGDIN		-1.5	-1	-0.5	µA
		T_A = +25°C, $\overline{SHDN}$, DPRSLPVR, $\overline{PSI}$, $\overline{DPRSTP}$, D0–D6 = 0 or 5V		-1		+1	

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
		V3P3		3.0		3.6	
		IN		4.5		26	
DC Output Voltage Accuracy	V_{OUT}	Measured at FB with respect to GNDS, includes load regulation error (Note 2)	DAC codes from 0.8125V to 1.5000V	-0.75		+0.75	%
			DAC codes from 0.3750V to 0.8000V	-10		+10	mV
			DAC codes from 0 to 0.3625V	-25		+25	
Boot Voltage	V_{BOOT}			1.185		1.215	V
OUTS to VPS Resistance				3.5		40	Ω
GNDS Input Range				-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97		1.03	V/V
GNDS Input Bias Current	I_{GNDS}	V(OUTS, GNDS) = 1.0V		-15		-4	µA
TIME Regulation Voltage	V_{TIME}	R_{TIME} = 71.5kΩ		1.985		2.015	V
TIME Slew-Rate Accuracy		R_{TIME} = 71.5kΩ (12.5mV/µs nominal)		-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)		-15		+15	
		Soft-start and soft-shutdown: R_{TIME} = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal)		-16		+30	
		Slow: $V_{\overline{DPRSTP}}$ = $V_{DPRSLPVR}$ = 5V, 1/4 normal slew rate, R_{TIME} = 35.7kΩ (6.25mV/µs nominal) to 178kΩ (1.25mV/µs nominal)		-12		+25	
On-Time Accuracy	t_{ON}	V_{IN} = 10V, V_{FB} = 1.0V, V_{CCI} = (1.0V + V_{DIODE}), measured at DH_, 300kHz per phase nominal (Note 3)		290	333	376	ns
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH_ (Note 3)				375	ns
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, $V_{DPRSLPVR}$ = 5V, FB forced above the regulation point				6	mA
Quiescent Supply Current (IN)	I_{IN}	Measured at IN, V_{IN} = 10V				25	µA

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT PROTECTION							
Output Overvoltage-Protection Threshold	V_{OVP}	Skip mode after output reaches the regulation voltage or PWM mode; measured at FB with respect to the voltage target set by the VID code (see Table 4)		250		350	mV
		Soft-start, soft-shutdown, skip mode, and output has not reached the regulation voltage; measured at FB		1.75		1.85	V
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to the voltage target set by the VID code (see Table 4)		-450		-350	mV
$\overline{CLKEN}$ Startup Delay and Boot Time Period	t_{BOOT}	Measured from the time when FB reaches the boot target voltage (Note 2)		20		100	µs
PWRGD Startup Delay		Measured at startup from the time when $\overline{CLKEN}$ goes low		3		10	ms
$\overline{CLKEN}$ and PWRGD Threshold		Measured at FB with respect to the voltage target set by the VID code (see Table 4), 20mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350		-250	mV
			Upper threshold, rising edge (overvoltage)	+150		+250	
$\overline{CLKEN}$ Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
$\overline{CLKEN}$ Output High Voltage		High state, I_{SOURCE} = 3mA		V3P3 - 0.4			V
PWRGD, PHASEGD Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
PWRGD, PHASEGD Leakage Current		High-impedance state; PWRGD, PHASEGD forced to 5V; T_A = +25°C				1	µA
V_{CC} Undervoltage-Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level		4.0		4.5	V
THERMAL PROTECTION							
THRM, NTC Pullup Current	I_{THRM}, I_{NTC}	V_{THRM} = V_{NTC} = 1V		40		60	µA
Ratio of NTC Pullup Current to THRM Pullup Current	I_{NTC}/I_{THRM}	V_{THRM} = V_{NTC} = 1V		0.993		1.03	µA/µA
$\overline{VRHOT}$ Trip Threshold		Measured at NTC with respect to THRM, V_{THRM} = 1V, falling edge; typical hysteresis = 100mV		-12		+12	mV
$\overline{VRHOT}$ Output On-Resistance	$R_{ON(\overline{VRHOT})}$	Low state				8	Ω

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
VALLEY CURRENT LIMIT, DROOP, CURRENT BALANCE, AND CURRENT MONITOR							
Current-Limit Threshold Voltage (Positive)	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$	V_{TIME} - V_{ILIM} = 100mV	7		13	mV
			V_{TIME} - V_{ILIM} = 500mV	45		55	
			ILIM = V_{CC}	20		25	
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	$V_{CSP\_}$ - $V_{CSN\_}$, nominally -125% of V_{LIMIT}		-5		+5	mV
CSPAVG, CSP_, CSN_ Common-Mode Input Range				0		2	V
Phase 2 Disable Threshold		Measured at CSP2		3		V_{CC} - 0.4	V
Droop Amplifier Offset		[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] at I_{FB} = 0	T_A = +25°C	-0.75		+0.75	mV
			T_A = 0°C to +85°C	-1		+1	
Droop Amplifier Transconductance	$G_{m(FB)}$	$\Delta I_{FB}/\Delta[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2]$, V_{FB} = V_{CSN-} = 0.45V to 1.5V		1.173		1.224	mS
Power Monitor Output Voltage for Typical HFM Conditions	V_{PMON}	V(OUTS, GNDS) = 1.200V, I_{PMON} = 0µA	[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 225mV	1.627		1.768	V
			[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 500mV	0.734		0.796	
Power Monitor Gain Referred to Output Voltage V(OUTS, GNDS)	$A_{PMON/VOUT}$	[V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2] = 15mV, V(TIME, ILIM) = 225mV, I_{PMON} = 0µA		1.375		1.452	V/V
Power Monitor Gain Referred to [V_{CSPAVG} - (V_{CSN1} + V_{CSN2})/2]	$A_{PMON/VCS}$	V(CSN, GNDS) = 1.200V, V(TIME, ILIM) = 225mV, I_{PMON} = 0µA		104		123	V/V
Power Monitor Load Regulation		Measured at PMON with respect to unloaded voltage	I_{PMON} = 0 to 500µA	-6			µV/µA
Current Balance Amplifier Offset		(V_{CSP1} - V_{CSN1}) - (V_{CSP2} - V_{CSN2}) at I_{CCI} = 0		-1.5		+1.5	mV

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V_{V3P3} = 3.3V, $V_{DPRSLPVR}$ = $V_{\overline{DPRSTP}}$ = V_{GNDS} = $V_{PGND\_}$ = 0, CSPAVG = CSP_ = CSN_ = OUTS = 1.0000V, R_{FB} = 3.57kΩ from FB to VPS, [D6–D0] = [0101000]; **T_A = -40°C to +105°C**, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V	High state (pullup)			2.5	Ω
			Low state (pulldown)			2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	High state (pullup)				2.0	Ω
		Low state (pulldown)				0.7	
Internal BST_ Switch On-Resistance	$R_{ON(BST\_)}$	$I_{BST\_}$ = 10mA				20	Ω
LOGIC AND I/O							
Logic Input High Voltage	V_{IH}	$\overline{SHDN}$, PGDIN, DPRSLPVR		2.3			V
Logic Input Low Voltage	V_{IL}	$\overline{SHDN}$, PGDIN, DPRSLPVR				1.0	V
Low-Voltage Logic Input High Voltage	V_{IHLV}	$\overline{PSI}$, D0–D6, $\overline{DPRSTP}$		0.67			V
Low-Voltage Logic Input Low Voltage	V_{ILLV}	$\overline{PSI}$, D0–D6, $\overline{DPRSTP}$				0.33	V

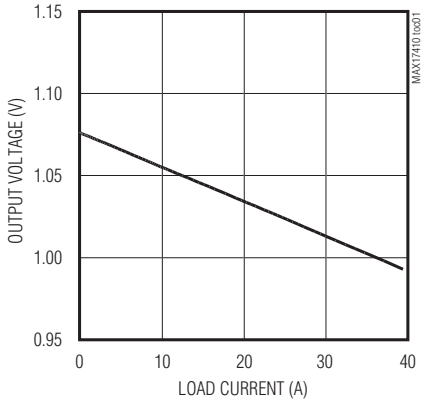
Note 2: DC output accuracy specifications refer to the trip level of the error amplifier. The output voltage has a DC regulation higher than the trip level by 50% of the output ripple. When pulse skipping, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

Note 3: On-time and minimum off-time specifications are measured from 50% to 50% at the DL_ and DH_ pins, with LX_ forced to GND, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times might be different due to MOSFET switching speeds.s

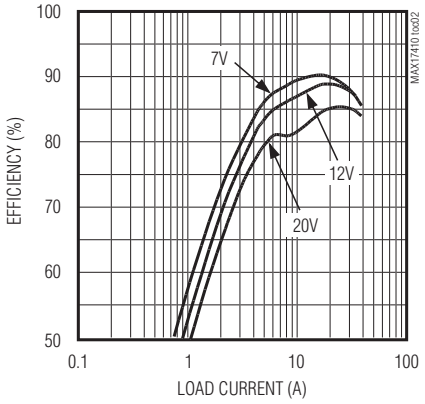
Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 1.1500V, T_A = +25°C, unless otherwise specified.)

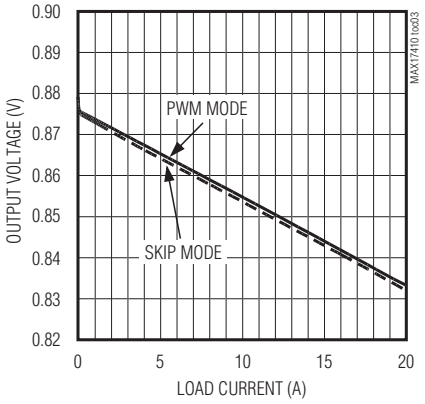
2-PHASE OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 1.075V)



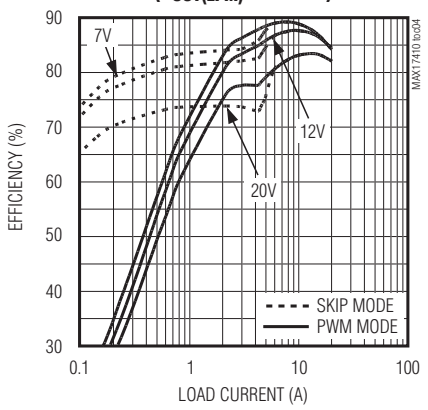
2-PHASE EFFICIENCY vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 1.075V)



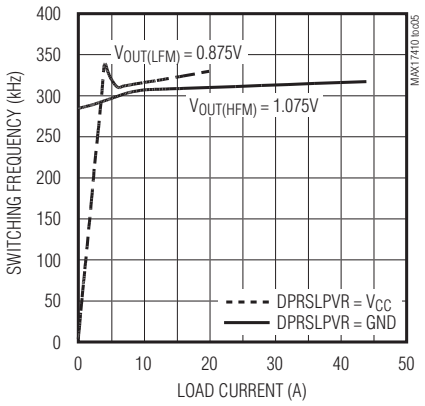
1-PHASE OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 0.875V)



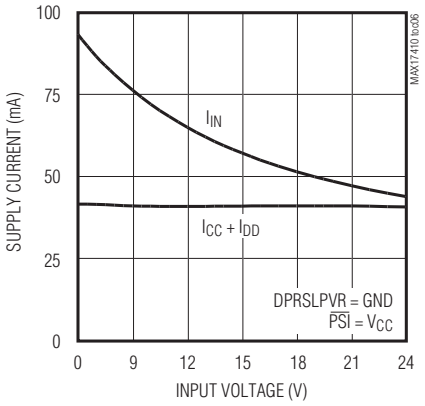
1-PHASE EFFICIENCY vs. LOAD CURRENT ($V_{OUT(LFM)}$ = 0.875V)



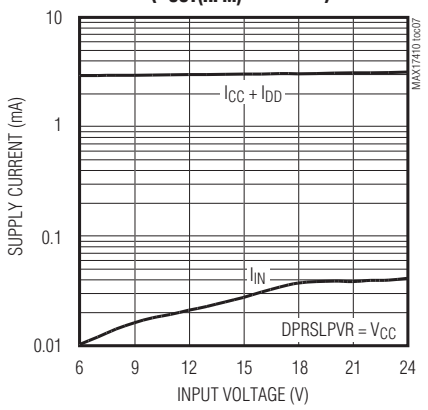
SWITCHING FREQUENCY vs. LOAD CURRENT



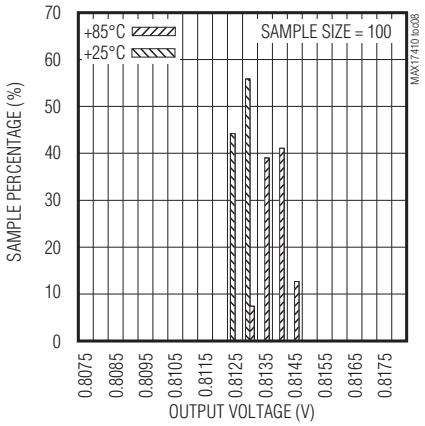
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE ($V_{OUT(HFM)}$ = 1.075V)



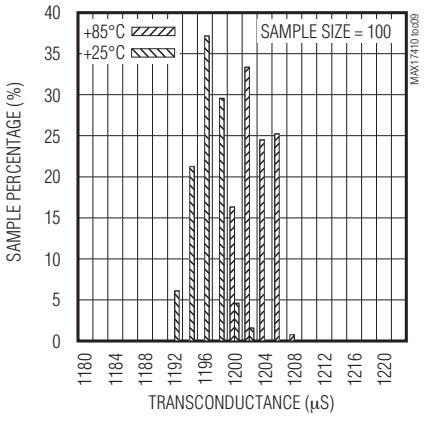
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE AT SKIP MODE ($V_{OUT(HFM)}$ = 1.075V)



0.8125V OUTPUT-VOLTAGE DISTRIBUTION



Gm(FB) TRANSCONDUCTANCE DISTRIBUTION

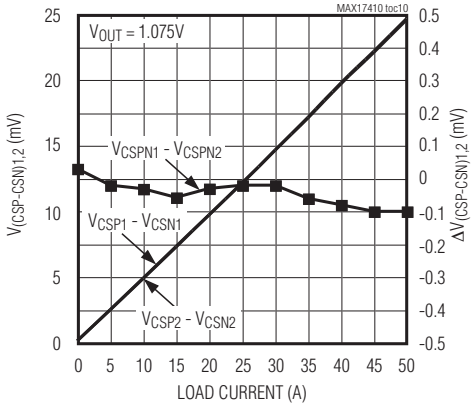


Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

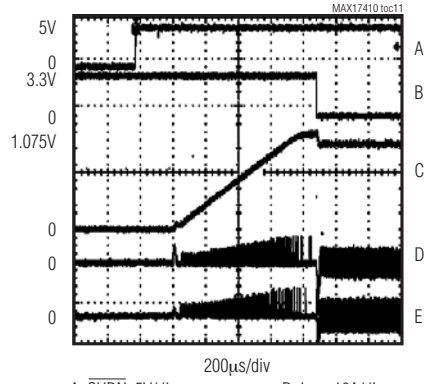
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 1.1500V, T_A = +25°C, unless otherwise specified.)

CURRENT BALANCE vs. LOAD CURRENT

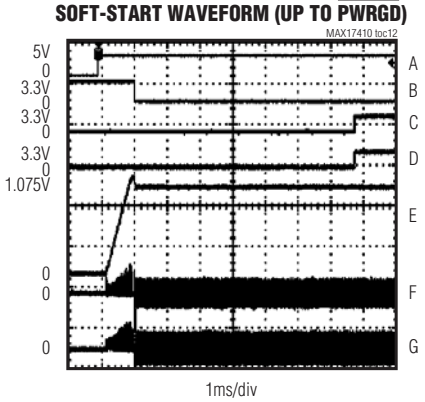


SOFT-START WAVEFORM (UP TO $\overline{CLKEN}$)



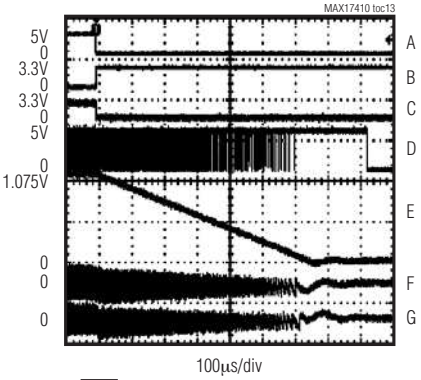
A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 3.3V/div
C. V_{OUT}, 500mV/div
D. I_{LX1}, 10A/div
E. I_{LX2}, 10A/div
I_{OUT} = 0

SOFT-START WAVEFORM (UP TO $\overline{PWRGD}$)



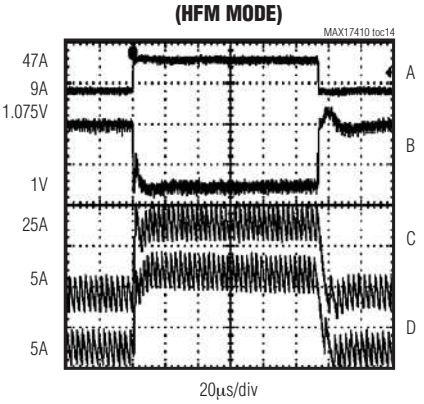
A. $\overline{SHDN}$, 10V/div
B. $\overline{CLKEN}$, 6.6V/div
C. PWRGD, 10V/div
D. PHASEGD, 10V/div
E. V_{OUT}, 500mV/div
F. I_{LX1}, 10A/div
G. I_{LX2}, 10A/div
I_{OUT} = 0

SHUTDOWN WAVEFORM



A. $\overline{SHDN}$, 10V/div
B. PWRGD, 10V/div
C. $\overline{CLKEN}$, 6.6V/div
D. DL1, 5V/div
E. V_{OUT}, 500mV/div
F. I_{LX1}, 10A/div
G. I_{LX2}, 10A/div

LOAD-TRANSIENT RESPONSE (HFM MODE)

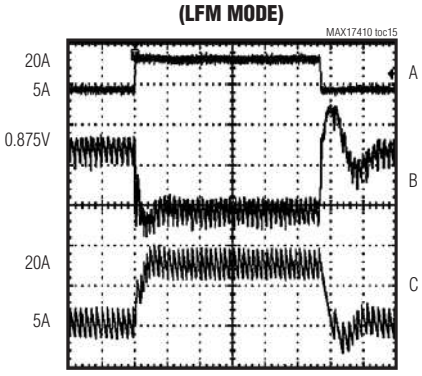


A. I_{OUT} = 9A–47A
B. V_{OUT}, 50mV/div
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

Typical Operating Characteristics (continued)

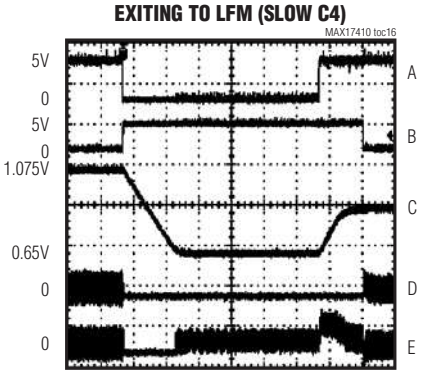
(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 1.1500V, T_A = +25°C, unless otherwise specified.)

LOAD-TRANSIENT RESPONSE (LFM MODE)



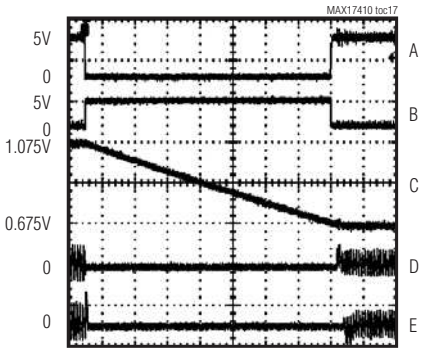
A. I_{OUT} = 5A–20A
B. V_{OUT}, 20mV/div
C. I_{LX1}, 10A/div
$\overline{PSI}$ = GND
DPRSLPVR = GND

ENTERING DEEPER SLEEP EXITING TO LFM (SLOW C4)



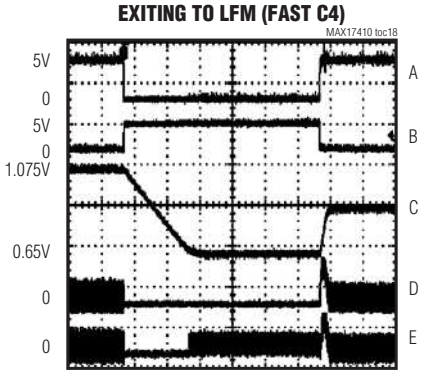
A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 10V/div
C. V_{OUT}, 200mV/div
D. I_{LX2}, 10A/div
E. I_{LX1}, 10A/div
I_{OUT} = 3A

ENTERING DEEPER SLEEP EXITING TO NEAREST VID



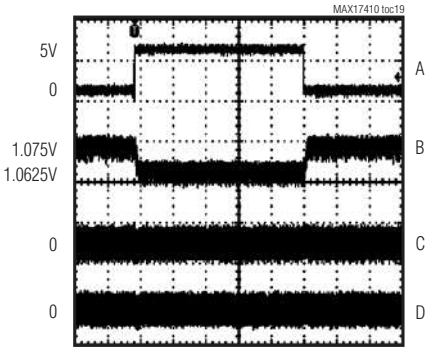
A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 10V/div
C. V_{OUT}, 200mV/div
D. I_{LX2}, 10A/div
E. I_{LX1}, 10A/div
I_{OUT} = 3Av

ENTERING DEEPER SLEEP EXITING TO LFM (FAST C4)



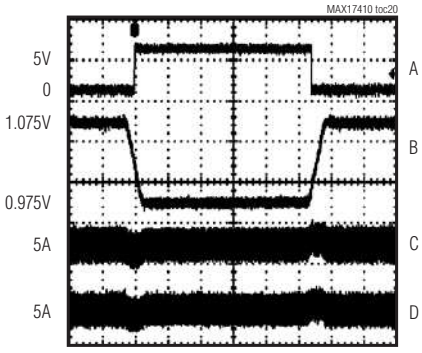
A. $\overline{DPRSTP}$, 5V/div
B. DPRSLPVR, 10V/div
C. V_{OUT}, 200mV/div
D. I_{LX2}, 10A/div
E. I_{LX1}, 10A/div
I_{OUT} = 3Av

D0 12.5mV DYNAMIC VID CODE CHANGE



A. VID0, 5V/div
B. V_{OUT}, 20mV/div
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

D3 10mV DYNAMIC VID CODE CHANGE



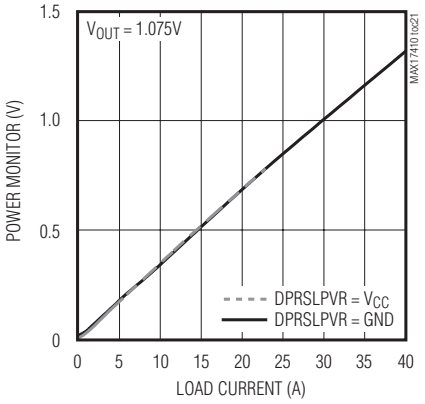
A. D3, 5V/div
B. V_{OUT}, 50mV/div
I_{OUT}, = 10A
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

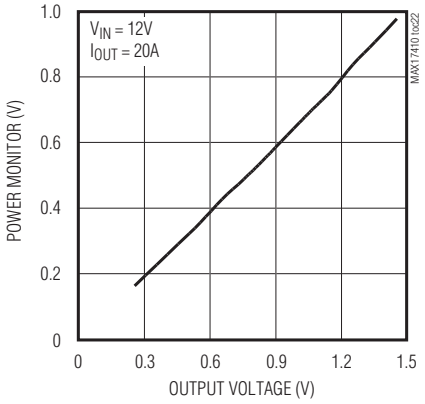
Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 1.1500V, T_A = +25°C, unless otherwise specified.)

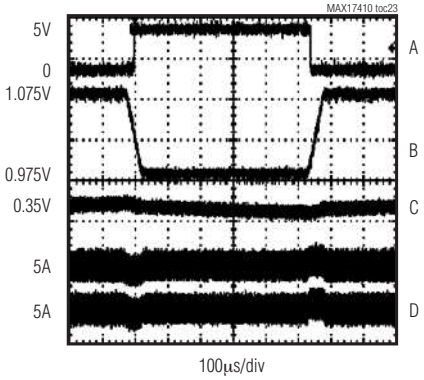
MAX17410 POWER MONITOR vs. LOAD CURRENT



MAX17410 POWER MONITOR vs. OUTPUT VOLTAGE

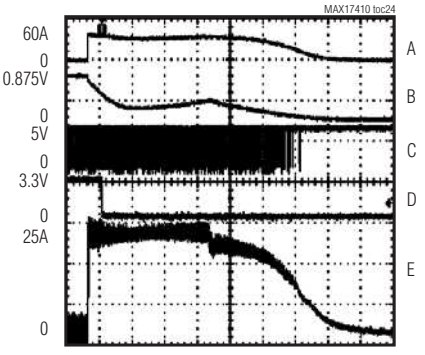


POWER MONITOR VID TRANSITION RESPONSE



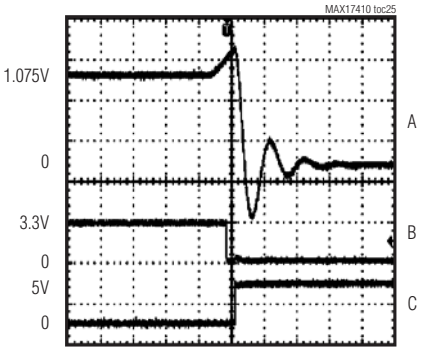
A. D3, 5V/div
B. V_{OUT}, 50mV/div
I_{OUT} = 10A
C. V_{PMON}, 50mV/div
D. I_{LX1}, 10A/div
E. I_{LX2}, 10A/div

OUTPUT UNDERVOLTAGE FAULT



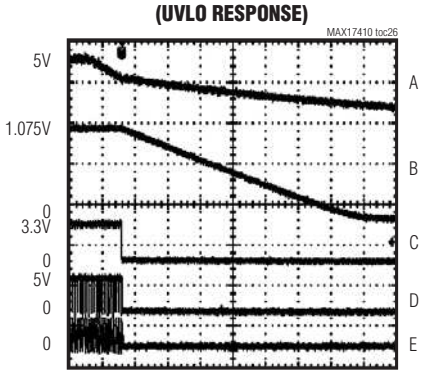
A. I_{OUT}, 100A/div
B. V_{OUT}, 500mV/div
C. DL, 5V/div
D. PWRGD, 3.3V/div
E. I_{LX1}, 10A/div

OUTPUT OVERVOLTAGE WAVEFORM



A. V_{OUT}, 500mV/div
B. PWRGD, 3.3V/div
C. DL1, 5V/div
DPRSLPVR = V_{CC}

BIAS SUPPLY REMOVAL (UVLO RESPONSE)



A. 5V BIAS SUPPLY, 2V/div
B. V_{OUT}, 500mV/div
C. PWRGD, 3.3V/div
D. DL1, 5V/div
E. I_{LX1}, 10A/div
I_{OUT} = 5A

Pin Description

PIN	NAME	FUNCTION
1	PWRGD	Open-Drain Power-Good Output. After output voltage transitions, except during power-up and power-down, if FB is in regulation, then PWRGD is high impedance. PWRGD is low during startup, continues to be low while the output is at the boot voltage, and stays low until 5ms (typ) after $\overline{CLKEN}$ goes low, after which it starts monitoring the FB voltage and goes high if FB is within the PWRGD threshold window. PWRGD is forced low during soft-shutdown and while in shutdown. PWRGD is forced high impedance whenever the slew-rate controller is active (output voltage transitions), and continues to be forced high impedance for an additional 20µs after the transition is completed. The PWRGD upper threshold is blanked during any downward output voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete and the output reaches regulation. A pullup resistor on PWRGD causes additional finite shutdown current.
2	$\overline{PSI}$	Power-State Indicator. This low-voltage logic input indicates power usage and sets the operating mode together with DPRSLPVR as shown in the truth table below. While DPRSLPVR is low, if $\overline{PSI}$ is forced low, the controller is immediately set to 1-phase forced-PWM mode. The controller returns to 2-phase forced-PWM mode when $\overline{PSI}$ is forced high. DPRSLPVR / $\overline{PSI}$ / Mode 1 / 0 / Very low current (1-phase skip) 1 / 1 / Low current (approx 3A) (1-phase skip) 0 / 0 / Intermediate power potential (1-phase PWM) 0 / 1 / Max power potential (full-phase PWM: 2-phase or 1-phase as set by user at CSP2) The controller is in 2-phase skip mode during startup, but is in 2-phase forced-PWM mode during soft-shutdown, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. The controller is also in 2-phase skip mode while in boot mode, but is in 2-phase forced-PWM mode during the transition from boot mode to VID mode, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. However, if phase 2 is disabled by connecting CSP2 to V_{CC}, then only phase 1 is active in the above modes.
3	PMON	Power Monitor Output: $V(PWR) = K_{PWR} \times V(OUTS, GNDS) \times V(CSPAVG, CSN)/V(TIME, ILIM)$ where K_{PWR} = 21.25 typical. If ILIM is externally connected to a 5V rail to enable the internal default/preset current-limit threshold, then the V(TIME, ILIM) value to be used in the above equation is 225mV. Do not use the power monitor in any configuration that would cause its output V(PMON) to exceed (V_{CC} - 0.5V). PMON is pulled to ground when the MAX17410 is in shutdown.
4	THRM	Resistive Input of Thermal Comparator. Connect a resistor to ground to set the $\overline{VRHOT}$ threshold. THRM and NTC have matched 50µA current sources, so the resistance value = the NTC resistance at the desired high temperature. $\overline{VRHOT}$ is pulled low when the voltage at NTC goes below the voltage at THRM.
5	$\overline{VRHOT}$	Open-Drain Output of Internal Comparator. $\overline{VRHOT}$ is pulled low when the voltage at NTC goes below the voltage at THRM. $\overline{VRHOT}$ is high impedance in shutdown.
6	NTC	Thermistor Input of Thermal Comparator. Connect a standard thermistor to ground. THRM and NTC have matched 50µA current sources, so the resistance value = the NTC resistance at the desired high temperature. $\overline{VRHOT}$ is pulled low when the voltage at NTC goes below the voltage at THRM.

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

Pin Description (continued)

PIN	NAME	FUNCTION
7	PHASEGD	Open-Drain Phase-Good Output. Used to signal the system that one of the two phases either has a fault condition or is not matched with the other. Detection is done by identifying the need for a large (more than 40%) on-time difference between phases to achieve or move towards current balance. PHASEGD is low in shutdown, and when phase 2 is disabled by connecting CSP2 to V_{CC}. PHASEGD is forced high impedance whenever the slew-rate controller is active (output voltage transitions), and when phase 2 is disabled by the DPRSLPVR and/or $\overline{PSI}$ inputs. When phase 2 is reenabled, PHASEGD stays high impedance for 32 DH2 pulses, after which it monitors the difference between the on-times of the two phases. PHASEGD is also forced high impedance when V_{FB} is below 0.5V.
8	PGDIN	Power-Good Logic Input. Indicates the power status of other system rails and used for supply sequencing. Connect this pin to the 5V supply rail or float it if the feature is not needed. During startup, after soft-starting to the boot voltage, the output voltage remains at V_{BOOT}, and the $\overline{CLKEN}$ and PWRGD outputs remain high and low, respectively, as long as the PGDIN input stays low. When PGDIN later goes high, the output is allowed to transition to the voltage set by the VID code, and $\overline{CLKEN}$ is allowed to go low. During normal operation, if PGDIN goes low, the controller immediately forces $\overline{CLKEN}$ high and PWRGD low, and slews the output to the boot voltage while in 2-phase skip mode at 1/8 the normal slew rate set by the TIME resistor. The output then stays at the boot voltage until the controller is turned off or power cycled, or until PGDIN goes high again.
9	FB	Feedback Voltage Input, and Output of the Voltage-Positioning Transconductance Amplifier. The voltage at the FB pin is compared with the slew-rate-controlled target voltage by the error comparator (fast regulation loop), as well as by the internal voltage integrator (slow, accurate regulation loop). Having sufficient ripple signal at FB that is in-phase with the sum of the inductor currents is essential for cycle-by-cycle stability. Connect resistor R_{FB} between FB and VPS to set the droop based on the voltage-positioning gain requirements: $$R_{FB} = R_{DROOP}/[R_{SENSE} \times G_{m(FB)}]$$ where R_{DROOP} is the desired voltage-positioning slope, $G_{m(FB)}$ = 1.2mS typ, and R_{SENSE} is the effective current-sense resistance that is used to provide the (CSPAVG, CSN_) current-sense voltage. If lossless sensing (inductor DCR sensing) is used, consider using a thermistor as part of the CSPAVG filter network to minimize the temperature dependence of the voltage-positioning slope. FB is high impedance in shutdown.
10	VPS	Internally Shorted to OUTS Through a 10Ω Resistance
11	SGND	Internally Shorted SGND (Pin 11) to AGND (Pin 21)
12	TIME	Slew-Rate Adjustment Pin. The total resistance R_{TIME} from TIME to GND sets the internal slew rate. SLEW RATE = (12.5mV/µs) x (71.5kΩ/R_{TIME}) where R_{TIME} is between 35.7kΩ and 178kΩ. This “normal” slew rate applies to transitions into and out of the low-power pulse-skipping modes and to the transition from boot mode to VID. The slew rate for startup and for entering shutdown is always 1/8 of normal. If DPRSLPVR and $\overline{DPRSTP}$ are both high, then the slew rate is reduced to 1/4 of normal. If the VID DAC inputs are clocked, the slew rate for all other VID transitions is set by the rate at which they are clocked, up to a maximum slew rate equal to the normal slew rate defined above.
13	ILIM	Current-Limit Adjust Input. The valley positive current-limit threshold voltages at V(CSP_, CSN_) are precisely 1/10 the differential voltage V(TIME, ILIM) over a 0.1V to 0.5V range of V(TIME, ILIM). The valley negative current-limit thresholds are typically -125% of the corresponding valley positive current-limit thresholds. Connect ILIM to V_{CC} to get the default current-limit threshold setting of 22.5mV typ.

Pin Description (continued)

PIN	NAME	FUNCTION
14	OUTS	Output Remote Sense. Internally shorted to VPS through a 10Ω resistance. OUTS is also the voltage feedback input to the power monitor.
15	GNDS	Feedback Remote-Sense Input, Negative Side. Normally connected to GND directly at the load. GNDS internally connects to a transconductance amplifier that fine tunes the output voltage—compensating for voltage drops from the regulator ground to the load ground.
16	CCI	Current-Balance Compensation. Connect a 470pF capacitor between CCI and the positive side of the feedback remote-sense input (or between CCI and GND). CCI is internally forced low in shutdown.
17	CSN2	Negative Input of the Output Current Sense of Phase 2. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
18	CSN1	Negative Input of the Output Current Sense of Phase 1. This pin should be connected to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
19	CSPAVG	Positive Input of the Output Current-Sense Averaging Network. This input should be connected to the positive current-sense averaging network (see the standard 2-phase IMVP6+ application circuit of Figure 1) and is utilized for load line control and power monitoring (input of the transconductance amplifiers used for FB and PMON).
20	IN	Input Sense for On-Time Control. An internal resistor sets the switching frequency to 300kHz per phase. IN is high impedance in shutdown.
21	GND	Analog Ground Connect
22	V_{CC}	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with 1µF minimum.
23	CSP2	Positive Input of the Output Current Sense of Phase 2. This pin should be connected to the positive side of the output current-sensing resistor, or to the filtering capacitor if the DC resistance of the output inductor is used for current sensing. This pin is utilized for current limit and current balance only. Connect CSP2 to V_{CC} to disable phase 2 and use the MAX17410 as a single-phase controller. In this configuration, connect LX2 to GND, connect BST2 to V_{DD}, CSN2 to CSN1, and float DH2, DL2, CCI, and PHASEGD.
24	CSP1	Positive Input of the Output Current Sense of Phase 1. This pin should be connected to the positive side of the output current-sensing resistor, or to the filtering capacitor if the DC resistance of the output inductor is used for current sensing. This pin is utilized for current limit and current balance only.
25	N.C.	No Connection. Not internally connected.
26	BST2	Phase 2 Boost Flying Capacitor Connection. BST2 is the internal upper supply rail for the DH2 high-side gate driver. An internal switch between V_{DD} and BST2 charges the BST2 - LX2 flying capacitor while the low-side MOSFET is on (DL2 pulled high).
27	DH2	Phase 2 High-Side Gate-Driver Output. DH2 swings from LX2 to BST2. Low in shutdown.
28	LX2	Phase 2 Inductor Connection. LX2 is the internal lower supply rail for the DH2 high-side gate driver. Also used as an input to phase 2's zero-crossing comparator.
29	PGND2	Power Ground. PGND2 is the internal lower supply rail for the DL2 low-side gate driver.
30	DL2	Phase 2 Low-Side Gate-Driver Output. DL2 swings from PGND2 to V_{DD}. DL2 is forced low in shutdown. DL2 is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DL2 is forced low in skip mode after detecting an inductor current zero crossing.
31	V_{DD}	Supply Voltage Input for the DL_ Drivers. V_{DD} is also the supply voltage used to internally recharge the BST_ - LX_ flying capacitor during the times the respective DL_ are high. Connect V_{DD} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD} to GND with a 1µF or greater ceramic capacitor.

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

Pin Description (continued)

PIN	NAME	FUNCTION
32	DL1	Phase 1 Low-Side Gate-Driver Output. DL1 swings from PGND1 to V_{DD}. DL1 is forced low in shutdown. DL1 is forced high when an output overvoltage fault is detected, overriding any negative current-limit condition that might be present. DL1 is forced low in skip mode after detecting an inductor current zero crossing.
33	PGND1	Power Ground. PGND1 is the internal lower supply rail for the DL1 low-side gate driver.
34	LX1	Phase 1 Inductor Connection. LX1 is the internal lower supply rail for the DH1 high-side gate driver. Also used as an input to phase 1's zero-crossing comparator.
35	DH1	Phase 1 High-Side Gate-Driver Output. DH1 swings from LX1 to BST1. Low in shutdown.
36	BST1	Phase 1 Boost Flying Capacitor Connection. BST1 is the internal upper supply rail for the DH1 high-side gate driver. An internal switch between V_{DD} and BST1 charges the BST1 - LX1 flying capacitor, while the low-side MOSFET is on (DL1 pulled high).
37–43	D0–D6	Low-Voltage (1.0V Logic) VID DAC Code Inputs. The D0–D6 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. The output voltage is set by the VID code indicated by the logic-level voltages on D0–D6 (see Table 4).
44	$\overline{SHDN}$	Shutdown Control Input. Connect to V_{CC} for normal operation. Connect to ground to put the IC into the 1µA (max at T_A = +25°C) shutdown state. During startup, the output voltage is ramped up at 1/8 the slew rate set by the TIME resistor to the boot voltage. During the transition from normal operation to shutdown, the output voltage is ramped down at 1/8 the slew rate set by the TIME resistor. Forcing $\overline{SHDN}$ to 11V ~ 13V disables overvoltage protection, undervoltage protection, and thermal shutdown, clears the fault latches, disables transient phase overlap, disables soar suppression, and turns off the internal BST_-to-V_{DD} switches. However, internal diodes still exist between BST_ and V_{DD} in this state.
45	DPRSLPVR	3.3V Logic Input. Indicates power usage and sets the operating mode together with $\overline{PSI}$ as shown in the truth table below. When DPRSLPVR is forced high, the controller is immediately set to 1-phase automatic pulse-skipping mode. The controller returns to forced-PWM mode when DPRSLPVR is forced low **and** the output is in regulation. The PWRGD upper threshold is blanked during any downward output voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete and the output reaches regulation. During this blanking period, the overvoltage fault threshold is changed from a tracking [VID + 300mV] threshold to a fixed 1.8V threshold. DPRSLPVR / $\overline{PSI}$ / Mode 1 / 0 / Very low current (1-phase skip) 1 / 1 / Low current (approx 3A) (1-phase skip) 0 / 0 / Intermediate power potential (1-phase PWM) 0 / 1 / Max power potential (full-phase PWM: 2-phase or 1-phase as set by user at CSP2) The controller is in 2-phase skip mode during startup, but is in 2-phase forced-PWM mode during soft-shutdown, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. The controller is in 2-phase skip mode while in boot mode, but is in 2-phase forced-PWM mode during the transition from boot mode to VID mode, irrespective of the DPRSLPVR and $\overline{PSI}$ logic levels. However, if phase 2 is disabled by connecting CSP2 to V_{CC}, then only phase 1 is active in the above modes.

Pin Description (continued)

PIN	NAME	FUNCTION
46	$\overline{DPRSTP}$	Low-Voltage Logic Input Signal. This is usually the logical complement of the DPRSLPVR signal. However, there is a special condition during C4 exit when both $\overline{DPRSTP}$ and DPRSLPVR could temporarily be simultaneously high. If this happens, the MAX17410 reduces the slew rate to 1/4 the normal (R_{TIME}-based) slew rate for the duration of this condition. The slew rate returns to normal when this condition is exited. Note that only DPRSLPVR and $\overline{PSI}$ (but **not** $\overline{DPRSTP}$) determine the mode of operation (PWM vs. skip and number of active phases). DPRSLPVR / $\overline{DPRSTP}$ / Functionality 0 / 0 / Normal slew rate, 1- or 2-phase forced-PWM mode (DPRSLPVR low ➔ $\overline{DPRSTP}$ is ignored) 0 / 1 / Normal slew rate, 1- or 2-phase forced-PWM mode (DPRSLPVR low ➔ $\overline{DPRSTP}$ is ignored) 1 / 0 / Normal slew rate, 1-phase automatic pulse-skipping mode 1 / 1 / Slew rate reduced to 1/4th of normal, 1-phase automatic pulse-skipping mode
47	$\overline{CLKEN}$	Clock Enable CMOS Push-Pull Logic Output Powered by V3P3. This inverted logic output indicates when the output voltage sensed at FB is in regulation. $\overline{CLKEN}$ is forced high in shutdown and during soft-start and soft-stop transitions. $\overline{CLKEN}$ is forced low during dynamic VID transitions and for an additional 20µs after the transition is completed. $\overline{CLKEN}$ is the inverse of PWRGD, except for the 5ms PWRGD startup delay period after $\overline{CLKEN}$ is pulled low. See the startup timing diagram (Figure 9). The $\overline{CLKEN}$ upper threshold is blanked during any downward output voltage transition that happens when the controller is in skip mode, and stays blanked until the slew-rate-controlled internal-transition-related PWRGD blanking period is complete **and** the output reaches regulation.
48	V3P3	3.3V Supply Input for the $\overline{CLKEN}$ CMOS Push-Pull Logic Output. Connect to the 3.0V to 3.6V system supply voltage.
—	EP	Exposed Backplate (Paddle) of Package. Internally connected to analog ground. Connect to the ground plane through a thermally enhanced via.

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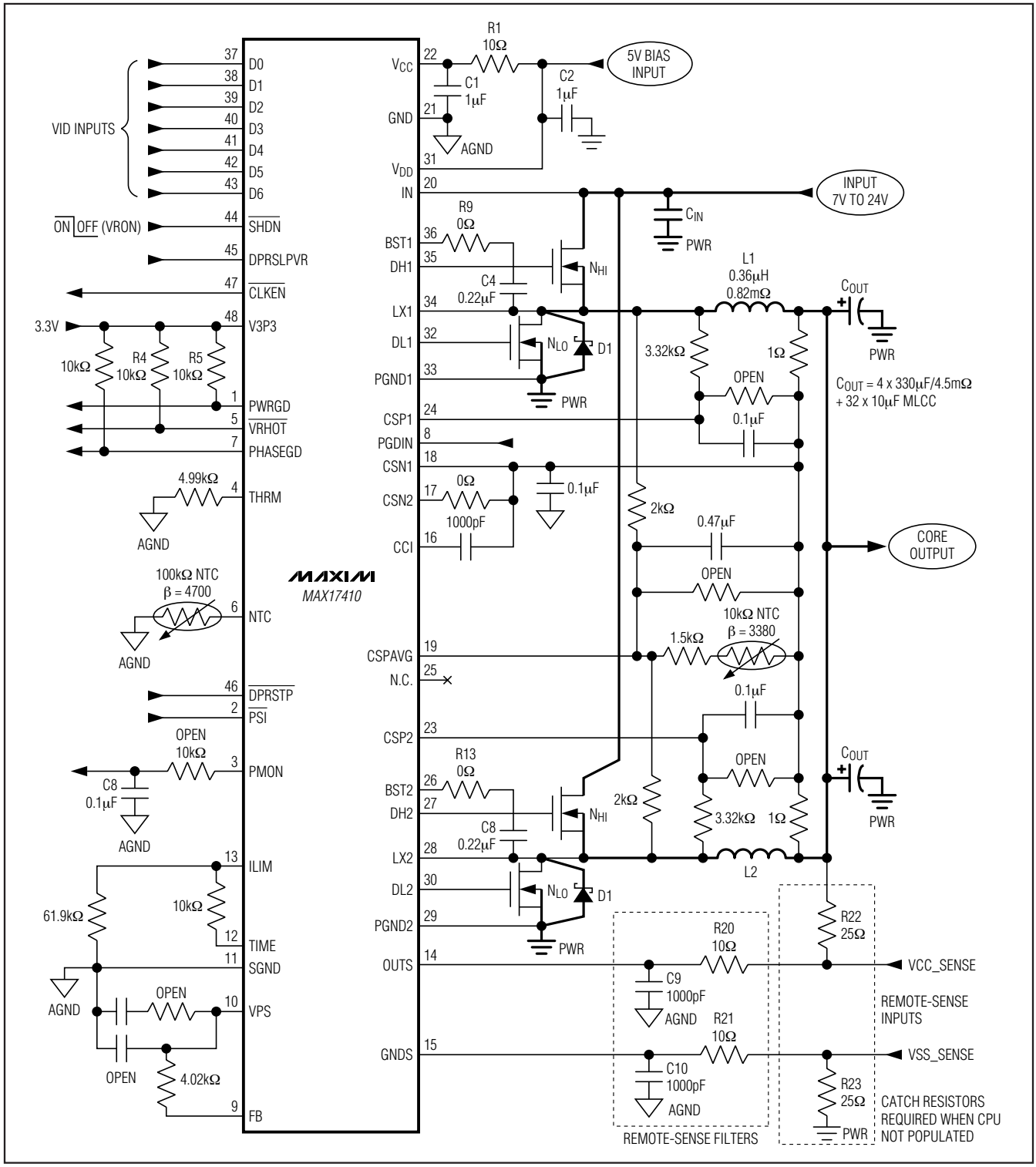

Figure 1. Standard 2-Phase IMVP6+ Application Circuit

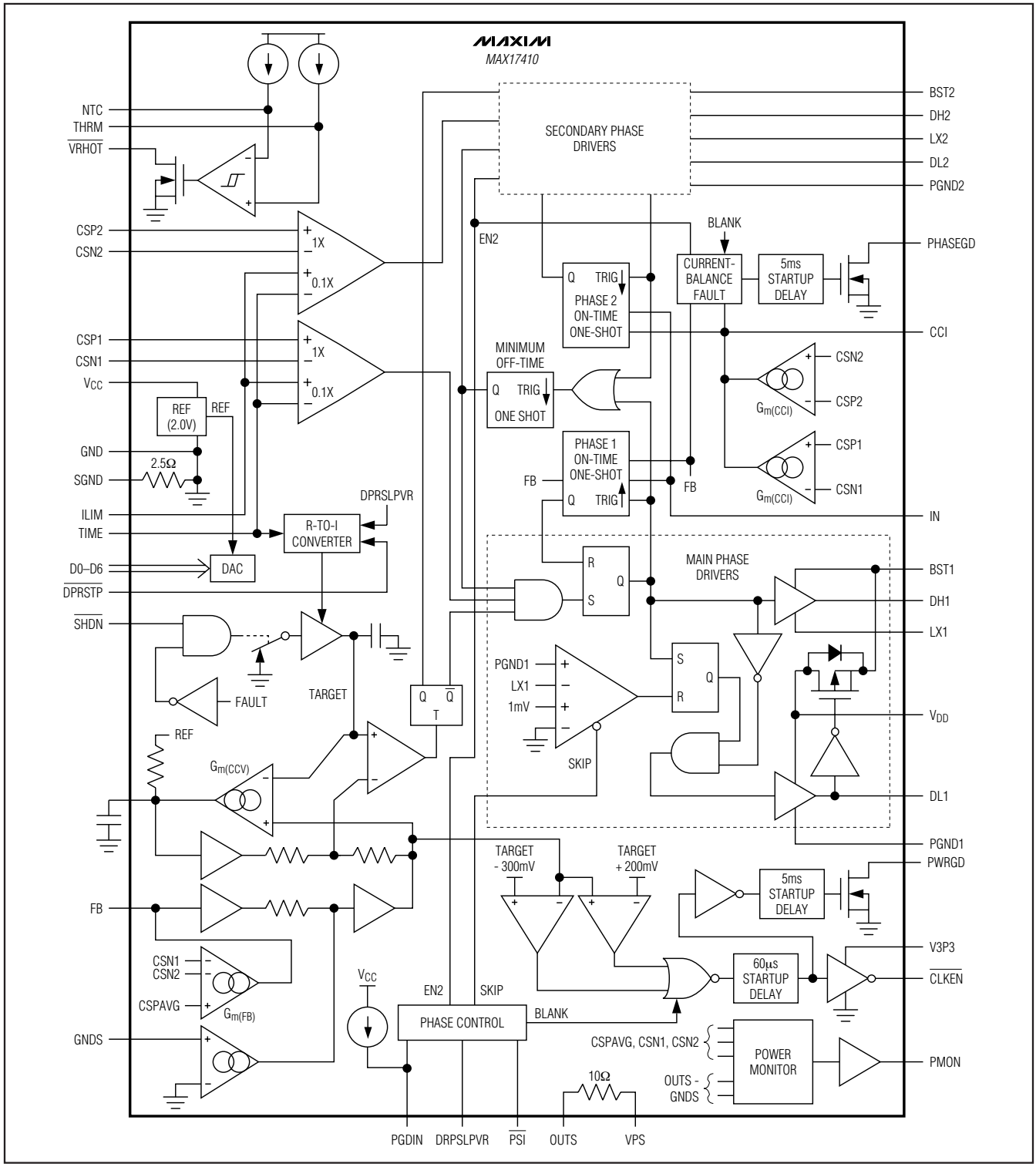

Figure 2. Functional Diagram

Dual-Phase, Quick-PWM Controller for IMVP6+ CPU Core Power Supplies

Table 1. Component Selection for Standard Applications

DESIGN PARAMETERS	IMVP6+ SV	IMVP6+ LV
Circuit	Figure 1	Figure 1
Input Voltage Range	7V to 20V	7V to 20V
Maximum Load Current	44A (34A)	23A (19A)
Transient Load Current	35A (10A/µs)	18A (10A/µs)
Load Line	-2.1mV/A	-4mV/A
Inductance (L)	NEC/Tokin MPC1055LR36 0.36µH, 32A, 0.8mΩ	NEC/Tokin MPC1055LR36 0.36µH, 32A, 0.8mΩ
High-Side MOSFET (N_H)	Siliconix 1x Si4386DY 7.8mΩ/9.5mΩ (typ/max)	Siliconix 1x Si4386DY 7.8mΩ/9.5mΩ (typ/max)
Low-Side MOSFET (N_L)	Siliconix 2x Si4642DY 3.9mΩ/4.7mΩ (typ/max)	Siliconix 2x Si4642DY 3.9mΩ/4.7mΩ (typ/max)
Output Capacitors (C_{OUT})	3x 330µF, 6mΩ, 2.5V Panasonic EEFSX0D0D331XR 28x 10µF, 6V ceramic (0805)	3x 330µF, 6mΩ, 2.5V Panasonic EEFSX0D0D331XR 28x 10µF, 6V ceramic (0805)
Input Capacitors (C_{IN})	4x 10µF, 25V ceramic (1210)	4x 10µF, 25V ceramic (1210)
TIME-ILIM Resistance (R1)	10kΩ	6.19kΩ
ILIM-GND Resistance (R2)	61.9kΩ	64.9kΩ
FB Resistance (R_{FB})	4.02kΩ	7.68kΩ
LX-CSP Resistance (R5)	2kΩ	2kΩ
CSP-CSN Series Resistance (R6)	1.50kΩ	1.50kΩ
Parallel NTC Resistance (R7)	open	open
DCR Sense NTC (NTC1)	10kΩ NTC B = 3380 TDK NTCG163JH103F	10kΩ NTC B = 3380 TDK NTCG163JH103F
DCR Sense Capacitance (C_{SENSE})	0.47µF, 6V ceramic (0805)	0.47µF, 6V ceramic (0805)

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
AVX Corporation	www.avxcorp.com
BI Technologies	www.bitechnologies.com
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp.	www.kemet.com
NEC/TOKIN America, Inc.	www.nec-tokin.com
Panasonic Corp.	www.panasonic.com

MANUFACTURER	WEBSITE
Pulse Engineering	www.pulseeng.com
Renesas Technology Corp.	www.renesas.com
SANYO Electric Co., Ltd.	www.sanyodevice.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com
Vishay/Siliconix	www.vishay.com

MAX17410 Detailed Description

Free-Running, Constant On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to the input voltage, and directly proportional to the output voltage or the difference between the main and secondary inductor currents (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low, the inductor current of the selected phase is below the valley current-limit threshold, and the minimum off-time one-shot times out. The controller maintains 180° out-of-phase operation by alternately triggering the main and secondary phases after the error comparator drops below the output-voltage set point.

Dual 180° Out-of-Phase Operation

The two phases in the MAX17410 operate 180° out-of-phase to minimize input and output filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making the MAX17410 ideal for high-power, cost-sensitive applications.

Typically, switching regulators provide power using only one phase instead of dividing the power among several phases. In these applications, the input capacitors must support high instantaneous current requirements. The high RMS ripple current can lower efficiency due to I^2R power loss associated with the input capacitor's effective series resistance (ESR). Therefore, the system typically requires several low-ESR input capacitors in parallel to minimize input voltage ripple, to reduce ESR-related power losses, and to meet the necessary RMS ripple current rating.

With the MAX17410, the controller shares the current between two phases that operate 180° out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of either phase is effectively halved, resulting in reduced input voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). Therefore, the same performance may be achieved with fewer or less expensive input capacitors.

+5V Bias Supply (V_{CC} and V_{DD})

The Quick-PWM controller requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient +5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the +5V bias supply can be generated with an external linear regulator.

The +5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW}\left(Q_{G(LOW)} + Q_{G(HIGH)}\right)$$

where I_{CC} is provided in the *Electrical Characteristics* table, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V_{IN} and V_{DD} can be connected together if the input power source is a fixed +4.5V to +5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency

IN (Pin 20) Open-Circuit Protection

The MAX17410 input sense (IN) is used to adjust the on-time. An internal resistor sets the switching frequency to 300kHz per phase. IN is high impedance in shutdown.

On-Time One-Shot

The core of each phase contains a fast, low-jitter, adjustable one-shot that sets the high-side MOSFET's on-time. The one-shot for the main phase varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the V+ input, and proportional to the feedback voltage (V_{FB}):

$$t_{ON(MAIN)} = \frac{t_{SW}\left(V_{FB} + 0.075V\right)}{V_{IN}}$$

where the switching period (t_{SW} = 1/f_{SW}) is set to 3.3µs internally, and 0.075V is an approximation to accommodate the expected drop across the low-side MOSFET switch.

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The one-shot for the secondary phase varies the on-time in response to the input voltage and the difference between the main and secondary inductor currents. Two identical transconductance amplifiers integrate the difference between the master and slave current-sense signals. The summed output is internally connected to CCI, allowing adjustment of the integration time constant with a compensation network connected between CCI and FB. The resulting compensation current and voltage are determined by the following equations:

$$I_{CCI} = G_m\left(V_{CSP1} - V_{CSN1}\right) - G_m\left(V_{CSP2} - V_{CSP2}\right)$$

$$V_{CCI} = V_{FB} + I_{CCI}Z_{CCI}$$

where Z_{CCI} is the impedance at the CCI output. The secondary on-time one-shot uses this integrated signal (V_{CCI}) to set the secondary high-side MOSFET's on-time. When the main and secondary current-sense signals become unbalanced, the transconductance amplifiers adjust the secondary on-time, which increases or decreases the secondary inductor current until the current-sense signals are properly balanced:

$$t_{ON(SEC)} = t_{SW}\left(\frac{V_{CCI} + 0.075V}{V_{IN}}\right)$$

$$= t_{SW}\left(\frac{V_{FB} + 0.075V}{V_{IN}}\right) + t_{SW}\left(\frac{I_{CCI}Z_{CCI}}{V_{IN}}\right)$$

$$= \left(\text{Main On-time}\right) + \left(\text{Secondary Current Balance Correction}\right)$$

This algorithm results in a nearly constant switching frequency and balanced inductor currents despite the lack of a fixed-frequency clock generator. The constant switching frequency allows the inductor ripple-current operating point to remain relatively constant, resulting in easy design methodology and predictable output voltage ripple.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* table are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, output capacitor ESR, and PCB copper losses in the output and ground tend to raise the switching frequency at higher output currents. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only during forced-PWM operation and dynamic output voltage transitions when the inductor current reverses at light or negative load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH rising dead time. For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency (per phase) is:

$$f_{SW} = \frac{\left(V_{OUT} + V_{DIS}\right)}{t_{ON}\left(V_{IN} + V_{DIS} - V_{CHG}\right)}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; V_{CHG} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time as defined in the *Electrical Characteristics* table.

Current Sense

The output current of each phase is sensed. Low offset amplifiers are used for current balance, voltage-positioning gain, and current limit. Sensing the current at the output of each phase offers advantages, including less noise sensitivity, more accurate current sharing between phases, and the flexibility of using either a current-sense resistor or the DC resistance of the output inductor.

Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and power monitor. This current-sense method uses an RC filtering network to extract the current information from the output inductor (see Figure 3). The resistive divider used should provide a current-sense resistance (R_{CS}) low enough to meet the current-limit requirements, and the time constant of the RC network should match the inductor's time constant (L/R_{CS}):

$$R_{CS} = \left(\frac{R2}{R1 + R2}\right)R_{DCR}$$

and:

$$R_{CS} = \frac{L}{C_{EQ}}\left[\frac{1}{R1} + \frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance, and R_{DCR} is the inductor's series DC resistance. Use the worst-case inductance and R_{DCR} values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load. To minimize the current-sense error due to the current-sense inputs' bias current ($I_{CSP\_}$ and $I_{CSN\_}$), choose R1 ll R2 to be less than 2kΩ and use the above equation to

determine the sense capacitance (C_{EQ}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage Positioning and Loop Compensation* section for detailed information.

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 3). The ESL-induced voltage step does not affect the average current-sense voltage, but results in a significant peak current-sense voltage error that results in unwanted offsets in the regulation voltage and results in early current-limit detection. Similar to the inductor DCR sensing method, the RC filter's time constant should match the L/R time constant formed by the current-sense resistor's parasitic inductance:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R1$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is current-sense resistance value, C_{EQ} and R1 are the time-constant matching components.

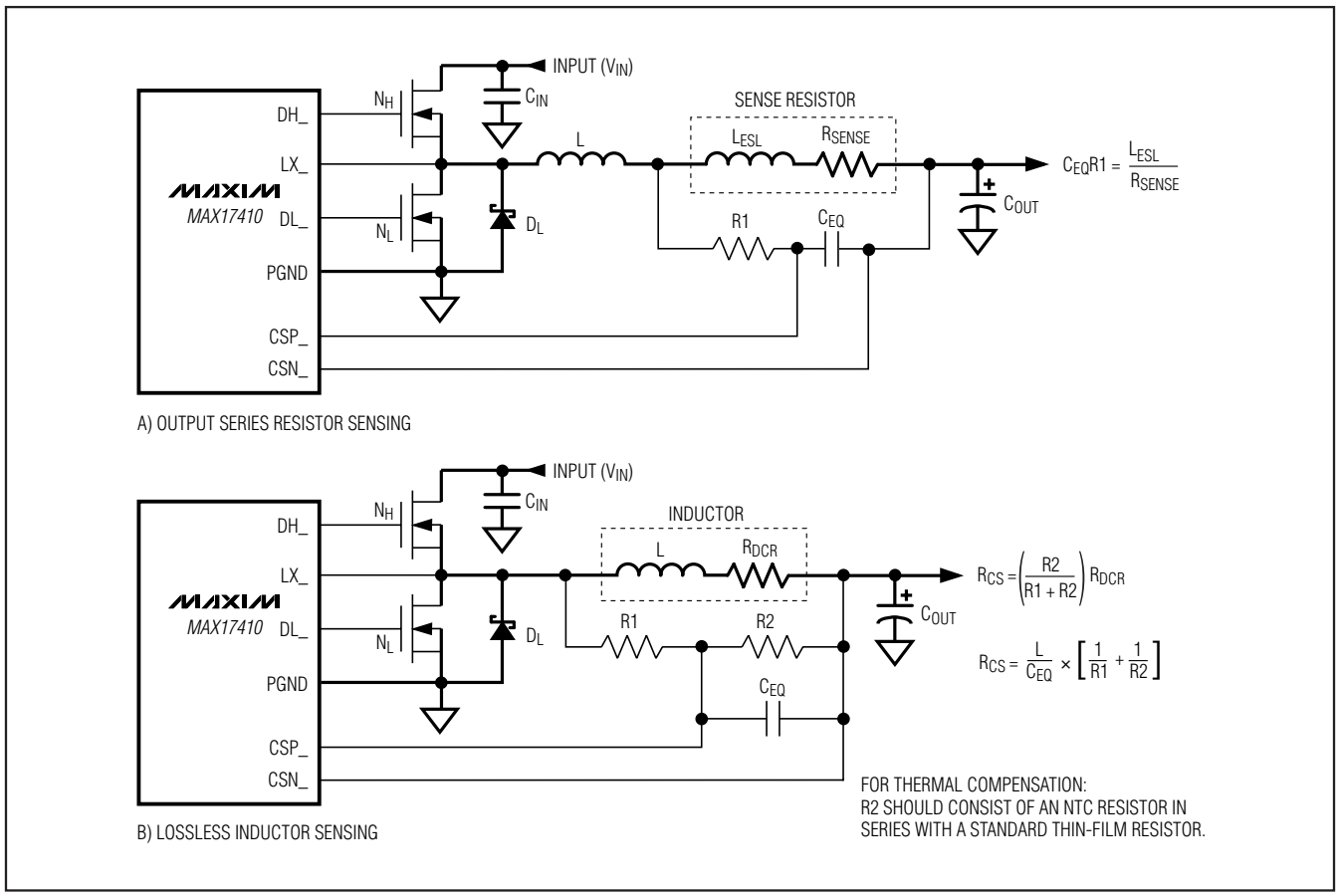

Figure 3. Current-Sense Methods