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EVALUATION KIT AVAILABLE

AMD 2-/3-Output Mobile Serial VID Controller

General Description

The MAX17480 is a triple-output, step-down, fixed-frequency controller for AMD's serial VID interface (SVI) CPU and northbridge (NB) core supplies. The MAX17480 consists of two high-current SMPSs for the CPU cores and one 4A internal switch SMPS for the NB core. The two CPU core SMPSs run 180° out-of-phase for true interleaved operation, minimizing input capacitance. The 4A internal switch SMPS runs at twice the switching frequency of the core SMPS, reducing the size of the external components.

The MAX17480 is fully AMD SVI compliant. Output voltages are dynamically changed through a 2-wire SVI, allowing the SMPSs to be individually programmed to different voltages. A slew-rate controller allows controlled transitions between VID codes and controlled soft-start. SVI also allows each SMPS to be individually set into a low-power pulse-skipping state.

Transient phase repeat improves the response of the fixed-frequency architecture, reducing the total output capacitance for the CPU core. A thermistor-based temperature sensor provides a programmable thermal-fault output ($\overline{VRHOT}$).

The MAX17480 includes output overvoltage protection (OVP), undervoltage protection (UVP), and thermal protection. When any of these protection features detect a fault, the controller shuts down. True differential current sensing improves current limit and load-line accuracy. The MAX17480 has an adjustable switching frequency, allowing 100kHz to 600kHz operation per core SMPS, and twice that for the NB SMPS.

Applications

Mobile AMD SVI Core Supplies

Multiphase CPU Core Supplies

Voltage-Positioned, Step-Down Converters

Notebook/Desktop Computers

Pin Configuration appears at end of data sheet.

Features

- **Dual-Output Fixed-Frequency Core Supply Controller**
  - **Split or Combinable Outputs Detected at Power-Up**
  - **Dynamic Phase Selection Optimizes Active/Sleep Efficiency**
  - **Transient Phase Repeat Reduces Output Capacitance**
  - **True Out-of-Phase Operation Reduces Input Capacitance**
  - **Programmable AC and DC Droop**
  - **Accurate Current Balance and Current Limit**
  - **Integrated Drivers for Large Synchronous-Rectifier MOSFETs**
  - **Programmable 100kHz to 600kHz Switching Frequency**
  - **4V to 26V Battery Input Voltage Range**
- **4A Internal Switch Northbridge SMPS**
  - **2.7V to 5.5V Input Voltage Range**
  - **2x Programmable Switching Frequency**
  - **75mΩ/40mΩ Power Switches**
- **±0.5% V_{OUT} Accuracy over Line, Load, and Temperature**
- **AMD SVI-Compliant Serial Interface with Switchable Address**
- **7-Bit On-Board DAC: 0 to +1.550V Output Adjust Range**
- **Integrated Boost Switches**
- **Adjustable Slew-Rate Control**
- **Power-Good (PWRGD) and Thermal-Fault ($\overline{VRHOT}$) Outputs**
- **System Power-OK (PGD_IN) Input**
- **Overvoltage, Undervoltage, and Thermal-Fault Protection**
- **Voltage Soft-Startup and Passive Shutdown**
- **< 1µA Typical Shutdown Current**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17480GTL+	-40°C to +105°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

AMD 2-/3-Output Mobile Serial VID Controller

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{DD}, V_{IN3}, V_{CC}, V_{DDIO} to AGND .....-0.3V to +6V
PWRGD to AGND .....-0.3V to +6V
$\overline{SHDN}$ to AGND .....-0.3V to +6V
GNDS1, GNDS2, THRM, $\overline{VRHOT}$ to AGND .....-0.3V to +6V
CSP_, CSN_, ILIM12 to AGND .....-0.3V to +6V
SVC, SVD, PGD_IN to AGND .....-0.3V to +6V
FBDC_, FBAC_, OUT3 to AGND .....-0.3V to +6V
OSC, TIME, OPTION, ILIM3 to AGND .....-0.3V to (V_{CC} + 0.3V)
BST1, BST2 to AGND .....-0.3V to +36V
BST1, BST2 to V_{DD} .....-0.3V to +30V
BST3 to AGND .....(V_{DD} - 0.3V) to (V_{LX3} + 6V)
LX1 to BST1 .....-6V to +0.3V
LX3 RMS Current (Note 2) .....±4A
LX2 to BST2 .....-6V to +0.3V
LX3 to PGND (Note 2) .....-0.6V to +6V
DH1 to LX1 .....-0.3V to (V_{BST1} + 0.3V)
DH2 to LX2 .....-0.3V to (V_{BST2} + 0.3V)
DL1 to PGND .....-0.3V to (V_{DD} + 0.3V)
DL2 to PGND .....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 22.2mW/°C above +70°C) 1778mW
Operating Temperature Range .....-40°C to +105°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Absolute Maximum Ratings measured with 20MHz scope bandwidth.

Note 2: LX3 has clamp diodes to PGND and IN3. If continuous current is applied through these diodes, thermal limits must be observed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLIES						
Input Voltage Range	V_{IN}	Drain of external high-side MOSFET	4		26	V
	V_{BIAS}	V_{CC}, V_{DD}	4.5		5.5	
	V_{IN3}		2.7		5.5	
	V_{DDIO}		1.0		2.7	
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	V_{CC} rising, 50mV typical hysteresis, latched, UV fault	4.10	4.25	4.45	V
V_{CC} Power-On Reset Threshold		Falling edge, typical hysteresis = 1.1V, faults cleared and DL_ forced high when V_{CC} falls below this level		1.8		V
V_{DDIO} Undervoltage-Lockout Threshold		V_{DDIO} rising, 100mV typical hysteresis, latched, UV fault	0.7	0.8	0.9	V
V_{IN3} Undervoltage-Lockout Threshold		V_{IN3} rising, 100mV typical hysteresis	2.5	2.6	2.7	V
Quiescent Supply Current (V_{CC})	I_{CC}	Skip mode, FBDC_ and OUT3 forced above their regulation points		5	10	mA
Quiescent Supply Currents (V_{DD})	I_{DD}	Skip mode, FBDC_ and OUT3 forced above their regulation points, T_A = +25°C		0.01	1	µA
Quiescent Supply Current (V_{DDIO})	I_{DDIO}			10	25	µA
Quiescent Supply Current (IN3)	I_{IN3}	Skip mode, OUT3 forced above its regulation point		50	200	µA
Shutdown Supply Current (V_{CC})		$\overline{SHDN}$ = GND, T_A = +25°C		0.01	1	µA

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown Supply Currents (V_{DD})		$\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
Shutdown Supply Current (V_{DDIO})		$\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
Shutdown Supply Current (IN3)		$\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
INTERNAL DACs, SLEW RATE, PHASE SHIFT							
DC Output Voltage Accuracy (Note 1)	V_{OUT}	Measured at FBDC_ for the core SMPSs; measured at OUT3 for the NB SMPS; 30% duty cycle, no load, ILIM3 = V_{CC}, V_{OUT3} = V_{DAC3} + 12.5mV (Note 3)	DAC codes from 0.8375V to 1.5500V	-0.5		+0.5	%
			DAC codes from 0.5000V to 0.8250V	-5		+5	mV
			DAC codes from 12.5mV to 0.4875V	-10		+10	
OUT3 Offset					12.5		mV
SMPS1 to SMPS2 Phase Shift		SMPS2 starts after SMPS1			50		%
					180		Degrees
SMPS3 to SMPS1 and SMPS2 Phase Shift		SMPS3 starts after SMPS1 or SMPS2			25		%
Slew-Rate Accuracy		During transition	R_{TIME} = 143kΩ, SR = 6.25mV/µs	-10		+10	%
			R_{TIME} = 35.7kΩ to 357kΩ, SR = 25mV/µs to 2.5mV/µs	-15		+15	
		Startup			1		mV/µs
FBAC_ Input Bias Current	$I_{FBAC\_}$	CSP_ = CSN_, T_A = +25°C		-3		+3	µA
FBDC_ Input Bias Current	$I_{FBDC\_}$	T_A = +25°C		-250		+250	nA
Switching Frequency Accuracy	f_{OSC1}, f_{OSC2}, f_{OSC3}	R_{OSC} = 143kΩ (f_{OSC1} = f_{OSC2} = 300kHz nominal, f_{OSC3} = 600kHz nominal)		-7		+7	%
		R_{OSC} = 71.4kΩ (f_{OSC1} = f_{OSC2} = 600kHz nominal, f_{OSC3} = 1.2MHz nominal) to 432kΩ (f_{OSC1} = f_{OSC2} = 99kHz nominal, f_{OSC3} = 199kHz nominal)		-9		+9	
SMPS1 AND SMPS2 CONTROLLERS							
DC Load Regulation		Either SMPS, PWM mode, droop disabled; zero to full load			-0.1		%
Line Regulation Error		Either SMPS, 4V < V_{IN} < 26V			0.03		%/V
GNDS_ Input Range	$V_{GNDS\_}$	Separate mode		-200		+200	mV
GNDS_ Gain	$A_{GNDS\_}$	Separate: $\Delta V_{OUT\_}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV; combined: $\Delta V_{OUT}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV		0.95	1.00	1.05	V/V
GNDS_ Input Bias Current	$I_{GNDS\_}$	T_A = +25°C		-2		+2	µA

AMD 2-/3-Output Mobile Serial VID Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Combined-Mode Detection Threshold		GNDS1, GNDS2, detection after REFOK, latched, cleared by cycling $\overline{SHDN}$	0.7	0.8	0.9	V
Maximum Duty Factor	D_{MAX}		90	92		%
Minimum On-Time	t_{ONMIN}				150	ns
SMPS1 AND SMPS2 CURRENT LIMIT						
Current-Limit Threshold Tolerance	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$ = 0.052 x (V_{REF} - V_{ILIM}), (V_{REF} - V_{ILM}) = 0.2V to 1.0V	-3		+3	mV
Zero-Crossing Threshold	V_{ZX}	$V_{GND\_}$ - $V_{LX\_}$, skip mode		1		mV
Idle Mode™ Threshold	V_{IMIN}	$V_{CSP\_}$ - $V_{CSN\_}$, skip mode, 0.15 x V_{LIMIT}	-2		+2	mV
CS_ Input Leakage Current		CSP_ and CSN_, T_A = +25°C	-0.2		+0.2	µA
CS_ Common-Mode Input Range		CSP_ and CSN_	0		2	V
SMPS1 AND SMPS2 DROOP, CURRENT BALANCE, AND TRANSIENT RESPONSE						
AC Droop and Current Balance Amplifier Transconductance	$G_{m(FBAC\_)}$	$\Delta I_{FBAC\_}/(\Delta V_{CS\_})$, $V_{FBAC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = 0 to +40mV	1.94	2.00	2.06	mS
AC Droop and Current Balance Amplifier Offset		$I_{FBAC\_}/G_{m(FBAC\_)}$	-1.5		+1.5	mV
No-Load Positive Offset		OPTION = 2V or GND		+12.5		mV
Transient Detection Threshold		Measured at FBDC_ with respect to steady-state FBDC_ regulation voltage, 10mV hysteresis (typ)	-47	-41	-33	mV
SMPS3 INTERNAL 4A STEP-DOWN CONVERTER						
OUT3 Load Regulation	R_{DROOP3}		4	5.5	7	mV/A
OUT3 Line Regulation		0 to 100% duty cycle		5		mV
OUT3 Input Current	I_{OUT3}	T_A = +25°C	-100	-5	+100	nA
LX3 Leakage Current	I_{LX3}	$\overline{SHDN}$ = GND, V_{LX3} = GND or 5.5V, V_{IN3} = 5.5V, T_A = +25°C	-20		+20	µA
Internal MOSFET On-Resistance	$R_{ON(NH3)}$	High-side n-channel		75	150	mΩ
	$R_{ON(NL3)}$	Low-side n-channel		40	75	
LX3 Peak Current Limit	I_{LX3PK}	ILIM3 = V_{CC}	4.75	5.25	6	A
		ILIM3 = GND	3.75	4.25	5	
LX3 Idle-Mode Trip Level	I_{LX3MIN}	Percentage of I_{LX3PK}		25		%
LX3 Zero-Crossing Trip Level	I_{ZX3}	Skip mode		20		mA
Maximum Duty Factor	D_{MAX}		84	87		%
Minimum On-Time	t_{ONMIN}				150	ns

Idle Mode is a trademark of Maxim Integrated Products, Inc.

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT DETECTION							
Output Overvoltage Trip Threshold (SMPS1 and SMPS2 Only)	$V_{OVP\_}$	Measured at FBDC_, rising edge	PWM mode	250	300	350	mV
			Skip mode and output has not reached the regulation voltage	1.80	1.85	1.90	V
			Minimum OVP threshold		0.8		
Output Overvoltage Fault Propagation Delay (SMPS1 and SMPS2 Only)	t_{OVP}	FBDC_ forced 25mV above trip threshold			10		µs
Output Undervoltage Protection Trip Threshold	V_{UVP}	Measured at FBDC_ or OUT3 with respect to unloaded output voltage		-450	-400	-350	mV
Output Undervoltage Fault Propagation Delay	t_{UVP}	FBDC_ forced 25mV below trip threshold			10		µs
PWRGD Threshold		Measured at FBDC_ or OUT3 with respect to unloaded output voltage,15mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350	-300	-250	mV
			Upper threshold, rising edge (overvoltage)	+150	+200	+250	
PWRGD Propagation Delay	t_{PWRGD}	FBDC_ or OUT3 forced 25mV outside the PWRGD trip thresholds			10		µs
PWRGD, Output Low Voltage		I_{SINK} = 4mA				0.4	V
PWRGD Leakage Current	I_{PWRGD}	High state, PWRGD forced to 5.5V, T_A = +25°C				1	µA
PWRGD Startup Delay and Transition Blanking Time	t_{BLANK}	Measured from the time when FBDC_ and OUT3 reach the target voltage			20		µs
$\overline{VRHOT}$ Trip Threshold		Measured at THRM, with respect to V_{CC}, falling edge, 115mV hysteresis (typ)		29.5	30	30.5	%
$\overline{VRHOT}$ Delay	$t_{\overline{VRHOT}}$	THRM forced 25mV below the $\overline{VRHOT}$ trip threshold, falling edge			10		µs
$\overline{VRHOT}$, Output Low Voltage		I_{SINK} = 4mA				0.4	V
$\overline{VRHOT}$ Leakage Current		High state, $\overline{VRHOT}$ forced to 5V, T_A = +25°C				1	µA
THRM Input Leakage		T_A = +25°C		-100		+100	nA
Thermal-Shutdown Threshold	$T_{\overline{SHDN}}$	Hysteresis = 15°C			+160		°C
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V (Note 4)	High state (pullup)		0.9	2.5	Ω
			Low state (pulldown)		0.7	2.5	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	DL_, high state			0.7	2.0	Ω
		DL_, low state			0.25	0.6	

AMD 2-/3-Output Mobile Serial VID Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DH_ Gate-Driver Source/Sink Current	$I_{DH\_}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V		2.2		A
DL_ Gate-Driver Source Current	$I_{DL\_}$	DL_ forced to 2.5V		2.7		A
DL_ Gate-Driver Sink Current	$I_{DL\_ (SINK)}$	DL_ forced to 2.5V		8		A
Dead Time	t_{DH_DL}	DH_ low to DL_ high	9	20	35	ns
	t_{DL_DH}	DL_ low to DH_ high	9	20	35	
Internal BST1, BST2 Switch R_{ON}		BST1, BST2 to V_{DD}, I_{BST1} = I_{BST2} = 10mA		10	20	Ω
Internal BST3 Switch R_{ON}		BST3 to V_{DD}, I_{BST3} = 10mA		10	20	Ω
2-WIRE I²C BUS LOGIC INTERFACE						
SVI Logic-Input Current		SVC, SVD, T_A = +25°C	-1		+1	µA
SVI Logic-Input Threshold		SVC, SVD, rising edge, hysteresis 0.14 x V_{DDIO} (V)	0.3 x V_{DDIO}		0.7 x V_{DDIO}	V
SVC Clock Frequency	f_{SVC}				3.4	MHz
START Condition Hold Time	$t_{HD;STA}$		160			ns
Repeated START Condition Setup Time	$t_{SU;STA}$		160			ns
STOP Condition Setup Time	$t_{SU;STO}$		160			ns
Data Hold	$t_{HD;DAT}$	A master device must internally provide a hold time of at least 300ns for the SVD signal (referred to the V_{IHMIN} of SVC signal) to bridge the undefined region of SVC's falling edge			70	ns
Data Setup Time	$t_{SU;DAT}$		10			ns
SVC Low Period	t_{LOW}		160			ns
SVC High Period	t_{HIGH}	Measured from 10% to 90% of V_{DDIO}	60			ns
SVC/SVD Rise and Fall Time	t_R, t_F	Input filters on SVD and SVC suppress noise spike less than 50ns			40	ns
Pulse Width of Spike Suppression				20		ns
INPUTS AND OUTPUTS						
Logic-Input Current		$\overline{SHDN}$, PGD_IN, T_A = +25°C	-1		+1	µA
		ILIM3, OPTION, T_A = +25°C	-200		+200	nA
Logic-Input Levels		$\overline{SHDN}$, rising edge, hysteresis = 225mV	0.8		2.0	V
Input Logic Levels		High, OPTION, ILIM3	V_{CC} - 0.4			V
		3.3V, OPTION	2.75		3.85	
		2V, OPTION	1.65		2.35	
		Low, OPTION, ILIM3			0.4	
PGD_IN Logic-Input Threshold		PGD_IN, rising edge, hysteresis = 65mV	0.3 x V_{DDIO}		0.7 x V_{DDIO}	V

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT SUPPLIES							
Input Voltage Range	V_{IN}	Drain of external high-side MOSFET		4		26	V
	V_{BIAS}	V_{CC}, V_{DD}		4.5		5.5	
	V_{IN3}			2.7		5.5	
	V_{DDIO}			1.0		2.7	
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	V_{CC} rising, 50mV typical hysteresis, latched, UV fault		4.10		4.45	V
V_{DDIO} Undervoltage-Lockout Threshold		V_{DDIO} rising, 100mV typical hysteresis, latched, UV fault		0.7		0.9	V
V_{IN3} Undervoltage-Lockout Threshold		V_{IN3} rising, 100mV typical hysteresis		2.5		2.7	V
Quiescent Supply Current (V_{CC})	I_{CC}	Skip mode, FBDC_ and OUT3 forced above their regulation points				10	mA
Quiescent Supply Current	I_{DDIO}					25	µA
Quiescent Supply Current (IN3)	I_{IN3}	Skip mode, OUT3 forced above its regulation point				200	µA
INTERNAL DACs, SLEW RATE, PHASE SHIFT							
DC Output Voltage Accuracy	V_{OUT}	Measured at FBDC_ for the core SMPSs; measured at OUT3 for the NB SMPS; 30% duty cycle, no load, ILIM3 = V_{CC}, V_{OUT3} = V_{DAC3} + 12.5mV (Note 3)	DAC codes from 0.8375V to 1.5500V	-0.7		+0.7	%
			DAC codes from 0.5000V to 0.8250V	-7.5		+7.5	mV
			DAC codes from 12.5mV to 0.4875V	-15		+15	
Slew-Rate Accuracy		During transition	R_{TIME} = 143kΩ, SR = 6.25mV/µs	-10		+10	%
			R_{TIME} = 35.7kΩ to 357kΩ, SR = 25mV/µs to 2.5mV/µs	-15		+15	
Switching Frequency Accuracy	f_{OSC1}, f_{OSC2}, f_{OSC3}	R_{OSC} = 143kΩ (f_{OSC1} = f_{OSC2} = 300kHz nominal, f_{OSC3} = 600kHz nominal)		-9		+9	%
		R_{OSC} = 71.4kΩ (f_{OSC1} = f_{OSC2} = 600kHz nominal, f_{OSC3} = 1.2MHz nominal) to 432kΩ (f_{OSC1} = f_{OSC2} = 99kHz nominal, f_{OSC3} = 199kHz nominal)		-12		+12	

AMD 2-/3-Output Mobile Serial VID Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SMPS1 AND SMPS2 CONTROLLERS						
GNDS_ Input Range	$V_{GNDS\_}$	Separate mode	-200		+200	mV
GNDS_ Gain	$A_{GNDS\_}$	Separate: $\Delta V_{OUT\_}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV; combined; $\Delta V_{OUT}/\Delta V_{GNDS\_}$, -200mV ≤ $V_{GNDS\_}$ ≤ +200mV	0.95		1.05	V/V
Combined-Mode Detection Threshold		GNDS1, GNDS2, detection after REFOK, latched, cleared by cycling $\overline{SHDN}$	0.7		0.9	V
Maximum Duty Factor	D_{MAX}		90			%
Minimum On-Time	t_{ONMIN}				150	ns
SMPS1 AND SMPS2 CURRENT LIMIT						
Current-Limit Threshold Tolerance	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$ = 0.052 x (V_{REF} - V_{ILIM}), (V_{REF} - V_{ILM}) = 0.2V to 1.0V	-3		+3	mV
Idle-Mode Threshold Tolerance	V_{IMIN}	$V_{CSP\_}$ - $V_{CSN\_}$, skip mode, 0.15 x V_{LIMIT}	-2		+2	mV
CS_ Common-Mode Input Range		CSP_ and CSN_	0		2	V
SMPS1 AND SMPS2 DROOP, CURRENT BALANCE, AND TRANSIENT RESPONSE						
AC Droop and Current Balance Amplifier Transconductance	$G_{m(FBAC\_)}$	$\Delta I_{FBAC\_}/(\Delta V_{CS\_})$, $V_{FBAC\_}$ = $V_{CSN\_}$ = 1.2V, $V_{CSP\_}$ - $V_{CSN\_}$ = 0 to +40mV	1.94		2.06	mS
AC Droop and Current Balance Amplifier Offset		$I_{FBAC\_}/G_{m(FBAC\_)}$	-1.5		+2.0	mV
Transient Detection Threshold		Measured at FBDC_ with respect to steady-state FBDC_ regulation voltage, 10mV hysteresis (typ)	-47		-33	mV
SMPS3 INTERNAL 4A STEP-DOWN CONVERTER						
OUT3 Load Regulation	R_{DROOP3}		4		7	mV/A
Internal MOSFET On-Resistance	$R_{ON(NH3)}$	High-side n-channel			150	mΩ
	$R_{ON(NL3)}$	Low-side n-channel			75	
LX3 Peak Current Limit	I_{LX3PK}	ILIM3 = V_{CC}, skip mode	4.75		6	A
Maximum Duty Factor	D_{MAX}		84			%
Minimum On-Time	t_{ONMIN}				150	ns

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT DETECTION							
Output Overvoltage Trip Threshold (SMPS1 and SMPS2 Only)	$V_{OVP\_}$	Measured at FBDC_, rising edge	PWM mode	250		350	mV
			Skip mode and output have not reached the regulation voltage	1.80		1.90	V
Output Undervoltage Protection Trip Threshold	V_{UVP}	Measured at FBDC_ or OUT3 with respect to unloaded output voltage		-450		-350	mV
PWRGD Threshold		Measured at FBDC_ or OUT3 with respect to unloaded output voltage, 15mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350		-250	mV
			Upper threshold, rising edge (overvoltage)	+150		+250	
PWRGD, Output Low Voltage		I_{SINK} = 4mA				0.4	V
$\overline{VRHOT}$ Trip Threshold		Measured at THRM, with respect to V_{CC}, falling edge, 115mV hysteresis (typ)		29.5		30.5	%
$\overline{VRHOT}$, Output Low Voltage		I_{SINK} = 4mA				0.4	V
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V (Note 4)	High state (pullup)			2.5	Ω
			Low state (pulldown)			2.5	
DL_ Gate-Driver On-Resistance	$R_{ON(DL\_)}$	DL_, high state				2.0	Ω
		DL_, low state				0.6	
Dead Time	t_{DH_DL}	DH_ low to DL_ high		9		35	ns
	t_{DL_DH}	DL_ low to DH_ high		9		35	
Internal BST1, BST2 Switch R_{ON}		BST1, BST2 to V_{DD}, I_{BST1} = I_{BST2} = 10mA				20	Ω
Internal BST3 Switch R_{ON}		BST3 to V_{DD}, I_{BST3} = 10mA				20	Ω
2-WIRE I²C BUS LOGIC INTERFACE							
SVI Logic-Input Threshold		SVC, SVD, rising edge, hysteresis = 0.14 x V_{DDIO}(V)		0.3 x V_{DDIO}		0.7 x V_{DDIO}	V
SVC Clock Frequency	f_{SVC}					3.4	MHz
START Condition Hold Time	$t_{SU;STA}$			160			ns
Repeated START Condition Setup Time	$t_{SU;STA}$			160			ns
STOP Condition Setup Time	$t_{SU;STO}$			160			ns
Data Hold	$t_{HD;DAT}$	A master device must internally provide a hold time of at least 300ns for the SVD signal (referred to the V_{IHMIN} of SVC signal) to bridge the undefined region of SVC's falling edge				70	ns

AMD 2-/3-Output Mobile Serial VID Controller

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{CC} = V_{DD} = V_{IN3} = $\overline{SHDN}$ = PGD_IN = 5V, V_{DDIO} = 1.8V, OPTION = GNDS_ = AGND = PGND, FBDC_ = FBAC_ = OUT3 = CSP_ = CSN_ = 1.2V, all DAC codes set to the 1.2V code, **T_A = -40°C to +105°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Data Setup Time	$t_{SU;DAT}$		10			ns
SVC Low Period	t_{LOW}		160			ns
SVC High Period	t_{HIGH}	Measured from 10% to 90% of V_{DDIO}	60			ns
SVC/SVD Rise and Fall Time	t_R, t_F	Input filters on SVD and SVC suppress noise spike less than 50ns			40	ns
INPUTS AND OUTPUTS						
Logic-Input Levels		$\overline{SHDN}$, rising edge, hysteresis = 225mV	0.8		2.0	V
Input Logic Levels		High, OPTION, ILIM3	V_{CC} - 0.4			V
		3.3V, OPTION	2.75		3.85	
		2V, OPTION	1.65		2.35	
		Low, OPTION, ILIM3			0.4	
PGD_IN Logic-Input Threshold		PGD_IN, rising edge, hysteresis = 65mV	0.3 x V_{DDIO}		0.7 x V_{DDIO}	V

Note 3: When the inductor is in continuous conduction, the output voltage has a DC regulation level lower than the error-comparator threshold by 50% of the ripple. In discontinuous conduction, the output voltage has a DC regulation level higher than the error-comparator threshold by 50% of the ripple. The core SMPSs have an integrator that corrects for this error. The NB SMPS has an offset determined by the ILIM3 pin, and a -6.5mV/A load line.

Note 4: Production testing limitations due to package handling require relaxed maximum on-resistance specifications for the TQFN package.

Note 5: Specifications to T_A = -40°C to +105°C are guaranteed by design, not production tested.

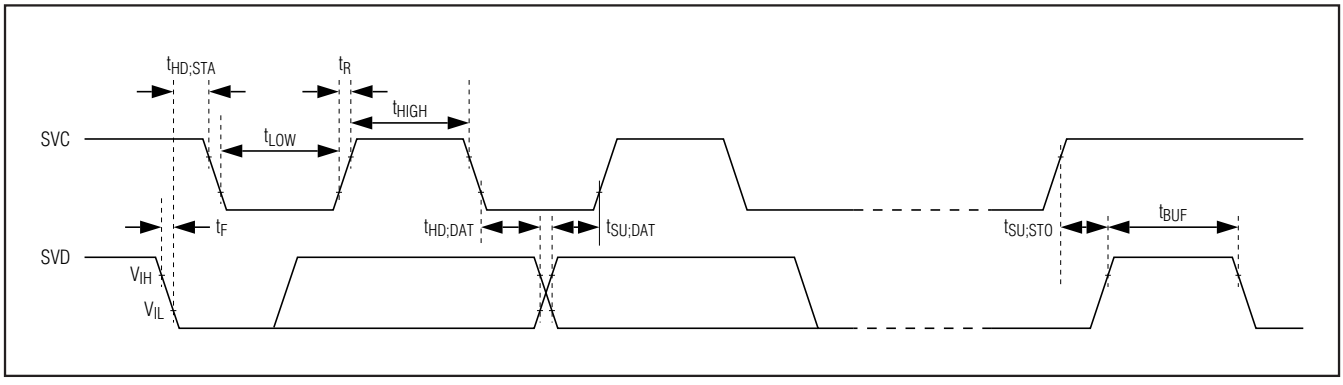
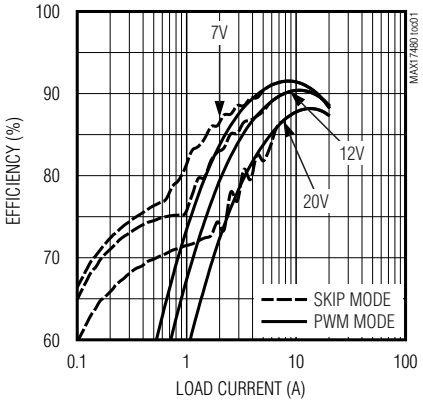


Figure 1. Timing Definitions Used in the Electrical Characteristics

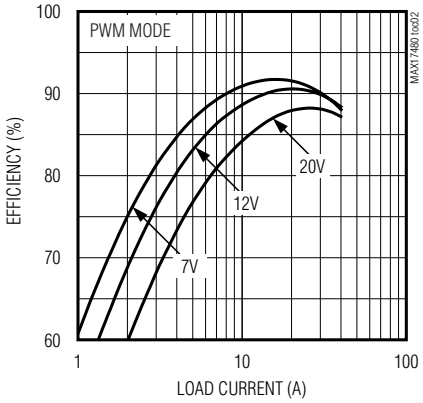
Typical Operating Characteristics

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

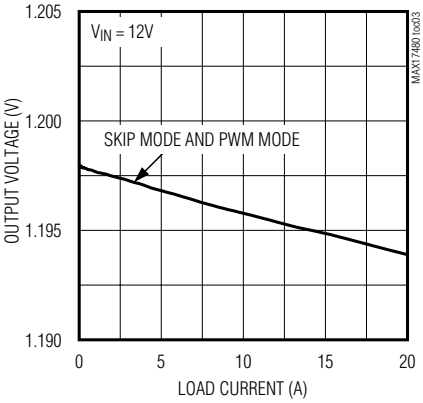
CORE SMPS 1-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.2V)



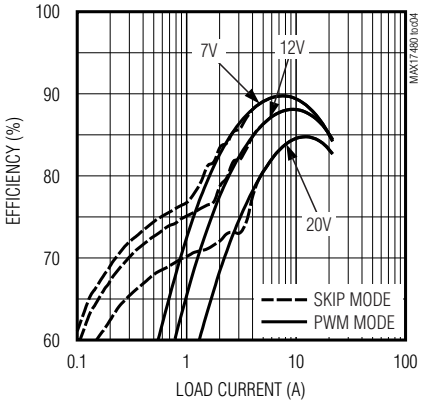
CORE SMPS 2-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.2V)



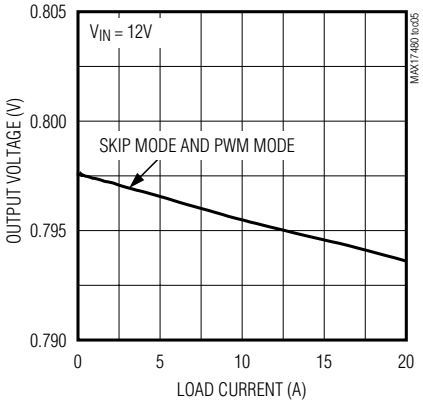
CORE SMPS OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 1.2V)



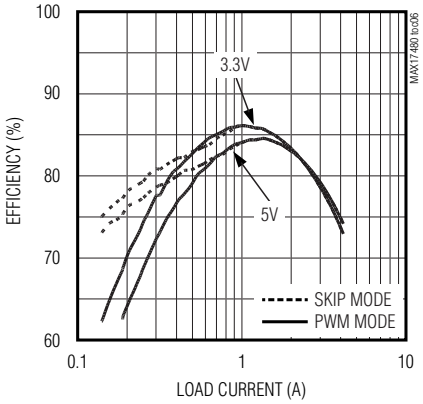
CORE SMPS 1-PHASE EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 0.8V)



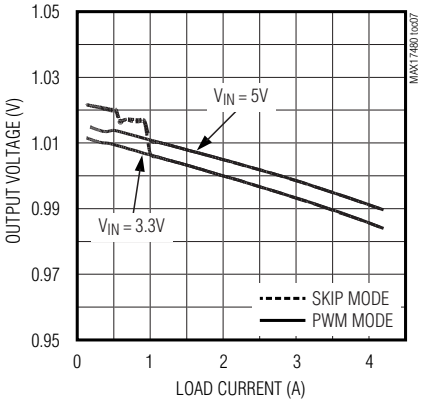
CORE SMPS OUTPUT VOLTAGE vs. LOAD CURRENT (V_{OUT} = 0.8V)



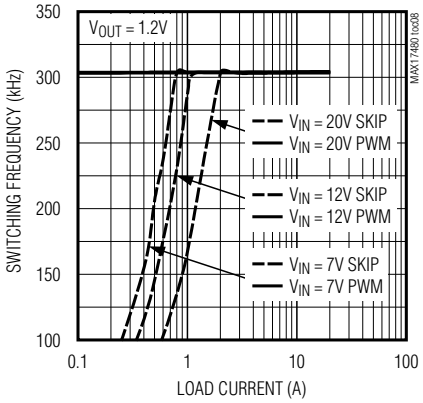
NB SMPS EFFICIENCY vs. LOAD CURRENT (1V)



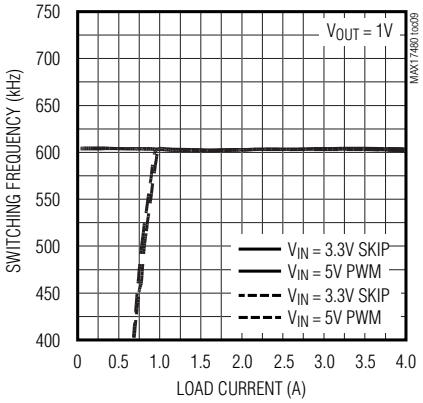
NB SMPS 1V OUTPUT VOLTAGE vs. LOAD CURRENT



CORE SMPS 1-PHASE SWITCHING FREQUENCY vs. LOAD CURRENT



NB SMPS SWITCHING FREQUENCY vs. LOAD CURRENT

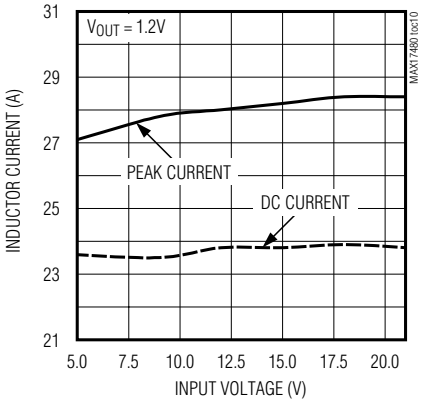


AMD 2-/3-Output Mobile Serial VID Controller

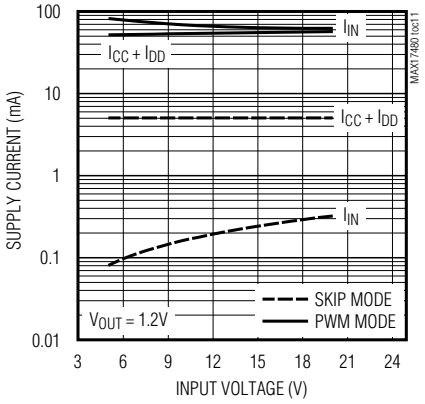
Typical Operating Characteristics (continued)

(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

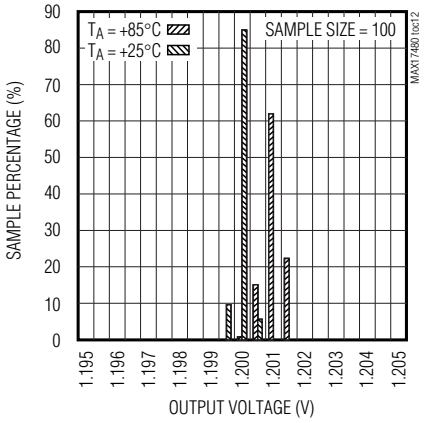
MAXIMUM INDUCTOR CURRENT vs. INPUT VOLTAGE



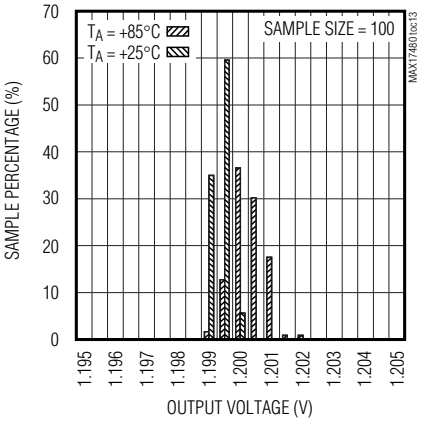
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



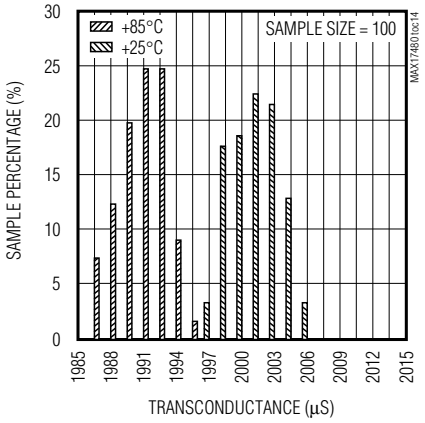
CORE SMPS VID = 1.2V OUTPUT VOLTAGE DISTRIBUTION



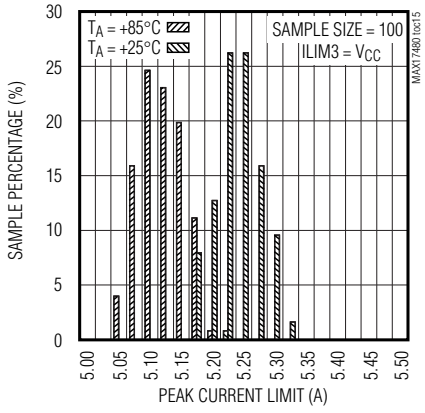
NB SMPS VID = 1.2V OUTPUT VOLTAGE DISTRIBUTION



$G_{m(FBAC)}$ TRANSCONDUCTANCE DISTRIBUTION



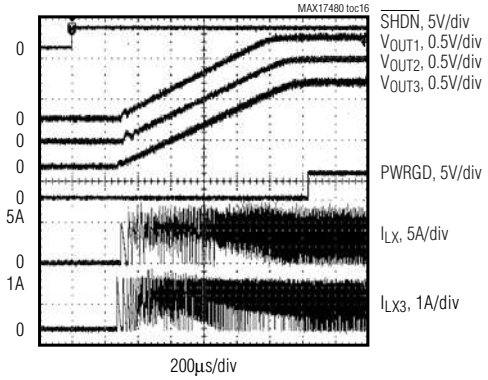
NB SMPS PEAK CURRENT-LIMIT DISTRIBUTION



Typical Operating Characteristics (continued)

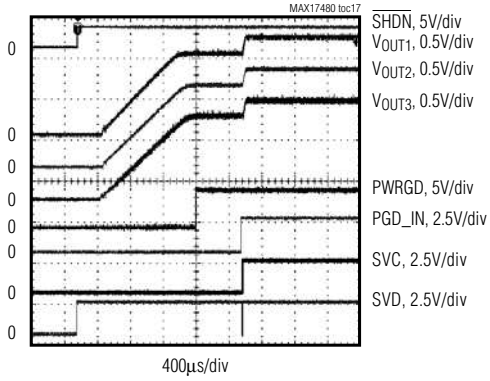
(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

STARTUP WAVEFORMS



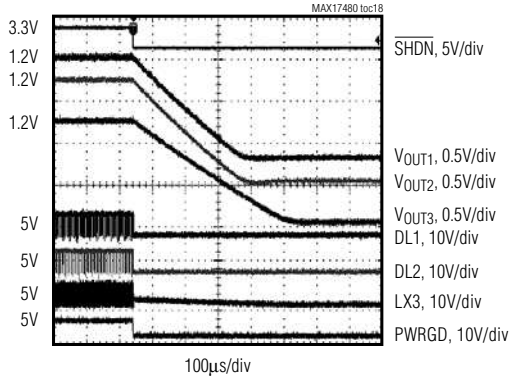
V_{IN} = 12V
V_{BOOT} = 1V
I_{LOAD1} = 3A
I_{LOAD2} = 3A
I_{LOAD3} = 0.5A

STARTUP SEQUENCE



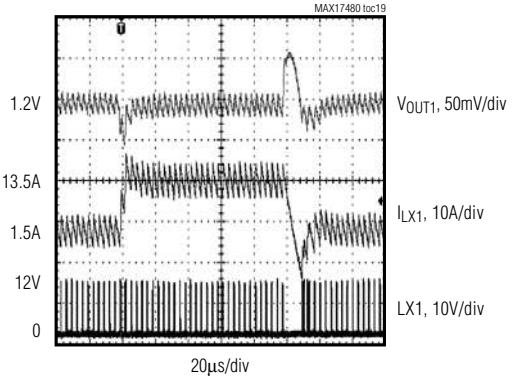
V_{IN} = 12V
V_{BOOT} = 1V
V_{SVID} = 1.2V

SHUTDOWN WAVEFORMS



V_{IN} = 12V
V_{SVID} = 1.2V
I_{LOAD1} = 3A
I_{LOAD2} = 3A
I_{LOAD3} = 0.5A

CORE SMPS 1-PHASE LOAD-TRANSIENT RESPONSE



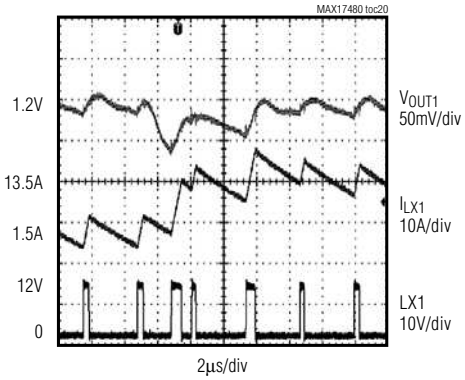
V_{IN} = 12V
V_{OUT1} = 1.2V
I_{LOAD1} = 1.5A TO 13.5A TO 1.5A
PWM MODE

AMD 2-/3-Output Mobile Serial VID Controller

Typical Operating Characteristics (continued)

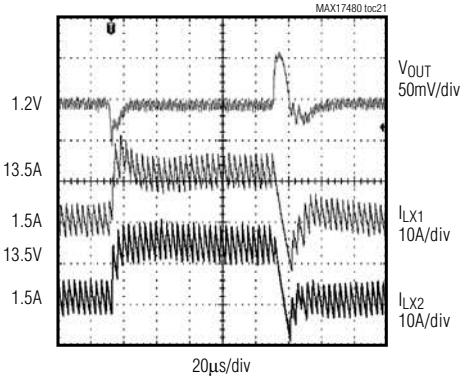
(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

CORE SMPS 1-PHASE TRANSIENT PHASE REPEAT



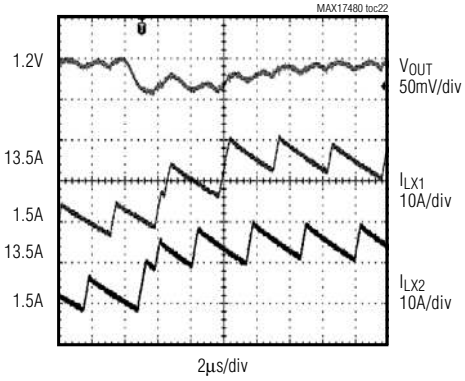
V_{IN} = 12V I_{LOAD1} = 1.5A TO 13.5A TO 1.5A
V_{OUT1} = 1.2V PWM MODE

CORE SMPS 2-PHASE LOAD-TRANSIENT RESPONSE



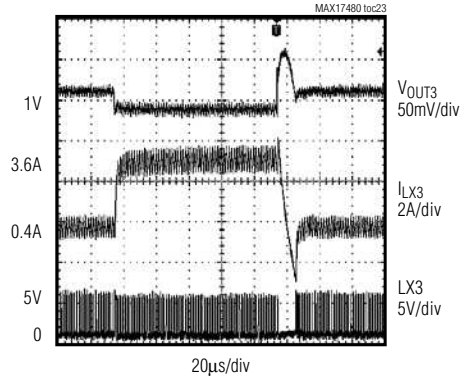
V_{IN} = 12V I_{LOAD} = 3A TO 27A TO 3A
V_{OUT1} = 1.2V PWM MODE

CORE SMPS 2-PHASE TRANSIENT PHASE REPEAT



V_{IN} = 12V I_{LOAD} = 3A TO 27A TO 3A
V_{OUT1} = 1.2V PWM MODE

NB SMPS LOAD-TRANSIENT RESPONSE

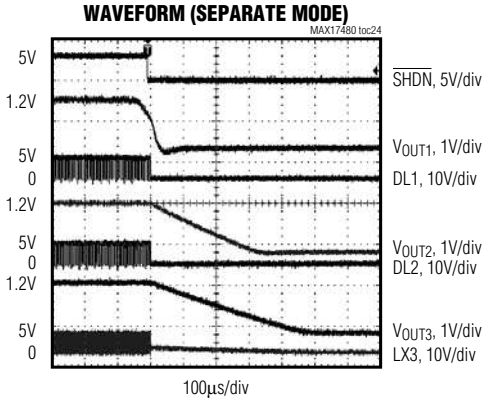


V_{IN3} = 5V I_{LOAD3} = 0.4A TO 3.6A TO 0.4A
V_{OUT3} = 1V PWM MODE

Typical Operating Characteristics (continued)

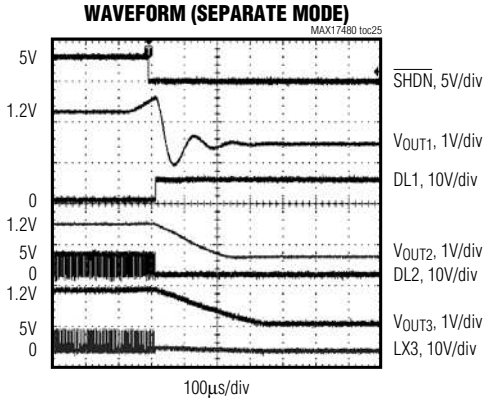
(Circuit of Figure 2, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, V_{DDIO} = 2.5V, T_A = +25°C, unless otherwise noted.)

CORE SMPS OUTPUT OVERLOAD WAVEFORM (SEPARATE MODE)



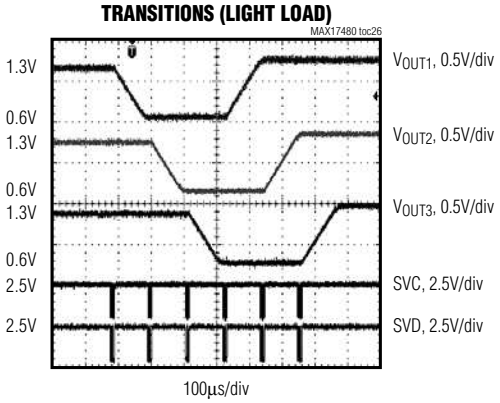
V_{IN} = 12V
V_{SVID} = 1.2V
I_{LOAD1} = 3A TO 40A
I_{LOAD2} = 3A
I_{LOAD3} = 0.5A

CORE SMPS OUTPUT OVERVOLTAGE WAVEFORM (SEPARATE MODE)



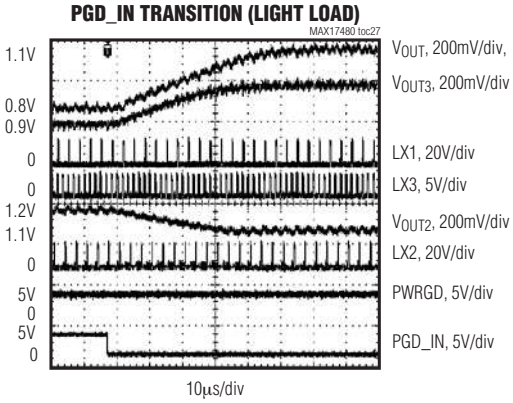
V_{IN} = 12V
V_{SVID} = 1.2V
I_{LOAD1} = NO LOAD
I_{LOAD2} = 3A
I_{LOAD3} = 0.5A

DYNAMIC OUTPUT-VOLTAGE TRANSITIONS (LIGHT LOAD)



V_{IN} = 12V
V_{SVID} = 1.3V TO 0.6V TO 1.3V

PGD_IN TRANSITION (LIGHT LOAD)



V_{IN} = 12V
V_{BOOT} = 1.1V
V_{OUT1} = 0.8V
V_{OUT2} = 1.2V
V_{OUT3} = 0.9V

AMD 2-/3-Output Mobile Serial VID Controller

Pin Description

PIN	NAME	FUNCTION
1	ILIM12	SMPS1 and SMPS2 Current-Limit Adjust Input. The positive current-limit threshold voltage is 0.052 times the voltage between TIME and ILIM over a 0.2V to 1.0V range of V(TIME, ILIM). The I_{MIN12} minimum current-limit threshold voltage in skip mode is precisely 15% of the corresponding positive current-limit threshold voltage.
2	ILIM3	SMPS3 Current-Limit Adjust Input. Two-level current-limit setting for SMPS3. The I_{LX3MIN} minimum current-limit threshold in skip mode is precisely 25% of the corresponding positive current-limit threshold. **ILIM3** | **I_{LX3PK} (A)** V_{CC} | 5.25 GND | 4.25
3, 4	IN3	Internal High-Side MOSFET Drain Connection for SMPS3. Bypass to PGND with a 10µF or greater ceramic capacitor close to the IC.
5, 6	LX3	Inductor Connection for SMPS3. Connect LX3 to the switched side of the inductor.
7	BST3	Boost Flying Capacitor Connection for SMPS3. An internal switch between V_{DD} and BST3 charges the flying capacitor during the time the low-side FET is on.
8	$\overline{SHDN}$	Active-Low Shutdown Control Input. This input cannot withstand the battery voltage. Connect to V_{CC} for normal operation. Connect to ground to put the IC into its 1µA max shutdown state. During startup, the output voltage is ramped up to the voltage set by the SVC and SVD inputs at a slew rate of 1mV/µs. In shutdown, the outputs are discharged using a 20Ω switch through the CSN_ pins for the core SMPSs and through the OUT3 pin for the northbridge SMPS. The MAX17480 powers up to the voltage set by the two SVI bits. **SVC** | **SVD** | **BOOT VOLTAGE V_{OUT} (V)** 0 | 0 | 1.1 0 | 1 | 1.0 1 | 0 | 0.9 1 | 1 | 0.8 The MAX17480 **stores** the boot VID when PWRGD first goes high. The stored boot VID is cleared by a rising $\overline{SHDN}$ signal.
9	OUT3	Feedback Input for SMPS3. A 20Ω discharge FET is enabled from OUT3 to PGND when SMPS3 is shut down.
10	AGND	Analog Ground
11	SVD	Serial VID Data
12	SVC	Serial VID Clock
13	V_{DDIO}	CPU I/O Voltage (1.8V or 1.5V). Logic thresholds for SVD and SVC are relative to the voltage at V_{DDIO}.
14	GNDS2	SMPS2 Remote Ground-Sense Input. Normally connected to GND directly at the load. GNDS2 internally connects to a transconductance amplifier that fine tunes the output voltage—compensating for voltage drops from the SMPS ground to the load ground. Connect GNDS1 or GNDS2 above 0.9V combined-mode operation (unified core). When GNDS2 is pulled above 0.9V, GNDS1 is used as the remote ground-sense input.

Pin Description (continued)

PIN	NAME	FUNCTION
15	FBAC2	Output of the Voltage-Positioning Transconductance Amplifier for SMPS2. The RC network between this pin and the positive side of the remote-sensed output voltage sets the transient AC droop: $$R_{DROOP\_AC2} = \frac{R_{FBAC2} \times R_{FBDC2}}{R_{FBAC2} + R_{FBDC2} + R_{FB2} \parallel Z_{CFB2}} \times R_{SENSE2} \times G_{m(FBAC2)}$$ where R_{DROOP_AC2} is the transient (AC) voltage-positioning slope that provides an acceptable trade-off between stability and load-transient response, $G_{m(FBAC2)}$ = 2mS (typ), and R_{SENSE2} is the value of the current-sense element that is used to provide the (CSP2, CSN2) current-sense voltage, Z_{CFB2} is the impedance of C_{FB2}, and FBAC2 is high impedance in shutdown.
16	FBDC2	Feedback-Sense Input for SMPS2. Connect a resistor R_{FBDC2} between FBDC2 and the positive side of the feedback remote sense, and a capacitor from FBAC2 to couple the AC ripple from FBAC2 to FBDC2. An integrator on FBDC2 corrects for output ripple and ground-sense offset. To enable a DC load-line less than the AC load-line, add a resistor from FBAC2 to FBDC2. To enable a DC load-line equal to the AC load-line, short FBAC2 to FBDC2. See the *Core Steady-State Voltage Positioning (DC Droop)* section. FBDC2 is high impedance in shutdown.
17	CSN2	Negative Current-Sense Input for SMPS2. Connect to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. A 20Ω discharge FET is enabled from CSN2 to PGND when the SMPS2 is shut down.
18	CSP2	Positive Current-Sense Input for SMPS2. Connect to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
19	PGD_IN	System Power-Good Input PGD_IN is low when $\overline{SHDN}$ first goes high. The MAX17480 decodes the two SVI bits to determine the boot voltage. The SVI bits can be changed dynamically during this time while PGD_IN remains low and PWRGD is still low. PGD_IN goes high after the MAX17480 reaches the boot voltage. This indicates that the SVI block is active, and the MAX17480 starts to respond to the SVI commands. The MAX17480 **stores** the boot VID when PWRGD first goes high. The stored boot VID is cleared by rising $\overline{SHDN}$. After PGD_IN has gone high, if at any time PGD_IN goes low, the MAX17480 regulates to the previously stored boot VID. The slew rate during this transition is set by the resistor between the TIME and GND pins. PWRGD follows the blanking for normal VID transition. The subsequent rising edge of PGD_IN does not change the stored VID.

AMD 2-/3-Output Mobile Serial VID Controller

Pin Description (continued)

PIN	NAME	FUNCTION
20	PWRGD	Open-Drain Power-Good Output. PWRGD is the wired-OR open-drain output of all three SMPS outputs. PWRGD is forced high impedance whenever the slew-rate controller is active (output voltage transitions). During startup, PWRGD is held low for an additional 20µs after the MAX17480 reaches the startup boot voltage set by the SVC and SVD pins. The MAX17480 stores the boot VID when PWRGD first goes high. The stored boot VID is cleared by rising $\overline{SHDN}$. PWRGD is forced low in shutdown. When SMPS is in pulse-skipping mode, the upper PWRGD threshold comparator for the respective SMPS is blanked during a downward VID transition. The upper PWRGD threshold comparator is re-enabled once the output is in regulation (Figure 6).
21	DH2	SMPS2 High-Side Gate-Driver Output. DH2 swings from LX2 to BST2. Low in shutdown.
22	LX2	SMPS2 Inductor Connection. LX2 is the internal lower supply rail for the DH2 high-side gate driver. Also used as an input to SMPS2's zero-crossing comparator.
23	BST2	Boost Flying Capacitor Connection for the DH2 High-Side Gate Driver. An internal switch between V_{DD} and BST2 charges the flying capacitor during the time the low-side FET is on.
24	DL2	SMPS2 Low-Side Gate-Driver Output. DL2 swings from GND2 to V_{DD}. DL2 is forced low in shutdown. DL2 is also forced high when an output overvoltage fault is detected. DL2 is forced low in skip mode after an inductor current zero crossing (GND2 - LX2) is detected.
25	V_{DD}	Supply Voltage Input for the DL_ Drivers. V_{DD} is also the supply voltage used to internally recharge the BST_ flying capacitors during the off-time. Connect V_{DD} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD} to GND with a 2.2µF or greater ceramic capacitor.
26	DL1	SMPS1 Low-Side Gate-Driver Output. DL1 swings from GND1 to V_{DD}. DL1 is forced low in shutdown. DL1 is also forced high when an output overvoltage fault is detected. DL1 is forced low in skip mode after an inductor current zero crossing (GND1 - LX1) is detected.
27	BST1	Boost Flying Capacitor Connection for the DH1 High-Side Gate Driver. An internal switch between V_{DD} and BST1 charges the flying capacitor during the time the low-side FET is on.
28	LX1	SMPS1 Inductor Connection. LX1 is the internal lower supply rail for the DH1 high-side gate driver. Also used as an input to SMPS1's zero-crossing comparator.
29	DH1	SMPS1 High-Side Gate-Driver Output. DH1 swings from LX1 to BST1. Low in shutdown.
30	$\overline{VRHOT}$	Active-Low Open-Drain Output of Internal Comparator. $\overline{VRHOT}$ is pulled low when the voltage at THRM goes below 1.5V (30% of V_{CC}). $\overline{VRHOT}$ is high impedance in shutdown.
31	THRM	Input of Internal Comparator. Connect the output of a resistor- and thermistor-divider (between V_{CC} and GND) to THRM. Select the components so the voltage at THRM falls below 1.5V (30% of V_{CC}) at the desired high temperature.
32	V_{CC}	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with a 1µF minimum capacitor. A V_{CC} UVLO event that occurs while the IC is functioning is latched, and can only be cleared by cycling V_{CC} power or by toggling $\overline{SHDN}$.

Pin Description (continued)

PIN	NAME	FUNCTION
33	CSP1	Positive Current-Sense Input for SMPS1. Connect to the positive side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing.
34	CSN1	Negative Current-Sense Input for SMPS1. Connect to the negative side of the output current-sensing resistor or the filtering capacitor if the DC resistance of the output inductor is utilized for current sensing. A 20Ω discharge FET is enabled from CSN1 to PGND when the SMPS1 is shut down.
35	FBDC1	Feedback Sense Input for SMPS1. Connect a resistor R_{FBDC1} between FBDC1 and the positive side of the feedback remote sense, and a capacitor from FBAC1 to couple the AC ripple from FBAC1 to FBDC1. An integrator on FBDC1 corrects for output ripple and ground-sense offset. To enable a DC load-line less than the AC load-line, add a resistor from FBAC1 to FBDC1. To enable a DC load-line equal to the AC load-line, short FBAC1 to FBDC1. See the *Core Steady-State Voltage Positioning (DC Droop)* section. FBDC1 is high impedance in shutdown.
36	FBAC1	Output of the AC Voltage-Positioning Transconductance Amplifier for SMPS1. The RC network between this pin and the positive side of the remote-sensed output voltage sets the transient AC droop: $$R_{DROOP\_AC1} = \frac{R_{FBAC1} \times R_{FBDC1}}{R_{FBAC1} + R_{FBDC1} + R_{FB1} \parallel Z_{CFB1}} \times R_{SENSE1} \times G_{m(FBAC1)}$$ where R_{DROOP_AC1} is the transient (AC) voltage-positioning slope that provides an acceptable trade-off between stability and load-transient response, $G_{m(FBAC1)}$ = 2mS (typ), R_{SENSE1} is the value of the current-sense element that is used to provide the (CSP1, CSN1) current-sense voltage, Z_{CFB1} is the impedance of C_{FB1}, and FBAC1 is high impedance in shutdown.
37	GNDS1	SMPS1 Remote Ground-Sense Input. Normally connected to GND directly at the load. GNDS1 internally connects to a transconductance amplifier that fine tunes the output voltage—compensating for voltage drops from the SMPS ground to the load ground. Connect GNDS1 or GNDS2 above 0.9V combined-mode operation (unified core). When GNDS1 is pulled above 0.9V, GNDS2 is used as the remote ground-sense input.
38	OPTION	Four-Level Input to Enable Offset and Change Core SMPS Address

OPTION	OFFSET ENABLED	SMPS1 ADDRESS	SMPS2 ADDRESS
V_{CC}	0	BIT 1 (VDD0)	BIT 2 (VDD1)
3.3V	0	BIT 2 (VDD1)	BIT 1 (VDD0)
2V	1	BIT 1 (VDD0)	BIT 2 (VDD1)
GND	1	BIT 2 (VDD1)	BIT 1 (VDD0)

When OFFSET is enabled, the MAX17480 enables a fixed +12.5mV offset on SMPS1 and SMPS2 VID codes after PGD_IN goes high. This configuration is intended for applications that implement a load line. An external resistor at FBDC_ sets the load-line. The offset can be disabled by setting the PSI_L bit to 0 through the serial interface.
Additionally, the OPTION level also allows core SMPS1 and SMPS2 to take on either the VDD0 or VDD1 addresses. VDD0 refers to CORE0, and VDD1 refers to CORE1 for the AMD CPU.
The NB SMPS is not affected by the OPTION setting.

AMD 2-/3-Output Mobile Serial VID Controller

Pin Description (continued)

PIN	NAME	FUNCTION
39	OSC	Oscillator Adjustment Input. Connect a resistor (R_{OSC}) between OSC and GND to set the switching frequency (per phase): f_{OSC} = 300kHz x 143kΩ/R_{OSC} A 71.4kΩ to 432kΩ resistor corresponds to switching frequencies of 600kHz to 100kHz, respectively, for SMPS1 and SMPS2. SMPS3 runs at twice the programmed switching frequency. Switching frequency selection is limited by the minimum on-time. See the Core Switching Frequency description in the *SMPS Design Procedure* section.
40	TIME	Slew-Rate Adjustment Pin. The total resistance R_{TIME} from TIME to GND sets the internal slew rate: PWM slew rate = (6.25mV/µs) x (143kΩ/R_{TIME}) where R_{TIME} is between 35.7kΩ and 357kΩ. This slew rate applies to both upward and downward VID transitions, and to the transition from boot mode to VID mode. Downward VID transition slew rate in skip mode can appear slower because the output transition is not forced by the SMPS. The slew rate for startup is fixed at 1mV/µs.
EP	PGND	Exposed Pad. Power ground connection and source connection of the internal low-side MOSFET.

Table 1. Component Selection for Standard Applications

COMPONENT	V_{IN} = 7V TO 24V, V_{OUT1} = V_{OUT2} = 1.0V TO 1.3V, 18A PER PHASE	V_{IN3} = 5V, V_{OUT3} = 1.0V TO 1.3V, 4A	V_{IN} = 4.5V TO 14V, V_{OUT1} = V_{OUT2} = 1.0V TO 1.3V, 18A PER PHASE	V_{IN3} = 3.3V, V_{OUT3} = 1.0V TO 1.3V, 4A
Mode	Separate, 2-phase mobile (GNDS1 = GNDS2 = low)	—	Separate, 2-phase mobile (GNDS1 = GNDS2 = low)	—
Switching Frequency	300kHz	600kHz	500kHz	1MHz
$C_{IN\_}$ Input Capacitor	(2) 10µF, 25V Taiyo Yuden TMK432BJ106KM	(1) 10µF, 6.3V TDK C2012X5R0J106M Taiyo Yuden JMK212BJ106M	(2) 10µF, 16V Taiyo Yuden TMK432BJ106KM	(1) 10µF, 6.3V TDK C2012X5R0J106M Taiyo Yuden JMK212BJ106M
$C_{OUT\_}$ Output Capacitor	(2) 330µF, 2V, 6mΩ, low-ESR capacitor Panasonic EEFSX0D331XE SANYO 2TPE330M6	(1) 220µF, 2V, 6mΩ, low-ESR capacitor Panasonic EEFSD0D221R SANYO 2TPE220M6	(2) 220µF, 2V, 6mΩ, low-ESR capacitor Panasonic EEFSD0D221R SANYO 2TPE220M6	(1) 47µF, ceramic capacitor
$N_{H\_}$ High-Side MOSFET	(1) Vishay/Siliconix SI7634DP	None	(1) International Rectifier IRF7811W	None
$N_{L\_}$ Low-Side MOSFET	(2) Vishay/Siliconix SI7336ADP	None	(2) Vishay/Siliconix SI7336ADP	None
$D_{L\_}$ Schottky Rectifier (if needed)	3A, 40V Schottky diode Central Semiconductor CMSH3-40	None	3A, 40V Schottky diode Central Semiconductor CMSH3-40	None
$L\_$ Inductor	0.45µH, 21A, 1.1mΩ power inductor Panasonic ETQP4LR45WFC	1.5µH, 5A, 21mΩ power inductor NEC/Tokin MPLCH0525LIR5 Toko FDV0530-1R5M	0.36µH, 21A, 1.1mΩ power inductor Panasonic ETQP4LR36WFC	0.6µH, 4.95A, 16mΩ power inductor Sumida CDR6D23MN

Note: *Mobile applications should be designed for separate mode operation. Component selection is dependent on AMD CPU AC and DC specifications.*

Table 2. Component Suppliers

MANUFACTURER	WEBSITE
AVX Corporation	www.avxcorp.com
BI Technologies	www.bitechnologies.com
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp.	www.kemet.com
NEC TOKIN America, Inc.	www.nec-tokinamerica.com
Panasonic Corp.	www.panasonic.com

MANUFACTURER	WEBSITE
Pulse Engineering	www.pulseeng.com
Renesas Technology Corp.	www.renesas.com
SANYO Electric Co., Ltd.	www.sanyodevice.com
Siliconix (Vishay)	www.vishay.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com

_____Standard Application Circuit

The MAX17480 standard application circuit (Figure 2) generates two independent 18A outputs and one 4A output for AMD mobile CPU applications. See Table 1 for component selections. Table 2 lists the component manufacturers.

AMD 2-/3-Output Mobile Serial VID Controller

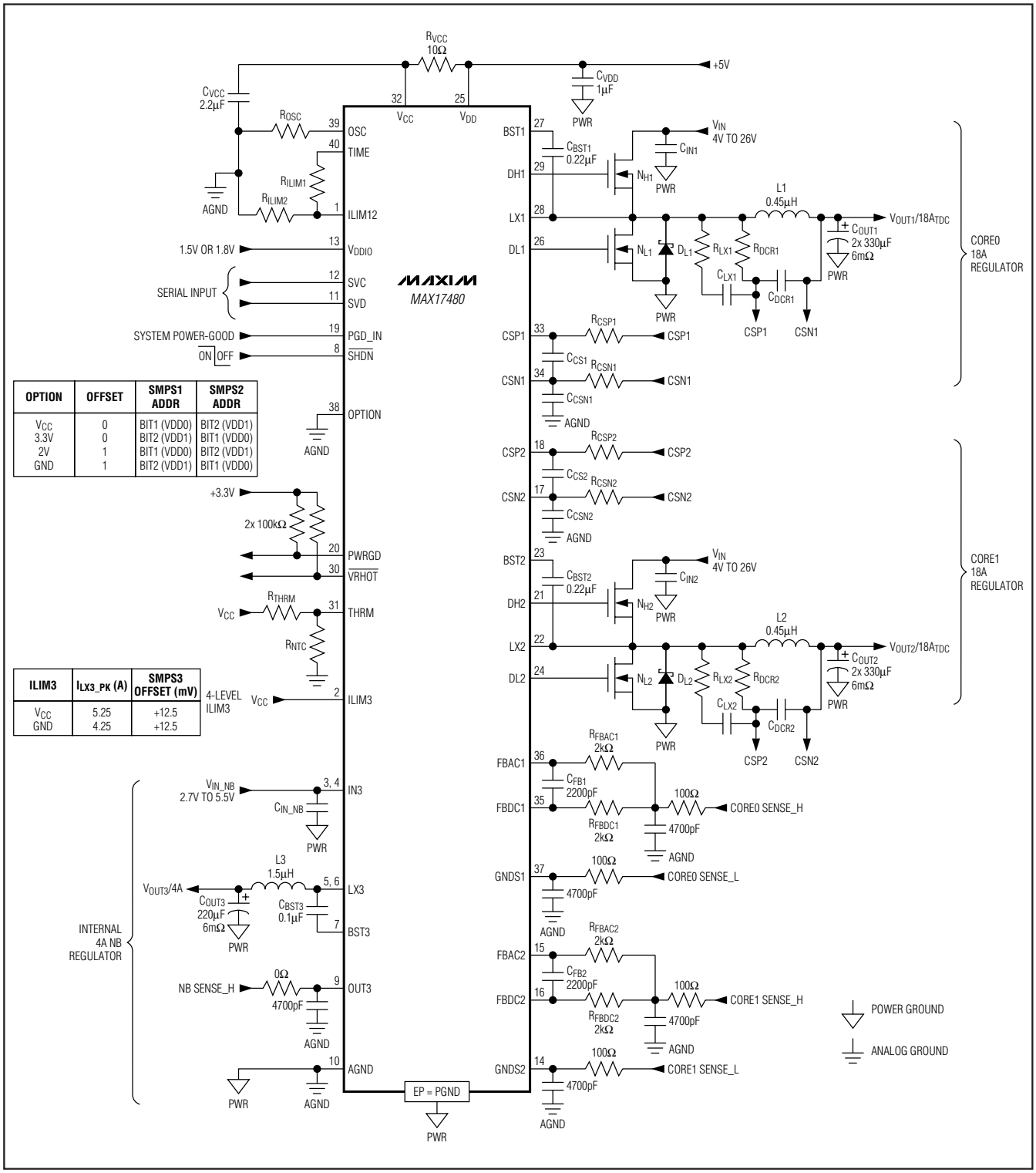


Figure 2. Griffin/Puma Standard Application Circuit

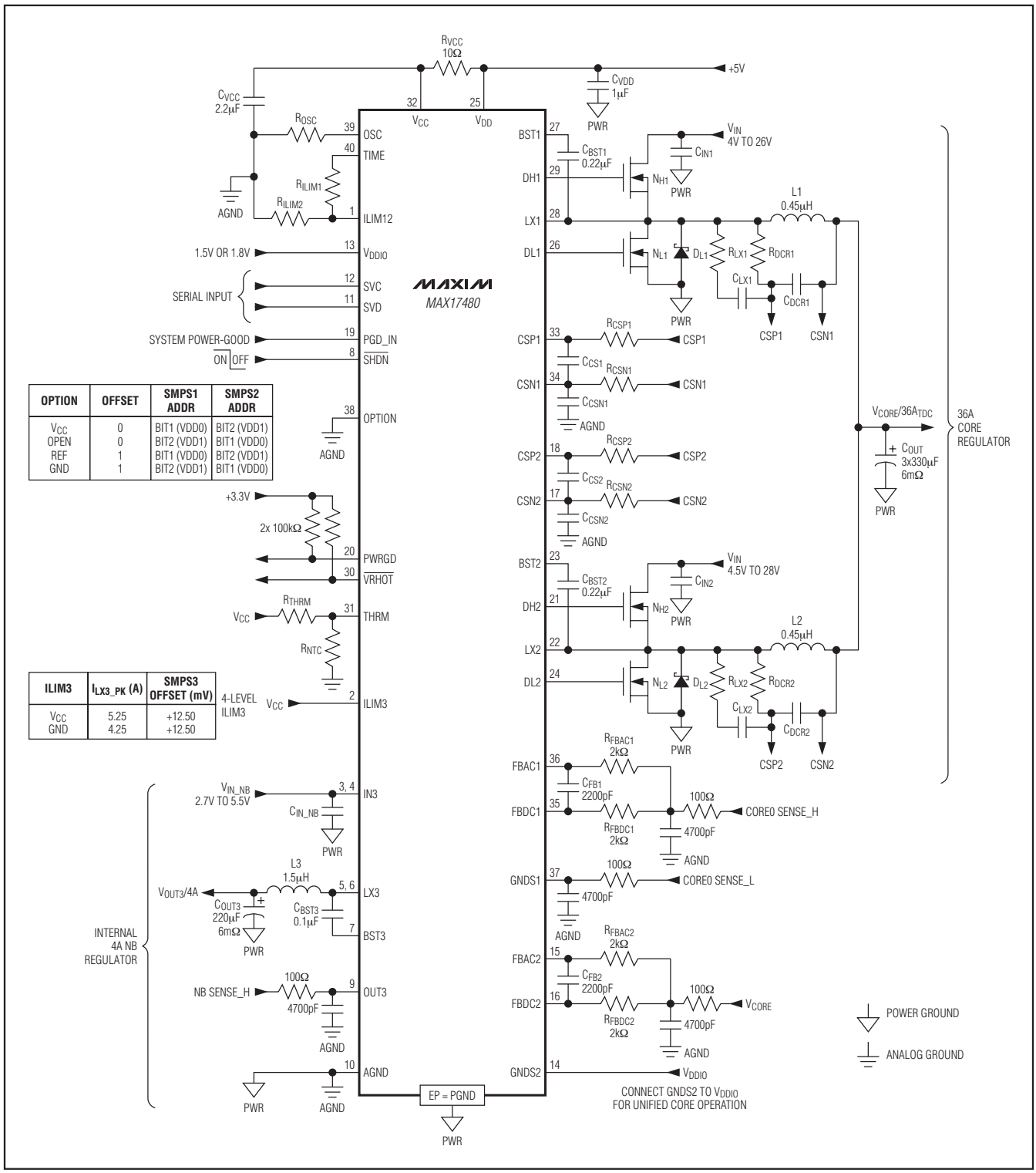


Figure 3. Caspian/Tigris Standard Application Circuit

AMD 2-/3-Output Mobile Serial VID Controller

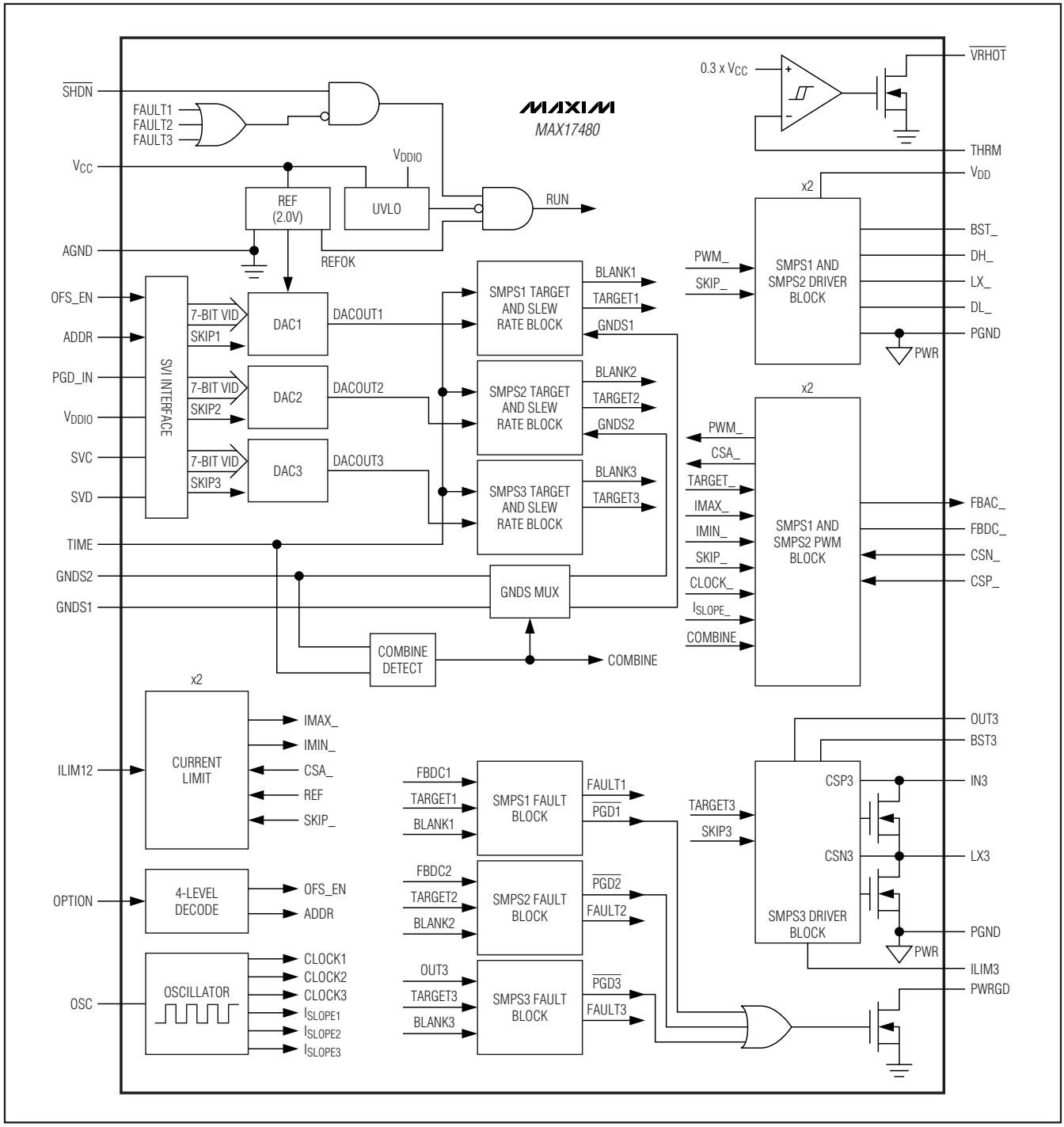


Figure 4. Functional Diagram

Detailed Description

The MAX17480 consists of a dual fixed-frequency PWM controller with external switches that generate the supply voltage for two independent CPU cores and one low-input-voltage internal switch SMPS for the separate NB SMPS. The CPU core SMPSs can be configured as independent outputs, or as a combined output by connecting the GNDS1 or GNDS2 pin-strap high (GNDS1 or GNDS2 pulled to 1.5V to 1.8V, which are the respective voltages for DDR3 and DDR2).

All three SMPSs can be programmed independently to any voltage in the VID table (see Table 4) using the serial VID interface (SVI). The CPU is the SVI bus master, while the MAX17480 is the SVI slave. Voltage transitions are commanded by the CPU as a single step command from one VID code to another. The MAX17480 slews the SMPS outputs at the slew rate programmed by the external R_{TIME} resistor during VID transitions and the transition from boot mode to VID mode.

During startup, the MAX17480 SMPSs are always in pulse-skipping mode. After exiting the boot mode, the individual PSI_L bit sets the respective SMPS into pulse-skipping mode or forced-PWM mode, depending on the system power state, and adds the +12.5mV offset for core supplies if enabled by the OPTION pin. In combined mode, the PSI_L bit adds the +12.5mV offset if enabled by the OPTION pin, and switches from 1-phase pulse-skipping mode to 2-phase PWM mode. Figure 4 is the MAX17480 functional diagram.

+5V Bias Supply (V_{CC}, V_{DD})

The MAX17480 requires an external 5V bias supply in addition to the battery. Typically, this 5V bias supply is the notebook's main 95%-efficient 5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the 5V linear SMPS that would otherwise be needed to supply the PWM circuit and gate drivers.

The 5V bias supply powers both the PWM controller and internal gate-drive power, so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW\_CORE}Q_{G\_CORE} + f_{SW\_NB}Q_{G\_NB} = 50mA \text{ to } 70mA \text{ (typ)}$$

where I_{CC} is provided in the *Electrical Characteristics* table, f_{SW_CORE} and f_{SW_NB} are the respective core and NB SMPS switching frequencies, Q_{G_CORE} is the gate charge of the external MOSFETs as defined in the MOSFET data sheets, and Q_{G_NB} is approximately 2nC. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (OSC)

Connect a resistor (R_{OSC}) between OSC and GND to set the switching frequency (per phase):

$$f_{SW} = 300kHz \times 143k\Omega / R_{OSC}$$

A 71.4kΩ to 432kΩ resistor corresponds to switching frequencies of 600kHz to 100kHz, respectively, for the core SMPSs, and 1.2MHz to 200kHz for the NB SMPS. High-frequency (600kHz) operation for the core SMPS optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This might be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (100kHz) operation offers the best overall efficiency at the expense of component size and board space.

The NB SMPS runs at twice the switching frequency of the core SMPSs. The low power of the NB rail allows for higher switching frequencies with little impact on the overall efficiency.

Minimum on-time ($t_{ON(MIN)}$) must be taken into consideration when selecting a switching frequency. See the Core Switching Frequency description in the *SMPS Design Procedure* section.

Interleaved Multiphase Operation

The MAX17480 interleaves both core SMPSs' phases—resulting in 180° out-of-phase operation that minimizes the input and output filtering requirements, reduces electromagnetic interference (EMI), and improves efficiency. The high-side MOSFETs do not turn on simultaneously during normal operation. The instantaneous input current is effectively reduced by the number of active phases, resulting in reduced input-voltage ripple, effective series resistance (ESR) power loss, and RMS ripple current (see the *Core Input Capacitor Selection* section). Therefore, the controller achieves high performance while minimizing the component count—which reduces cost, saves board space, and lowers component power requirements—making the MAX17480 ideal for high-power, cost-sensitive applications.