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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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EVALUATION KIT AVAILABLE

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

General Description

The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T are dual-output, step-down, constant on-time Quick-PWM™ controllers for VR12/IMVP-7 CPU core supplies. The controllers consist of two high-current switching power supplies for CPU and GFX cores. The CPU regulator (regulator A) is a three-phase constant on-time architecture. The GFX regulator (regulator B) is also constant on-time architecture. The MAX17411 supports 2-phase operation and the MAX17511/MAX17511C/MAX17511N/MAX17511T support 1-phase operation. The MAX17411/MAX17511/MAX17511C/MAX17511N/MAX17511T include two internal drivers on regulator A and one internal driver on regulator B. External drivers such as the MAX17491 enable the additional phases.

Both regulator A and regulator B include output voltage sensing and accurate load-line gain. Switching frequencies are programmable from 200kHz to 600kHz per phase. Output overvoltage protection (OVP, MAX17411/MAX17511/MAX17511C/MAX17511N), undervoltage protection (UVP), and thermal protection ensure effective and reliable operation. When any of these protection features detect a fault, the controller shuts down both outputs.

The multiphase regulators include transient-phase overlap and active overshoot suppression, which speed up the response time and reduce the total output capacitance. The CPU and GFX outputs are controlled independently by writing the appropriate data into a function-mapped register file. VID code transitions and soft-start are enabled with a precision slew-rate control circuit. The SVID interface also allows each regulator to be individually set into a low-power, single-phase, pulse-skipping state to optimize efficiency. The MAX17411 is available in a 48-pin, 6mm x 6mm, TQFN package. The MAX17511/MAX17511C/MAX17511N/MAX17511T are available in a 40-pin, 5mm x 5mm, TQFN lead-free package.

Applications

VR12/IMVP-7 CPU Core Power Supplies

Notebooks/Desktops/Servers

Features

- **Intel VR12/IMVP-7-Compliant Serial Interface**
- **3-/2-/1-Phase Quick-PWM CPU Core Regulator**
  - **Two Internal Drivers and One External Driver**
  - **Transient-Phase Overlap Mode**
  - **Dynamic Phase Selection**
- **2-/1-Phase Quick-PWM GFX Regulator**
  - **One Internal and One External Driver**
- **Active Overshoot Suppression**
- **8-Bit VR12/IMVP-7 DAC**
- **±0.5% V_{OUT} Accuracy Over Line, Load, and Temperature**
- **Active Voltage Positioning with Programmable Gain**
- **Accurate Lossless Current Balance**
- **Accurate Droop and Current Limit**
- **Remote Output and Ground Sense**
- **Power-Good Window Comparators (POKA and POKB)**
- **4.5V to 24V Battery-Input Voltage Range**
- **Programmable 200kHz to 600kHz Switching Frequency**
- **External Thermal-Fault Detection Output (VR_HOT#)**
- **Overvoltage (MAX17411/MAX17511/MAX17511C/MAX17511N), Undervoltage, and Thermal-Fault Protection**
- **Slew-Rate Controlled Soft-Start**
- **Passive Soft-Shutdown (20Ω Discharge Switches)**
- **Integrated Boost Switches**
- **Low-Profile, 48-Lead/40-Lead TQFN Packages**

Quick PWM is a trademark of Maxim Integrated Products, Inc.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	FEATURE
MAX17411GTM+	-40°C to +105°C	48 TQFN-EP*	3-/2-/1-Phase + 2-/1-Phase
MAX17511GTL+	-40°C to +105°C	40 TQFN-EP*	3-/2-/1-Phase + 1-Phase

Ordering Information continued on last page.

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{DDA}, V_{DDB} to GND (AGND) ..... -0.3V to +6V
VDIO, CLK, ALERT# to GND (AGND) ..... -0.3V to +6V
CSPAAVE, CSPBAVE, CSP_,
CSN_ to GND (AGND) ..... -0.3V to +6V
FBA, FBB to GND (AGND) ..... -0.3V to (V_{CC} + 0.3V)
SR, IMAX_ to GND (AGND) ..... -0.3V to (V_{CC} + 0.3V)
POKA, POKB, EN to GND (AGND) ..... -0.3V to +6V
VR_HOT# to GND (AGND) ..... -0.3V to +6V
THERMA, THERMB to GND (AGND) ..... -0.3V to (V_{CC} + 0.3V)
GNDSA, GNDSB to GND (AGND) ..... -0.3V to +0.3V
TON to GND ..... -0.3V to +26V
DRVPWMA to GND (AGND) ..... -0.3V to (V_{DDA} + 0.3V)
DRVPWMB to GND (AGND) ..... -0.3V to (V_{DDB} + 0.3V)
DLA_ to GND (PGND) ..... -0.3V to (V_{DDA} + 0.3V)
DLB to GND (PGND) ..... -0.3V to (V_{DDB} + 0.3V)
BSTA_ to V_{DDA} ..... -0.3V to +26V
BSTB to V_{DDB} ..... -0.3V to +26V
LXA_ to BSTA_ ..... -6V to +0.3V
LXB to BSTB ..... -6V to +0.3V
LX_ to GND (AGND) ..... -6V to +26V
DHA_ to LXA_ ..... -0.3V to ($V_{BSTA\_}$ + 0.3V)
DHB to LXB ..... -0.3V to (V_{BSTB} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
40-Pin TQFN (derate 35.7mW/°C above +70°C) ... 2857.1mW
48-Pin TQFN (derate 37mW/°C above +70°C) 2963mW
Operating Temperature Range ..... -40°C to +105°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +165°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

40 TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 28°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1.6°C/W

48 TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 27°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1.3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DDA}, V_{DDB}		4.5		5.5	V
DC Output Voltage Accuracy		Measured at FB_ with respect to GNDS_; includes load regulation error (Note 2)	DAC codes from 1.000V to 1.520V	-0.5		+0.5	%
			DAC codes from 0.800V to 0.995V	-5		+5	mV
			DAC codes from 0.250V to 0.795V	-8		+8	
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 24V			0.1		mV
$V_{SETTLED}$ Bit Accuracy		Upward transitions		-15	-10	-5	mV
		Downward transitions		5	10	15	
GNDS_ Input Range				-200		+200	mV
GNDS_ Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS\_}$		0.97	1.00	1.03	V/V
GNDS_ Input Bias Current		T_A = +25°C		-0.5		+0.5	µA
TON Shutdown Current		EN = GND, V_{IN} = 24V, V_{CC} = 0V, T_A = +25°C			0.01	0.1	µA
Boot Voltage	V_{BOOT}	MAX17511N only, Reg A and Reg B		1.094	1.100	1.106	V
		MAX17511C only, Reg B only		0.895	0.900	0.905	

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DHA_ On-Time (Note 3)	t_{ONA}	Measured at DHA_ (600kHz - 10%), R_{TON} = 96.7kΩ (MAX17411 only), R_{TON} = 48.35kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)		157	185	213	ns
		Measured at DHA_, V_{IN} = 12V (300kHz - 10%), R_{TON} = 200kΩ (MAX17411 only), R_{TON} = 100kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)		276	307	338	
		Measured at DHA_ (200kHz - 10%), R_{TON} = 303.3kΩ (MAX17411 only), R_{TON} = 151.65kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)		470	554	638	
DHB On-Time (Note 3)	t_{ONB}	Measured at DHB (600kHz + 10%), R_{TON} = 96.7kΩ (MAX17411 only), R_{TON} = 48.35kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)		128	151	174	ns
		Measured at DHB, V_{IN} = 12V (300kHz + 10%), R_{TON} = 200kΩ (MAX17411 only), R_{TON} = 100kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)		226	251	277	
		Measured at DHB (200kHz + 10%), R_{TON} = 303.3kΩ (MAX17411 only), R_{TON} = 151.65kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)		385	453	521	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	Measured at DH_		150	200	250	ns
Minimum DRVPWM_ Pulse Width					40		ns
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{BIAS}	Measured at V_{CC}, SKIP mode, FB_ forced above the regulation point			5	10	mA
Quiescent Supply Current ($V_{DD\_}$)	I_{DRV}	T_A = +25°C, measured at $V_{DD\_}$, FPWM mode, FB_ forced above the regulation point			0.02	1	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, EN = GND			16	30	µA
Shutdown Supply Current ($V_{DD\_}$)		T_A = +25°C, measured at V_{DD}, EN = GND			0.01	1	µA
SLEW-RATE CONTROL							
Slew-Rate Accuracy		V_{SR} = 0V or V_{SR} = 5V	SetVID - fast slew rate = 10mV/µs (min)	10			mV/µs
			SetVID - slow slew rate = 2.5mV/µs (min)	2.5			
		V_{SR} = 3V or V_{SR} = 1.5V	SetVID - fast slew rate = 20mV/µs (min)	20			
			SetVID - slow slew rate = 5mV/µs (min)	5			

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Soft-Start Slew Rate		Non-zero V_{BOOT}	2.5			mV/µs
Discharge Switch Resistance		CSNA, CSNB		20		Ω
SR Four-Level Logic Thresholds		Low			0.4	V
		Mid-low	1.2		1.8	
		Mid-high	2.2		V_{CC} - 1.2V	
		High	V_{CC} - 0.4V			
FAULT PROTECTION						
Upper POK_ (MAX17411/ MAX17511/MAX17511C/ MAX17511N/MAX17511T) and Output Overvoltage Protection Trip Threshold(MAX17411/ MAX17511/MAX17511C/ MAX17511N)	V_{OVP}	SKIP mode after output reaches the regulation voltage or PWM mode; measured at FB_ with respect to the voltage target set by the VID code (see Table 3)	200	250	300	mV
		Soft-start, SKIP mode, and output has not reached the regulation voltage; measured at FB_	1.72	1.77	1.82	V
		Minimum OVP threshold, measured at FB_		0.8		
Upper POK_ and Output Overvoltage Propagation Delay	t_{OVP}	FB_ forced 25mV above trip threshold (MAX17411/MAX17511/MAX17511C/MAX17511N)		5		µs
Lower POK_ and Output Undervoltage Protection Trip Threshold	V_{UVP}	Measured at FB_ with respect to unloaded output voltage	-300	-250	-200	mV
Lower POK_ Propagation Delay		FB_ forced 25mV below trip threshold		5		µs
Output Undervoltage Propagation Delay	t_{UVP}	FB_ forced 25mV below trip threshold	100	200	350	µs
POK_ Output Low Voltage		I_{SINK} = 4mA			0.3	V
POK_ Leakage Current		High state, POK_ forced to 5V, T_A = +25°C			1	µA
POK_ Startup Delay and Transitions Blanking Time	$t_{POK\_}$	Measured from the time when FB_ reaches the target voltage		20		µs
V_{CC} Undervoltage-Lockout Threshold	V_{UVLO}	Rising edge, 50mV typical hysteresis, controller disabled below this level	4.05	4.25	4.45	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
THERMAL PROTECTION							
VR_HOT# Trip Threshold		Measured at THERM_ with respect to V_{CC} falling edge; specify as % error for all TEMP MAX DAC code settings, typical hysteresis = 100mV		49.5		50.5	%
Thermal Zone Registers Trip Points		Thermal zone comparator trip points, measured with respect to V_{CC}; voltage threshold corresponding to TMAX x (1 - N%), N = 0, 3, 6, 9, 12, 15, 18, 25		49 + 24 x N/31	50 + 24 x N/31	51 + 24 x N/31	%
THERM_ Input Leakage	I_{THRM}	$V_{THERM\_}$ = 2.5V, T_A = +25°C		-100		+100	nA
VR_HOT# Leakage Current		High-Z state (THERM_ > 0.505 x V_{CC}), VR_HOT# forced to 5V, T_A = +25°C				1	µA
Internal Thermal Fault Shutdown Threshold	T_{TSHDN}	Typical hysteresis = 15°C			160		°C
VALLEY CURRENT LIMIT AND DROOP							
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMA}	$V_{CSP\_}$ - $V_{CSN\_}$, V_{SR} = 0V, V_{SR} = 1.5V, or one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXA} = 39A	22.5	25.5	28.5	mV
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 36A	21.5	24.5	27.5	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 30A	17.0	20.0	23.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 26A	15.0	18.0	21.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 39A	27.0	30.0	33.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 36A	25.0	28.0	31.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 30A	20.0	23.0	26.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 26A	17.0	20.0	23.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 39A	30.0	33.0	36.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 36A	28.0	31.0	34.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 30A	22.5	25.5	28.5	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 26A	20.0	23.0	26.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 39A	33.5	36.5	39.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 36A	31.0	34.0	37.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 30A	25.0	28.0	31.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 26A	21.5	24.5	27.5	

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMA}	$V_{CSP\_}$ - $V_{CSN\_}$, V_{SR} = 3V or V_{SR} = 5V, exclude one-phase operaton	R_{SENSE} = 0.65mΩ, I_{MAXA} = 39A	29.0	33.0	37.0	mV
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 36A	28.0	32.0	36.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 30A	22.0	26.0	30.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 26A	19.5	23.5	27.5	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 39A	35.0	39.0	43.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 36A	32.5	36.5	40.5	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 30A	26.0	29.9	33.8	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 26A	22.0	26.0	30.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 39A	39.0	43.0	47.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 36A	36.5	40.5	44.5	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 30A	29.0	33.0	37.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 26A	26.0	30.0	34.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 39A	43.5	47.5	51.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 36A	40.0	44.0	48.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 30A	32.5	36.5	40.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 26A	28.0	32.0	36.0	
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMB}	$V_{CSP\_}$ - $V_{CSN\_}$, V_{SR} = 0V, V_{SR} = 1.5V, or one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXB} = 39A	22.5	25.5	28.5	mV
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 36A	21.5	24.5	27.5	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 23A	13.0	16.0	19.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 20A	11.0	14.0	17.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 39A	27.0	30.0	33.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 36A	25.0	28.0	31.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 23A	15.0	18.0	21.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 20A	13.0	16.0	19.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 39A	30.0	33.0	36.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 36A	28.0	31.0	34.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 23A	17.0	20.0	23.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 20A	15.0	18.0	21.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 39A	33.5	36.5	39.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 36A	31.0	34.0	37.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 23A	20.0	23.0	26.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 20A	17.0	20.0	23.0	

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMB}	$V_{CSP\_}$ - $V_{CSN\_}$, V_{SR} = 3V or V_{SR} = 5V, exclude one-phase operaton	R_{SENSE} = 0.65mΩ, I_{MAXB} = 39A	29.0	33.0	37.0	mV
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 36A	28.0	32.0	36.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 23A	17.0	21.0	25.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 20A	14.0	18.0	22.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 39A	35.0	39.0	43.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 36A	32.5	36.5	40.5	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 23A	19.5	23.5	27.5	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 20A	17.0	21.0	25.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 39A	39.0	43.0	47.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 36A	36.5	40.5	44.5	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 23A	22.0	26.0	30.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 20A	19.5	23.5	27.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 39A	43.5	47.5	51.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 36A	40.0	44.0	48.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 23A	26.0	30.0	34.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 20A	22.0	26.0	30.0	
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZERO}	V_{GND} - $V_{LX\_}$			1		mV
Current-Balance Offset Voltage				-1.5		+1.5	mV
CSPAAVE, CSPBAVE, CSP_, Input Current		T_A = +25°C		-0.12		+0.12	µA
CSN_ Pulldown Current				7		14	µA
Phase Disable Threshold		CSPB2, CSPB1, CSPA3, CSPA2, CSPA1		3	V_{CC} - 1	V_{CC} - 0.4	V
FB_ Droop Amplifier (GMD) Offset		(V_{CSP_AVE} - $V_{CSN\_}$) at $I_{FB\_}$ = 0mA		-1.0		+1.0	mV
FB_ Droop Amplifier (GMD) Transconductance		$\Delta I_{FB\_}/\Delta(V_{CSP\_AVE} - V_{CSN\_})$, V_{CSP_AVE} - $V_{CSN\_}$ = -15mV to +15mV		591	600	609	µS

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IMAX_ LOGIC						
IMAX_ Detection Thresholds		Threshold 0, fault			13.65 x V_{CC}/50	V
		Threshold 1, R_{SENSE} = 0.65mΩ, I_{MAX} = 39A	14.20 x V_{CC}/50		14.65 x V_{CC}/50	
		Threshold 2, R_{SENSE} = 0.65mΩ, I_{MAX} = 36A	15.20 x V_{CC}/50		15.65 x V_{CC}/50	
		Threshold 3, R_{SENSE} = 0.65mΩ, $I_{MAXA/B}$ = 30A/23A	16.20 x V_{CC}/50		16.65 x V_{CC}/50	
		Threshold 4, R_{SENSE} = 0.65mΩ, $I_{MAXA/B}$ = 26A/20A	17.20 x V_{CC}/50		17.65 x V_{CC}/50	
		Threshold 5, R_{SENSE} = 0.75mΩ, I_{MAX} = 39A	18.20 x V_{CC}/50		18.65 x V_{CC}/50	
		Threshold 6, R_{SENSE} = 0.75mΩ, I_{MAX} = 36A	19.20 x V_{CC}/50		19.65 x V_{CC}/50	
		Threshold 7, R_{SENSE} = 0.75mΩ, I_{MAX} = 30A/23A	20.20 x V_{CC}/50		20.65 x V_{CC}/50	
		Threshold 8, R_{SENSE} = 0.75mΩ, I_{MAX} = 26A/20A	21.20 x V_{CC}/50		21.65 x V_{CC}/50	
		Threshold 9, R_{SENSE} = 0.85mΩ, I_{MAX} = 39A	22.20 x V_{CC}/50		22.65 x V_{CC}/50	
		Threshold 10, R_{SENSE} = 0.85mΩ, I_{MAX} = 36A	23.20 x V_{CC}/50		23.65 x V_{CC}/50	
		Threshold 11, R_{SENSE} = 0.85mΩ, $I_{MAXA/B}$ = 30A/23A	24.20 x V_{CC}/50		24.65 x V_{CC}/50	
		Threshold 12, R_{SENSE} = 0.85mΩ, $I_{MAXA/B}$ = 26A/20A	25.20 x V_{CC}/50		25.65 x V_{CC}/50	
		Threshold 13, R_{SENSE} = 0.95mΩ, I_{MAX} = 39A	26.20 x V_{CC}/50		26.65 x V_{CC}/50	
		Threshold 14, R_{SENSE} = 0.95mΩ, I_{MAX} = 36A	27.20 x V_{CC}/50		27.65 x V_{CC}/50	
		Threshold 15, R_{SENSE} = 0.95mΩ, $I_{MAXA/B}$ = 30A/23A	28.20 x V_{CC}/50		28.65 x V_{CC}/50	
		Threshold 16, R_{SENSE} = 0.95mΩ, $I_{MAXA/B}$ = 26A/20A	29.20 x V_{CC}/50		29.65 x V_{CC}/50	
		Threshold 17, fault	30.20 x V_{CC}/50			

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V	High state (pullup)		0.9	2.5	Ω
			Low state (pulldown)		0.7	2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			0.7	2.0	Ω
		Low state (pulldown)			0.25	0.7	
Internal BST_ Switch On-Resistance	R_{BST}	BSTA1 to V_{DDA}, BSTA2 to V_{DDA}, BSTB to V_{DDB}, $V_{DD\_}$ = 5V			10	20	Ω
DH_ Gate-Driver Source Current	$I_{DH(SRC)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.2		A
DH_ Gate-Driver Sink Current	$I_{DH(SINK)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.7		A
DL_ Gate-Driver Source Current	$I_{DL(SRC)}$	DL_ forced to 2.5V			2.7		A
DL_ Gate-Driver Sink Current	$I_{DL(SINK)}$	DL_ forced to 2.5V			8		A
Driver Propagation Delay		DH_ low to DL_ high			30		ns
		DL_ low to DH_ high			30		
DL_ Transition Time		DL_ falling, C_{DL} = 3nF			20		ns
		DL_ rising, C_{DL} = 3nF			20		
DH_ Transition Time		DH_ falling, C_{DH} = 3nF			20		ns
		DH_ rising, C_{DH} = 3nF			20		
DRVPWMA, DRVPWMB Logic-High Voltage		I_{SOURCE} = 3mA		$V_{DD\_}$ - 0.4			V
DRVPWMA, DRVPWMB Logic-Low Voltage		I_{SINK} = 3mA				0.4	V
LOGIC AND I/O							
Enable Input High Voltage	V_{EN_IH}			0.67			V
Enable Input Low Voltage	V_{EN_IL}					0.33	V
Enable Input Current		T_A = +25°C		-1		+1	µA
SERIALVID INTERFACE (per Intel SerialVID Specification—see the *Detailed Description*)							
SerialVID Input Low Voltage (CLK, VDIO)	V_{IL}			-0.1		+0.45	V
SerialVID Input High Voltage (CLK, VDIO)	V_{IH}			0.65		V_{TT} + 1V	V
SerialVID Output High Voltage (VDIO, ALERT#)	V_{OH}	Open-drain pullup to V_{TT}			V_{TT}		V
SerialVID Output Low Level (VDIO, ALERT#)	V_{OL}	Open-drain pullup to V_{TT}, R_{PU} = 50Ω				0.36	V

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C. All devices 100% tested at T_A = +25°C. Limits over temperature guaranteed by design.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SerialVID Open-Drain Output On-Resistance (VDIO, ALERT#, VRHOT#)	R_{ON}	I_{SINK} = 30mA	4		13	Ω
SerialVID Logic-Input Leakage Current (CLK, VDIO)		T_A = +25°C	-1		+1	µA
ALERT# Deasserted Leakage Current		T_A = +25°C, $V_{ALERT\#}$ = 3.3V			1	µA
SerialVID Logic Slew Rate (CLK, VDIO, ALERT#)			0.5		2.0	V/ns
SerialVID Input Capacitance	C_{PAD}				4	pF
CLK Frequency	f_{CLK}		13	25	33.3	MHz
CLK Absolute Min/Max Period		Specified as a percentage of f_{CLK}	-5		+5	%
CLK High Time	t_{HIGH}	Specified as a percentage of t_{CLK} period	45			%
CLK Low Time	t_{LOW}	Specified as a percentage of t_{CLK} period	45			%
Rise Time	t_{RISE}		0.25		2.5	ns
Fall Time	t_{FALL}		0.25		2.5	ns
Duty Cycle			45		55	%
SerialVID Inactivity Timeout	t_{RSTNA}		0.14		0.40	µs

ELECTRICAL CHARACTERISTICS

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input Voltage Range		V_{CC}, V_{DDA}, V_{DDB}		4.5		5.5	V
DC Output Voltage Accuracy		Measured at FB_ with respect to GNDS_; includes load regulation error (Note 2)	DAC codes from 1.000V to 1.520V	-0.8		+0.8	%
			DAC codes from 0.800V to 0.995V	-8		+8	mV
			DAC codes from 0.250 to 0.795V	-8		+8	
$V_{SETTLED}$ BIT Accuracy		Upward transitions		-15		-5	mV
		Downward transitions		5		15	
GNDS_ Input Range				-200		+200	mV
GNDS_ Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS\_}$		0.97		1.03	V/V
Boot Voltage	V_{BOOT}	MAX17511N only, Reg A and Reg B		1.091		1.109	V
		MAX17511C only, Reg B only		0.892		0.908	

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DHA_ On-Time (Note 3)	t_{ONA}	Measured at DHA_ (600kHz - 10%), R_{TON} = 96.7kΩ (MAX17411 only), R_{TON} = 48.35K (MAX17511/MAX17511C/MAX17511N/MAX17511T)		157		213	ns
		Measured at DHA_, V_{IN} = 12V (300kHz - 10%), R_{TON} = 200kΩ (MAX17411 only), R_{TON} = 100kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)		276		338	
		Measured at DHA_ (200kHz - 10%), R_{TON} = 303.3kΩ (MAX17411 only), R_{TON} = 151.65kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)		470		638	
DHB On-Time (Note 3)	t_{ONB}	Measured at DHB (600kHz + 10%), R_{TON} = 96.7kΩ (MAX17411 only), R_{TON} = 48.35kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)		128		174	ns
		Measured at DHB, V_{IN} = 12V (300kHz + 10%), R_{TON} = 200kΩ (MAX17411 only), R_{TON} = 100kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)		226		277	
		Measured at DHB (200kHz + 10%), R_{TON} = 303.3kΩ (MAX17411 only), R_{TON} = 151.65kΩ (MAX17511/MAX17511C/MAX17511N/MAX17511T)		385		521	
Minimum Off-Time (Note 3)	$t_{OFF(MIN)}$	Measured at DH_		150		250	ns
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{BIAS}	Measured at V_{CC}, SKIP mode, FB_ forced above the regulation point				10	mA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, EN = GND				30	µA
SLEW-RATE CONTROL							
Slew-Rate Accuracy		V_{SR} = 0V or V_{SR} = 5V	SetVID - fast slew rate = 10mV/µs (min)	10			mV/µs
			SetVID - slow slew rate = 2.5mV/µs (min)	2.5			
		V_{SR} = 3V or V_{SR} = 1.5V	SetVID - fast slew rate = 20mV/µs (min)	20			
			SetVID - slow slew rate = 5mV/µs (min)	5			
Soft-Start Slew Rate		Non-zero V_{BOOT}		2.5			mV/µs
SR Four-Level Logic Thresholds		Low				0.4	V
		Mid-low		1.2		1.8	
		Mid-high		2.2		V_{CC} - 1.2V	
		High		V_{CC} - 0.4V			

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT PROTECTION							
Upper POK_ (MAX17411/ MAX17511/MAX17511N/ MAX17511T) and Output Overvoltage Protection Trip Threshold (MAX17411/ MAX17511/MAX17511C/ MAX17511N)	V_{OVP}	SKIP mode after output reaches the regulation voltage or PWM mode; measured at FB_ with respect to the voltage target set by the VID code (see Table 3)		200		300	mV
		Soft-start, SKIP mode, and output has not reached the regulation voltage, measured at FB_		1.72		1.82	V
Lower POK_ and Output Undervoltage Protection Trip Threshold	V_{UVP}	Measured at FB_ with respect to unloaded output voltage		-300		-200	mV
Output Undervoltage Propagation Delay	t_{UVP}	FB_ forced 25mV below trip threshold		100		350	µs
POK_ Output Low Voltage		I_{SINK} = 4mA				0.3	V
V_{CC} Undervoltage Lockout Threshold	V_{UVLO}	Rising edge, 50mV typical hysteresis, controller disabled below this level		4.05		4.45	V
THERMAL PROTECTION							
VR_HOT# Trip Threshold		Measured at THERM_ with respect to V_{CC} falling edge; specify as % error for all TEMP MAX DAC code settings; typical hysteresis = 100mV		49.5		50.5	%
Thermal Zone Registers Trip Points		Thermal zone comparator trip points, measured with respect to V_{CC}, voltage threshold corresponding to TMAX x (1 - N%), N = 0, 3, 6, 9, 12, 15, 18, 25		49 + 24 x N/31		51 + 24 x N/31	%
VALLEY CURRENT LIMIT AND DROOP							
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMA}	$V_{CSP\_}$ - $V_{CSN\_}$, V_{SR} = 0V, V_{SR} = 1.5V, or one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXA} = 39A	22.5		28.5	mV
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 36A	21.5		27.5	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 30A	17.0		23.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 26A	15.0		21.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 39A	27.0		33.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 36A	25.0		31.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 30A	20.0		26.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 26A	17.0		23.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 39A	30.0		36.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 36A	28.0		34.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 30A	22.5		28.5	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 26A	20.0		26.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 39A	33.5		39.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 36A	31.0		37.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 30A	25.0		31.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 26A	21.5		27.5	

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMA}	$V_{CSP\_}$ - $V_{CSN\_}$, V_{SR} = 3V or V_{SR} = 5V, exclude one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXA} = 39A	29.0		37.0	mV
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 36A	28.0		36.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 30A	22.0		30.0	
			R_{SENSE} = 0.65mΩ, I_{MAXA} = 26A	19.5		27.5	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 39A	35.0		43.0	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 36A	32.5		40.5	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 30A	26.0		33.8	
			R_{SENSE} = 0.75mΩ, I_{MAXA} = 26A	22.0		30.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 39A	39.0		47.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 36A	36.5		44.5	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 30A	29.0		37.0	
			R_{SENSE} = 0.85mΩ, I_{MAXA} = 26A	26.0		34.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 39A	43.5		51.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 36A	40.0		48.0	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 30A	32.5		40.5	
			R_{SENSE} = 0.95mΩ, I_{MAXA} = 26A	28.0		36.0	
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMB}	$V_{CSP\_}$ - $V_{CSN\_}$, V_{SR} = 0V, V_{SR} = 1.5V, or one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXB} = 39A	22.5		28.5	mV
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 36A	21.5		27.5	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 23A	13.0		19.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 20A	11.0		17.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 39A	27.0		33.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 36A	25.0		31.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 23A	15.0		21.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 20A	13.0		19.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 39A	30.0		36.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 36A	28.0		34.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 23A	17.0		23.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 20A	15.0		21.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 39A	33.5		39.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 36A	31.0		37.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 23A	20.0		26.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 20A	17.0		23.0	

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Valley Current-Limit Threshold Voltage (Positive)	V_{ILIMB}	$V_{CSP\_}$ - $V_{CSN\_}$, V_{SR} = 3V or V_{SR} = 5V, exclude one-phase operation	R_{SENSE} = 0.65mΩ, I_{MAXB} = 39A	29.0		37.0	mV
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 36A	28.0		36.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 23A	17.0		25.0	
			R_{SENSE} = 0.65mΩ, I_{MAXB} = 20A	14.0		22.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 39A	35.0		43.0	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 36A	32.5		40.5	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 23A	19.5		27.5	
			R_{SENSE} = 0.75mΩ, I_{MAXB} = 20A	17.0		25.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 39A	39.0		47.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 36A	36.5		44.5	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 23A	22.0		30.0	
			R_{SENSE} = 0.85mΩ, I_{MAXB} = 20A	19.5		27.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 39A	43.5		51.5	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 36A	40.0		48.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 23A	26.0		34.0	
			R_{SENSE} = 0.95mΩ, I_{MAXB} = 20A	22.0		30.0	
Current-Balance Offset Voltage				-1.5		+1.5	mV
Phase Disable Threshold		CSPB2, CSPB1, CSPA3, CSPA2, CSPA1		3		V_{CC} - 0.4	V
FB_ Droop Amplifier (G_{MD}) Offset		V_{CSP_AVE} - $V_{CSN\_}$ at $I_{FB\_}$ = 0mA		-1.0		+1.0	mV
FB_ Droop Amplifier (G_{MD}) Transconductance		$\Delta I_{FB\_}/\Delta(V_{CSP\_AVE} - V_{CSN\_})$, V_{CSP_AVE} - $V_{CSN\_}$ = -15mV to +15mV		588		612	µS

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
IMAX_ LOGIC							
IMAX_ Detection Thresholds		Threshold 0, fault				13.65 x V_{CC}/50	V
		Threshold 1, R_{SENSE} = 0.65mΩ, I_{MAX} = 39A		14.20 x V_{CC}/50		14.65 x V_{CC}/50	
		Threshold 2, R_{SENSE} = 0.65mΩ, I_{MAX} = 36A		15.20 x V_{CC}/50		15.65 x V_{CC}/50	
		Threshold 3, R_{SENSE} = 0.65mΩ, $I_{MAXA/B}$ = 30A/23A		16.20 x V_{CC}/50		16.65 x V_{CC}/50	
		Threshold 4, R_{SENSE} = 0.65mΩ, $I_{MAXA/B}$ = 26A/20A		17.20 x V_{CC}/50		17.65 x V_{CC}/50	
		Threshold 5, R_{SENSE} = 0.75mΩ, I_{MAX} = 39A		18.20 x V_{CC}/50		18.65 x V_{CC}/50	
		Threshold 6, R_{SENSE} = 0.75mΩ, I_{MAX} = 36A		19.20 x V_{CC}/50		19.65 x V_{CC}/50	
		Threshold 7, R_{SENSE} = 0.75mΩ, I_{MAX} = 30A/23A		20.20 x V_{CC}/50		20.65 x V_{CC}/50	
		Threshold 8, R_{SENSE} = 0.75mΩ, I_{MAX} = 26A/20A		21.20 x V_{CC}/50		21.65 x V_{CC}/50	
		Threshold 9, R_{SENSE} = 0.85mΩ, I_{MAX} = 39A		22.20 x V_{CC}/50		22.65 x V_{CC}/50	
		Threshold 10, R_{SENSE} = 0.85mΩ, I_{MAX} = 36A		23.20 x V_{CC}/50		23.65 x V_{CC}/50	
		Threshold 11, R_{SENSE} = 0.85mΩ, $I_{MAXA/B}$ = 30A/23A		24.20 x V_{CC}/50		24.65 x V_{CC}/50	
		Threshold 12, R_{SENSE} = 0.85mΩ, $I_{MAXA/B}$ = 26A/20A		25.20 x V_{CC}/50		25.65 x V_{CC}/50	
		Threshold 13, R_{SENSE} = 0.95mΩ, I_{MAX} = 39A		26.20 x V_{CC}/50		26.65 x V_{CC}/50	
		Threshold 14, R_{SENSE} = 0.95mΩ, I_{MAX} = 36A		27.20 x V_{CC}/50		27.65 x V_{CC}/50	
		Threshold 15, R_{SENSE} = 0.95mΩ, $I_{MAXA/B}$ = 30A/23A		28.20 x V_{CC}/50		28.65 x V_{CC}/50	
		Threshold 16, R_{SENSE} = 0.95mΩ, $I_{MAXA/B}$ = 26A/20A		29.20 x V_{CC}/50		29.65 x V_{CC}/50	
		Threshold 17, fault		30.20 x V_{CC}/50			
GATE DRIVERS							
DH_ Gate-Driver On-Resistance	$R_{ON(DH)}$	BST_ - LX_ forced to 5V	High state (pullup)			2.5	Ω
			Low state (pulldown)			2.0	
DL_ Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)				2.0	Ω
		Low state (pulldown)				0.7	

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

ELECTRICAL CHARACTERISTICS (continued)

(Circuits of Figures 1 and 2. V_{IN} = 10V, V_{CC} = V_{DDA} = V_{DDB} = 5V, EN = V_{CC}, $V_{GNDS\_}$ = 0V, $V_{FB\_}$ = V_{CSP_AVE} = $V_{CSP\_}$ = $V_{CSN\_}$ = 1V; [SerialVID = 1.00, FPWM MODE]; **T_A = -40°C to +105°C**, unless otherwise noted. Specifications to -40°C and +105°C are guaranteed by design, not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Internal BST_ Switch On-Resistance	R_{BST}	BSTA1 to V_{DDA}, BSTA2 to V_{DDA}, BSTB to V_{DDB} $V_{DD\_}$ = 5V			20	Ω
DRVPWMA, DRVPWMB Logic-High Voltage		I_{SOURCE} = 3mA	$V_{DD\_}$ - 0.4			V
DRVPWMA, DRVPWMB Logic-Low Voltage		I_{SINK} = 3mA			0.4	V
LOGIC AND I/O						
Enable Input High Voltage	V_{EN_IH}		0.67			V
Enable Input Low Voltage	V_{EN_IL}				0.33	V
SERIALVID INTERFACE (per Intel SerialVID specification—see the *Detailed Description*)						
SerialVID Input Low Voltage (CLK, VDIO)	V_{IL}		-0.1		+0.45	V
SerialVID Input High Voltage (CLK, VDIO)	V_{IH}		0.65		V_{TT} + 1V	V
SerialVID Output Low Level (VDIO, ALERT#)	V_{OL}	Open-drain pullup to V_{TT}, R_{PU} = 50Ω			0.36	V
SerialVID Open-Drain Output On-Resistance (VDIO, ALERT#, VRHOT#)	R_{ON}	I_{SINK} = 30mA, T_A = 0°C to +105°C	4		13	Ω
SerialVID Logic Slew Rate (CLK, VDIO, ALERT#)			0.5		2.0	V/ns
SerialVID Input Capacitance	C_{PAD}				4	pF
CLK Frequency	f_{CLK}		13		33.3	MHz
CLK Absolute Min/Max Period		Specified as a percentage of f_{CLK}	-5		+5	%
CLK High Time	t_{HIGH}	Specified as a percentage of t_{CLK} period	45			%
CLK Low Time	t_{LOW}	Specified as a percentage of t_{CLK} period	45			%
Rise Time	t_{RISE}		0.25		2.5	ns
Fall Time	t_{FALL}		0.25		2.5	ns
Duty Cycle			45		55	%
SerialVID Inactivity Timeout	t_{RSTNA}		0.14		0.40	µs

Note 2: The equation for the target voltage V_{TARGET} is:

V_{TARGET} = the slew-rate-controlled version of either V_{DAC}

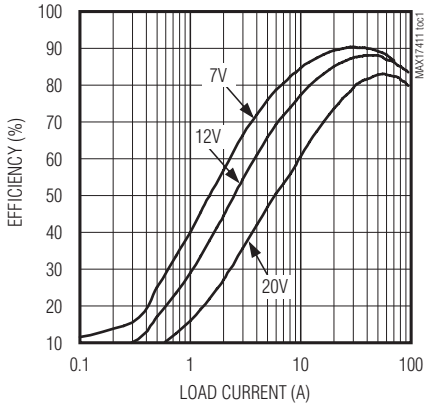
where V_{DAC} = 0V for shutdown, V_{DAC} = V_{BOOT} during startup, otherwise V_{DAC} = V_{ID} (the V_{ID} voltages for all possible VID codes are given in Table 3 and V_{OFFSET} = the negative or positive offset to the output voltage based on the voltage set from the offset register and the mode of operation (startup, shutdown, deeper sleep, or normal operation), as defined elsewhere in this document.

Note 3: On-time and minimum off-time specifications are measured from 50% to 50% at the DH_ pin, with LX_ forced to 0V, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times may be different due to MOSFET switching speeds.

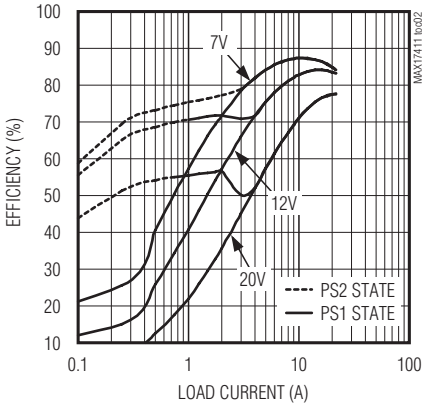
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

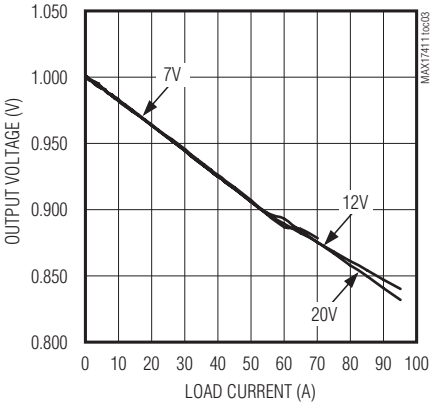
REG A EFFICIENCY vs. LOAD CURRENT IN PS0 STATE (SVID = 1V)



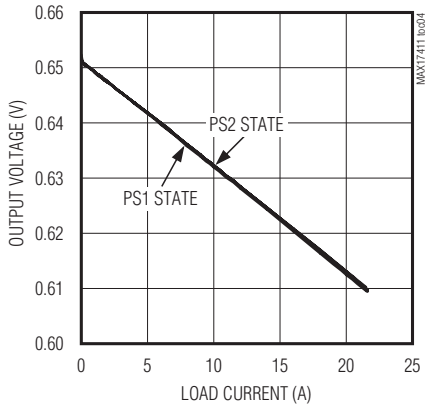
REG A EFFICIENCY vs. LOAD CURRENT IN PS1 AND PS2 STATES (SVID = 0.65V)



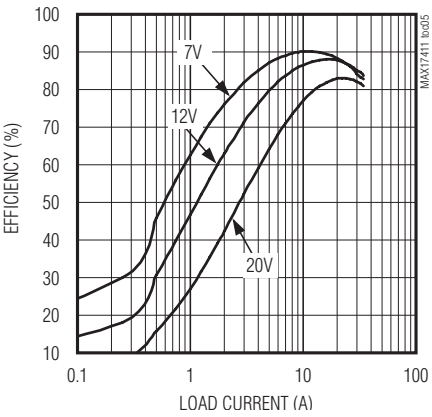
REG A OUTPUT VOLTAGE vs. LOAD CURRENT IN PS0 STATE (SVID = 1V)



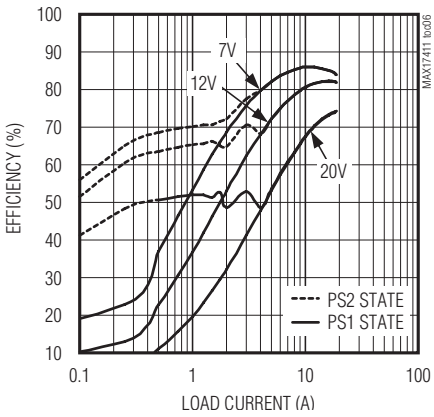
REG A OUTPUT VOLTAGE vs. LOAD CURRENT IN PS1 AND PS2 STATES (SVID = 0.65V)



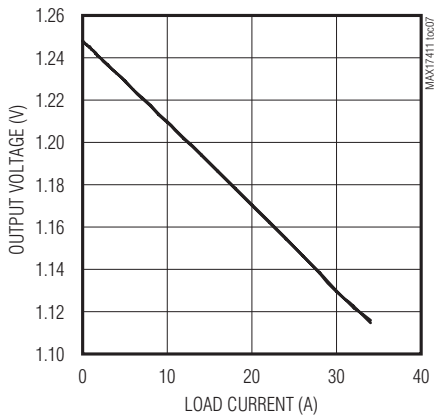
REG B EFFICIENCY vs. LOAD CURRENT IN PS0 STATE (SVID = 1.25V) (MAX17511/C/N/T ONLY)



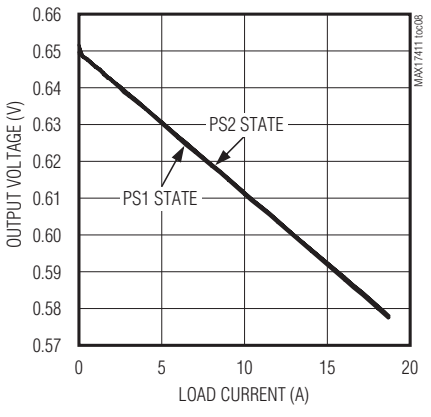
REG B EFFICIENCY vs. LOAD CURRENT IN PS1 AND PS2 STATES (SVID = 0.65V) (MAX17511/C/N/T ONLY)



REG B OUTPUT VOLTAGE vs. LOAD CURRENT IN PS0 STATE (SVID = 1.25V) (MAX17511/C/N/T ONLY)



REG B OUTPUT VOLTAGE vs. LOAD CURRENT IN PS1 AND PS2 STATES (SVID = 0.65V) (MAX17511/C/N/T ONLY)

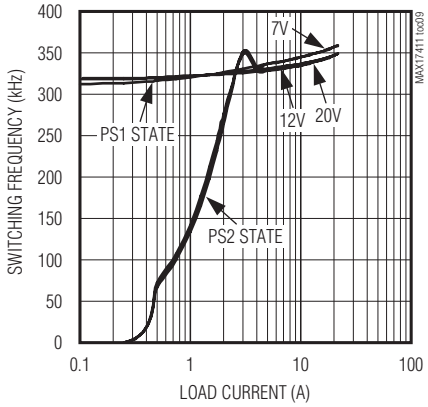


Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

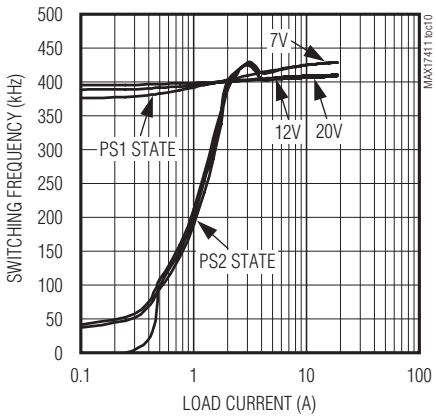
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

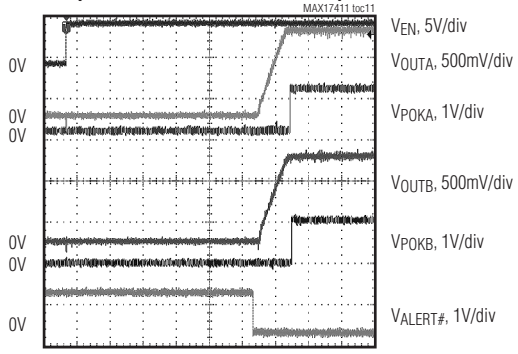
REG A SWITCHING FREQUENCY vs. LOAD CURRENT (SVID = 0.65V)



REG B SWITCHING FREQUENCY vs. LOAD CURRENT (SVID = 0.65V) (MAX17511/C/N/T ONLY)

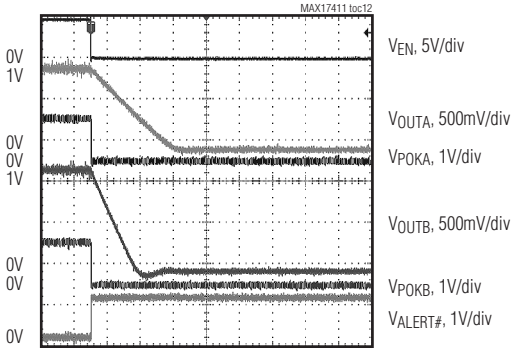


NON-ZERO V_{BOOT} STARTUP WAVEFORMS (V_{BOOT}, 1.05V) (MAX17511/MAX17511T ONLY)



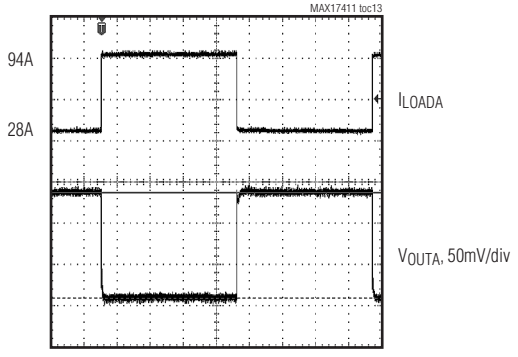
V_{IN} = 12V THERMA = THERMB = GND

SHUTDOWN WAVEFORMS

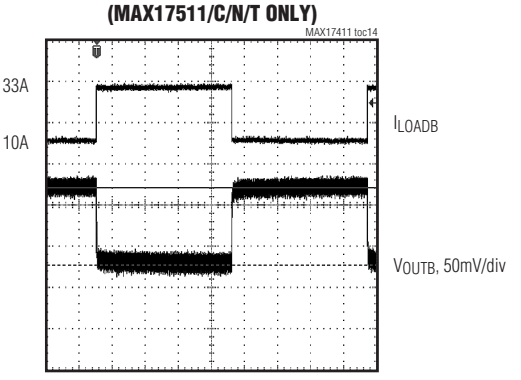


V_{IN} = 12V V_{LOADA} = 5A V_{LOADB} = 5A

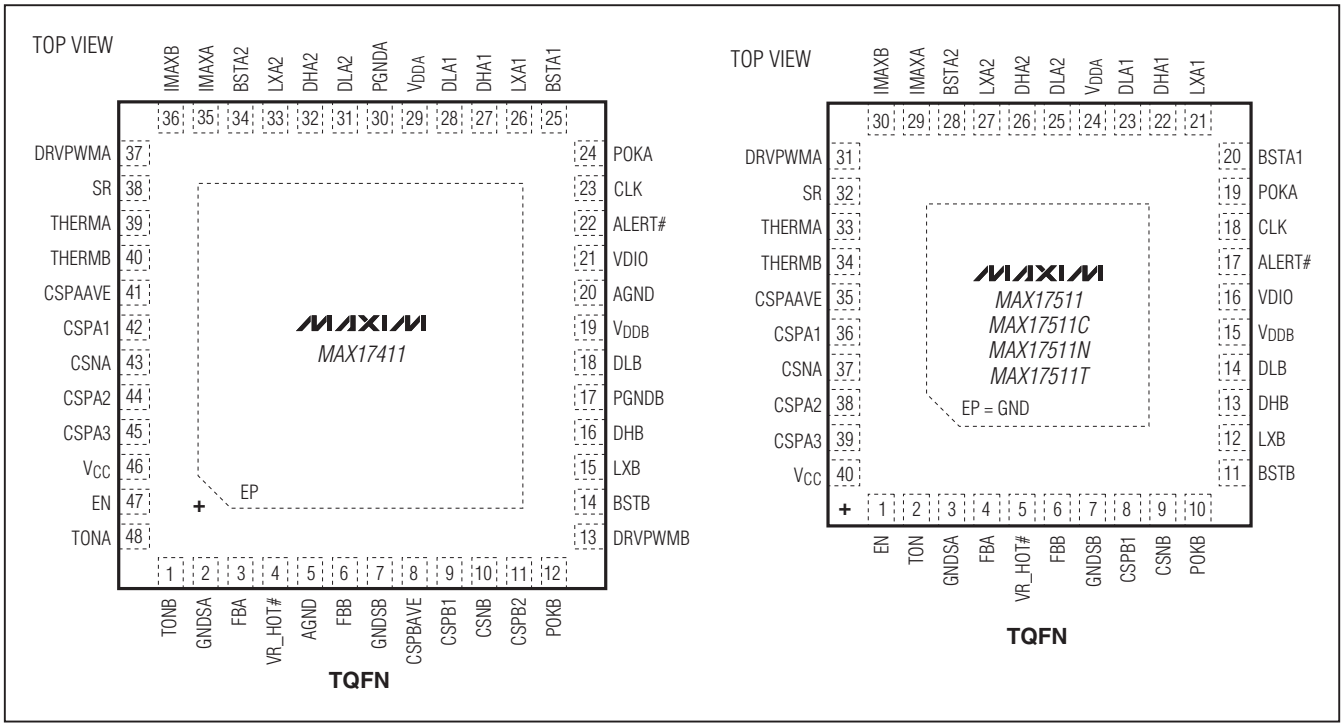
REG A LOAD-TRANSIENT RESPONSE



REG B LOAD-TRANSIENT RESPONSE (MAX17511/C/N/T ONLY)



Pin Configurations



Pin Description

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
1	—	TONB	Switching Frequency Adjustment Input for Regulator B. An external resistor between the input power source and TONB sets the switching period (per phase) for regulator B according to the following equation: $t_{SWB} = (R_{TONB} + 6.5k\Omega) \times 14.6pF$ where $f_{SWB} = 1/t_{SWB}$ is the nominal switching frequency. TONB is high-impedance in shutdown. If REG B is disabled, connect TONB to GND or V_{CC}.
—	2	TON	Switching Frequency Adjustment Input for Both Regulators. An external resistor between the input power source and TON sets the switching period (per phase) according to the following equations: $t_{SWA} = (2 \times R_{TON} + 6.5k\Omega) \times 17.9pF$ $t_{SWB} = (2 \times R_{TON} + 6.5k\Omega) \times 14.6pF$ where $f_{SW} = 1/t_{SW}$ is the nominal switching frequency. If REG B is disabled: $t_{SWA} = (R_{TON} + 6.5k\Omega) \times 17.9pF$ TON is high-impedance in shutdown.

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
2	3	GNDSA	Ground Remote-Sense Input for Regulator A. Connect GNDSA to the ground-sense pin of the CPU located directly at the point of load. GNDSA internally connects to an internal transconductance amplifier that adjusts the output voltage to compensate for voltage drops between the controller analog ground and the load ground.
3	4	FBA	Feedback Remote-Sense Input and Voltage Positioning Transconductance (VPS) Amplifier Output for Regulator A. Connect a resistor (R_{FBA}) between FBA and the positive side of the feedback remote sense (the CPU output remote sense (V_{CC_SENSE})) to set the DC steady-state droop based on the voltage-positioning gain requirement. $$R_{FBA} = (N_{PH} \times R_{DROOP})/(R_{SENSEA} \times G_{MD})$$ where R_{DROOP} is the desired voltage-positioning slope, G_{MD} = 600µS (typ), and R_{SENSEA} is the current-sense resistance with respect to the CSPAAVE to CSNA current-sense inputs. See the *CSP_AVE - CSN_ Inputs* section. FBA is internally connected to the input of an error comparator and an integrator that corrects for output ripple, error comparator offsets, and the ground-sense offset of regulator A as shown in Figure 5. Shorting FBA directly to the output disables voltage positioning, but impacts the stability requirements. Designs that disable voltage positioning require a higher minimum output capacitance ESR to maintain stability (see the *Output Capacitor Selection* section). FBA enters a high-impedance state in shutdown.
4	5	VR_HOT#	Open-Drain Output of the Thermal Comparators that monitor THERMA and THERMB. These comparators are wire-ORed with output at VR_HOT#. This output is required as backup to the temperature zone register in the event of an SVID bus failure. The comparator responds to the temperature threshold voltage of 2.5V at THERMA OR THERMB. This threshold is equivalent to the 100% threshold defined in the Temperature-Zone register (12h).
5, 20	—	AGND	Analog Ground

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
6	6	FBB	Feedback Remote-Sense Input and Voltage Positioning Transconductance (VPS) Amplifier Output for Regulator B. Connect a resistor (R_{FBB}) between FBB and the positive side of the feedback remote sense to set the DC steady-state droop based on the voltage-positioning gain requirement. $$R_{FBB} = (N_{PH} \times R_{DROOP})/(R_{SENSEB} \times G_{MD})$$ where R_{DROOP} is the desired voltage-positioning slope, G_{MD} = 600µS (typ), and R_{SENSEB} is the current-sense resistance with respect to the CSPBAVE to CSNB (MAX17411) or CSPB1 - CSNB (MAX17511/MAX17511C/MAX17511N/MAX17511T) current-sense inputs. See the *CSP_AVE – CSN_ Inputs* section. FBB is internally connected to the input of an error comparator and an integrator that corrects for output ripple, error comparator offsets, and the ground-sense offset of regulator B as shown in Figures 6 and 7. Shorting FBB directly to the output disables voltage positioning, but impacts the stability requirements. Designs that disable voltage positioning require a higher minimum output capacitance ESR to maintain stability (see the *Output Capacitor Selection* section). FBB enters a high-impedance state in shutdown.
7	7	GNDSB	Ground Remote-Sense Input for Regulator B. Connect GNDSB to the ground-sense pin of the GFX located directly at the point of load. GNDSB internally connects to an internal transconductance amplifier that adjusts the output voltage to compensate for voltage drops between the controller analog ground and the load ground.
8	—	CSPBAVE	Positive Current-Sense Average Input for Regulator B. Connect CSPBAVE to the positive side of the differential output of external current-sense averaging network. The averaging is achieved by using a resistive summation and current-sense resistors, or by using a parallel DCR sense network with a single NTC thermistor for thermal compensation (see Figure 9). The average current-sense input is used for the load-line and current monitor.
9	8	CSPB1	Positive Current-Sense Input for Regulator B. Connect CSPB1 to the positive side of the current-sense resistor or the DCR sense filter capacitor of regulator B as shown in Figure 8. To *completely* disable Regulator B, Connect CSPB1 and CSPB2 to V_{CC}. Also leave BSTB, DHB, LXB, DLB, CSPBAVE, and CSNB unconnected. Address 1 is disabled from the SVID bus.
10	9	CSNB	Negative Current-Sense Input of Regulator B. Connect CSNB to the negative side of the current-sense element as shown in Figure 8. An internal 20Ω discharge MOSFET between CSNB and ground is enabled under an input UVLO or shutdown condition. A bypass capacitor between CSNB and GND in the range of 1nF to 0.1µF is recommended.

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
11	—	CSPB2	Positive Current-Sense Input for Second Phase of Regulator B. Connect CSPB2 to the positive side of the current-sense element of the second phase of regulator B as shown in Figure 8.Connect CSPB2 to V_{CC} and leave DRVPWMB unconnected to disable the second phase of Regulator B.
12	10	POKB	Open-Drain Power-Good Output for Regulator B. During soft-start and shutdown, POKB stays low. At the end of soft-start, approximately 20µs (typ) after FBB reaches the output voltage set by the VID code, POKB becomes high-impedance and remains high-impedance as long as FBB is in regulation. POKB is blanked high-impedance when the slew-rate controller for regulator B is active (VID transition occurs). In pulse-skipping mode, the upper POKB threshold is blanked during downward transitions until the output voltage reaches its regulation value.POKB is forced low in shutdown (EN = GND) and after any fault condition is detected on either regulator.To obtain a logic signal, pull up POKB with an external resistor connected to a positive logic supply of +5V and lower.
13	—	DRVPWMB	Direct-Drive PWM Output for Controlling the External Second Phase Driver for Regulator B. DRVPWMB is three-stated in shutdown when the controller detects an output overvoltage fault condition on regulator B.
14	11	BSTB	Boost Flying Capacitor Connection for High-Side Gate Voltage for the First Phase of Regulator B. Connect a ceramic capacitor between BSTB and LXB. See the *Boost Capacitors* section.
15	12	LXB	Inductor Connection for the First Phase of Regulator B. LXB serves as the lower supply rail for the DHB high-side gate driver. LXB is also used as an input to the zero-crossing comparator for regulator B.
16	13	DHB	High-Side Gate-Driver Output for Regulator B. DHB output voltage swings from V_{BSTB} to V_{LXB}. DHB is pulled low in shutdown.
17	—	PGNDB	Power Ground of the Low-Side Driver of Regulator B
18	14	DLB	Low-Side Gate-Driver Output for the First Phase of Regulator B. DLB output voltage swings from V_{DDB} to GND. DLB is forced high when the controller detects an output overvoltage fault condition on regulator B. DLB is forced low in shutdown and in pulse-skipping mode when an inductor current zero crossing (LXB - GND) is detected.
19	15	V_{DDB}	Driver-Supply Voltage Input for Regulator B. V_{DDB} provides power for the low-side driver of regulator B and is used to recharge the BSTB flying capacitor during the on-time of DLB. Connect V_{DDB} to the 4.5V to 5.5V system supply voltage. Bypass V_{DDB} to power ground with a 1µF or greater ceramic capacitor.
21	16	VDIO	Serial VID Input/Output
22	17	ALERT#	Serial VID Alert Output. ALERT# is in the high state in shutdown.
23	18	CLK	Serial VID Clock Input

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
24	19	POKA	Open-Drain Power-Good Output for Regulator A. During soft-start and shutdown, POKA stays low. At the end of soft-start, approximately 20µs (typ) after FBA reaches the output voltage set by the VID code, POKA becomes high-impedance and remains high-impedance as long as FBA is in regulation. POKA is blanked high-impedance when the slew-rate controller for regulator A is active (VID transition occurs). In pulse-skipping mode, the upper POKA threshold is blanked during downward transitions until the output voltage reaches its regulation value. POKA is forced low in shutdown (EN = GND) and after any fault condition is detected on either regulator. To obtain a logic signal, pull up POKA with an external resistor connected to a positive logic supply of +5V and lower.
25	20	BSTA1	Boost Flying Capacitor Connection for High-Side Gate Voltage for the First Phase of Regulator A. Connect a ceramic capacitor between BSTA1 and LXA1. See the *Boost Capacitors* section.
26	21	LXA1	Inductor Connection for the First Phase of Regulator A. LXA1 serves as the lower supply rail for the DHA1 high-side gate driver. LXA1 is also used as an input to the zero-crossing comparator for regulator A.
27	22	DHA1	High-Side Gate-Driver Output for the First Phase of Regulator A. DHA1 output voltage swings from V_{BSTA1} to V_{LXA1}. DHA1 is pulled low in shutdown.
28	23	DLA1	Low-Side Gate-Driver Output for the First Phase of Regulator A. DLA1 output voltage swings from V_{DDA} to V_{GND}. DLA1 is forced high when the controller detects an output overvoltage fault condition on regulator A. DLA1 is forced low in shutdown and in pulse-skipping mode when an inductor current zero crossing (LXA1 - GND) is detected.
29	24	V_{DDA}	Driver Supply Voltage Input for Regulator A. V_{DDA} is the driver supply voltage used for the DLA_ low-side drivers, and to recharge the BSTA_ flying capacitors when the corresponding DLA_s are high. Connect V_{DDA} to the 4.5V to 5.5V system supply voltage. Bypass V_{DDA} to power ground with a 1µF or greater ceramic capacitor.
30	—	PGNDA	Power Ground of the Low-Side Drivers of Regulator A.
31	25	DLA2	Low-Side Gate-Driver Output for the Second Phase of Regulator A. DLA2 Output Voltage swings from V_{DDA} to V_{GND}. DLA2 is forced high when the controller detects an output overvoltage fault condition on regulator A. DLA2 is forced low in shutdown and in pulse-skipping mode when an inductor current zero crossing (LXA2 - GND) is detected.
32	26	DHA2	High-Side Gate-Driver Output for the Second Phase of Regulator A. DHA2 Output Voltage swings from V_{BSTA2} to V_{LXA2}. DHA2 is pulled low in shutdown.
33	27	LXA2	Inductor Connection for the Second Phase of Regulator A. LXA2 serves as the lower supply rail for the DHA2 high-side gate driver. LXA2 is also used as an input to the zero crossing comparator for Regulator A.

Dual-Output, 3-/2-/1-Phase + 2-/1-Phase Quick-PWM Controllers for VR12/IMVP7

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
34	28	BSTA2	Boost Flying Capacitor Connection for High-Side Gate Voltage for the Second Phase of Regulator A. Connect a ceramic capacitor between BSTA2 and LXA2. See the *Boost Capacitors* section.
35	29	IMAXA	Maximum Current Threshold for Regulator A. This multivalued logic input sets the valley current limit and compensates for inductor DCR. The maximum output current value in register 21h is determined by the number of phases times the maximum output current per phase set by IMAXA. If the voltage applied to IMAXA is not within the defined threshold, the MAX17411/MAX17511/MAX17511C/ MAX17511N/MAX17511T detect a fault and latch off. See Table 6 for more details.
36	30	IMAXB	Maximum Current Threshold for Regulator B. This multivalued logic input sets the valley current limit and compensates for inductor DCR. The maximum output current value in register 21h is determined by the number of phases times the maximum output current per phase set by IMAXB. If the voltage applied to IMAXB is not within the defined threshold, the MAX17411/MAX17511/MAX17511C/ MAX17511N/MAX17511T detect a fault and latch off. See Table 6 for more details.
37	31	DRVPWMA	Direct-Drive PWM Output for Controlling the External Third Phase Driver for Regulator A. DRVPWMA is three-stated in shutdown when the controller detects an output overvoltage fault condition on regulator A.
38	32	SR	Fast Slew-Rate Adjustment for Both Regulators. The SR setting determines the value stored in the Slew Rate Fast (24h) and Slew Rate Slow (25h) registers. The input uses a four-level voltage sense to determine the slew rate setting upon power-up and if NTC are used for the CSP_ signals. The SR values in the registers (24h and 25h) change accordingly.

SR THRESHOLD (V)	SR (min) (mV/µs)	NTC
0	10	Yes
1.5	20	Yes
3	20	No
V_{CC}	10	No

39	33	THERMA	Thermal-Sense Input for Regulator A. Connect THERMA to a resistor/thermistor-divider network between V_{CC} and THERMA to analog ground. The VR_HOT# is pulled low when the voltage at THERMA or THERMB drops below 0.5 x V_{CC}. If THERMA is held low at startup, REG A is forced in to non-zero V_{BOOT} mode with an output voltage of 1.05V (MAX17411/MAX17511/MAX17511T).
40	34	THERMB	Thermal-Sense Input for Regulator B. Connect THERMB to a resistor/thermistor-divider network between V_{CC} and THERMB to analog ground. The VR_HOT# is pulled low when the voltage at THERMA or THERMB drops below 0.5 x V_{CC}. If THERMB is held low at startup, REG B is forced in to non-zero V_{BOOT} mode with a output voltage of 1.05V (MAX17411/MAX17511/MAX17511T).
41	35	CSPAAVE	Positive Current-Sense Average Input for Regulator A. Connect CSPAAVE to the positive side of the differential output of external current-sense averaging network. The averaging is achieved by using a resistive summation and current-sense resistors, or by using a parallel DCR sense network with a single NTC thermistor for thermal compensation (see Figures 1, 2, and 3). The average current-sense input is used for the load-line and current monitor.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX17411	MAX17511/ MAX17511C/ MAX17511N/ MAX17511T		
42	36	CSPA1	Positive Current-Sense Input for the First Phase of Regulator A. Connect CSPA1 to the positive side of the current-sense resistor or the DCR sense filter capacitor of regulator A as shown in Figure 8. To *completely* disable Regulator A, connect CSPA1, CSPA2, and CSPA3 to V_{CC} and leave BSTA1, DHA1, LXA1, DLA1, CSPAAVE, and CSNA unconnected. Address 0 is also disabled from the SVID bus.
43	37	CSNA	Negative Current-Sense Input of Regulator A. Connect CSNA to the negative side of the current-sense element as shown in Figure 8. An internal 20Ω discharge MOSFET between CSNA and ground is enabled under an input UVLO or shutdown condition. A bypass capacitor between CSNA and GND in the range of 1nF to 0.1µF is recommended.
44	38	CSPA2	Positive Current-Sense Input for the Second Phase of Regulator A. Connect CSPA2 to the positive side of the current-sense resistor or the DCR sense filter capacitor of regulator A as shown in Figure 8. To *completely* disable Regulator A, connect CSPA1, CSPA2, and CSPA3 to V_{CC}. Address 0 is also disabled from the SVID bus. When Phase 2 is disabled, leave BSTA2, DHA2, LXA2, and DLA2 unconnected. If phase 2 is disabled, phase 3 must be disabled as well.
45	39	CSPA3	Positive Current-Sense Input for Third Phase of Regulator A. Connect CSPA3 to the positive side of the current-sense element of the third phase of regulator A as shown in Figure 8. Connect CSPA3 to V_{CC} and leave DRVPWMA unconnected to disable the third phase of Regulator A.
46	40	V_{CC}	Analog Supply Voltage. Connect to a filtered 4.5V to 5.5V source. Bypass V_{CC} to AGND with a 1µF or greater ceramic capacitor.
47	1	EN	Controller Enable Input. Pull EN high or connect EN to V_{CC} for normal operation. Connect to ground to put the controller into its 30µA (max) shutdown state. During soft-start, the controller slowly ramps the output voltage up to the boot voltage with a 2.5mV/µs (min) slew rate. During the transition from normal operation to shutdown, the output is discharged through a 20Ω internal CSN_ FET. Toggling EN resets the fault latches. EN cannot withstand the battery voltage.
48	—	TONA	Switching Frequency Adjustment Input for Regulator A. An external resistor between the input power source and TONA sets the switching period (per phase) for regulator A according to the following equation: $t_{SWA} = (R_{TONA} + 6.5k\Omega) \times 17.9pF$ where $f_{SWA} = 1/t_{SWA}$ is the nominal switching frequency. TONA is high-impedance in shutdown. If REG A is disabled, connect TONA to GND.
EP	—	PAD (AGND)	Exposed Pad. Connect EP to the ground plane with thermally enhanced vias.
—	EP	PAD (GND)	Exposed Pad. Connect EP to the ground plane with thermally enhanced vias. Power ground pads and analog ground pads are all internally connected to the exposed pad.