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EVALUATION KIT AVAILABLE

1-Phase Quick-PWM Intel IMVP-6.5/GMCH Controllers

MAX17528

General Description

The MAX17528 comprises 1-phase Quick-PWM™ step-down VID power-supply controllers for Intel notebook CPUs. The Quick-PWM control provides instantaneous response to fast-load current steps. Active voltage positioning reduces power dissipation and bulk output capacitance requirements and allows ideal positioning compensation for tantalum, polymer, or ceramic bulk output capacitors.

The MAX17528 is intended for two different notebook CPU/GPU core applications: either bucking down the battery directly to create the core voltage, or bucking down the +5V system supply. The single-stage conversion method allows these devices to directly step down high-voltage batteries for the highest possible efficiency. Alternatively, 2-stage conversion (stepping down the +5V system supply instead of the battery) at higher switching frequency provides the minimum possible physical size.

A slew-rate controller allows controlled transitions between VID codes. A thermistor-based temperature sensor provides programmable thermal protection. A current monitor provides an analog output current proportional to the processor load current.

The MAX17528 implements both the Intel IMVP-6.5 CPU core specifications ($\overline{CLKEN}$ pullup to 3.3V), as well as the Intel GMCH graphics core specifications ($\overline{CLKEN}$ = GND). The MAX17528 is available in a 32-pin, 5mm x 5mm TQFN package.

Applications

IMVP-6.5 Core Power Supply
Intel GMCH 2009

Intel Calpella Platforms

Graphics Core Power Supply

Voltage-Positioned Step-Down Converters

1-to-4 Lithium-Ion (Li+)-Cell Battery-to-CPU Core Supply Converters

Notebooks/Desktops/Servers

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Features

- **1-Phase Quick-PWM Controller**
- **±0.5% V_{OUT} Accuracy Over Line, Load, and Temperature**
- **7-Bit IMVP-6.5 DAC**
- **IMVP-6.5 and GMCH Compliant**
- **Active Voltage Positioning with Adjustable Gain**
- **Accurate Droop and Current Limit**
- **Remote Output and Ground Sense**
- **Adjustable Output-Voltage Slew Rate**
- **Power-Good Window Comparator**
- **Current Monitor**
- **Temperature Comparator**
- **Drives Large Synchronous Rectifier FETs**
- **2V to 26V Battery Input Range**
- **Adjustable Switching Frequency (600kHz max)**
- **Undervoltage and Thermal-Fault Protection**
- **Soft-Startup and Soft-Shutdown**
- **Internal Boost Diode**

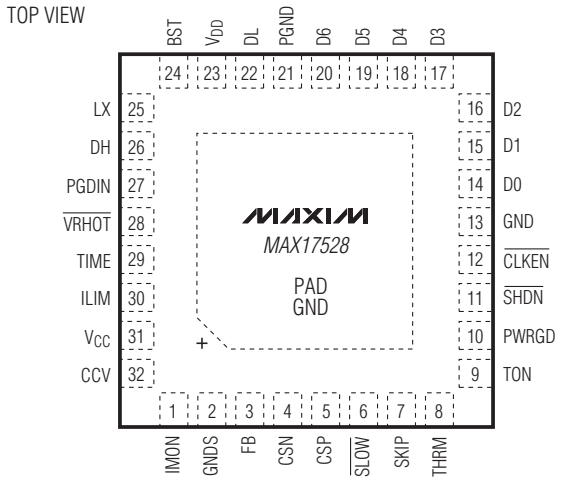
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17528GTJ+	-40°C to +105°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.

**EP = Exposed pad.*

Pin Configuration



THIN QFN
5mm x 5mm

1-Phase Quick-PWM Intel IMVP-6.5/GMCH Controllers

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{DD} to GND .....-0.3V to +6V
D0–D6 to GND.....-0.3V to +6V
CSP, CSN to GND .....-0.3V to +6V
ILIM, THRM, PGDIN, $\overline{VRHOT}$, PWRGD to GND .....-0.3V to +6V
$\overline{CLKEN}$ to GND.....-0.3V to +6V
SKIP, $\overline{SLOW}$ to GND.....-0.3V to +6V
CCV, FB, IMON, TIME to GND .....-0.3V to (V_{CC} + 0.3V)
$\overline{SHDN}$ to GND (Note 1).....-0.3V to +30V
TON to GND .....-0.3V to +30V
GNDS, PGND to GND .....-0.3V to +0.3V
DL to PGND.....-0.3V to (V_{DD} + 0.3V)
BST to GND .....-0.3V to +36V
LX to BST.....-6V to +0.3V
BST to V_{DD}.....-0.3V to +30V
DH to LX.....-0.3V to (V_{BST} + 0.3V)
Continuous Power Dissipation (32-pin, 5mm x 5mm TQFN)
Up to +70°C 1702mW
Derating above +70°C .....21.3mW/°C
Operating Temperature Range .....-40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: $\overline{SHDN}$ can be forced to 12V for the purpose of debugging prototype breadboards using the no-fault test mode, which disables fault protection.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ, $\overline{SHDN}$ = $\overline{SLOW}$ = ILIM = PGDIN = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input-Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
DC Output-Voltage Accuracy		Measured at FB with respect to GNDS; includes load-regulation error (Note 3)	DAC codes from 0.8125V to 1.5000V	-0.5		+0.5	%
			DAC codes from 0.3750V to 0.8000V	-7		+7	mV
			DAC codes from 0V to 0.3625V	-20		+20	
Boot Voltage	V_{BOOT}	IMVP-6.5 ($\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ)		1.094	1.100	1.106	V
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 26V			0.1		%
GNDS Input Range				-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$, -200mV ≤ V_{GNDS} ≤ +200mV		0.97	1.00	1.03	V/V
GNDS Input Bias Current	I_{GNDS}	T_A = +25°C		-2		+2	µA
TIME Voltage	V_{TIME}	V_{CC} = 4.5V to 5.5V, I_{TIME} = 28µA (R_{TIME} = 71.5kΩ)		1.985	2.000	2.015	V
TIME Slew-Rate Accuracy		R_{TIME} = 71.5kΩ (12.5mV/µs nominal)		-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)		-15		+15	
		Soft-start and soft-shutdown; R_{TIME} = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal)		-20		+20	
		$\overline{SLOW}$ = GND, R_{TIME} = 35.7kΩ (12.5mV/µs nominal) to 178kΩ (2.5mV/µs nominal)		-20		+20	

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ, $\overline{SHDN}$ = $\overline{SLOW}$ = ILIM = PGDIN = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
On-Time	t_{ON}	V_{IN} = 12V, V_{FB} = 1.2V (Note 4)	R_{TON} = 96.75kΩ	142	167	192	ns
			R_{TON} = 200kΩ	300	333	366	
			R_{TON} = 303.25kΩ	425	500	575	
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH (Note 4)			300	375	ns
TON Shutdown Input Current		$\overline{SHDN}$ = GND, V_{IN} = 26V, V_{CC} = V_{DD} = 0V or 5V, T_A = +25°C			0.01	1	µA
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, V_{SKIP} = 5V, FB forced above the regulation point			1.5	3	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, SKIP = GND, FB forced above the regulation point, T_A = +25°C			0.02	1	µA
Shutdown Supply Current (V_{CC})		Measured at V_{CC}, $\overline{SHDN}$ = GND			15	30	µA
Shutdown Supply Current (V_{DD})		Measured at V_{DD}, $\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
FAULT PROTECTION							
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to unloaded output voltage		-450	-400	-350	mV
Output Undervoltage Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold			10		µs
IMVP-6.5 $\overline{CLKEN}$ Startup Delay (Boot Time Period, $\overline{CLKEN}$ Pullup to 3.3V with 1.9kΩ)	t_{BOOT}	IMVP-6.5: $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ; measured from the time when FB reaches the boot target voltage (Note 3); the time needed for FB to reach this target voltage is based on the slew rate set by R_{TIME}		20	60	100	µs
PWRGD Startup Delay		IMVP-6.5: $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ; measured at startup from the time when $\overline{CLKEN}$ goes low		3	5	8	ms
		GMCH: $\overline{CLKEN}$ = GND; measured from the time when FB reaches the target voltage (Note 3); the time needed for FB to reach this target voltage is based on the slew rate set by R_{TIME}		3	5	8	
PWRGD and $\overline{CLKEN}$ (IMVP-6.5, $\overline{CLKEN}$ Pullup to 3.3V with 1.9kΩ) Threshold		Measured at FB with respect to unloaded output voltage, 15mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350	-300	-250	mV
			Upper threshold, rising edge (overvoltage)	+150	+200	+250	
PWRGD and $\overline{CLKEN}$ (IMVP-6.5, $\overline{CLKEN}$ Pullup to 3.3V with 1.9kΩ) Transition Blanking Time	t_{BLANK}	Measured from the time when FB reaches the target voltage (Note 3) based on the slew rate set by R_{TIME}			20		µs
PWRGD and $\overline{CLKEN}$ (IMVP-6.5, $\overline{CLKEN}$ Pullup to 3.3V with 1.9kΩ) Delay		FB forced 25mV outside the PWRGD trip thresholds			10		µs

1-Phase Quick-PWM Intel IMVP-6.5/GMCH Controllers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ, $\overline{SHDN}$ = $\overline{SLOW}$ = ILIM = PGDIN = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IMVP-6.5 $\overline{CLKEN}$ Output Low Voltage		IMVP-6.5: $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ; I_{SINK} = 3mA			0.4	V
IMVP-6.5 $\overline{CLKEN}$ High Leakage Current		IMVP-6.5: V_{PGDIN} = 5V, $V_{\overline{CLKEN}}$ = 3.3V		2	4	µA
IMVP-6.5 $\overline{CLKEN}$ Shutdown Leakage Current		IMVP-6.5: $V_{\overline{SHDN}}$ = GND, $V_{\overline{CLKEN}}$ = 3.3V		0.01	1	µA
PWRGD Output Low Voltage		I_{SINK} = 3mA			0.4	V
PWRGD Leakage Current		High state, PWRGD forced to 5V, T_A = +25°C			1	µA
V_{CC} Undervoltage Lockout Threshold	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level	4.05	4.27	4.48	V
CSN Discharge Resistance in UVLO and Shutdown		$\overline{SHDN}$ = GND and drivers disabled (not switching)		8		Ω
THERMAL PROTECTION						
$\overline{VRHOT}$ Trip Threshold		Measured at THRM with respect to V_{CC}; falling edge; typical hysteresis = 100mV	29.2	30	30.8	%
$\overline{VRHOT}$ Delay	$t_{\overline{VRHOT}}$	THRM forced 25mV below the $\overline{VRHOT}$ trip threshold; falling edge		10		µs
$\overline{VRHOT}$ Output On-Resistance	$R_{\overline{VRHOT}}$	Low state		2	8	Ω
$\overline{VRHOT}$ Leakage Current	$I_{\overline{VRHOT}}$	High state, $\overline{VRHOT}$ forced to 5V, T_A = +25°C			1	µA
THRM Input Leakage	I_{THRM}	V_{THRM} = 0V to 5V, T_A = +25°C	-100		+100	nA
Thermal-Shutdown Threshold	$T_{\overline{SHDN}}$	Typical hysteresis = 15°C		+160		°C
VALLEY CURRENT LIMIT AND DROOP						
Current-Limit Threshold Voltage (Positive Adjustable)	V_{LIMIT}	V_{CSP} - V_{CSN}; V_{TIME} - V_{ILIM} = 100mV	7	10	13	mV
		V_{TIME} - V_{ILIM} = 500mV	45	50	55	
Current-Limit Threshold Voltage (Positive Default) Preset		V_{CSP} - V_{CSN}, ILIM = V_{CC}	20	22.5	25	mV
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	V_{CSP} - V_{CSN}, nominally -125% of V_{LIMIT}	-4		+4	mV
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZERO}	V_{PGND} - V_{LX}, SKIP = V_{CC}		1		mV
CSP, CSN Common-Mode Input Range			0		2	V
CSP, CSN Input Current		T_A = +25°C	-0.2		+0.2	µA
ILIM Input Current		T_A = +25°C	-100		+100	nA
DC Droop Amplifier (GMD) Offset		(V_{CSP} - V_{CSN}) at I_{FB} = 0	-0.75		+0.75	mV
DC Droop Amplifier (GMD) Transconductance		$\Delta I_{FB}/\Delta(V_{CSP} - V_{CSN})$; V_{FB} = V_{CSN} = 0.45V to 2.0V, and (V_{CSP} - V_{CSN}) = -15.0mV to +15.0mV	592	600	608	µS

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ, $\overline{SHDN}$ = $\overline{SLOW}$ = ILIM = PGDIN = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = 0°C to +85°C**, unless otherwise specified. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVERS							
DH Gate-Driver On-Resistance	$R_{ON(DH)}$	BST - LX forced to 5V	High state (pullup)		0.9	2.5	
			Low state (pulldown)		0.7	2.0	
DL Gate-Driver On-Resistance	$R_{ON(DL)}$	High state (pullup)			0.7	2.0	
		Low state (pulldown)			0.25	0.7	
DH Gate-Driver Source Current	$I_{DH(SOURCE)}$	DH forced to 2.5V, BST - LX forced to 5V			2.2		A
DH Gate-Driver Sink Current	$I_{DH(SINK)}$	DH forced to 2.5V, BST - LX forced to 5V			2.7		A
DL Gate-Driver Source Current	$I_{DL(SOURCE)}$	DL forced to 2.5V			2.7		A
DL Gate-Driver Sink Current	$I_{DL(SINK)}$	DL forced to 2.5V			8		A
Driver Propagation Delay		DH low to DL high			20		ns
		DL low to DH high			20		
DL Transition Time		DL falling, C_{DL} = 3nF			20		ns
		DL rising, C_{DL} = 3nF			20		
DH Transition Time		DH falling, C_{DH} = 3nF			20		ns
		DH rising, C_{DH} = 3nF			20		
Internal BST Switch On-Resistance	R_{BST}	I_{BST} = 10mA, V_{DD} = 5V (Note 6)			10	20	
CURRENT MONITOR							
Current-Monitor Transconductance	$G_{m(IMON)}$	$\Delta I_{IMON}/\Delta(V_{CSP} - V_{CSN})$, V_{CSN} = 0.45V to 2.0V		4.9	5.0	5.1	mS
Current-Monitor Offset Referred to V(CSP, CSN)		I_{IMON} = 0		-1.0		+1.0	mV
IMON Clamp Voltage	V_{IMON}	I_{IMON} = -1mA		1.05	1.10	1.15	V
LOGIC AND I/O							
Logic-Input High Voltage	V_{IH}	PGDIN		2.3			V
Logic-Input Low Voltage	V_{IL}	PGDIN				1.0	V
Low-Voltage Logic-Input High Voltage	V_{IHLV}	$\overline{SHDN}$, SKIP, $\overline{SLOW}$, D0–D6		0.67			V
Low-Voltage Logic-Input Low Voltage	V_{ILLV}	$\overline{SHDN}$, SKIP, $\overline{SLOW}$, D0–D6				0.33	V
Logic-Input Current		PGDIN, $\overline{SHDN}$, SKIP, $\overline{SLOW}$, D0–D6 = 0 or 5V, T_A = +25°C		-1		+1	µA
$\overline{CLKEN}$ Logic-Input High Voltage for IMVP-6.5 Startup				2.3			V
$\overline{CLKEN}$ Logic-Input Low Voltage for GMCH						1.0	V

1-Phase Quick-PWM Intel IMVP-6.5/GMCH Controllers

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ, $\overline{SHDN}$ = $\overline{SLOW}$ = ILIM = PGDIN = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = -40°C to +105°C**, unless otherwise specified.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PWM CONTROLLER						
Input-Voltage Range		V_{CC}, V_{DD}		4.5	5.5	V
DC Output-Voltage Accuracy		Measured at FB with respect to GNDS; includes load-regulation error (Note 3)	DAC codes from 0.8125V to 1.5000V	-0.75	+0.75	%
			DAC codes from 0.3750V to 0.8000V	-10	+10	mV
			DAC codes from 0V to 0.3625V	-25	+25	
Boot Voltage	V_{BOOT}	IMVP-6.5 ($\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ)		1.085	1.115	V
GNDS Input Range				-200	+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$, -200mV ≤ V_{GNDS} ≤ +200mV		0.95	1.05	V/V
TIME Voltage	V_{TIME}	V_{CC} = 4.5V to 5.5V, I_{TIME} = 28µA (R_{TIME} = 71.5kΩ)		1.98	2.02	V
TIME Slew-Rate Accuracy		R_{TIME} = 71.5kΩ (12.5mV/µs nominal)		-10	+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)		-15	+15	
		Soft-start and soft-shutdown; R_{TIME} = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal)		-20	+20	
		$\overline{SLOW}$ = GND, R_{TIME} = 35.7kΩ (12.5mV/µs nominal) to 178kΩ (2.5mV/µs nominal)		-20	+20	
On-Time	t_{ON}	V_{IN} = 12V, V_{FB} = 1.2V (Note 4)	R_{TON} = 96.75kΩ	142	192	ns
			R_{TON} = 200kΩ	300	366	
			R_{TON} = 303.25kΩ	425	575	
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH (Note 4)			400	ns
BIAS CURRENTS						
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, V_{SKIP} = 5V, FB forced above the regulation point			3	mA
FAULT PROTECTION						
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to unloaded output voltage		-460	-340	mV
IMVP-6.5 $\overline{CLKEN}$ Startup Delay (Boot Time Period, $\overline{CLKEN}$ Pullup to 3.3V with 1.9kΩ)	t_{BOOT}	IMVP-6.5, $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ; measured from the time when FB reaches the boot target voltage (Note 3); the time needed for FB to reach this target voltage is based on the slew rate set by R_{TIME}		20	100	µs

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ, $\overline{SHDN}$ = $\overline{SLOW}$ = ILIM = PGDIN = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = -40°C to +105°C**, unless otherwise specified.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
PWRGD Startup Delay		IMVP-6.5, $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ; measured at startup from the time when $\overline{CLKEN}$ goes low		3	8	ms
		GMCH, $\overline{CLKEN}$ = GND; measured from the time when FB reaches the target voltage (Note 3); the time needed for FB to reach this target voltage is based on the slew rate set by R_{TIME}		3	8	µs
PWRGD and $\overline{CLKEN}$ (IMVP-6.5, $\overline{CLKEN}$ Pullup to 3.3V with 1.9kΩ) Threshold		Measured at FB with respect to unloaded output voltage, 15mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-360	-240	mV
			Upper threshold, rising edge (overvoltage)	+140	+260	
IMVP-6.5 $\overline{CLKEN}$ Output Low Voltage		IMVP-6.5: $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ, I_{SINK} = 3mA			0.4	V
IMVP-6.5 $\overline{CLKEN}$ High Leakage Current		IMVP-6.5 = PGDIN = 5V, $V_{\overline{CLKEN}}$ = 3.3V			4	µA
PWRGD Output Low Voltage		I_{SINK} = 3mA			0.4	V
V_{CC} Undervoltage Lockout (UVLO) Threshold	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level		4.0	4.5	V
THERMAL PROTECTION						
$\overline{VRHOT}$ Trip Threshold		Measured at THRM with respect to V_{CC}; falling edge; typical hysteresis = 100mV		29	31	%
$\overline{VRHOT}$ Output On-Resistance	$R_{\overline{VRHOT}}$	Low state			8	Ω
VALLEY CURRENT LIMIT AND DROOP						
Current-Limit Threshold Voltage (Positive Adjustable)	V_{LIMIT}	V_{CSP} - V_{CSN}	V_{TIME} - V_{ILIM} = 100mV	7	13	mV
			V_{TIME} - V_{ILIM} = 500mV	45	55	
Current-Limit Threshold Voltage (Positive Default Preset)		V_{CSP} - V_{CSN}, ILIM = V_{CC}		20	25	mV
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	V_{CSP} - V_{CSN}, nominally -125% of V_{LIMIT}		-5	+5	mV
CSP, CSN Common-Mode Input Range				0	2	V
DC Droop Amplifier (GMD) Offset		(V_{CSP} - V_{CSN}) at I_{FB} = 0		-1.0	+1.0	mV
DC Droop Amplifier (GMD) Transconductance		$\Delta I_{FB}/\Delta(V_{CSP} - V_{CSN})$; FB = V_{CSN} = 0.45V to 2.0V, and (V_{CSP} - V_{CSN}) = -15.0mV to +15.0mV		588	612	µS

1-Phase Quick-PWM Intel IMVP-6.5/GMCH Controllers

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 12V, V_{DD} = V_{CC} = 5V, $\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ, $\overline{SHDN}$ = $\overline{SLOW}$ = ILIM = PGDIN = V_{CC}, SKIP = GNDS = PGND = GND, V_{FB} = V_{CSP} = V_{CSN} = 1.200V, D0–D6 set for 1.20V (D0–D6 = 0001100). **T_A = -40°C to +105°C**, unless otherwise specified.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GATE DRIVERS							
DH Gate-Driver On-Resistance	$R_{ON(DH)}$	BST - LX forced to 5V	High state (pullup)			2.5	
			Low state (pulldown)			2.0	
DL Gate-Driver On-Resistance	$R_{ON(DL)}$		High state (pullup)			2.0	
			Low state (pulldown)			0.7	
Internal BST Switch On-Resistance	R_{BST}	I_{BST} = 10mA, V_{DD} = 5V				20	
CURRENT MONITOR							
Current-Monitor Transconductance	$G_{m(IMON)}$	$\Delta I_{IMON}/\Delta(V_{CSP} - V_{CSN})$, V_{CSN} = 0.45V to 2.0V		4.9		5.1	mS
Current-Monitor Offset Referred to V(CSP, CSN)		I_{IMON} = 0		-1.5		+1.5	mV
I_{MON} Clamp Voltage	V_{IMON}	I_{IMON} = -1mA		1.05		1.15	V
LOGIC AND I/O							
Logic-Input High Voltage	V_{IH}	PGDIN		2.3			V
Logic-Input Low Voltage	V_{IL}	PGDIN				1.0	V
Low-Voltage Logic-Input High Voltage	V_{IHLV}	$\overline{SHDN}$, SKIP, $\overline{SLOW}$, D0–D6		0.67			V
Low-Voltage Logic-Input Low Voltage	V_{ILLV}	$\overline{SHDN}$, SKIP, $\overline{SLOW}$, D0–D6				0.33	V
CLKEN Logic-Input High Voltage for IMVP-6.5 Startup				2.3			V
CLKEN Logic-Input Low Voltage for GMCH						1.0	V

Note 2: Limits are 100% production tested at T_A = +25°C. Maximum and minimum limits over temperature are guaranteed by design and characterization.

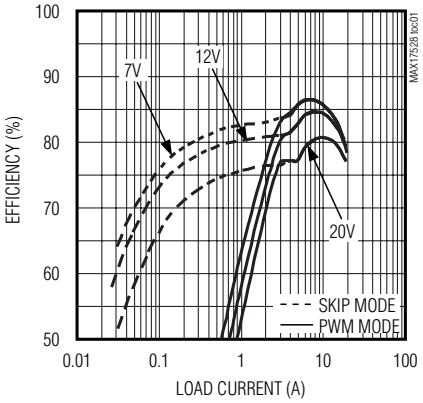
Note 3: The equation for the target voltage V_{TARGET} is:
V_{TARGET} = the slew-rate-controlled version of V_{DAC}, where V_{DAC} = 0V for shutdown, V_{DAC} = V_{BOOT} (IMVP-6.5) or V_{VID} (GMCH) during startup, and V_{DAC} = V_{VID} otherwise (the V_{VID} voltages for all possible VID codes are given in Table 2).
In pulse-skipping mode, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

Note 4: On-time and minimum off-time specifications are measured from 50% to 50% at the DH pin, with LX forced to 0V, BST forced to 5V, and a 500pF capacitor from DH to LX to simulate external MOSFET gate capacitance. Actual in-circuit times can be different due to MOSFET switching speeds.

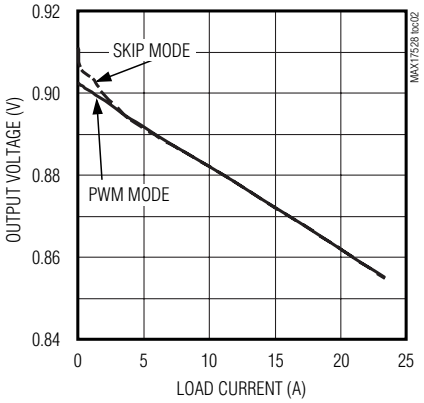
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted. Circuit of Figure 1.)

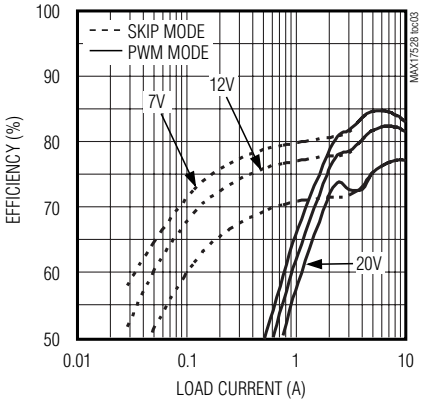
0.9V OUTPUT EFFICIENCY vs. LOAD CURRENT



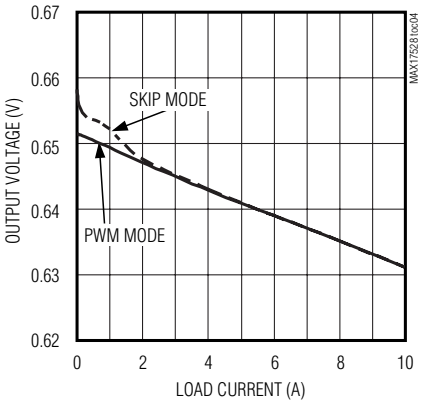
0.9V OUTPUT VOLTAGE vs. LOAD CURRENT



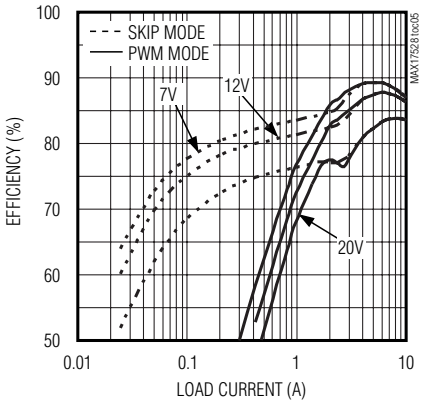
0.65V OUTPUT EFFICIENCY vs. LOAD CURRENT



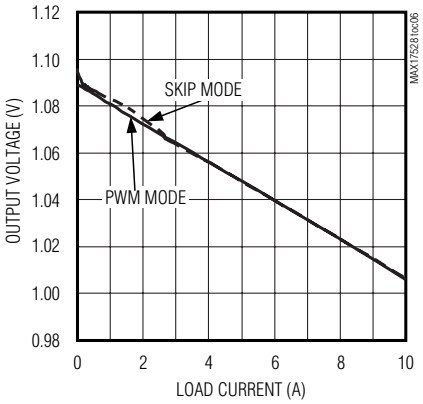
0.65V OUTPUT VOLTAGE vs. LOAD CURRENT



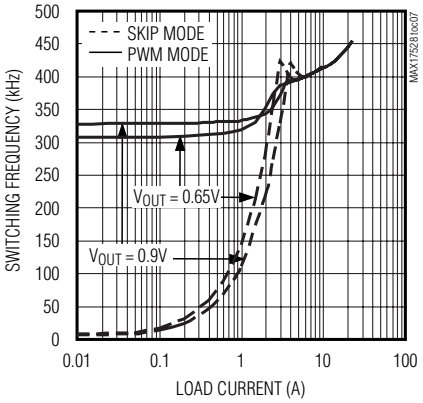
OUTPUT EFFICIENCY vs. LOAD CURRENT



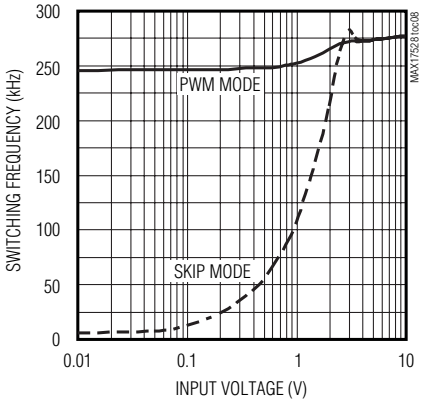
OUTPUT VOLTAGE vs. LOAD CURRENT



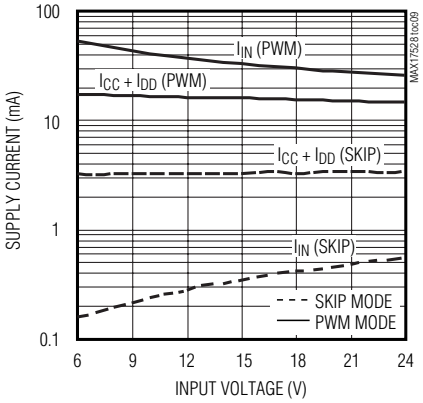
SWITCHING FREQUENCY vs. LOAD CURRENT



SWITCHING FREQUENCY vs. LOAD CURRENT



V_{OUT} = 0.9V NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE

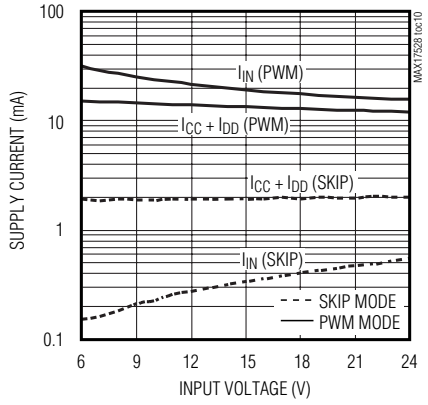


1-Phase Quick-PWM Intel IMVP-6.5/GMCH Controllers

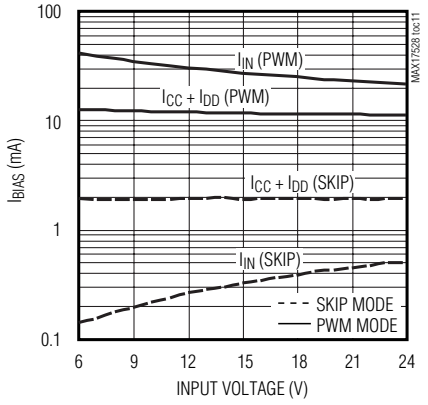
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted. Circuit of Figure 1.)

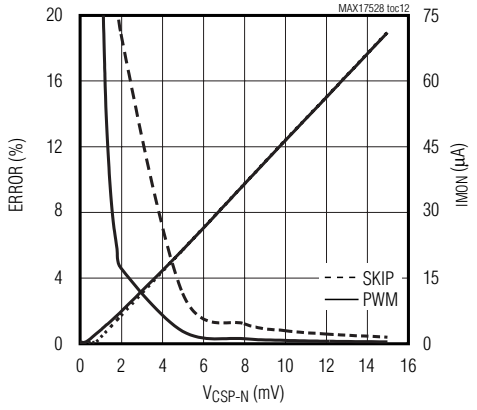
V_{OUT} = 0.65V NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



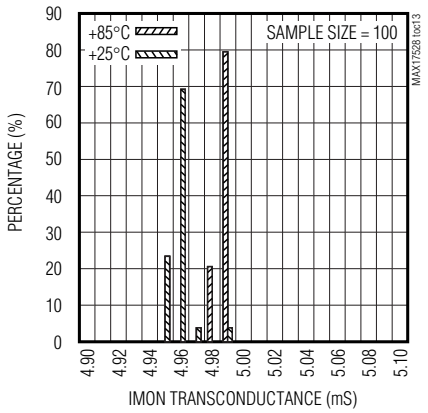
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE



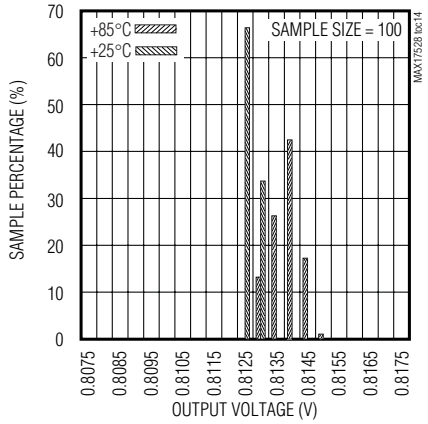
IMON CURRENT AND ERROR vs. LOAD CURRENT



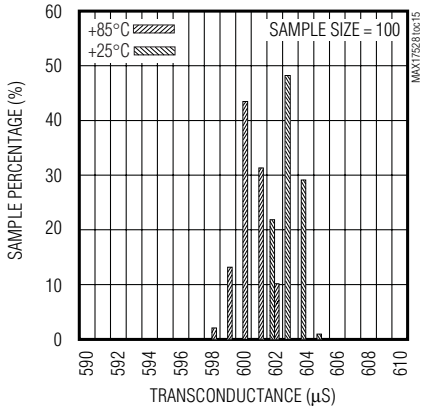
IMON TRANSCONDUCTANCE DISTRIBUTION



0.8125V OUTPUT VOLTAGE DISTRIBUTION



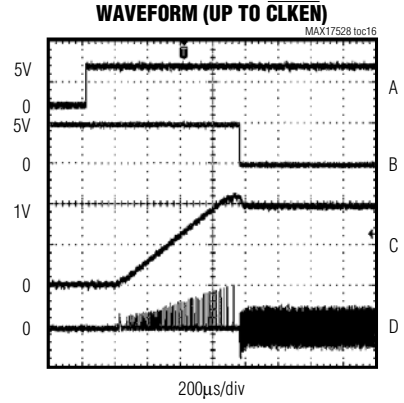
G_m (FB) TRANSCONDUCTANCE DISTRIBUTION



Typical Operating Characteristics (continued)

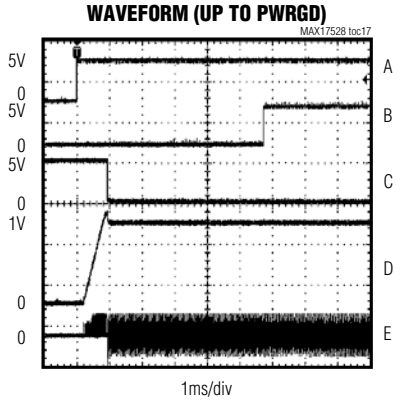
(T_A = +25°C, unless otherwise noted. Circuit of Figure 1.)

IMVP-6.5 SOFT-START WAVEFORM (UP TO $\overline{CLKEN}$)



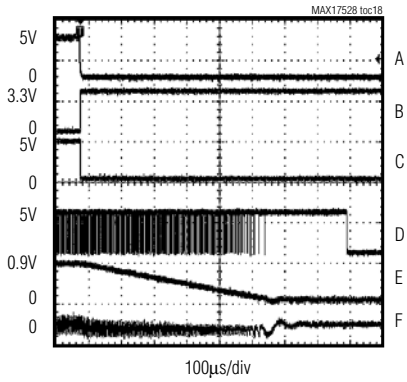
A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 5V/div
C. V_{OUT}, 500mV/div
D. INDUCTOR CURRENT, 10A/div

IMVP-6.5 SOFT-START WAVEFORM (UP TO PWRGD)



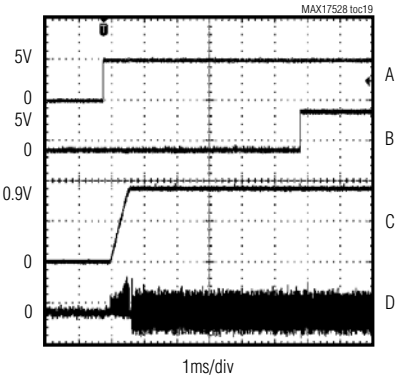
A. $\overline{SHDN}$, 5V/div
B. PWRGD, 5V/div
C. $\overline{CLKEN}$, 5V/div
D. V_{OUT}, 500mV/div
E. INDUCTOR CURRENT, 10A/div

IMVP-6.5 SHUTDOWN WAVEFORM



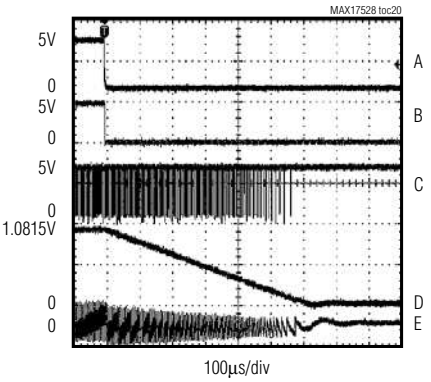
A. $\overline{SHDN}$, 5V/div
B. $\overline{CLKEN}$, 3.3V/div
C. PWRGD, 5V/div
D. V_{OUT}, 1V/div
E. DL, 5V/div
F. INDUCTOR CURRENT, 5A/div

GMCH SOFT-START WAVEFORM



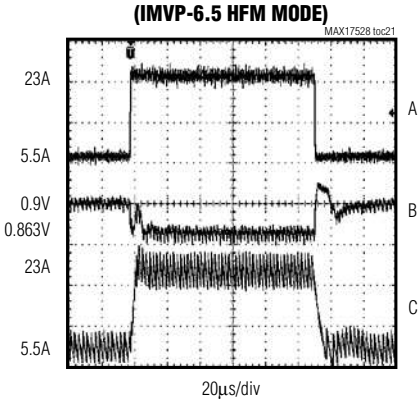
A. $\overline{SHDN}$, 5V/div
B. PWRGD, 5V/div
C. V_{OUT}, 500mV/div
D. INDUCTOR CURRENT, 10A/div

GMCH SHUTDOWN WAVEFORM



A. $\overline{SHDN}$, 5V/div
B. PWRGD, 5V/div
C. DL, 5V/div
D. V_{OUT}, 500mV/div
E. INDUCTOR CURRENT, 5A/div

LOAD-TRANSIENT RESPONSE (IMVP-6.5 HFM MODE)



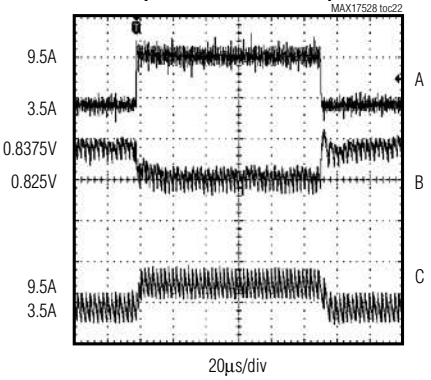
A. I_{OUT} = 5.5A TO 23A, 10A/div
B. V_{OUT}, 50mV/div
C. INDUCTOR CURRENT, 10A/div

1-Phase Quick-PWM Intel IMVP-6.5/GMCH Controllers

Typical Operating Characteristics (continued)

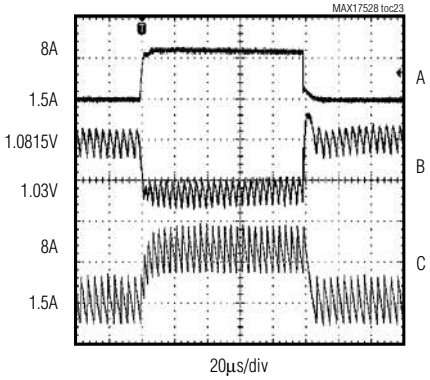
(T_A = +25°C, unless otherwise noted. Circuit of Figure 1.)

LOAD-TRANSIENT RESPONSE (IMVP-6.5 LFM MODE)



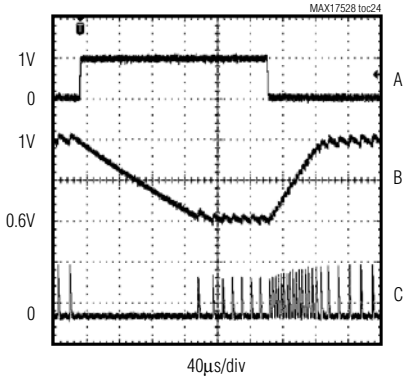
A. I_{OUT} = 3.5A TO 9.5A, 5A/div
B. V_{OUT}, 20mV/div
C. INDUCTOR CURRENT, 10A/div

LOAD-TRANSIENT RESPONSE



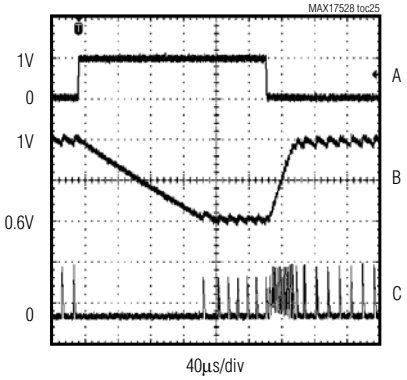
A. I_{OUT} = 1.5A TO 8A, 5A/div
B. V_{OUT}, 50mV/div
C. INDUCTOR CURRENT, 5A/div

DPRSLPVR = HIGH, $\overline{SLOW}$ = LOW, VID5 TRANSITION



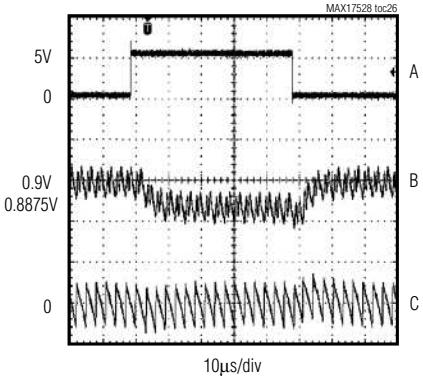
A. VID5, 1V/div
B. V_{OUT}, 200mV/div
I_{OUT} = 1A
C. INDUCTOR CURRENT, 10A/div

DPRSLPVR = HIGH, $\overline{SLOW}$ = HIGH, VID5 TRANSITION



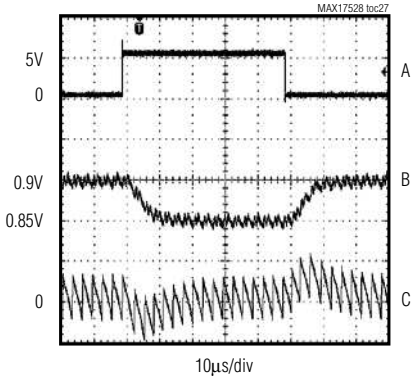
A. VID5, 1V/div
B. V_{OUT}, 200mV/div
I_{OUT} = 1A
C. INDUCTOR CURRENT, 10A/div

D0 12.5mV DYNAMIC VID CODE CHANGE



A. D0, 5V/div
B. V_{OUT}, 20mV/div
C. INDUCTOR CURRENT, 2A/div

D2 50mV DYNAMIC VID CODE CHANGE

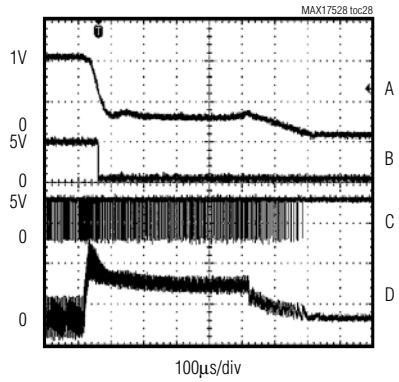


A. D2, 5V/div
B. V_{OUT}, 50mV/div
C. INDUCTOR CURRENT, 2A/div

Typical Operating Characteristics (continued)

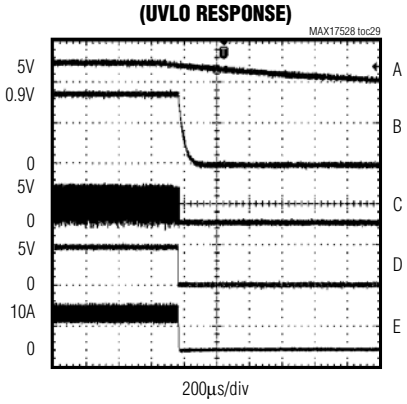
(T_A = +25°C, unless otherwise noted. Circuit of Figure 1.)

OUTPUT OVERLOAD WAVEFORM



A. V_{OUT}, 500mV/div
B. PGOOD, 5V/div
C. DL, 5V/div
D. INDUCTOR CURRENT, 10A/div

BIAS SUPPLY REMOVAL (UVLO RESPONSE)



A. 5V BIAS SUPPLY, 5V/div
B. V_{OUT}, 500mV/div
C. DL, 5V/div
D. PGOOD, 5V/div
E. INDUCTOR CURRENT, 10A/div

Pin Description

PIN	NAME	FUNCTION
1	IMON	Current Monitor Output. The MAX17528 IMON output sources a current that is directly proportional to the current-sense voltage as defined by: $I_{IMON} = G_{m(IMON)} \times (V_{CSP} - V_{CSN})$ where $G_{m(IMON)}$ = 5mS (typ). The IMON current is unidirectional (sources current out of IMON only) for positive current-sense values. For negative current-sense voltages, the IMON current is zero. Connect an external resistor between IMON and VSS_SENSE to create the desired IMON gain based on the following equation: $R_{IMON} = 0.999V/(IMAX \times R_{SENSE} \times G_{m(IMON)})$ where IMAX is defined in the *Current Monitor (IMON)* section of the Intel IMVP-6.5 specification and based on discrete increments (20A, 30A, 40A, etc.,), R_{SENSE} is the typical effective value of the current-sense element (sense resistor or inductor DCR) that is used to provide the current-sense voltage, and $G_{m(IMON)}$ is the typical transconductance amplifier gain as defined in the *Electrical Characteristics* table. The IMON voltage is internally clamped to a maximum of 1.1V (typ). The transconductance amplifier and voltage clamp are internally compensated, so IMON cannot directly drive large capacitance values. To filter the IMON signal, use an RC filter as shown in Figure 1. IMON is pulled to ground when the MAX17528 is in shutdown.
2	GNDS	Remote Ground-Sense Input. Connect directly to the CPU or GMCH V_{SS} sense pin (ground sense) or directly to the ground connection of the load. GNDS internally connects to a transconductance amplifier that adjusts the feedback voltage, compensating for voltage drops between the regulator's ground and the processor's ground.
3	FB	Output of the Voltage-Positioning Transconductance Amplifier. Connect a resistor, R_{FB}, between FB and the positive side of the feedback remote sense to set the steady-state droop based on the voltage-positioning gain requirement. $R_{FB} = R_{DROOP}/(R_{SENSE} \times GMD)$ where R_{DROOP} is the desired voltage-positioning slope, GMD = 600µS typ and R_{SENSE} is the value of the current-sense resistor that is used to provide the (CSP, CSN), current-sense voltage. If lossless sensing is used, $R_{SENSE} = R_L$. In this case, consider using a thermistor-resistor network to minimize the temperature dependence of the voltage-positioning slope. Droop can be disabled by shorting FB to the positive remote-sense point, but doing so increases the minimum ESR requirement of the output capacitance for stability, and FB might therefore need to be driven by a carefully designed feed-forward network. FB is high impedance in shutdown.
4	CSN	Negative Inductor Current-Sense Input. Connect CSN to the negative terminal of the inductor current-sensing resistor or directly to the negative terminal of the inductor if the lossless DCR sensing method is used (see Figure 4). Under V_{CC} UVLO conditions and after soft-shutdown is completed, CSN is internally pulled to GND through a 10Ω FET to discharge the output.
5	CSP	Positive Inductor Current-Sense Input. Connect CSP to the positive terminal of the inductor current-sensing resistor or directly to the positive terminal of the filtering capacitor used when the lossless DCR sensing method is used (see Figure 4).
6	$\overline{SLOW}$	Active-Low Slew-Rate Select Input. This 1.0V logic input signal selects between the nominal and slow (half of nominal rate) slew rates. When $\overline{SLOW}$ is forced high, the selected nominal slew rate is set by the time resistance. When $\overline{SLOW}$ is forced low, the slew rate is reduced to half of the nominal slew rate. For IMVP-6.5 applications ($\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ), the fast slew rate is not needed. Connect $\overline{SLOW}$ to GND. For GMCH 2009 applications ($\overline{CLKEN}$ = GND), connect to the system GFXDPRSLPVR signal.

Pin Description (continued)

PIN	NAME	FUNCTION
7	SKIP	Pulse-Skipping Control Input. This 1.0V logic input signal indicates power usage and sets the operating mode of the MAX17528. When SKIP is forced high, the controller is immediately set to automatic pulse-skipping mode. The controller returns to forced-PWM mode when SKIP is forced low and the output is in regulation. The PWRGD upper threshold is blanked during any downward output-voltage transition that happens when the controller is in skip mode, and stays blanked until the transition-related PWRGD blanking period is complete and the output reaches regulation. IMVP-6.5: The MAX17528 is in skip mode during startup and while in boot mode, but is in forced-PWM mode during the transition from boot mode to VID mode plus 20µs, and during soft-shutdown, irrespective of the skip logic level. Connect to the system DPRSLPVR signal. GMCH 2009: The MAX17528 is in skip mode during startup, while in standby mode, and while exiting standby mode, but is in forced-PWM mode during soft-shutdown, and while entering standby mode, irrespective of the skip logic level. Connect to the system GFXDPRSLPVR signal.
8	THRM	Comparator Input for Thermal Protection. THRM connects to the positive input of an internal comparator. The comparator's negative input connects to an internal resistive voltage-divider that accurately sets the THRM threshold to 30% of the V_{CC} voltage. Connect the output of a resistor and thermistor-divider (between V_{CC} and GND) to THRM with the values selected so the voltage at THRM falls below 30% of V_{CC} (1.5V when V_{CC} = 5V) at the desired high temperature.
9	TON	Switching Frequency Setting Input. An external resistor between the input power source and this pin sets the switching period ($t_{SW} = 1/f_{SW}$) according to the following equation: $t_{SW} = 16.3pF \times (R_{TON} + 6.5k\Omega)$ TON becomes high impedance in shutdown to reduce the input quiescent current. If the TON current is less than 10µA, the MAX17528 disables the controller, sets the TON open fault latch, and pulls DL and DH low.
10	PWRGD	Open-Drain Power-Good Output. PWRGD is high impedance after output-voltage transitions (except during power-up and power-down) if FB is in regulation. During startup, PWRGD is held low. IMVP-6.5: PWRGD continues to be low while the output is at the boot voltage, and stays low until 5ms (typ) after $\overline{CLKEN}$ goes low. GMCH 2009: PWRGD starts monitoring the FB voltage 5ms (typ) after startup (from shutdown or standby mode) is complete. PWRGD is also held low while in standby mode, and while entering and exiting standby mode. PWRGD is forced low during soft-shutdown and while in shutdown. PWRGD is forced high impedance whenever the slew-rate controller is active (output-voltage transitions), and continues to be forced high impedance for an additional 20µs after the transition is completed. The PWRGD upper threshold is blanked during any downward output-voltage transition that happens when the MAX17528 is in skip mode, and stays blanked until the transition-related PWRGD blanking period is complete and the output reaches regulation. A pullup resistor on PWRGD causes additional finite shutdown current.
11	$\overline{SHDN}$	Active-Low Shutdown Control Input. Connect to V_{CC} for normal operation. Connect to ground to put the controller into the low-power 1µA (max) shutdown state. During startup, the controller ramps up the output voltage at 1/8 the slew rate set by the TIME resistor to the target voltage defined by the application circuit: For IMVP-6.5 ($\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ), the startup target is the 1.1V boot voltage. For GMCH 2009 ($\overline{CLKEN}$ = GND), the startup target is the voltage set by the VID inputs. During the shutdown transition, the MAX17528 softly ramps down the output voltage at 1/8 the slew rate set by the TIME resistor. Forcing $\overline{SHDN}$ to 11V~13V disables UVP, thermal shutdown, and clears the fault latches.

1-Phase Quick-PWM Intel IMVP-6.5/GMCH Controllers

Pin Description (continued)

PIN	NAME	FUNCTION
12	$\overline{\text{CLKEN}}$	Dual-Function GMCH/IMVP-6.5 Select Input and Active-Low IMVP-6.5 CPU Clock Enable Open-Drain Output. Connect to system 3.3V supply through pullup resistors for proper IMVP-6.5 operation. $\overline{\text{CLKEN}}$ voltage has to be higher than 2.3V before $\overline{\text{SHDN}}$ is pulled high. Connect to GND to select the Intel GMCH feature set. This active-low logic output indicates when the feedback voltage is in regulation. The MAX17528 forces $\overline{\text{CLKEN}}$ low during dynamic VID transitions and for an additional 20µs after the VID transition is completed. $\overline{\text{CLKEN}}$ is the inverse of PWRGD, except for the 5ms PWRGD startup delay period after $\overline{\text{CLKEN}}$ is pulled low. See the startup timing diagram (Figure 9). The $\overline{\text{CLKEN}}$ upper threshold is blanked during any downward output-voltage transition that happens when the MAX17528 are in skip mode, and stays blanked until the transition-related PWRGD blanking period is complete and the output reaches regulation.
13	GND	Analog Ground
14–20	D0–D6	Low-Voltage (1.0V Logic) VID DAC Code Inputs. The D0–D6 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. The output voltage is set by the VID code indicated by the logic-level voltages on D0–D6 (see Table 2). The 1111111 code corresponds to standby mode. When this code is detected, the MAX17528 enters standby mode while in forced-PWM mode, and slews to 0V at 1/8 the slew rate set by the TIME resistor. After slewing to 0V, the IC enters skip mode (DH and DL low). If D6–D0 is changed from 1111111 to a different code, the MAX17528 exits standby mode (while in skip mode) and slews the output voltage to the target voltage set by the VID code at 1x the slew rate set by the TIME resistor. Note that the standby supply current consumed by the MAX17528 is the same as its quiescent supply current, because no analog blocks are turned off. This is necessary because of the fast wake-up requirement.
21	PGND	Power Ground. Ground connection for the DL driver. Also used as an input to the MAX17528's zero-crossing comparator.
22	DL	Low-Side Gate-Driver Output. DL swings from PGND to V_{DD}. DL is forced low after shutdown. DL is forced low in skip mode after detecting an inductor current zero-crossing.
23	V_{DD}	Supply Voltage Input for the DL Driver. V_{DD} is also the supply voltage used to internally recharge the BST flying capacitor during the time DL is high. Connect V_{DD} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD} to PGND with a 1µF or greater ceramic capacitor.
24	BST	Boost Flying Capacitor Connection. BST provides the upper supply rail for the DH high-side gate driver. An internal switch between V_{DD} and BST charges the flying capacitor while the low-side MOSFET is on (DL pulled high and LX pulled to ground).
25	LX	Inductor Connection. LX is the internal lower supply rail for the DH high-side gate driver. Also used as an input to the MAX17528's zero-crossing comparator.
26	DH	High-Side Gate-Driver Output. DH swings from LX to BST. The controller pulls DH low in shutdown.
27	PGDIN	IMVP-6.5 Power-Good Logic Input. PGDIN indicates the power status of other system rails used to power the chipset and CPU V_{CCP} supplies. For the IMVP-6.5 ($\overline{\text{CLKEN}}$ pullup to 3.3V with 1.9kΩ), the MAX17528 powers up and remains at the boot voltage (V_{BOOT}) as long as PGDIN remains low. When PGDIN is forced high, the MAX17528 transitions the output to the voltage set by the VID code, and $\overline{\text{CLKEN}}$ is allowed to go low. If PGDIN is pulled low at any time, the MAX17528 immediately forces $\overline{\text{CLKEN}}$ high and PWRGD low and sets the output to the boot voltage. The output remains at the boot voltage until the system either disables the controller or until PGDIN goes high again. For GMCH 2009 applications ($\overline{\text{CLKEN}}$ = GND), connect PGDIN to the 5V bias supply.

Pin Description (continued)

PIN	NAME	FUNCTION
28	$\overline{\text{VRHOT}}$	Active-Low Open-Drain Output of Internal Comparator. $\overline{\text{VRHOT}}$ is pulled low when the voltage at THRM goes below 1.5V (30% of V_{CC}). $\overline{\text{VRHOT}}$ is high-impedance in shutdown.
29	TIME	Slew-Rate Adjustment Pin. TIME regulates to 2.0V and the load current determines the slew rate of the internal error-amplifier target. The sum of the resistance between TIME and GND (R_{TIME}) determines the nominal slew rate: Slew rate = (12.5mV/µs) x (71.5kΩ/R_{TIME}) The guaranteed R_{TIME} range is between 35.7kΩ and 178kΩ. This nominal slew rate applies to VID transitions and to the transition from boot mode to VID. If the VID DAC inputs are clocked, the slew rate for all other VID transitions is set by the rate at which they are clocked, up to a maximum slew rate equal to the nominal slew rate defined above. The startup and shutdown slew rates are always 1/8 of nominal slew rate to minimize surge currents. If $\overline{\text{SLOW}}$ is high, the slew rate is reduced to 1/2 of nominal.
30	ILIM	Valley Current-Limit Adjustment Input. The valley current-limit threshold voltage at CSP to CSN equals precisely 1/10 the differential TIME to ILIM voltage over a 0.1V to 0.5V range (10mV to 50mV current-sense range). The negative current-limit threshold is nominally -125% of the corresponding valley current-limit threshold. Connect ILIM directly to V_{CC} to set the default current-limit threshold setting of 22.5mV (typ) nominal.
31	V_{CC}	Controller Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with 1µF minimum.
32	CCV	Integrator Capacitor Connection. Connect a capacitor (C_{CCV}) from CCV to GND to set the integration time constant. Choose the capacitor value according to: $16\pi \times (C_{CCV}/G_{m(CCV)}) \times f_{SW} >> 1$ where $G_{m(CCV)}$ = 320µS (max) is the integrator's transconductance and f_{SW} is the switching frequency set by the R_{TON} value. The integrator is internally disabled during any downward output-voltage transition that occurs in pulse-skipping mode, and remains disabled until the transition blanking period expires and the output reaches regulation (error amplifier transition detected).
—	EP (GND)	Exposed Pad (Back Side) and Analog Ground. Internally connected to GND. Connect to the ground plane through a thermally enhanced via.

1-Phase Quick-PWM Intel IMVP-6.5/GMCH Controllers

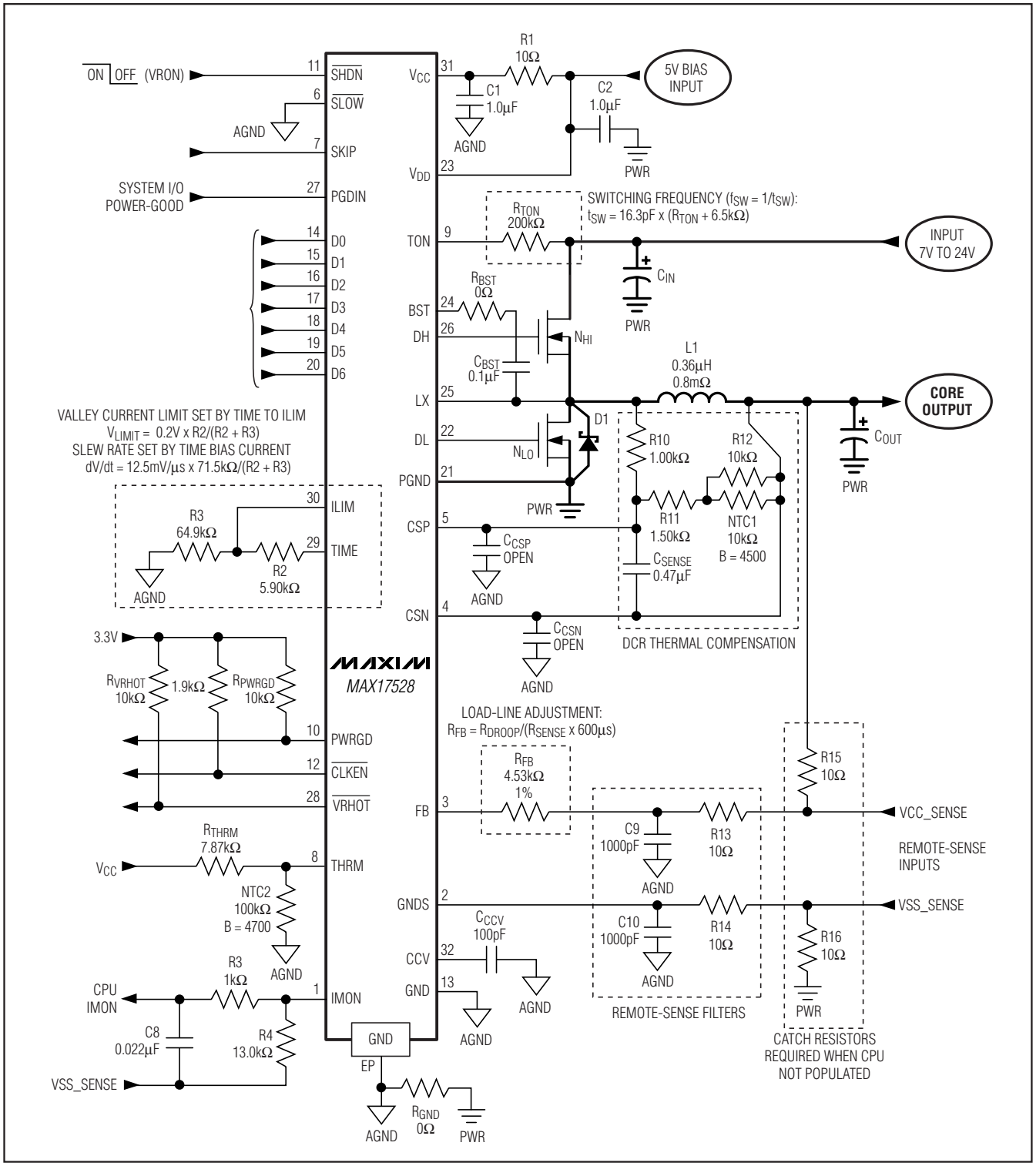


Figure 1. IMVP-6.5 CPU Core Application Circuit

Table 1. IMVP-6.5 Component Selection

DESIGN PARAMETERS	AUBURNDALE IMVP-6.5 ULV	AUBURNDALE IMVP-6.5 ULV	AUBURNDALE RENDER GMCH SV	AUBURNDALE RENDER GMCH ULV
Circuit	Figure 1	Figure 1	Figure 2	Figure 2
Input-Voltage Range	7V to 20V	5V	7V to 20V	7V to 20V
Maximum Load Current (TDC Current)	20A (15A)	20A (15A)	15A (10A)	7A (5A)
Transient Load Current	14A (10A/µs)	14A (10A/µs)	12A (10A/µs)	5A (10A/µs)
Load Line	3mV/A	3mV/A	7mV/A	7mV/A
POC Setting	20A	20A	20A	20A
COMPONENTS				
TON Resistance (R_{TON})	200kΩ (f_{SW} = 300kHz)	120kΩ (f_{SW} = 500kHz)	200kΩ (f_{SW} = 300kHz)	200kΩ (f_{SW} = 300kHz)
Inductance (L)	NEC/TOKIN MPC1055LR36 0.36µH, 32A, 0.8mΩ	NEC/TOKIN MPC1055LR36 0.36µH, 32A, 0.8mΩ	NEC/TOKIN MPCG0740LR42 0.42µH, 20A, 1.55mΩ	NEC/TOKIN MPC1040LR88C 0.88µH, 24A, 2.3mΩ
High-Side MOSFET (N_H)	Siliconix 1x Si4386DY 7.8mΩ/9.5mΩ (typ/max)	Siliconix 1x Si4386DY 7.8mΩ/9.5mΩ (typ/max)	Siliconix 1x Si4386DY 7.8mΩ/9.5mΩ (typ/max)	Siliconix 1x Si4386DY 7.8mΩ/9.5mΩ (typ/max)
Low-Side MOSFET (N_L)	Siliconix 2x Si4642DY 3.9mΩ/4.7mΩ (typ/max)	Siliconix 2x Si4642DY 3.9mΩ/4.7mΩ (typ/max)	Siliconix 1x Si4642DY 3.9mΩ/4.7mΩ (typ/max)	Siliconix 1x Si4642DY 3.9mΩ/4.7mΩ (typ/max)
Output Capacitors (C_{OUT})	4x 330µF, 6mΩ, 2.5V Panasonic EEFSX0D0D331XR 32x 10µF, 6V ceramic (0805)	4x 330µF, 6mΩ, 2.5V Panasonic EEFSX0D0D331XR 32x 10µF, 6V ceramic (0805)	1x 470µF, 6mΩ, 2.5V SANYO 2R5TPD470M6L 10x 10µF, 6V ceramic (0805)	1x 220µF, 7mΩ, 2V SANYO 2TPF220M7L 10x 10µF, 6V ceramic (0805)
Input Capacitors (C_{IN})	4x 10µF, 25V ceramic (1210)	6x 10µF, 6V ceramic (0805)	2x 10µF, 25V ceramic (1210)	2x 10µF, 25V ceramic (1210)
TIME-ILIM Resistance (R1)	5.90kΩ	5.90kΩ	6.65kΩ	6.65kΩ
ILIM-GND Resistance (R2)	64.9kΩ	64.9kΩ	64.9kΩ	64.9kΩ
FB Resistance (R_{FB})	4.53kΩ	4.53kΩ	10.0kΩ	5.62kΩ
IMON Resistance (R4)	13.0kΩ	13.0kΩ	7.68kΩ	4.42kΩ
LX-CSP Resistance (R5)	1.00kΩ	1.00kΩ	1.50kΩ	0.806kΩ
CSP-CSN Series Resistance (R6)	1.50kΩ	1.50kΩ	1.50kΩ	1.20kΩ
Parallel NTC Resistance (R7)	10.0kΩ	10.0kΩ	4.02kΩ	15.0kΩ
DCR Sense NTC (NTC1)	10kΩ NTC B = 3380 TDK NTCG163JH103F	10kΩ NTC B = 3380 TDK NTCG163JH103F	10kΩ NTC B = 3380 TDK NTCG163JH103F	10kΩ NTC B = 3380 TDK NTCG163JH103F
DCR Sense Capacitance (C_{SENSE})	0.47µF, 6V ceramic (0805)	0.47µF, 6V ceramic (0805)	0.22µF, 6V ceramic (0805)	0.47µF, 6V ceramic (0805)

1-Phase Quick-PWM Intel IMVP-6.5/GMCH Controllers

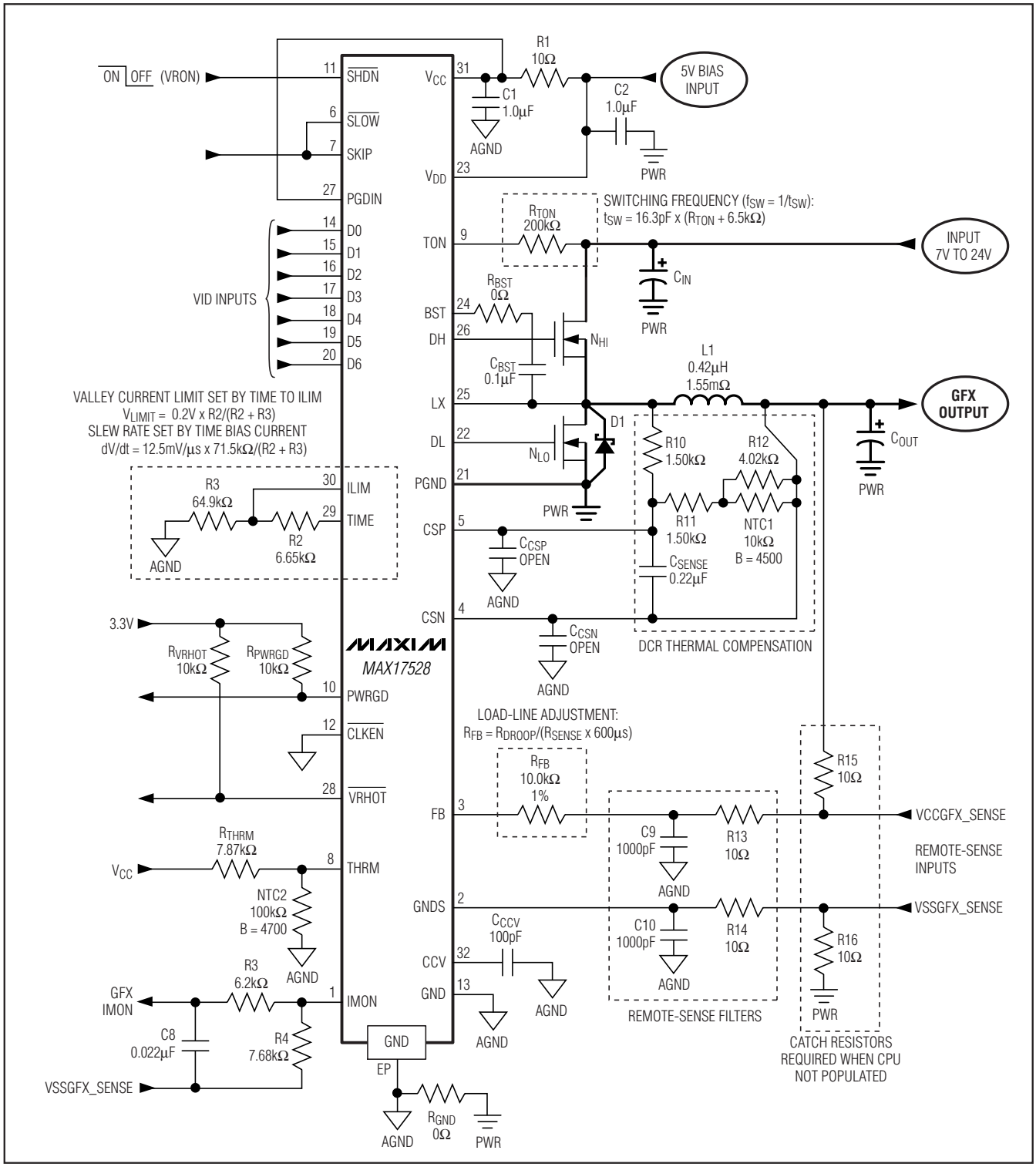


Figure 2. GMCH (Render Core) Application Circuit

Detailed Description

Free-Running, Constant On-Time Controllers with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward (Figure 3). This architecture relies on the output filter capacitor's ESR and the load regulation to provide the proper current-mode compensation, so the resulting feedback ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage, and directly proportional to the feedback voltage (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low (the feedback voltage drops below the target voltage), the inductor current is below the valley current-limit threshold, and the minimum off-time one-shot times out.

+5V Bias Supply (V_{CC} and V_{DD})

The Quick-PWM controller requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95%-efficient, +5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the +5V bias supply can be generated with an external linear regulator.

The +5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW}\left(Q_{G(LOW)} + Q_{G(HIGH)}\right)$$

where I_{CC} is provided in the *Electrical Characteristics* table, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V_{IN} and V_{DD} can be connected if the input power source is a fixed +4.5V to +5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (TON)

Connect a resistor (R_{TON}) between TON and V_{IN} to set the switching period ($t_{SW} = 1/f_{SW}$):

$$t_{SW} = 16.3pF \times (R_{TON} + 6.5k\Omega)$$

A 96.75kΩ to 303.25kΩ corresponds to switching periods of 1.67µs (600kHz) to 5µs (200kHz), respectively. High-frequency (over 500kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This may be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (under 300kHz) operation offers the best overall efficiency at the expense of component size and board space.

TON Open-Circuit Fault Protection

The TON input includes open-circuit protection to avoid long, uncontrolled on-times that could result in an overvoltage condition on the output. The MAX17528 detects an open-circuit fault if the TON current drops below 10µA for any reason—the TON resistor (R_{TON}) is unpopulated, a high resistance value is used, the input voltage is low, etc. Under these conditions, the MAX17528 stops switching (DH and DL pulled low) and immediately sets the fault latch. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

On-Time One-Shot

The core contains a fast, low-jitter, adjustable one-shot that sets the high-side MOSFET's on-time. The one-shot varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the R_{TON} input, and proportional to the feedback voltage (V_{FB}):

$$t_{ON} = t_{SW}\left(\frac{V_{FB}}{V_{IN}}\right)$$

where the switching period ($t_{SW} = 1/f_{SW}$) is set by the resistor between V_{IN} and TON.

This algorithm results in a nearly constant switching frequency despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions, such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output voltage ripple. The on-time one-shots have good accuracy at the operating points specified in the *Electrical Characteristics* table. On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* table can vary over a wider range.

1-Phase Quick-PWM Intel IMVP-6.5/GMCH Controllers

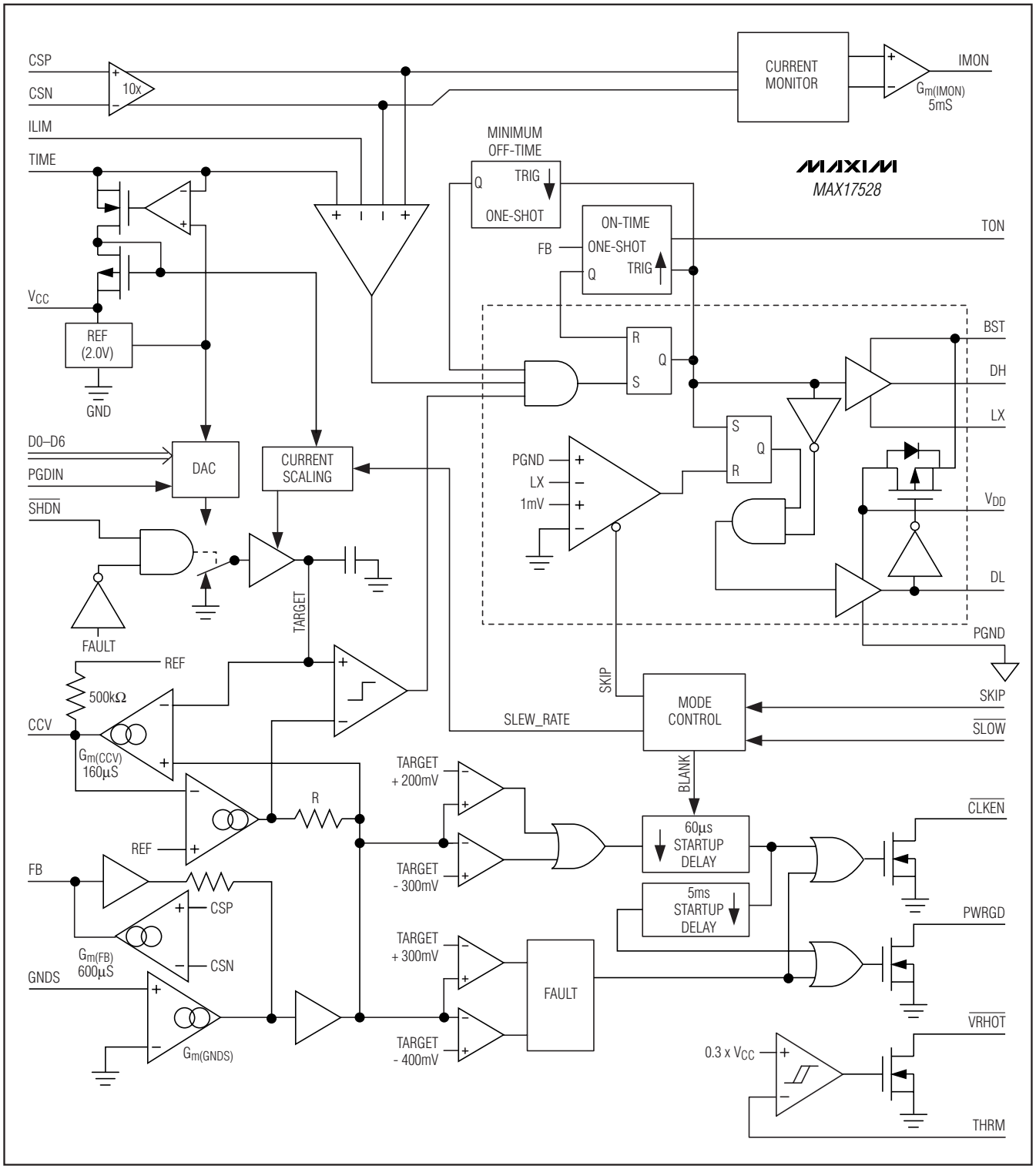


Figure 3. Functional Diagram

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* table are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, and printed-circuit board (PCB) copper losses in the output and ground tend to raise the switching frequency as the load current increases. Under light-load conditions, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only during forced-PWM operation and dynamic output-voltage transitions when the inductor current reverses at light- or negative-load currents. With reversed inductor current, the inductor's EMF causes LX to go high earlier than normal, extending the on-time by a period equal to the DH-rising dead time. For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency is:

$$f_{SW} = \frac{(V_{OUT} + V_{DIS})}{t_{ON}(V_{IN} + V_{DIS} - V_{CHG})}$$

where V_{DIS} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; V_{CHG} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time as determined above.

Current Sense

The output current is differentially sensed by the high-impedance current-sense inputs (CSP and CSN). Low-offset amplifiers are used for voltage-positioning gain, current-limit protection, and current monitoring. Sensing the current at the output offers advantages, including less noise sensitivity and the flexibility to use either a current-sense resistor or the DC resistance of the power inductor.

Using the DC resistance (R_{DCR}) of the inductor allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and current monitor. This current-sense method uses an RC filtering network to extract the current information from the inductor (see Figure 4). The resistive divider used should provide a current-sense resistance (R_{CS}) low enough to meet the current-limit requirements (R_{CS} x $I_{OUT(MAX)}$ < 50mV), and the time constant of the RC network should match the inductor's time constant (L/R_{DCR}):

$$R_{CS} = \left(\frac{R2}{R1+R2}\right)R_{DCR}$$

and:

$$R_{DCR} = \frac{L}{C_{EQ}}\left[\frac{1}{R1} + \frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance, and R_{DCR} is the inductor's series DC resistance. Use the worst-case inductance and R_{DCR} values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load. To minimize the current-sense error due to the current-sense inputs' bias current (I_{CSP}), choose R1 ll R2 to be less than 2kΩ and use the above equation to determine the sense capacitance (C_{EQ}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage Positioning and Loop Compensation* section for detailed information.

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 4). The ESL-induced voltage step does not affect the average current-sense voltage, but results in a significant peak current-sense voltage error that results in unwanted offsets in the regulation voltage and results in early current-limit detection. Similar to the inductor DCR sensing method, the RC filter's time constant should match the L/R time constant formed by the current-sense resistor's parasitic inductance:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R1$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is the current-sense resistance value, C_{EQ} and R1 are the time-constant matching components.

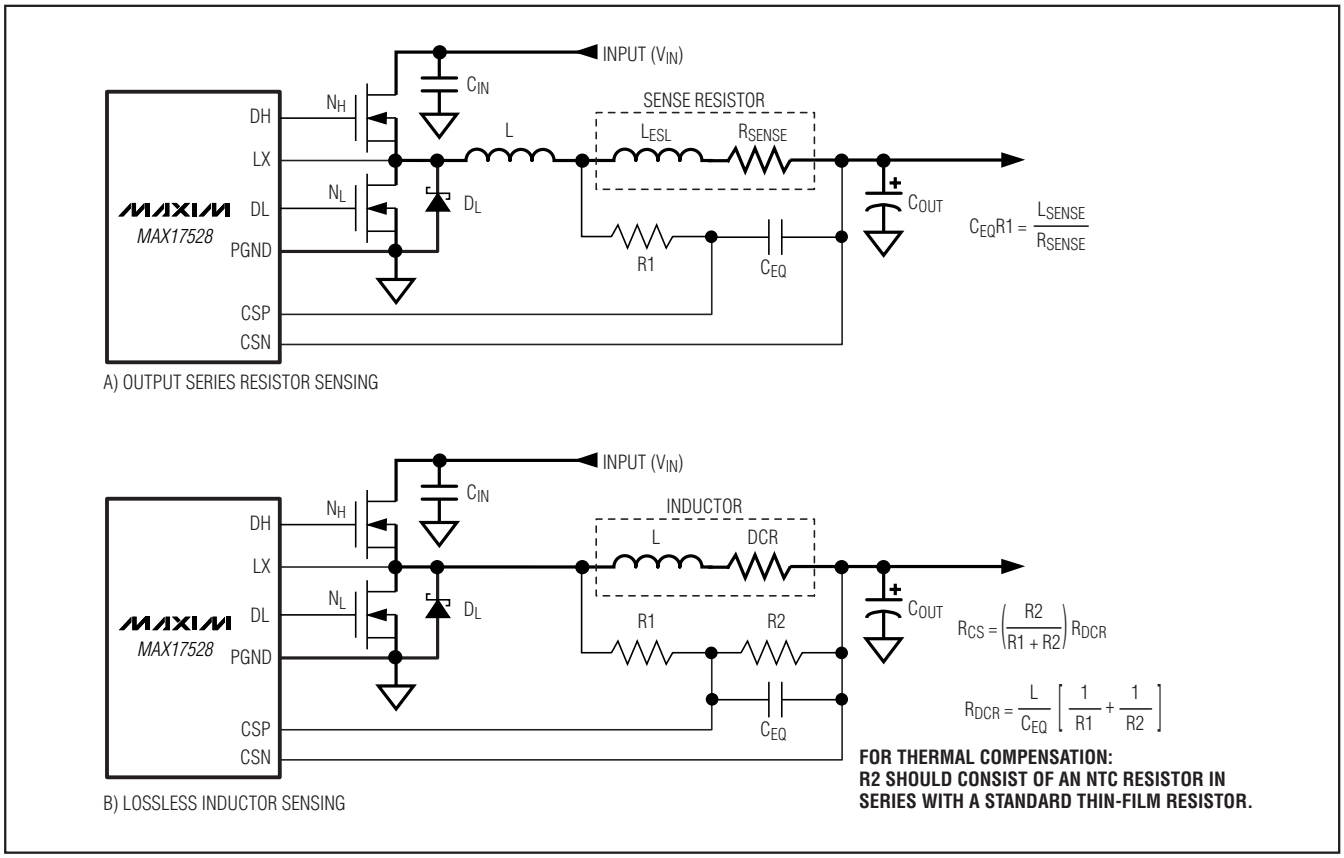


Figure 4. Current-Sense Methods

Current Limit

The current-limit circuit employs a "valley" current-sensing algorithm that uses a current-sense element (see Figure 4) between the current-sense inputs (CSP to CSN) to detect the inductor current. If the differential current-sense voltage exceeds the current-limit threshold, the PWM controller does not initiate a new cycle until the inductor current drops below the valley current-limit threshold. Since only the valley current level is actively limited, the actual peak inductor current exceeds the valley current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense impedance, inductor value, and battery voltage. When combined with the undervoltage protection circuit, this current-limit method is effective in almost every circumstance.

The positive valley current-limit threshold voltage at CSP to CSN equals precisely 1/10 of the differential TIME to ILIM voltage over a 0.1V to 0.5V range (10mV to 50mV current-sense range). Connect ILIM directly to V_{CC} to set the default current-limit threshold setting of 22.5mV nominal.

The negative current-limit threshold (forced-PWM mode only) is nominally -125% of the corresponding valley current-limit threshold. When the inductor current drops below the negative current limit, the controller immediately activates an on-time pulse—DL turns off, and DH turns on—allowing the inductor current to remain above the negative current threshold.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (CSP, CSN).

Feedback

The nominal no-load output voltage (V_{TARGET}) is defined by the VID-selected DAC voltage (see Table 2) plus the remote ground-sense adjustment (V_{GNDS}) as defined in the following equation:

$$V_{TARGET} = V_{FB} = V_{DAC} + V_{GNDS}$$

where V_{DAC} is the selected VID voltage. On startup, IMVP-6.5 ($\overline{CLKEN}$ pullup to 3.3V with 1.9kΩ) applications slew the target voltage from ground to the preset 1.1V boot voltage and GMCH ($\overline{CLKEN}$ = GND) applications slew the target voltage directly to the VID-selected DAC target.

Voltage-Positioning Amplifier (Steady-State Droop)

The MAX17528 includes a transconductance amplifier for adding gain to the voltage-positioning sense path. The amplifier's input is generated by the differential current-sense inputs that sense the inductor current by measuring the voltage across either current-sense resistors or the inductor's DCR. The amplifier's output connects directly to the regulator's voltage-positioned feedback input (FB), so the resistance between FB and the output-voltage sense point determines the voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FB}I_{FB}$$

where the target voltage (V_{TARGET} = V_{FB}) is defined by the selected VID code (Table 3 for IMVP6 or Table 4 for GMCH), and the FB amplifier's output current (I_{FB}) is determined by the sum of the current-sense voltages:

$$I_{FB} = G_{m(FB)}(V_{CSP} - V_{CSN})$$

where $G_{m(FB)}$ is typically 600µS as defined in the *Electrical Characteristics* table.

Differential Remote Sense

The MAX17528 includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PCB traces and through the processor's power pins. The feedback-sense node connects to the voltage-positioning resistor (R_{FB}). The ground-sense (GNDS) input connects to an amplifier that adds an offset directly to the feedback voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the voltage-positioning resistor (R_{FB}) and ground-sense (GNDS) input directly to the processor's remote-sense outputs as shown in Figures 1 and 2.

Integrator Amplifier

An integrator amplifier forces the DC average of the FB voltage to equal the target voltage. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 3), allowing accurate DC output-voltage regulation regardless of the output ripple voltage. The integrator amplifier has the ability to shift the output voltage by ±50mV (typ). The integration time constant can be set easily with an external compensation capacitor between CCV and analog ground, with the minimum recommended CCV capacitor value determined by:

$$C_{CCV} >> G_{m(CCV)}/(16\pi \times f_{SW})$$

where $G_{m(CCV)}$ = 320µS (max) is the integrator's transconductance and f_{SW} is the switching frequency set by the R_{TON} resistance.

The MAX17528 disables the integrator by connecting the amplifier inputs together at the beginning of all downward VID transitions done in pulse-skipping mode (SKIP = high). The integrator remains disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

DAC Inputs (D0–D6)

The digital-to-analog converter (DAC) programs the output voltage using the D0–D6 inputs. D0–D6 are low-voltage (1.0V) logic inputs designed to interface directly with the CPU. Do not leave D0–D6 unconnected. Changing D0–D6 initiates a transition to a new output-voltage level. Change D0–D6 together, avoiding greater than 20ns skew between bits. Otherwise, incorrect DAC readings can cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages are compatible with the Intel IMVP-6.5/GMCH specifications (Table 2).