Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

MAX17546

4.5V–42V, 5A, High-Efficiency, Synchronous Step-Down DC-DC Converter with Internal Compensation

General Description

The MAX17546 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated high-side MOSFET operates over a 4.5V to 42V input. The converter can deliver up to 5A and generates output voltages from 0.9V up to 0.9 x V_{IN}. The feedback (FB) voltage is accurate to within ±1.4% over -40°C to 125°C.

The MAX17546 uses peak current-mode control. The device can be operated in the pulse-width modulation (PWM), pulse-frequency modulation (PFM), and discontinuous conduction mode (DCM) control schemes.

The device is available in a 20-pin (5mm x 5mm) Thin QFN (TQFN) package. Simulation models are available.

Applications

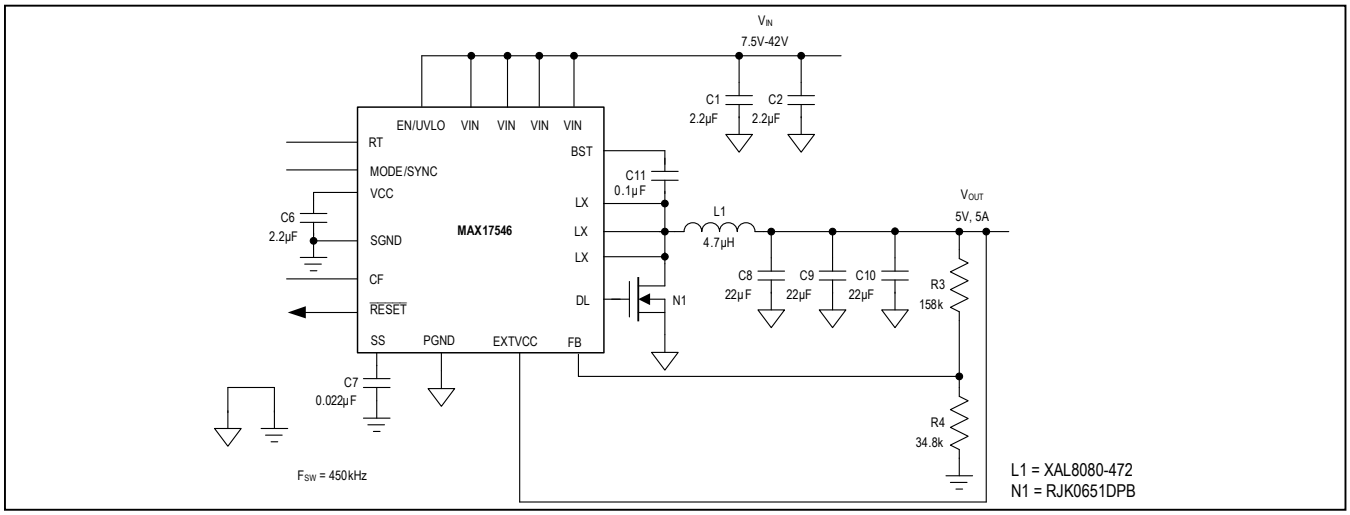
- Industrial Power Supplies
- Distributed Supply Regulation
- Base Station Power Supplies
- Wall Transformer Regulation
- High-Voltage Single-Board Systems
- General-Purpose Point-of-Load

***Ordering Information* appears at end of data sheet.**

Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky-Synchronous Operation
  - Internal Compensation for Any Output Voltage
  - Built-In Soft-Start
  - All-Ceramic Capacitors, Compact Layout
- Reduce Number of DC-DC Regulators to Stock
  - Wide 4.5V to 42V Input
  - Adjustable 0.9V to 0.9 x V_{IN} Output
  - 100kHz to 2.2MHz Adjustable Switching Frequency with External Synchronization
- Reduces Power Dissipation
  - Peak Efficiency > 95%
  - PFM/DCM Modes Enable Enhanced Light-Load Efficiency
  - Auxiliary Bootstrap LDO for Improved Efficiency
  - 3.5µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup or Latchoff Mode Overload Protection
  - DL to LX Short Detection Feature
  - Built-In Output Voltage Monitoring with $\overline{\text{RESET}}$
  - Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Load
  - Overtemperature Protection
  - -40°C to +125°C Operation

Typical Application Circuit for 5V Output



maxim integrated™

Absolute Maximum Ratings

V_{IN} to PGND .....-0.3V to +48V
EN/UVLO, SS to SGND .....-0.3V to +48V
LX to PGND.....-0.3V to (V_{IN} + 0.3V)
BST to PGND .....-0.3V to +53V
BST to LX.....-0.3V to +6.5V
BST to V_{CC} .....-0.3V to +48V
FB, CF, $\overline{RESET}$, MODE/SYNC, RT to SGND .....-0.3V to +6.5V
DL, V_{CC} to PGND .....-0.3V to +6.5V
SGND to PGND.....-0.3V to +0.3V
EXTVCC to PGND .....-0.3V to +26V
LX Total RMS Current .....±9.9A
Output Short-Circuit Duration.....Continuous
Continuous Power Dissipation (T_A = +70°C) (multilayer board)
TQFN (derate 33.3mW/°C above T_A = +70°C).....2666.7mW
Operating Temperature Range..... -40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +160°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Thermal Characteristics

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 23°C/W (Note 1)
Junction-to-Case Thermal Resistance (θ_{JC}).....2°C/W

Note 1: Applicable only to the Evaluation Kit in free space with no airflow.

Electrical Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = OPEN (450kHz), C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = $V_{MODE/SYNC}$ = 0V, LX = SS = $\overline{RESET}$ = open, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUT SUPPLY (V_{IN})						
Input Voltage Range	V_{IN}		4.5		42	V
Input Shutdown Current	I_{IN-SH}	$V_{EN/UVLO}$ = 0V (shutdown mode)		3.5	5.5	µA
Input Quiescent Current	I_{Q_PFM}	V_{FB} = 1V, MODE = RT= open		128		µA
		V_{FB} = 1V, MODE = open, R_{RT} = 40.2k		168		
	I_{Q_DCM}	DCM mode, V_{LX} = 0.1V		1.27	2	mA
ENABLE/UVLO (EN/UVLO)						
EN/UVLO Threshold	V_{ENR}	$V_{EN/UVLO}$ rising	1.19	1.215	1.24	V
	V_{ENF}	$V_{EN/UVLO}$ falling	1.068	1.09	1.112	
EN/UVLO Input Leakage Current	I_{EN}	$V_{EN/UVLO}$ = 1.245V, T_A = +25°C	-50	0	+50	nA
LDO						
V_{CC} Output Voltage Range	V_{CC}	6V < V_{IN} < 42V, I_{VCC} = 1mA	4.75	5	5.25	V
		1mA ≤ I_{VCC} ≤ 45mA				
V_{CC} Current Limit	$I_{VCC-MAX}$	V_{CC} = 4.3V, V_{IN} = 6V	50	90	140	mA
V_{CC} Dropout	V_{CC-DO}	V_{IN} = 4.5V, I_{VCC} = 45mA	4.1			V

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = OPEN (450kHz), C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = $V_{MODE/SYNC}$ = 0V, LX = SS = $\overline{RESET}$ = open, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{CC} UVLO	V_{CC_UVR}	V_{CC} rising	4.1	4.2	4.3	V
	V_{CC_UVF}	V_{CC} falling	3.7	3.8	3.9	
EXT LDO						
EXT V_{CC} Operating Voltage Range			4.84		24	V
EXT V_{CC} Switchover Voltage		EXT V_{CC} rising	4.56	4.7	4.84	V
EXT V_{CC} Switchover Voltage Hysteresis			0.205	0.232	0.255	V
EXT V_{CC} Dropout	EXT V_{CC-DO}	EXT V_{CC} = 4.75V, $I_{EXT\ VCC}$ = 45mA			0.4	V
EXT V_{CC} Current Limit	EXT IV_{CC-MAX}	V_{CC} = 4.3V, EXT V_{CC} = 5V	45	85	140	mA
POWER MOSFET AND LOW-SIDE DRIVER						
High-Side nMOS On-Resistance	R_{DS-ONH}	I_{LX} = 1.0A		45	90	mΩ
LX Leakage Current	I_{LX_LKG}	V_{LX} = V_{IN} - 1V, V_{LX} = V_{PGND} + 1V, T_A = +25°C	-4	1	+4	µA
Pullup Resistance		I_{SOURCE} = 100mA		1.9	2.9	Ω
Pulldown Resistance		I_{SINK} = 100mA		1	1.65	Ω
SOFT-START (SS)						
Charging Current	I_{SS}	V_{SS} = 0V	4.7	5	5.3	µA
FEEDBACK (FB)						
FB Regulation Voltage	V_{FB_REG}	MODE = SGND or MODE = V_{CC}	0.887	0.9	0.912	V
		MODE = open	0.887	0.915	0.936	
FB Input Bias Current	I_{FB}	0 < V_{FB} < 1V, T_A = +25°C	-75		+75	nA
MODE/SYNC						
MODE Threshold	V_{M-DCM}	MODE = V_{CC} (DCM mode)	V_{CC} - 0.6			V
	V_{M-PFM}	MODE = open (PFM mode)		V_{CC}/2		
	V_{M-PWM}	MODE = GND (PWM mode)			0.6	
SYNC Frequency Capture Range		f_{SW} set bt R_{RT}	1.1 x f_{SW}		1.4 x f_{SW}	kHz
SYNC Pulse Width			50			ns
SYNC Threshold	V_{IH}		2.0			V
	V_{IL}				0.8	
CURRENT LIMIT						
Peak Current-Limit Threshold	$I_{PEAK-LIMIT}$	R_{DL} = open or R_{DL} = 174kΩ	6.5	7.8	9.1	A
		R_{DL} = 61.9k or R_{DL} = 26.1k	5.85	7	8.15	A
Runaway Current-Limit Threshold	$I_{RUNAWAY-LIMIT}$	R_{DL} = open or R_{DL} = 174kΩ	7.33	8.8	10.4	A
		R_{DL} = 61.9k or R_{DL} = 26.1k	6.7	8.05	9.4	A

Electrical Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, R_{RT} = OPEN (450kHz), C_{VCC} = 2.2µF, V_{PGND} = V_{SGND} = $V_{MODE/SYNC}$ = 0V, LX = SS = $\overline{RESET}$ = open, V_{BST} to V_{LX} = 5V, V_{FB} = 1V, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Negative Current Limit Comparator Voltage Reference		MODE = open or MODE = V_{CC}		0		mV
		MODE = GND	42	50	58	
PFM Current-Limit Threshold	I_{PFM}	MODE = open		2		A
RT						
Switching Frequency	f_{SW}	R_{RT} = 93.1kΩ	180	200	220	kHz
		R_{RT} = open	420	450	480	
		R_{RT} = 6.98kΩ	1950	2200	2450	
V_{FB} Undervoltage Trip Level to Cause Hiccup	$V_{FB-HICF}$		0.56	0.58	0.61	V
HICCUP Timeout		(Note 3)		32768		Cycles
Minimum On-Time	t_{ON-MIN}			95	160	ns
Minimum Off-Time	$t_{OFF-MIN}$		140		160	ns
LX Dead Time				22		ns
$\overline{RESET}$						
$\overline{RESET}$ Output Level Low		$I_{\overline{RESET}}$ = 10mA			0.200	V
$\overline{RESET}$ Output Leakage Current		T_A = T_J = +25°C, $V_{\overline{RESET}}$ = 5.5V	-0.1		+0.1	µA
V_{OUT} Threshold for $\overline{RESET}$ Assertion	V_{FB-OKF}	V_{FB} falling	90.4	92.5	94.6	%
V_{OUT} Threshold for $\overline{RESET}$ Deassertion	V_{FB-OKR}	V_{FB} rising	93.4	95.5	97.7	%
$\overline{RESET}$ Deassertion Delay After FB Reaches 95% Regulation				1024		Cycles
THERMAL SHUTDOWN						
Thermal-Shutdown Threshold		Temperature rising		165		°C
Thermal-Shutdown Hysteresis				10		°C

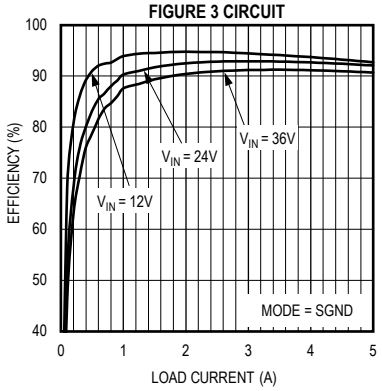
Note 2: All limits are 100% tested at +25°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.

Note 3: See the *Overcurrent Protection/HICCUP Mode* section for more details.

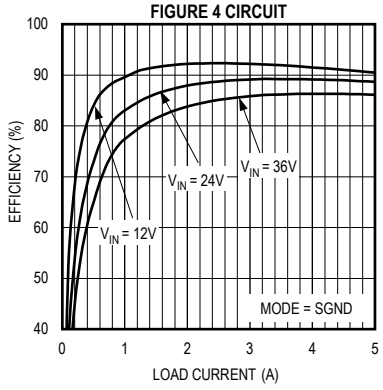
Typical Operating Characteristics

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 22,000pF, RT = MODE/SYNC = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

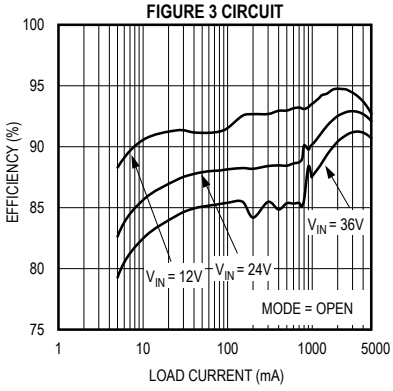
5V OUTPUT, PWM MODE, EFFICIENCY vs. LOAD CURRENT FIGURE 3 CIRCUIT



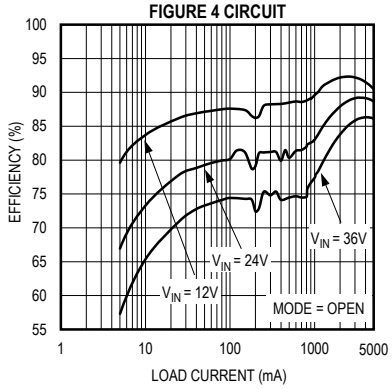
3.3V OUTPUT, PWM MODE, EFFICIENCY vs. LOAD CURRENT FIGURE 4 CIRCUIT



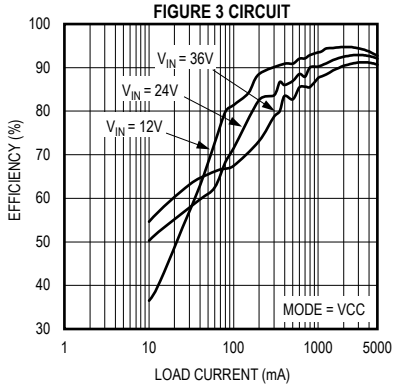
5V OUTPUT, PFM MODE, EFFICIENCY vs. LOAD CURRENT FIGURE 3 CIRCUIT



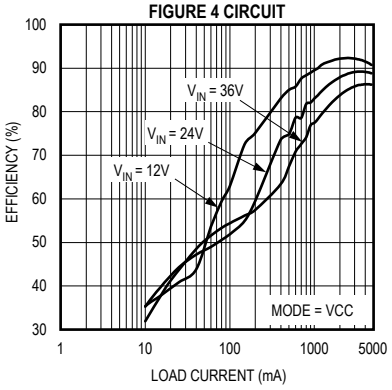
3.3V OUTPUT, PFM MODE, EFFICIENCY vs. LOAD CURRENT FIGURE 4 CIRCUIT



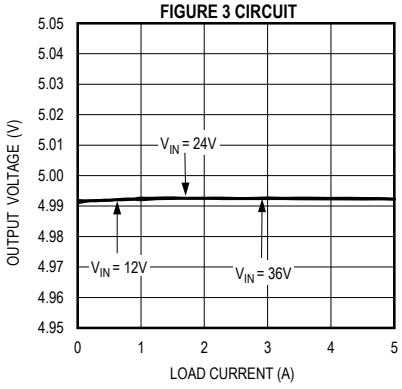
5V OUTPUT, DCM MODE, EFFICIENCY vs. LOAD CURRENT FIGURE 3 CIRCUIT



3.3V OUTPUT, DCM MODE, EFFICIENCY vs. LOAD CURRENT FIGURE 4 CIRCUIT



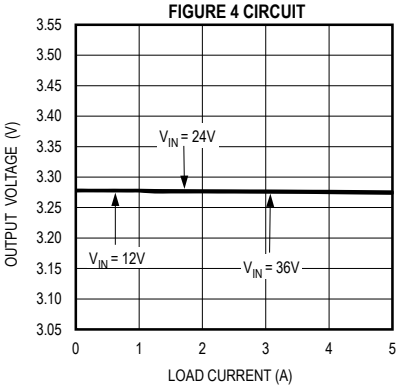
5V OUTPUT, PWM MODE, LOAD AND LINE REGULATION FIGURE 3 CIRCUIT



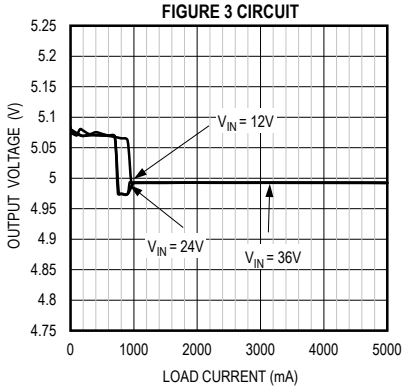
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 22,000pF, RT = MODE/SYNC = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

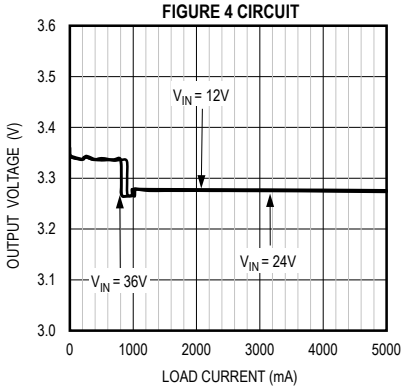
3.3V OUTPUT, PWM MODE, LOAD AND LINE REGULATION FIGURE 4 CIRCUIT



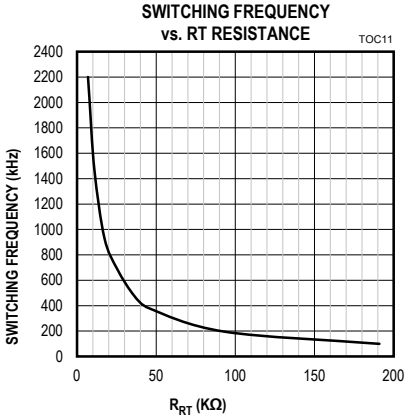
5V OUTPUT, PFM MODE, LOAD AND LINE REGULATION FIGURE 3 CIRCUIT



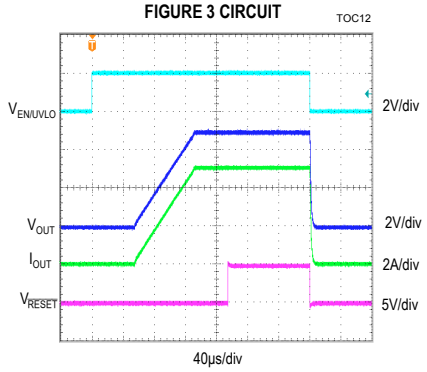
3.3V OUTPUT, PFM MODE, LOAD AND LINE REGULATION FIGURE 4 CIRCUIT



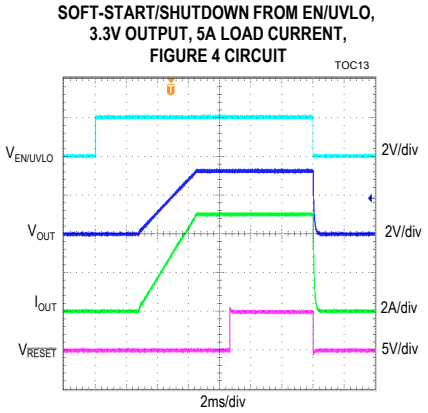
SWITCHING FREQUENCY vs. RT RESISTANCE



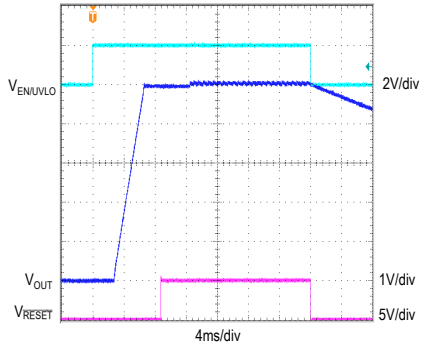
SOFT-START/SHUTDOWN FROM EN/UVLO, 5V OUTPUT, 5A LOAD CURRENT, FIGURE 3 CIRCUIT



SOFT-START/SHUTDOWN FROM EN/UVLO, 3.3V OUTPUT, 5A LOAD CURRENT, FIGURE 4 CIRCUIT



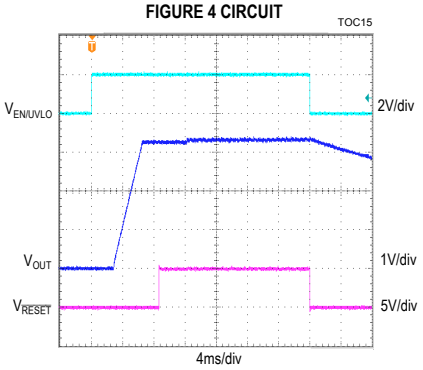
SOFT-START/SHUTDOWN FROM EN/UVLO, 5V OUTPUT, PFM MODE, 5mA LOAD CURRENT, FIGURE 3 CIRCUIT



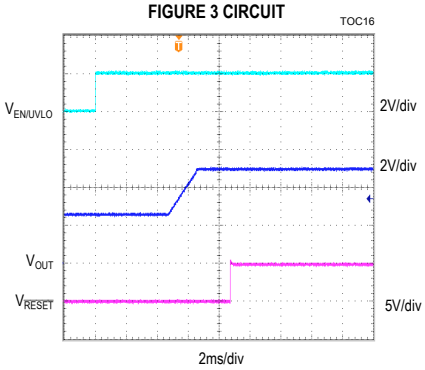
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 22,000pF, RT = MODE/SYNC = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

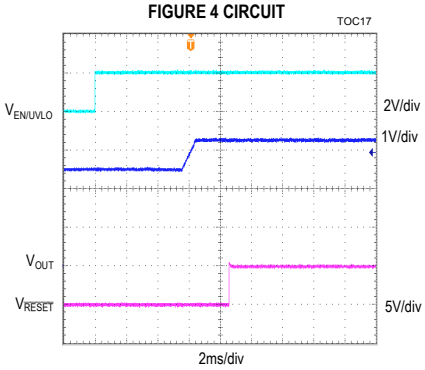
SOFT-START/SHUTDOWN FROM EN/UVLO, 3.3V OUTPUT, PFM MODE, 50mA LOAD CURRENT, FIGURE 4 CIRCUIT



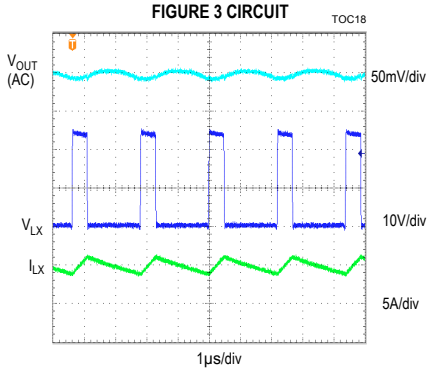
SOFT-START WITH 2.5V PREBIAS, 5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT



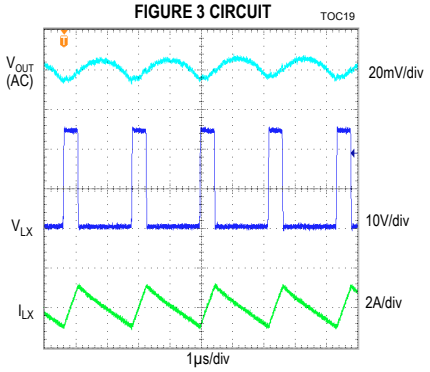
SOFT-START WITH 2.5V PREBIAS, 3.3V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT



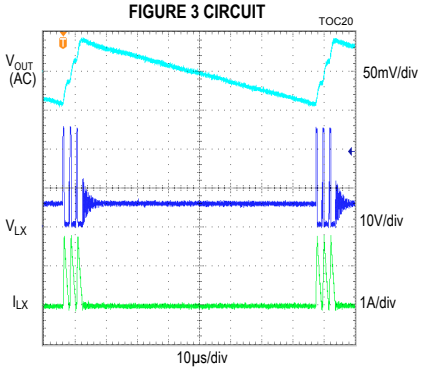
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, 5A LOAD CURRENT, FIGURE 3 CIRCUIT



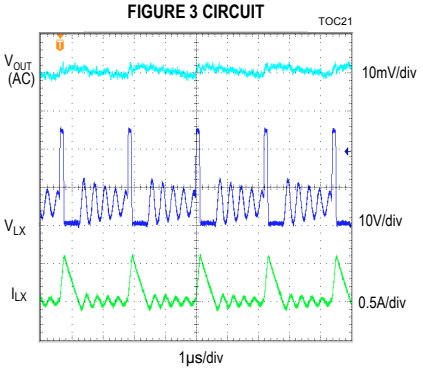
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, NO LOAD CURRENT, FIGURE 3 CIRCUIT



STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, PFM MODE, 25mA LOAD CURRENT, FIGURE 3 CIRCUIT



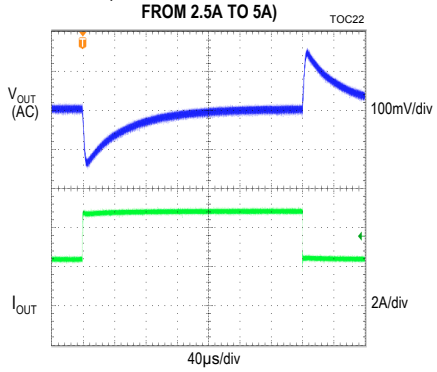
STEADY-STATE SWITCHING WAVEFORMS, 5V OUTPUT, DCM MODE, 25mA LOAD CURRENT, FIGURE 3 CIRCUIT



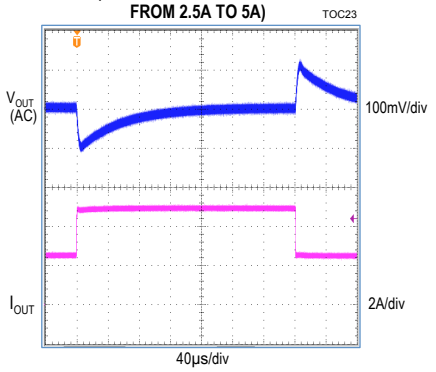
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 22,000pF, RT = MODE/SYNC = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

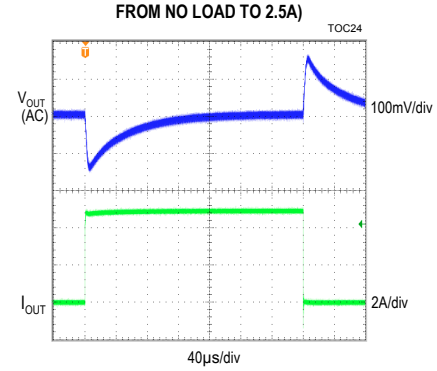
5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT (LOAD CURRENT STEPPED FROM 2.5A TO 5A)



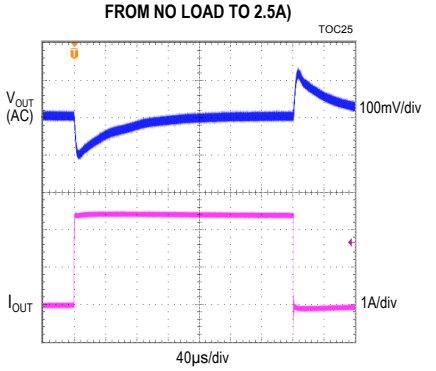
3.3V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT (LOAD CURRENT STEPPED FROM 2.5A TO 5A)



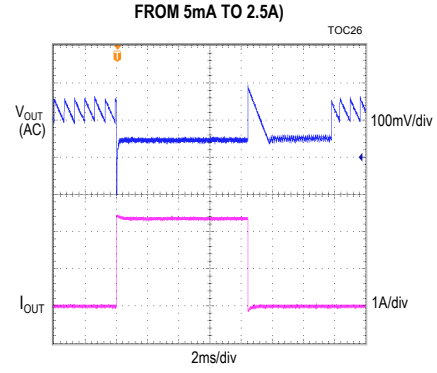
5V OUTPUT, PWM MODE, FIGURE 3 CIRCUIT (LOAD CURRENT STEPPED FROM NO LOAD TO 2.5A)



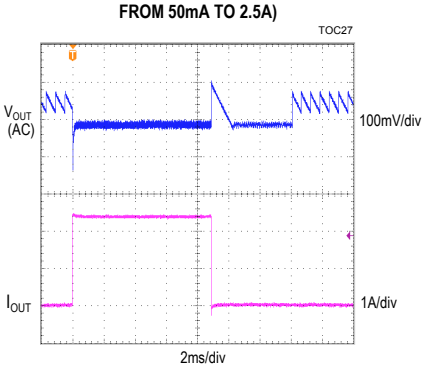
3.3V OUTPUT, PWM MODE, FIGURE 4 CIRCUIT (LOAD CURRENT STEPPED FROM NO LOAD TO 2.5A)



5V OUTPUT, PFM MODE, FIGURE 3 CIRCUIT (LOAD CURRENT STEPPED FROM 5mA TO 2.5A)



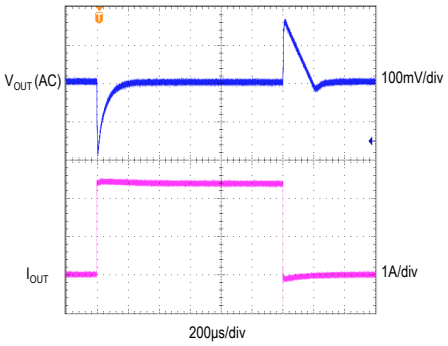
3.3V OUTPUT, PFM MODE, FIGURE 4 CIRCUIT (LOAD CURRENT STEPPED FROM 50mA TO 2.5A)



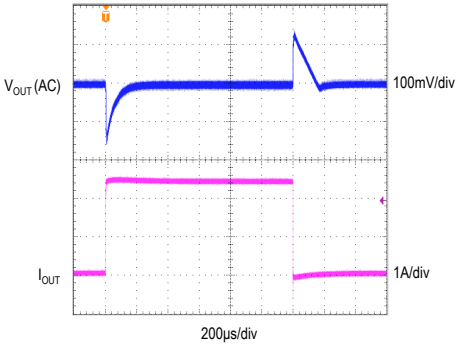
Typical Operating Characteristics (continued)

(V_{IN} = $V_{EN/UVLO}$ = 24V, V_{PGND} = V_{SGND} = 0V, C_{VIN} = 2 x 2.2µF, C_{VCC} = 2.2µF, C_{BST} = 0.1µF, C_{SS} = 22,000pF, RT = MODE/SYNC = open, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All voltages are referenced to SGND, unless otherwise noted.)

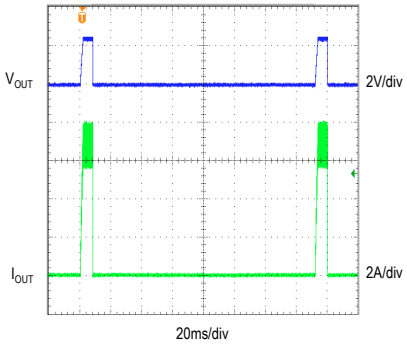
5V OUTPUT, DCM MODE (LOAD CURRENT STEPPED FROM 50mA TO 2.5A) FIGURE 3 CIRCUIT TOC28



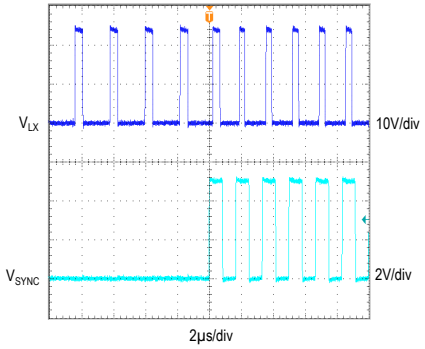
3.3V OUTPUT, DCM MODE (LOAD CURRENT STEPPED FROM 50mA TO 2.5A) FIGURE 4 CIRCUIT TOC29



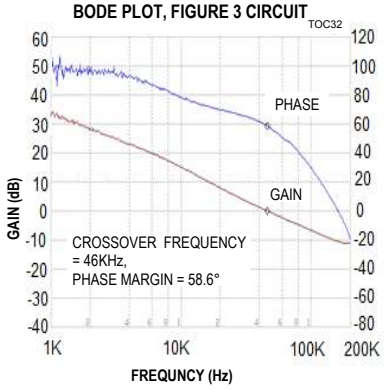
OVERLOAD PROTECTION 5V OUTPUT, FIGURE 3 CIRCUIT TOC30



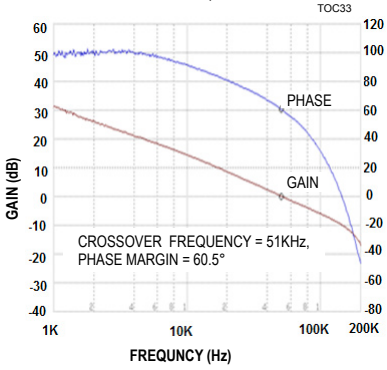
APPLICATION OF EXTERNAL CLOCK AT 600kHz, 5V OUTPUT, FIGURE 3 CIRCUIT TOC31



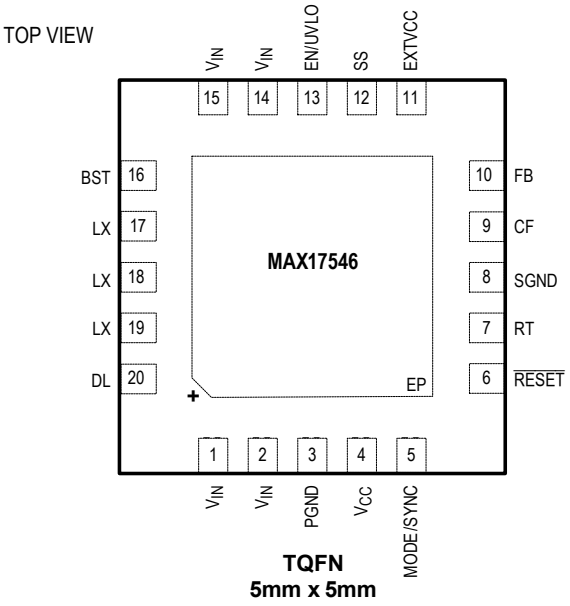
5V OUTPUT, 5A LOAD CURRENT, BODE PLOT, FIGURE 3 CIRCUIT TOC32



3.3V OUTPUT, 5A LOAD CURRENT, FIGURE 4 CIRCUIT, BODE PLOT TOC33



Pin Configuration



TQFN
5mm x 5mm

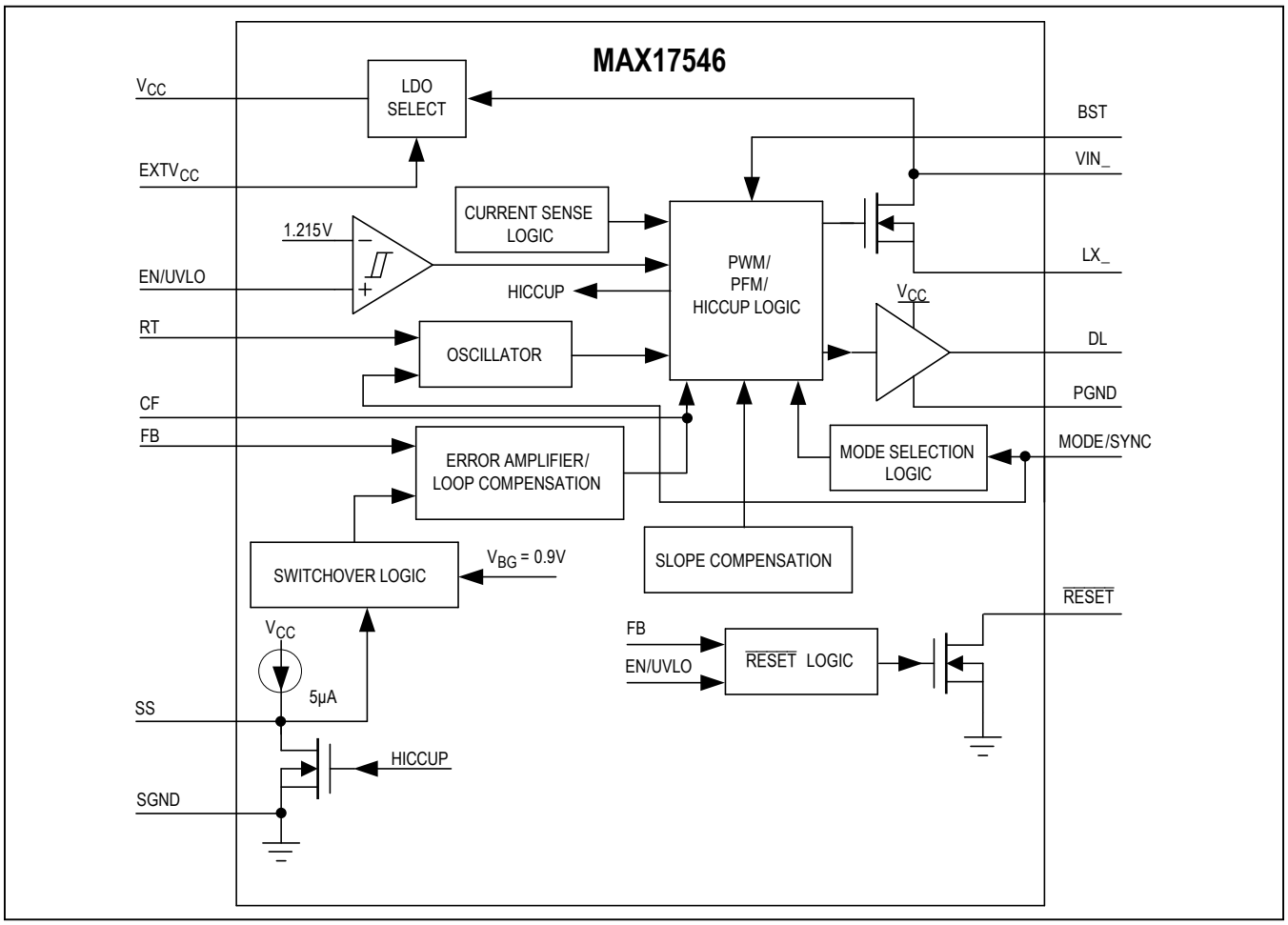
Pin Description

PIN	NAME	FUNCTION
1, 2, 14,15	V_{IN}	Power-Supply Input. 4.5V to 42V input supply range. Connect the V_{IN} pins together. Decouple to PGND with two 2.2µF capacitors; place the capacitors close to the V_{IN} and PGND pins. Refer to the MAX17546 Evaluation Kit datasheet for a layout example.
3	PGND	Power Ground. Connect the PGND pins externally to the power ground plane. Connect the SGND and PGND pins together at the ground return path of the V_{CC} bypass capacitor. Refer to the MAX17546 Evaluation Kit datasheet for a layout example.
4	V_{CC}	5V LDO Output. Bypass V_{CC} with a 2.2µF ceramic capacitance to SGND.
5	MODE/ SYNC	MODE/SYNC configures the MAX17546 to operate in PWM, PFM or DCM modes of operation. Leave MODE/SYNC unconnected for PFM operation (pulse skipping at light loads). Connect MODE/SYNC to SGND for constant-frequency PWM operation at all loads. Connect MODE/SYNC to V_{CC} for DCM operation. The device can be synchronized to an external clock using this pin. See the *MODE Selection* section ant the *External Frequency Synchronization* section for more details.
6	$\overline{\text{RESET}}$	Open-Drain $\overline{\text{RESET}}$ Output. The $\overline{\text{RESET}}$ output is driven low if FB drops below 92.5% of its set value. $\overline{\text{RESET}}$ goes high 1024 clock cycles after FB rises above 95.5% of its set value.
7	RT	Connect a resistor from RT to SGND to set the regulator's switching frequency. Leave RT open for the default 450kHz frequency. See the *Setting the Switching Frequency (RT)* section for more details.
8	SGND	Analog Ground
9	CF	At switching frequencies lower than 450kHz, connect a capacitor from CF to FB. Leave CF open if the switching frequency is equal to or more than 450kHz. See the *Loop Compensation* section for more details.
10	FB	Feedback Input. Connect FB to the center tap of an external resistor-divider from the output to SGND to set the output voltage. See the *Adjusting Output Voltage* section for more details.
11	EXTVCC	External Power Supply Input for the internal LDO. Applying a voltage between 4.84V and 24V at EXTVCC pin will bypass the internal LDO and improve efficiency.

Pin Description (continued)

PIN	NAME	FUNCTION
12	SS	Soft-Start Input. Connect a capacitor from SS to SGND to set the soft-start time.
13	EN/UVLO	Enable/Undervoltage Lockout. Drive EN/UVLO high to enable the output voltage. Connect to the center of the resistor-divider between V_{IN} and SGND to set the input voltage at which the MAX17546 turns on. Pull up to V_{IN} for always on operation.
16	BST	Boost Flying Capacitor. Connect a 0.1µF ceramic capacitor between BST and LX.
17, 18, 19	LX	Switching Node. Connect LX pins to the switching side of the inductor.
20	DL	Use DL pin to drive the gate of the low-side external n-MOSFET. A resistor connected between the DL pin and SGND selects the overload protection method and the peak and runaway current limits. See the *Overcurrent Protection/HICCUP Mode* section for more details.
—	EP	Exposed pad. Connect to the SGND pin. Connect to a large copper plane below the IC to improve heat dissipation capability. Add thermal vias below the exposed pad. Refer to the MAX17546 Evaluation Kit datasheet for a layout example.

Block Diagram



Detailed Description

The MAX17546 high-efficiency, high-voltage, synchronously rectified step-down converter with integrated high-side MOSFET operates over a 4.5V to 42V input. It delivers up to 5A and 0.9V to 90% V_{IN} output voltage. Built-in compensation across the output voltage range eliminates the need for external components. The feedback (FB) regulation accuracy over -40°C to +125°C is ±1.4%.

The device features a peak-current-mode control architecture. An internal transconductance error amplifier produces an integrated error voltage at an internal node that sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET's on-time, the inductor current ramps up. During the second-half of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

The device features a MODE/SYNC pin that can be used to operate the device in PWM, PFM, or DCM control schemes and to synchronize the switching freqeuncy to an external clock. The device integrates adjustable-input undervoltage lockout, adjustable soft-start, open-drain $\overline{\text{RESET}}$, auxiliary bootstrap LDO and DL to LX short detection features.

Mode Selection (MODE)

The logic state of the MODE/SYNC pin is latched when V_{CC} and EN/UVLO voltages exceed the respective UVLO rising thresholds and all internal voltages are ready to allow LX switching. If the MODE/SYNC pin is open at power-up, the device operates in PFM mode at light loads. If the MODE/SYNC pin is grounded at power-up, the device operates in constant-frequency PWM mode at all loads. Finally, if the MODE/SYNC pin is connected to V_{CC} at power-up, the device operates in constant-frequency DCM mode at light loads. State changes on the MODE/SYNC pin are ignored during normal operation.

PWM Mode Operation

In PWM mode, the inductor current is allowed to go negative. PWM operation provides constant frequency operation at all loads, and is useful in applications sensitive to switching frequency. However, the PWM mode of operation gives lower efficiency at light loads compared to PFM and DCM modes of operation.

PFM Mode Operation

PFM mode of operation disables negative inductor current and additionally skips pulses at light loads for high efficiency. In PFM mode, the inductor current is forced to a fixed peak of 2A every clock cycle until the output rises to 102.3% of the nominal voltage. Once the output reaches 102.3% of the nominal voltage, both the high-side and low-side FETs are turned off and the device enters hibernate operation until the load discharges the output to 101.1% of the nominal voltage. Most of the internal blocks are turned off in hibernate operation to save quiescent current. After the output falls below 101.1% of the nominal voltage, the device comes out of hibernate operation, turns on all internal blocks, and again commences the process of delivering pulses of energy to the output until it reaches 102.3% of the nominal output voltage.

The advantage of the PFM mode is higher efficiency at light loads because of lower quiescent current drawn from supply. The disadvantage is that the output-voltage ripple is higher compared to PWM or DCM modes of operation and switching frequency is not constant at light loads.

DCM Mode Operation

DCM mode of operation features constant frequency operation down to lighter loads than PFM mode, by not skipping pulses but only disabling negative inductor current at light loads. DCM operation offers efficiency performance that lies between PWM and PFM modes.

Linear Regulator (V_{CC} and EXTVCC)

The MAX17546 has two internal LDO (low-dropout) regulators which powers V_{CC}. One LDO is powered from VIN_ (INLDO) and the other LDO is powered from EXTVCC (EXTVCC LDO). Only one of the two LDOs is in operation at a time, depending on the voltage levels present at EXTVCC. If EXTVCC voltage is greater than 4.84V, V_{CC} is powered from EXTVCC. If EXTVCC is lower than 4.56V, VCC is powered from VIN_. Powering V_{CC} from EXTVCC increases efficiency at higher input voltages. EXTVCC voltage should not exceed 24V.

Typical V_{CC} output voltage is 5V. Bypass V_{CC} to SGND with a 2.2µF low ESR ceramic capacitor. V_{CC} powers the internal blocks and the low-side MOSFET driver and re-charges the external bootstrap capacitor. Both INLDO and EXTVCC LDO can source up to 100mA. The MAX17546 employs an under-voltage lockout circuit that forces both the regulators off when V_{CC} falls below 3.8V (typ). The regulators can be immediately enabled again when V_{CC} > 4.2V. The 400mV UVLO hysteresis prevents chattering on power-up/power-down.

In applications where the buck converter output is connected to EXTVCC pin, if the output is shorted to ground then the transfer from EXTVCCLDO to INLDO happens seamlessly without any impact on the normal functionality.

Setting the Switching Frequency (RT)

The switching frequency of the MAX17546 can be programmed from 100kHz to 2.2MHz by using a resistor connected from RT to SGND. The switching frequency (f_{SW}) is related to the resistor connected at the RT pin (R_{RT}) by the following equation:

$$R_{RT} \cong \frac{19 \times 10^3}{f_{SW}} - 1.7$$

where R_{RT} is in kΩ and f_{SW} is in kHz. Leaving the RT pin open causes the device to operate at the default switching frequency of 450kHz. See Table 1 for RT resistor values for a few common switching frequencies.

Operating Input Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT(MAX)} \times (R_{DCR} + 0.075))}{1 - (f_{SW(MAX)} \times t_{OFF(MAX)})} + (I_{OUT(MAX)} \times 0.075)$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON(MIN)}}$$

where V_{OUT} is the steady-state output voltage, $I_{OUT(MAX)}$ is the maximum load current, R_{DCR} is the DC resistance of the inductor, $f_{SW(MAX)}$ is the maximum switching frequency, $t_{OFF(MAX)}$ is the worst-case minimum switch off-time (158ns), and $t_{ON(MIN)}$ is the worst-case minimum switch on-time (137ns).

External Frequency Synchronization

The internal oscillator of the MAX17546 can be synchronized to an external clock signal on the MODE/SYNC pin. The external synchronization clock frequency must be between 1.1 x f_{SW} and 1.4 x f_{SW}, where f_{SW} is the frequency programmed by the RT resistor. When an external clock is applied to MODE/SYNC pin, the internal oscillator frequency changes to external clock frequency (from original frequency based on RT setting) after detecting 16 external clock edges. The converter will operate in PWM mode during synchronization operation. When the external clock is applied on-fly then the mode of operation will change to PWM from the initial state of PFM/DCM/PWM. When the external clock is removed on-fly then the internal oscillator frequency changes to the RT set frequency and the converter will still continue to operate in PWM mode. The minimum external clock pulse-width high should be greater than 22ns. See the MODE/SYNC section in the *Electrical Characteristics* table for details.

Table 1. Switching Frequency vs. RT Resistor

SWITCHING FREQUENCY (kHz)	RT RESISTOR (kΩ)
450	OPEN
200	93.1
2200	6.98

DL to LX short detection

In MAX17546, DL and LX_ pins are adjacent to each other. To prevent damage to the low side external FET in case DL pin is shorted to the LX_ pins, DL to LX_ short detection feature has been implemented. If the MAX17546 detects that the DL pin is shorted to the LX_ pins before startup, the startup sequence will not be initiated and output voltage will not be soft-started.

Overcurrent Protection/HICCUP Mode

The MAX17546 is provided with a robust over-current protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch current exceeds an internal limit. A runaway current limit on the high-side switch current protects the device under high input voltage, short circuit conditions when there is insufficient output voltage available to restore the Inductor current that was built up during the on period of the step-down converter. One occurrence of the runaway current limit triggers a hiccup mode. In addition, if due to a fault condition, output voltage drops to 68% (typ) of its nominal value any time after soft-start is complete, hiccup mode is triggered.

The MAX17546 has two modes of operation under overload conditions – the hiccup mode and the latchoff mode. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32768 clock

cycles. Once the hiccup timeout period expires, soft-start is attempted again. In latchoff mode, the converter does not attempt to soft-start the output after a timeout period. The power supply to the MAX17546 needs to be cycled to turn-on the part again in latchoff mode of operation. A resistor connected from DL to SGND sets the peak and runaway current limits and the operating mode during overload condition.

RESISTANCE (kΩ)	PEAK CURRENT LIMIT (A)	RUNAWAY CURRENT LIMIT (A)	FAULT OPERATING MODE
Open	7.8	8.8	Hiccup
174	7.8	8.8	Latchoff
61.9	7.2	8.2	Hiccup
26.1	7.2	8.2	Latchoff

$\overline{\text{RESET}}$ Output

The MAX17546 includes a $\overline{\text{RESET}}$ comparator to monitor the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high-impedance) 1024 switching cycles after the regulator output increases above 95.5% of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below 92.5% of the nominal regulated voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown.

Prebiased Output

When the MAX17546 starts into a prebiased output, both the high-side and the low-side switches are turned off so that the converter does not sink current from the output. High-side and low-side switches do not start switching until the PWM comparator commands the first PWM pulse, at which point switching commences. The output voltage is then smoothly ramped up to the target value in alignment with the internal reference.

Thermal Shutdown Protection

Thermal shutdown protection limits total power dissipation in the MAX17546. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The thermal sensor turns the device on again after the junction temperature cools by 10°C. Soft-start resets during thermal shutdown. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown in normal operation.

Applications Information

Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. The input capacitor RMS current requirement (I_{RMS}) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. I_{RMS} has a maximum value when the input voltage equals twice the output voltage (V_{IN} = 2 x V_{OUT}), so $I_{RMS(MAX)}$ = $I_{OUT(MAX)}/2$.

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high ripple current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{IN}}$$

where D = V_{OUT}/V_{IN} is the duty ratio of the controller, f_{SW} is the switching frequency, ΔV_{IN} is the allowable input voltage ripple, and η is the efficiency.

In applications where the source is located distant from the MAX17546 input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

Inductor Selection

Three key inductor parameters must be specified for operation with the MAX17546: inductance value (L), inductor saturation current (I_{SAT}), and DC resistance (R_{DCR}). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{V_{OUT}}{2.2 \times f_{SW}}$$

where V_{OUT} and f_{SW} are nominal values.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating (I_{SAT}) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value.

Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output voltage deviation is contained to 3% of the output voltage change. The minimum required output capacitance can be calculated as follows:

$$C_{OUT} = \frac{1}{2} \times \frac{I_{STEP} \times t_{RESPONSE}}{\Delta V_{OUT}}$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_C} + \frac{1}{f_{sw}}\right)$$

where I_{STEP} is the load current step, $t_{RESPONSE}$ is the response time of the controller, ΔV_{OUT} is the allowable output voltage deviation, f_C is the target closed-loop crossover frequency, and f_{SW} is the switching frequency. Select f_C to be 1/9th of f_{SW} if the switching frequency is less than or equal to 450kHz. If the switching frequency is more than 450kHz, select f_C to be 50kHz.

Soft-Start Capacitor Selection

The MAX17546 implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to SGND programs the soft-start time. The selected output capacitance (C_{SEL}) and the output voltage (V_{OUT}) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 28 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time (t_{SS}) is related to the capacitor connected at SS (C_{SS}) by the following equation:

$$t_{SS} = C_{SS}/(5.55 \times 10^{-6})$$

For example, to program a 4ms soft-start time, a 22nF capacitor should be connected from the SS pin to SGND.

Setting the Input Undervoltage Lockout Level

The MAX17546 offers an adjustable input undervoltage lockout level. Set the voltage at which MAX17546 turns on, with a resistive voltage-divider connected from V_{IN} to SGND. Connect the center node of the divider to EN/UVLO.

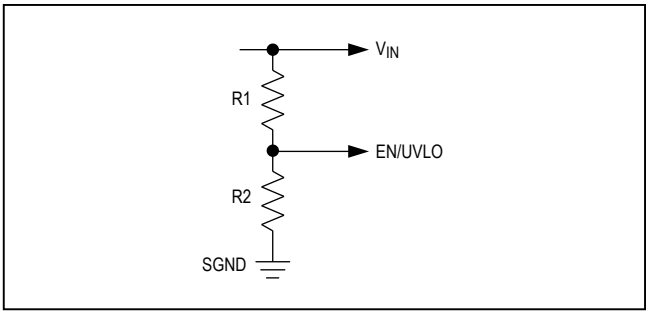


Figure 1. Setting the Input Undervoltage Lockout

Choose R1 to be 3.3MΩ and then calculate R2 as follows:

$$R2 = \frac{R1 \times 1.215}{(V_{INU} - 1.215)}$$

where V_{INU} is the voltage at which the MAX17546 is required to turn on. Ensure that V_{INU} is higher than 0.8 x V_{OUT}.

Loop Compensation

The MAX17546 is internally loop compensated. However, if the switching frequency is less than 450kHz, connect a 0402 capacitor (C6) between the CF pin and the FB pin. Use Table 2 to select the value of C6.

Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the positive terminal of the output capacitor (V_{OUT}) to SGND (see Figure 2). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R3 from the output to FB as follows:

$$R3 = \frac{451 \times 10^3}{f_C \times C_{OUT}}$$

where R3 is in kΩ, crossover frequency f_C is in kHz, and output capacitor C_{OUT} is in µF. Choose f_C to be 1/9th of the switching frequency, f_{SW}, if the switching frequency is less than or equal to 450kHz. If the switching frequency is more than 450kHz, select f_C to be 50kHz.

Calculate resistor R4 from FB to SGND as follows:

$$R4 = \frac{R3 \times 0.9}{(V_{OUT} - 0.9)}$$

Table 2. C6 Capacitor Value at Various Switching Frequencies

SWITCHING FREQUENCY RANGE (kHz)	C6 (pF)
200 to 300	2.2
300 to 450	1.2

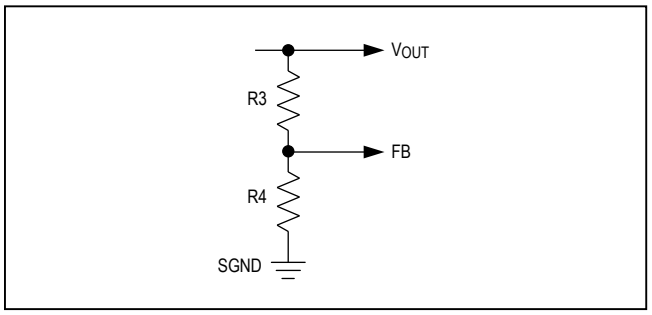


Figure 2. Setting the Output Voltage

Power Dissipation

Ensure that the junction temperature of the MAX17546 does not exceed +125°C under the operating conditions specified for the power supply.

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - (I_{OUT}^2 \times R_{DCR}) - (I_{OUT}^2 \times (1 - D) \times R_{LS}$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where, P_{OUT} is the total output power, η is the efficiency of the converter, R_{DCR} is the DC resistances of the inductor, R_{LS} is the on-resistance of the low-side external MOSFET and D = V_{OUT}/V_{IN} is the duty ratio of the converter. (See the typical operating characteristics curves for more information on efficiency at typical operating conditions).

For the MAX17546 EV kit, the thermal performance metrics for the package are given below:

$$\theta_{JA} = 23°C/W$$

$$\theta_{JC} = 2°C/W$$

The junction temperature of the MAX17546 can be estimated at any given maximum ambient temperature (T_{A_MAX}) from the equation below:

$$T_{J\_MAX} = T_{A\_MAX} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal management system that ensures that the exposed pad of the MAX17546 is maintained at a given temperature (T_{EP_MAX}) by using proper heat sinks, then the junction temperature of the MAX17546 can be estimated at any given maximum ambient temperature from the equation below:

$$T_{J\_MAX} = T_{EP\_MAX} + (\theta_{JC} \times P_{LOSS})$$

PCB Layout Guidelines

All connections carrying pulsed currents must be very short and as wide as possible. The inductance of these connections must be kept to an absolute minimum due to the high di/dt of the currents. Since inductance of a current carrying loop is proportional to the area enclosed by the loop, if the loop area is made very small, inductance is reduced. Additionally, small current loop areas reduce radiated EMI.

A ceramic input filter capacitor should be placed close to the V_{IN} pins of the IC. This eliminates as much trace inductance effects as possible and give the IC a cleaner voltage supply. A bypass capacitor for the V_{CC} pin also should be placed close to the pin to reduce effects of trace impedance.

When routing the circuitry around the IC, the analog small-signal ground and the power ground for switching currents must be kept separate. They should be connected together at a point where switching activity is at a minimum, typically the return terminal of the V_{CC} bypass capacitor. This helps keep the analog ground quiet. The ground plane should be kept continuous/unbroken as far as possible. No trace carrying high switching current should be placed directly over any ground plane discontinuity.

PCB layout also affects the thermal performance of the design. A number of thermal vias that connect to a large ground plane should be provided under the exposed pad of the part, for efficient heat dissipation.

For a sample layout that ensures first pass success, refer to the MAX17546 evaluation kit layout available at www.maximintegrated.com.

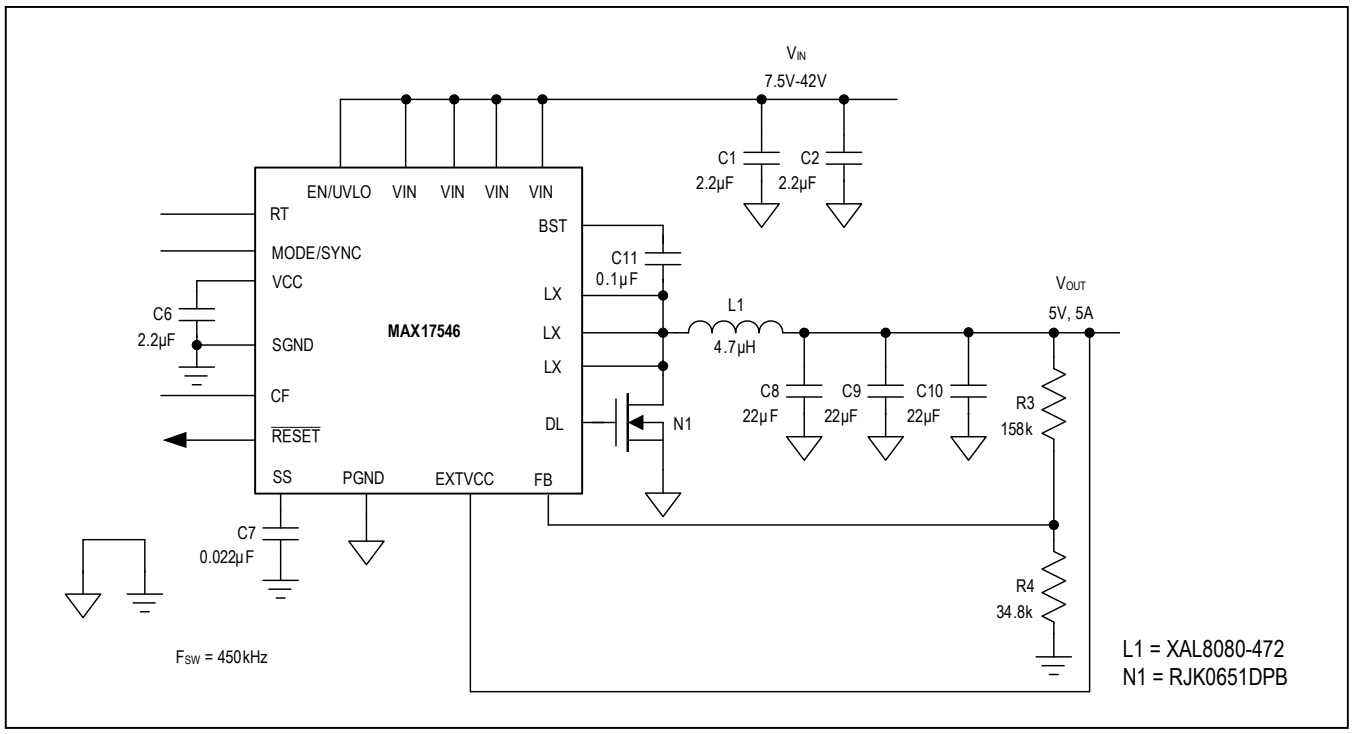


Figure 3. Typical Application Circuit for 5V Output

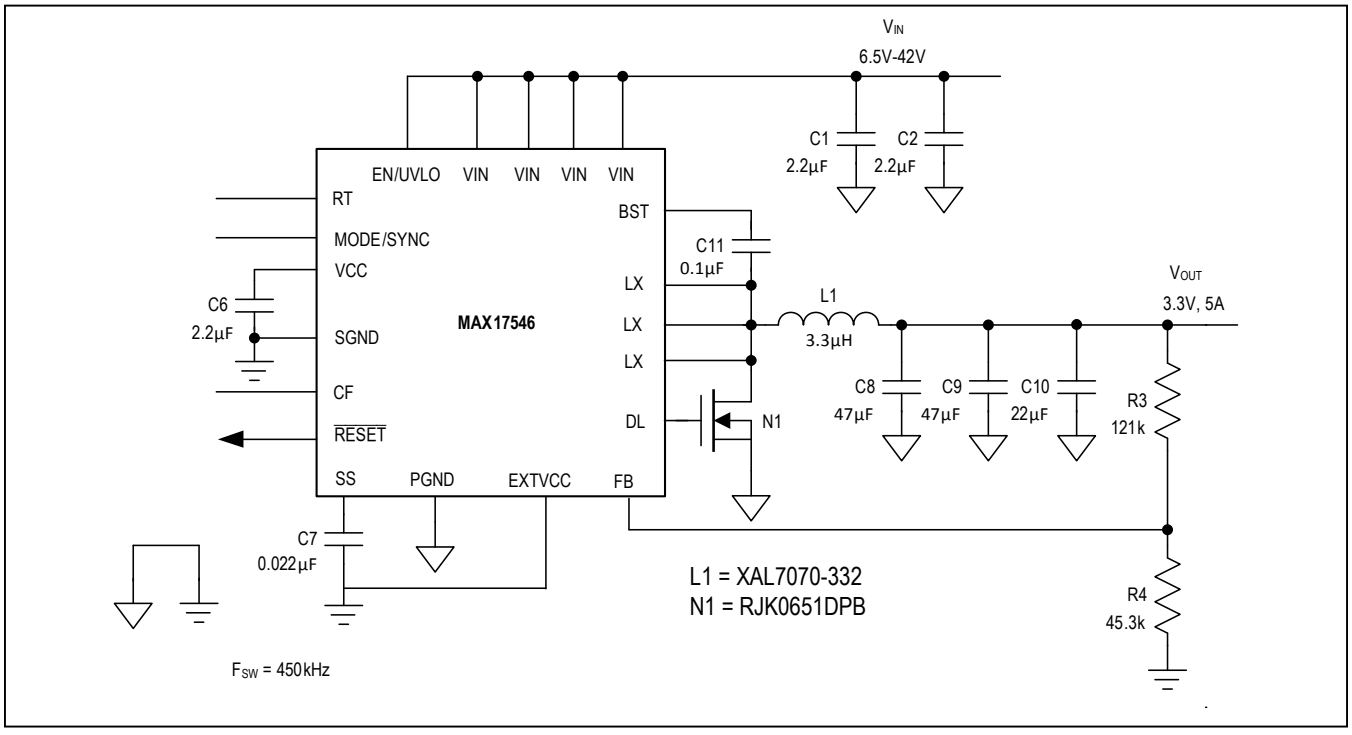


Figure 4. Typical Application Circuit for 3.3V Output

Ordering Information

PART	PIN-PACKAGE
MAX17546ATP+	20 TQFN 5mm x 5mm

Note: *All devices operate over the temperature range of -40ºC to +125ºC, unless otherwise noted.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
20 TQFN-EP*	T2055+4	21-0140	90-0009

**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/15	Initial release	—

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

