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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

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EVALUATION KIT AVAILABLE

Dual-Phase, Quick-PWM Controller for IMVP-6.5 CPU Core Power Supplies

MAX17582

General Description

The MAX17582 is a 2-/1-phase-interleaved Quick-PWM™ step-down VID power-supply controller for notebook CPUs. True out-of-phase operation reduces input-ripple-current requirements and output-voltage ripple, while easing component selection and layout difficulties. The Quick-PWM control provides instantaneous response to fast load-current steps. Active voltage positioning reduces power dissipation and bulk output capacitance requirements and allows ideal positioning compensation for tantalum, polymer, or ceramic bulk output capacitors.

A slew-rate controller allows controlled transitions among VID codes, controlled soft-start and shutdown, and controlled exit from suspend. A thermistor-based temperature sensor provides a programmable thermal-fault output ($\overline{VRHOT}$). A current-monitor output (IMON) provides an analog current output proportional to the power consumed by the CPU. The MAX17582 includes output undervoltage and thermal protection. When any of these protection features detect a fault, the controller shuts down. A voltage-regulator power-OK (PWRGD) output indicates the output is in regulation. Additionally, the MAX17582 features true differential current sense and a phase-good (PHASEGD) output that indicates a phase imbalance fault condition.

The MAX17582 implements the Intel IMVP-6.5 VID code set. The MAX17582 is available in a 6mm x 6mm, 48-pin TQFN package.

Applications

IMVP-6.5 Core Supply

Multiphase CPU Core Supply

Voltage-Positioned, Step-Down Converters

Notebook/Desktop Computers

Blade Servers

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX17582GTM+	-40°C to +105°C	48 TQFN-EP*

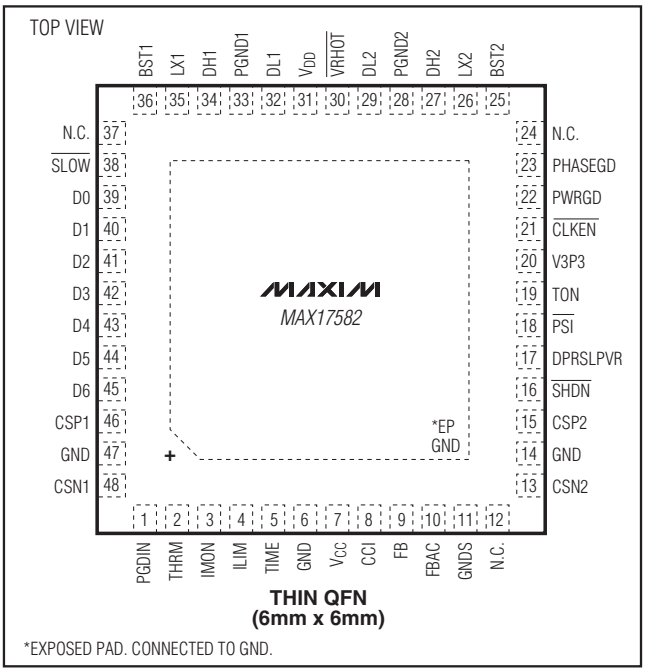
+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Quick-PWM is a trademark of Maxim Integrated Products, Inc.

Features

- **Single-/Dual-Phase, Quick-PWM Controller**
- **±8mV V_{OUT} Accuracy Over Line, Load, and Temperature**
- **7-Bit 0 to 1.50V VID Control**
- **Dynamic Phase Selection Optimizes Active/Sleep Efficiency**
- **Transient Phase Overlap Reduces Output Capacitance**
- **Integrated Boost Switches**
- **Active Voltage Positioning with Adjustable Gain**
- **Programmable 200kHz to 800kHz Switching Frequency**
- **Accurate Current Balance and Current Limit**
- **Adjustable Slew-Rate Control**
- **Power-Good, Clock Enable, and Thermal-Fault Outputs**
- **Phase Current Imbalance Fault Output**
- **Drives Large Synchronous Rectifier MOSFETs**
- **4V to 26V Battery Input-Voltage Range**
- **Undervoltage and Thermal-Fault Protection**
- **IMVP-6.5 Power Sequencing and Timing Compliant**
- **Soft-Startup and Soft-Shutdown**

Pin Configuration



Dual-Phase, Quick-PWM Controller for IMVP-6.5 CPU Core Power Supplies

ABSOLUTE MAXIMUM RATINGS

V_{CC}, V_{DD}, V3P3 to GND .....-0.3V to +6V
D0–D6 to GND.....-0.3V to +6V
PGDIN, DPRSLPVR, $\overline{PSI}$ to GND.....-0.3V to +6V
$\overline{SLOW}$ to GND .....-0.3V to +6V
CSP1, CSP2, CSN1, CSN2 to GND.....-0.3V to +6V
THRM, ILIM, PHASEGD to GND.....-0.3V to +6V
PWRGD, $\overline{VRHOT}$ to GND .....-0.3V to +6V
$\overline{CLKEN}$ to GND .....(-0.3V to V3P3) + 0.3V
FB, FBAC to GND.....(-0.3V to V_{CC}) + 0.3V
TIME, IMON, CCI to GND.....(-0.3V to V_{CC}) + 0.3V
PGND, GNDS to GND .....-0.3V to +0.3V
$\overline{SHDN}$ to GND (Note 1).....-0.3V to +16V
TON to GND .....-0.3V to +30V
DL1, DL2 to GND .....-0.3V to (V_{DD} + 0.3V)
BST1, BST2 to GND .....-0.3V to +36V
BST1, BST2 to V_{DD}.....-0.3V to +30V
LX1 to BST1.....-6V to +0.3V
LX2 to BST2.....-6V to +0.3V
DH1 to LX1 .....(-0.3V to V_{BST1}) + 0.3V
DH2 to LX2 .....(-0.3V to V_{BST2}) + 0.3V
Continuous Power Dissipation
6mm x 6mm, 48-Pin TQFN Up to +70°C 2105mW
(derate above +70°C) .....26.3mW/°C
Operating Temperature Range .....-40°C to +105°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +165°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: $\overline{SHDN}$ might be forced to 12V for the purpose of debugging prototype boards using the no-fault test mode, which disables fault protection and overlapping operation.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V3P3 = 3.3V, DPRSLPVR = GNDS = GND, V_{CSP1} = V_{CSN1} = V_{CSP2} = V_{CSN1} = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN1, D6–D0 = [0101000]; $V_{\overline{SLOW}}$ = 5V; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input-Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
		V3P3		3.0		3.6	
DC Output-Voltage Accuracy	V_{OUT}	Measured at FB with respect to GNDS; includes load-regulation error (Note 2)	DAC codes from 0.8125V to 1.5000V	-0.5		+0.5	%
			DAC codes from 0.3750V to 0.8000V	-7		+7	mV
			DAC codes from 0 to 0.3625V	-20		+20	
Boot Voltage	V_{BOOT}			1.094	1.100	1.106	V
Line Regulation Error		V_{CC} = 4.5V to 5.5V, V_{IN} = 4.5V to 26V			0.1		%
FB Input Bias Current		T_A = +25°C		-0.1		+0.1	µA
GNDS Input Range				-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97	1.00	1.03	V/V
GNDS Input Bias Current	I_{GNDS}	T_A = +25°C		-0.5		+0.5	µA
TIME Regulation Voltage	V_{TIME}	R_{TIME} = 71.5kΩ		1.985	2.000	2.015	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V3P3 = 3.3V, DPRSLPVR = GNDS = GND, V_{CSP1} = V_{CSN1} = V_{CSP2} = V_{CSN1} = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN1, D6–D0 = [0101000]; $V_{\overline{SLOW}}$ = 5V; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
TIME Slew-Rate Accuracy		R_{TIME} = 71.5kΩ (12.5mV/µs nominal)		-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)		-15		+15	
		Soft-start and soft-shutdown: R_{TIME} = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal)		-25		+25	
		Slow: $V_{\overline{SLOW}}$ = 0V, 1/2 of nominal slew rate, R_{TIME} = 71.5kΩ (6.25mV/µs nominal)		-15		+15	
		Slow: $V_{\overline{SLOW}}$ = 0V, 1/2 of nominal slew rate, R_{TIME} = 35.7kΩ (12.5mV/µs nominal) to 178kΩ (2.5mV/µs nominal)		-15		+15	
On-Time	t_{ON}	Measured at DH_ (Note 3)	R_{TON} = 96.75kΩ (600kHz per phase), 167ns nominal	-15		+15	%
			R_{TON} = 200kΩ (300kHz per phase), 333ns nominal	-10		+10	
			R_{TON} = 303.25kΩ (200kHz per phase), 500ns nominal	-15		+15	
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH_ (Note 3)			300	350	ns
TON Shutdown Input Current	$I_{RTON,SDN}$	$\overline{SHDN}$ = GND, V_{IN} = 26V, V_{CC} = V_{DD} = 0V or 5V, T_A = +25°C			0.01	0.1	µA
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, $V_{DPRSLPVR}$ = 5V, FB forced above the regulation point			2.5	5	mA
Quiescent Supply Current (V_{DD})	I_{DD}	Measured at V_{DD}, $V_{DPRSLPVR}$ = 0V, FB forced above the regulation point, T_A = +25°C			0.02	1	µA
Quiescent Supply Current (V3P3)	I_{3P3}	Measured at V3P3, FB forced within the $\overline{CLKEN}$ power-good window			2	4	µA
Shutdown Supply Current (V_{CC})	$I_{CC,SDN}$	Measured at V_{CC}, $\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
Shutdown Supply Current (V_{DD})	$I_{DD,SDN}$	Measured at V_{DD}, $\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA
Shutdown Supply Current (V3P3)	$I_{3P3,SDN}$	Measured at V3P3, $\overline{SHDN}$ = GND, T_A = +25°C			0.01	1	µA

Dual-Phase, Quick-PWM Controller for IMVP-6.5 CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V3P3 = 3.3V, DPRSLPVR = GNDS = GND, V_{CSP1} = V_{CSN1} = V_{CSP2} = V_{CSN1} = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN1, D6–D0 = [0101000]; $V_{\overline{SLOW}}$ = 5V; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT PROTECTION							
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to the voltage target set by the VID code; see Table 4		-450	-400	-350	mV
Output Undervoltage-Propagation Delay	t_{UVP}	FB forced 25mV below trip threshold			10		µs
$\overline{CLKEN}$ Startup Delay and Boot Time Period	t_{BOOT}	Measured from the time when FB reaches the boot target voltage (Note 2)		20	60	100	µs
PWRGD Startup Delay		Measured at startup from the time when $\overline{CLKEN}$ goes low		3	6.5	10	ms
$\overline{CLKEN}$ and PWRGD Threshold		Measured at FB with respect to the voltage target set by the VID code; see Table 4, 20mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350	-300	-250	mV
			Upper threshold, rising edge (overvoltage)	+150	+200	+250	
$\overline{CLKEN}$ and PWRGD Delay		FB forced 25mV outside the PWRGD trip thresholds			10		µs
PHASEGD Delay		$V_{(CCI,FB)}$ forced 25mV outside trip thresholds			10		µs
$\overline{CLKEN}$, PWRGD, and PHASEGD Transition Blanking Time (VID Transitions)	t_{BLANK}	Measured from the time when FB reaches the target voltage (Note 2)			20		µs
PHASEGD Transition Blanking Time (Phase 2 Enable Transitions)		Number of DH2 pulses for which PHASEGD is blanked after phase 2 is enabled			32		Pulses
$\overline{CLKEN}$ Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
$\overline{CLKEN}$ Output High Voltage		High state, I_{SOURCE} = 3mA		V3P3 - 0.4			V
PWRGD, PHASEGD Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
PWRGD, PHASEGD Leakage Current		High-impedance state, PWRGD, PHASEGD forced to 5V, T_A = +25°C				1	µA
CSN1 Pulldown Resistance in Shutdown		$\overline{SHDN}$ = 0, measured after soft-shutdown completed (DL_ = low)			10		Ω
V_{CC} Undervoltage Lockout (UVLO) Threshold	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level		4.05	4.27	4.48	V

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V3P3 = 3.3V, DPRSLPVR = GNDS = GND, V_{CSP1} = V_{CSN1} = V_{CSP2} = V_{CSN1} = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN1, D6–D0 = [0101000]; $V_{\overline{SLOW}}$ = 5V; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
THERMAL PROTECTION							
$\overline{VRHOT}$ Trip Threshold		Measured at THRM as a percentage of V_{CC}, falling edge, typical hysteresis = 75mV		29	30	31	%
$\overline{VRHOT}$ Delay	$t_{\overline{VRHOT}}$	THRM forced 25mV below the $\overline{VRHOT}$ trip threshold, falling edge			10		µs
$\overline{VRHOT}$ Output On-Resistance	$R_{ON(\overline{VRHOT})}$	Low state			2	10	Ω
$\overline{VRHOT}$ Leakage Current		High-impedance state, $\overline{VRHOT}$ forced to 5V, T_A = +25°C				1	µA
THRM Input Leakage	I_{THRM}	V_{THRM} = 0 to 5V, T_A = +25°C		-0.1		+0.1	µA
Thermal-Shutdown Threshold	T_{SHDN}	Typical hysteresis = 15°C			160		°C
VALLEY CURRENT LIMIT, DROOP, AND CURRENT BALANCE							
Current-Limit Threshold Voltage (Positive)	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$	V_{TIME} - V_{ILIM} = 100mV	7	10	13	mV
			V_{TIME} - V_{ILIM} = 500mV	45	50	55	
			ILIM = V_{CC}	20	22.5	25	
Current-Limit Threshold Voltage (Negative) Accuracy	$V_{LIMIT(NEG)}$	$V_{CSP\_}$ - $V_{CSN\_}$, nominally -125% of V_{LIMIT}		-4		+4	mV
Current-Limit Threshold Voltage (Zero Crossing)	V_{ZERO}	V_{GND} - $V_{LX\_}$, DPRSLPVR = 5V			1		mV
CSP_, CSN_ Common-Mode Input Range				0		2	V
Phase 2 Disable Threshold		Measured at CSP2		3	V_{CC} - 1	V_{CC} - 0.4	V
CSP_, CSN_ Input Current	$I_{CSP\_}$, $I_{CSN\_}$	T_A = +25°C		-0.2		+0.2	µA
ILIM Input Current	I_{ILIM}	T_A = +25°C		-0.1		+0.1	µA
Droop Amplifier Offset		(1/N) x Σ ($V_{CSP\_}$ - $V_{CSN\_}$) at I_{FBAC} = 0; Σ indicates summation over all phases from 1 to N, N = 2	T_A = +25°C	-0.5		+0.5	mV/ phase
			T_A = 0°C to +85°C	-0.75		+0.75	
Droop Amplifier Transconductance	$G_{m(FBAC)}$	$\Delta I_{FBAC}/\Delta[\Sigma (V_{CSP\_} - V_{CSN\_})]$; Σ indicates summation over all phases from 1 to N, N = 2, V_{FBAC} = V_{CSN-} = 0.45V to 2V		590	600	608	µS
Current-Balance Amplifier Offset		(V_{CSP1} - V_{CSN1}) - (V_{CSP2} - V_{CSN2}) at I_{CCI} = 0V		-1.0		+1.0	mV
Current-Balance Amplifier Transconductance	$G_{m(CCI)}$	$I_{CCI}/[(V_{CSP1} - V_{CSN1}) - (V_{CSP2} - V_{CSN2})]$			200		µS

Dual-Phase, Quick-PWM Controller for IMVP-6.5 CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V3P3 = 3.3V, DPRSLPVR = GNDS = GND, V_{CSP1} = V_{CSN1} = V_{CSP2} = V_{CSN1} = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN1, D6–D0 = [0101000]; $V_{\overline{SLOW}}$ = 5V; **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT MONITOR							
Current-Monitor Output Current at Full Load Condition	I_{IMON}	V_{CSP1} - V_{CSN1} = V_{CSP2} - V_{CSN2} = 20mV, $V_{CSN\_}$ = 0.45V to 2.0V		93.12	96	98.88	µA
Current-Monitor Transconductance	$G_{m(IMON)}$	$\Delta I_{IMON}/\Delta[\Sigma (V_{CSP\_} - V_{CSN\_})]$; Σ indicates summation over all phases from 1 to N, N = 2, CSN_ = 0.45V to 2V		2.2	2.4	2.6	mS
IMON Clamp Voltage	$V_{IMON,MAX}$	I_{SINK} = 10mA		1.05	1.10	1.15	V
IMON Pulldown Resistance in Shutdown		$\overline{SHDN}$ = 0, measured after soft-shutdown completed (DL_ = low)			10		Ω
GATE DRIVERS							
DH_ Gate Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V	High state (pullup)		0.9	2.5	Ω
			Low state (pulldown)		0.7	2.0	
DL_ Gate Driver On-Resistance	$R_{ON(DL\_)}$		High state (pullup)		0.7	2.0	Ω
			Low state (pulldown)		0.25	0.7	
DH_ Gate Driver Source Current	$I_{DH\_(SOURCE)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.2		A
DH_ Gate Driver Sink Current	$I_{DH\_(SINK)}$	DH_ forced to 2.5V, BST_ - LX_ forced to 5V			2.7		A
DL_ Gate Driver Source Current	$I_{DL\_(SOURCE)}$	DL_ forced to 2.5V			2.7		A
DL_ Gate Driver Sink Current	$I_{DL\_(SINK)}$	DL_ forced to 2.5V			8		A
Internal BST_ Switch On-Resistance	$R_{ON(BST\_)}$				10	20	Ω
LOGIC AND I/O							
Logic Input High Voltage	V_{IH}	$\overline{SHDN}$, PGDIN		2.3			V
Logic Input Low Voltage	V_{IL}	$\overline{SHDN}$, PGDIN				1.0	V
$\overline{SHDN}$ No-Fault Level		To enable no-fault mode		11		13	V
Low-Voltage Logic Input High Voltage	V_{IHLV}	$\overline{PSI}$, D0–D6; DPRSLPVR, $\overline{SLOW}$		0.67			V
Low-Voltage Logic Input Low Voltage	V_{ILLV}	$\overline{PSI}$, D0–D6; DPRSLPVR, $\overline{SLOW}$				0.33	V
Logic Input Current		T_A = +25°C, $\overline{SHDN}$, DPRSLPVR, PGDIN, $\overline{PSI}$, $\overline{SLOW}$, D0–D6 = 0 or 5V		-1		+1	µA

ELECTRICAL CHARACTERISTICS

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V3P3 = 3.3V, DPRSLPVR = GNDS = GND, V_{CSP1} = V_{CSN1} = V_{CSP2} = V_{CSN2} = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN1, D6–D0 = [0101000]; $V_{\overline{SLOW}}$ = 5V; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
PWM CONTROLLER							
Input-Voltage Range		V_{CC}, V_{DD}		4.5		5.5	V
		V3P3		3.0		3.6	
DC Output-Voltage Accuracy	V_{OUT}	Measured at FB with respect to GNDS; includes load-regulation error (Note 2)	DAC codes from 0.8125V to 1.5000V	-0.75		+0.75	%
			DAC codes from 0.3750V to 0.8000V	-10		+10	mV
			DAC codes from 0 to 0.3625V	-25		+25	
Boot Voltage	V_{BOOT}			1.09		1.11	V
GNDS Input Range				-200		+200	mV
GNDS Gain	A_{GNDS}	$\Delta V_{OUT}/\Delta V_{GNDS}$		0.97		1.03	V/V
TIME Regulation Voltage	V_{TIME}	R_{TIME} = 71.5kΩ		1.985		2.015	V
TIME Slew-Rate Accuracy		R_{TIME} = 71.5kΩ (12.5mV/µs nominal)		-10		+10	%
		R_{TIME} = 35.7kΩ (25mV/µs nominal) to 178kΩ (5mV/µs nominal)		-15		+15	
		Soft-start and soft-shutdown: R_{TIME} = 35.7kΩ (3.125mV/µs nominal) to 178kΩ (0.625mV/µs nominal)		-25		+25	
		Slow: $V_{\overline{SLOW}}$ = 0V, 1/2 of nominal slew rate, R_{TIME} = 71.5kΩ (6.25mV/µs nominal)		-15		+15	
		Slow: $V_{\overline{SLOW}}$ = 0V, 1/2 of nominal slew rate, R_{TIME} = 35.7kΩ (12.5mV/µs nominal) to 178kΩ (2.5mV/µs nominal)		-17		+17	
On-Time	t_{ON}	Measured at DH_ (Note 3)	R_{TON} = 96.75kΩ (600kHz per phase), 167ns nominal	-15		+15	%
			R_{TON} = 200kΩ (300kHz per phase), 333ns nominal	-15		+15	
			R_{TON} = 303.25kΩ (200kHz per phase), 500ns nominal	-15		+15	
Minimum Off-Time	$t_{OFF(MIN)}$	Measured at DH_ (Note 3)				350	ns
BIAS CURRENTS							
Quiescent Supply Current (V_{CC})	I_{CC}	Measured at V_{CC}, $V_{DPRSLPVR}$ = 5V, FB forced above the regulation point				5	mA
Quiescent Supply Current (V3P3)	I_{3P3}	Measured at V3P3, FB forced within the $\overline{CLKEN}$ power-good window				4	µA

Dual-Phase, Quick-PWM Controller for IMVP-6.5 CPU Core Power Supplies

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V3P3 = 3.3V, DPRSLPVR = GNDS = GND, V_{CSP1} = V_{CSN1} = V_{CSP2} = V_{CSN2} = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN1, D6–D0 = [0101000]; $V_{\overline{SLOW}}$ = 5V; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
FAULT PROTECTION							
Output Undervoltage-Protection Threshold	V_{UVP}	Measured at FB with respect to the voltage target set by the VID code; see Table 4		-450		-350	mV
$\overline{CLKEN}$ Startup Delay and Boot Time Period	t_{BOOT}	Measured from the time when FB reaches the boot target voltage (Note 3)		20		100	µs
PWRGD Startup Delay		Measured at startup from the time when $\overline{CLKEN}$ goes low		3		10	ms
$\overline{CLKEN}$ and PWRGD Threshold		Measured at FB with respect to the voltage target set by the VID code; see Table 4, 20mV hysteresis (typ)	Lower threshold, falling edge (undervoltage)	-350		-250	mV
			Upper threshold, rising edge (overvoltage)	+150		+250	
$\overline{CLKEN}$ Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
$\overline{CLKEN}$ Output High Voltage		High state, I_{SOURCE} = 3mA		V3P3 - 0.4			V
PWRGD, PHASEGD Output Low Voltage		Low state, I_{SINK} = 3mA				0.4	V
V_{CC} Undervoltage-Lockout Threshold (UVLO)	$V_{UVLO(VCC)}$	Rising edge, 65mV typical hysteresis, controller disabled below this level		4.0		4.5	V
THERMAL PROTECTION							
$\overline{VRHOT}$ Trip Threshold		Measured at THRM as a percentage of V_{CC}, falling edge, typical hysteresis = 75mV		28		32	%
$\overline{VRHOT}$ Output On-Resistance	$R_{ON(\overline{VRHOT})}$	Low state				10	Ω
VALLEY CURRENT LIMIT, DROOP, AND CURRENT BALANCE							
Current-Limit Threshold Voltage (Positive)	V_{LIMIT}	$V_{CSP\_}$ - $V_{CSN\_}$	V_{TIME} - V_{ILIM} = 100mV	7		13	mV
			V_{TIME} - V_{ILIM} = 500mV	40		60	
			ILIM = V_{CC}	19		26	
CSP_, CSN_ Common-Mode Input Range				0		2	V
Droop Amplifier Transconductance	$G_{m(FBAC)}$	$\Delta I_{FBAC}/\Delta[\Sigma(V_{CSP\_} - V_{CSN\_})]$, Σ indicates summation over all phases from 1 to N, N = 2, V_{FBAC} = V_{CSN-} = 0.45V to 2V		585		610	µS
Current-Balance Amplifier Offset		(V_{CSP1} - V_{CSN1}) - (V_{CSP2} - V_{CSN2}) at I_{CCI} = 0V		-1.25		+1.25	mV

ELECTRICAL CHARACTERISTICS (continued)

(Circuit of Figure 1, V_{IN} = 10V, V_{CC} = V_{DD} = $V_{\overline{SHDN}}$ = V_{PGDIN} = $V_{\overline{PSI}}$ = V_{ILIM} = 5V, V3P3 = 3.3V, DPRSLPVR = GNDS = GND, V_{CSP1} = V_{CSN1} = V_{CSP2} = V_{CSN2} = 1.0000V, FB = FBAC, R_{FBAC} = 3.57kΩ from FBAC to CSN1, D6–D0 = [0101000]; $V_{\overline{SLOW}}$ = 5V; **T_A = -40°C to +105°C**, unless otherwise noted.) (Note 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
CURRENT MONITOR							
Current-Monitor Transconductance	$G_{m(IMON)}$	$\Delta I_{IMON}/\Delta[\Sigma(V_{CSP\_} - V_{CSN\_})]$, Σ indicates summation over all phases from 1 to N, N = 2, $V_{CSN\_}$ = 0.45V to 2V		2.2		2.6	mS
IMON Clamp Voltage	$V_{IMON,MAX}$	I_{SINK} = 10mA		1.05		1.15	V
GATE DRIVERS							
DH_ Gate Driver On-Resistance	$R_{ON(DH\_)}$	BST_ - LX_ forced to 5V	High state (pullup)			2.5	Ω
			Low state (pulldown)			2.0	
DL_ Gate Driver On-Resistance	$R_{ON(DL\_)}$		High state (pullup)			2.0	Ω
			Low state (pulldown)			0.7	
LOGIC AND I/O							
Logic Input High Voltage	V_{IH}	$\overline{SHDN}$, PGDIN		2.3			V
Logic Input Low Voltage	V_{IL}	$\overline{SHDN}$, PGDIN				1.0	V
Low-Voltage Logic Input High Voltage	V_{IHLV}	$\overline{PSI}$, D0–D6: DPRSLPVR, $\overline{SLOW}$		0.67			V
Low-Voltage Logic Input Low Voltage	V_{ILLV}	$\overline{PSI}$, D0–D6: DPRSLPVR, $\overline{SLOW}$				0.33	V

Note 2: When pulse skipping, the output rises by approximately 1.5% when transitioning from continuous conduction to no load.

Note 3: On-time and minimum off-time specifications are measured from 50% to 50% at the DH_ and DL_ pins, with LX_ forced to GND, BST_ forced to 5V, and a 500pF capacitor from DH_ to LX_ to simulate external MOSFET gate capacitance. Actual in-circuit times might be different due to MOSFET switching speeds.

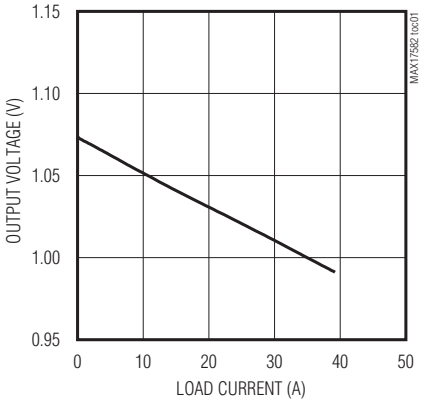
Note 4: Specifications to T_A = -40°C and +105°C are guaranteed by design and are not production tested.

Dual-Phase, Quick-PWM Controller for IMVP-6.5 CPU Core Power Supplies

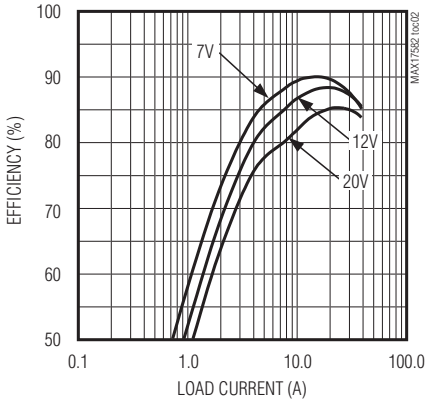
Typical Operating Characteristics

(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 1.075V, T_A = +25°C, unless otherwise specified.)

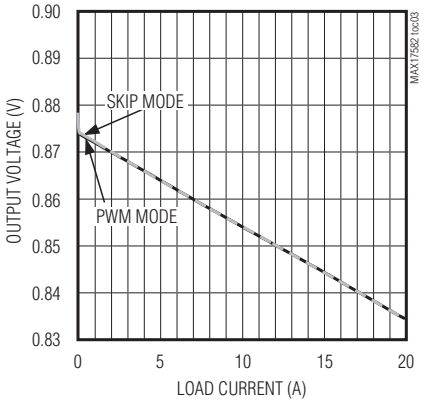
OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 1.075V)



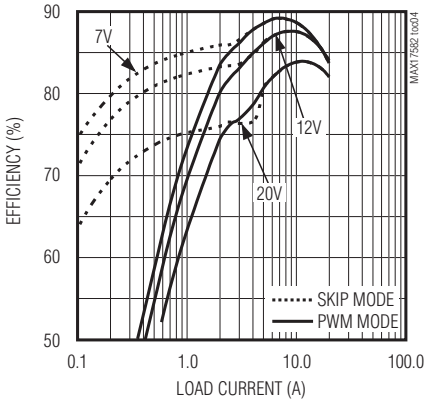
EFFICIENCY vs. LOAD CURRENT ($V_{OUT(HFM)}$ = 1.075V)



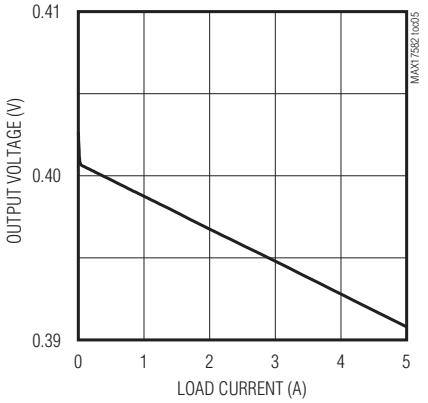
OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(LFM)}$ = 0.875V)



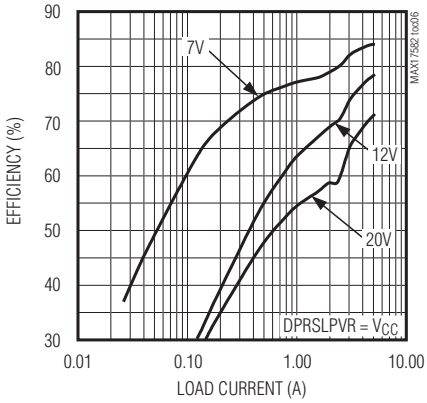
EFFICIENCY vs. LOAD CURRENT ($V_{OUT(LFM)}$ = 0.875V)



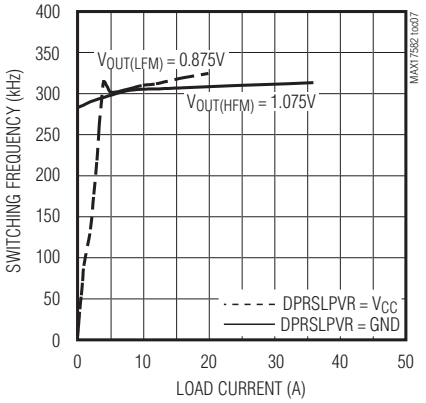
OUTPUT VOLTAGE vs. LOAD CURRENT ($V_{OUT(C4)}$ = 0.4V)



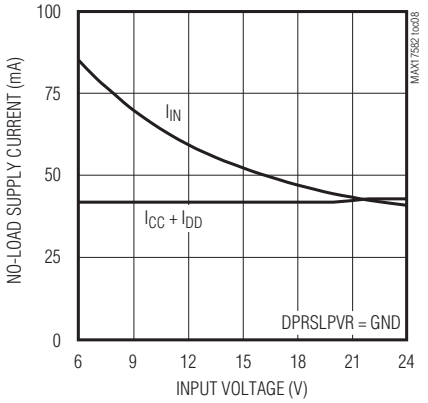
EFFICIENCY vs. LOAD CURRENT ($V_{OUT(C4)}$ = 0.4V)



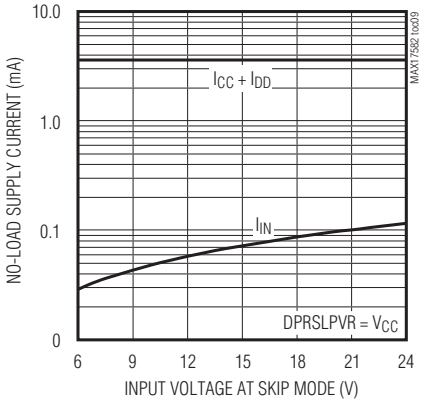
SWITCHING FREQUENCY vs. LOAD CURRENT



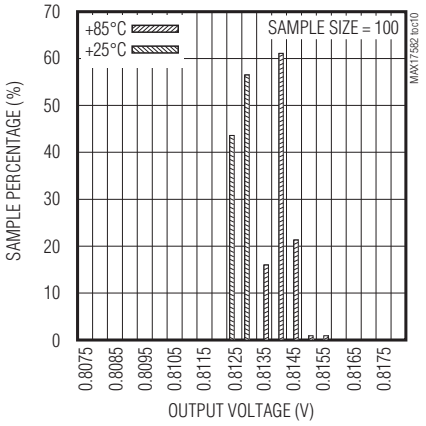
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE ($V_{OUT(HFM)}$ = 1.075V)



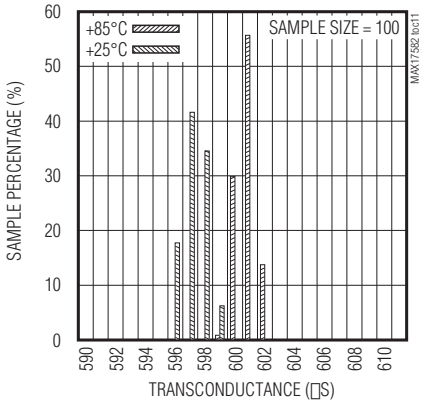
NO-LOAD SUPPLY CURRENT vs. INPUT VOLTAGE AT SKIP MODE ($V_{OUT(HFM)}$ = 1.075V)



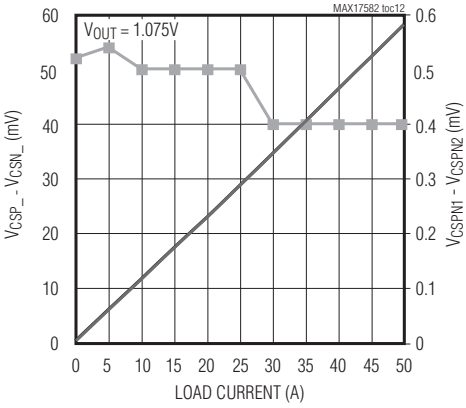
0.8125V OUTPUT-VOLTAGE DISTRIBUTION



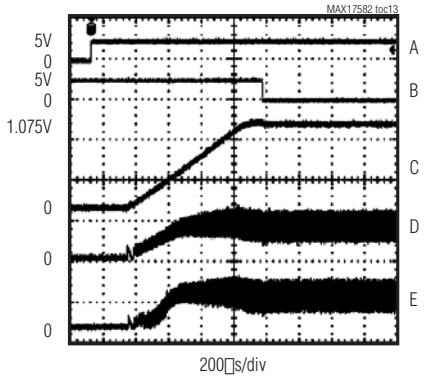
$G_{m(FB)}$ TRANSCONDUCTANCE DISTRIBUTION



CURRENT BALANCE vs. LOAD CURRENT

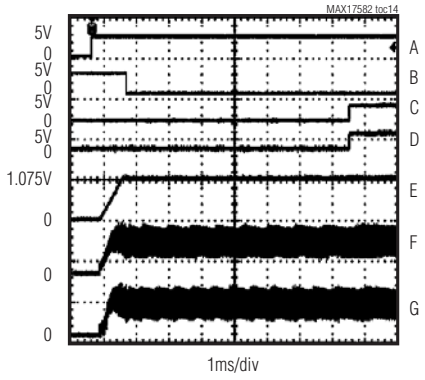


SOFT-START WAVEFORM (UP TO $\overline{CLKEN}$)



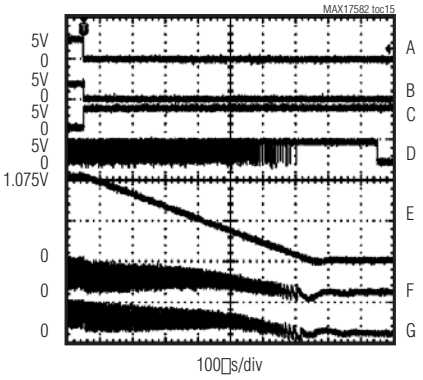
A. SHDN, 10V/div
B. $\overline{CLKEN}$, 10V/div
C. V_{OUT}, 500mV/div
D. I_{LX1}, 10A/div
E. I_{LX2}, 10A/div
I_{OUT} = 15A

SOFT-START WAVEFORM (UP TO PWRGD)



A. SHDN, 10V/div
B. PWRGD, 10V/div
C. PHASEGD, 10V/div
D. $\overline{CLKEN}$, 10V/div
E. V_{OUT}, 1V/div
F. I_{LX1}, 10A/div
G. I_{LX2}, 10A/div
I_{OUT} = 15A

SHUTDOWN WAVEFORM



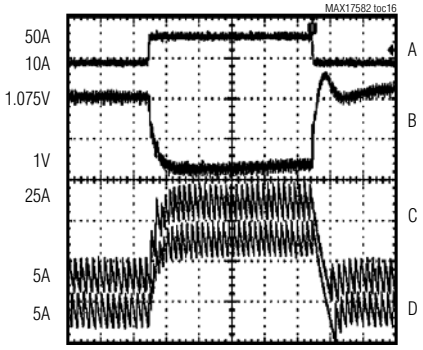
A. SHDN, 10V/div
B. $\overline{CLKEN}$, 10V/div
C. PWRGD, 10V/div
D. DL_, 10V/div
E. V_{OUT}, 500mV/div
F. I_{LX1}, 10A/div
G. I_{LX2}, 10A/div

Dual-Phase, Quick-PWM Controller for IMVP-6.5 CPU Core Power Supplies

Typical Operating Characteristics (continued)

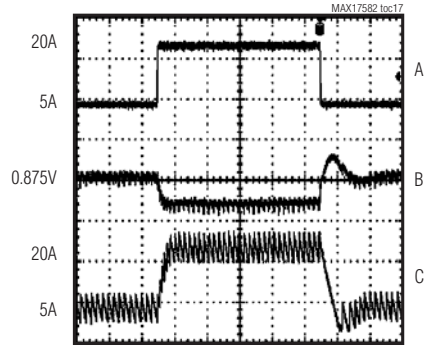
(Circuit of Figure 1. V_{IN} = 12V, V_{CC} = V_{DD} = 5V, $\overline{SHDN}$ = V_{CC}, D0–D6 set for 1.075V, T_A = +25°C, unless otherwise specified.)

LOAD-TRANSIENT RESPONSE (HFM MODE)



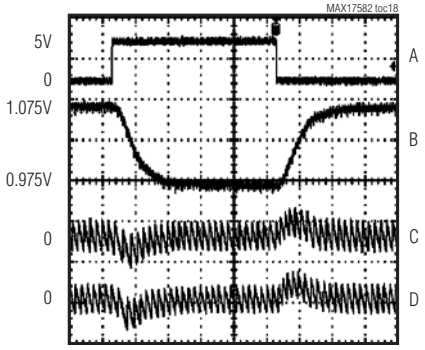
A. I_{OUT} = 10A TO 50A
B. V_{OUT}, 50mV/div
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

LOAD-TRANSIENT RESPONSE (LFM MODE)



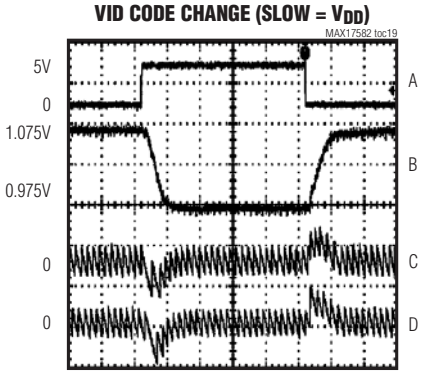
A. I_{OUT} = 5A TO 20A
B. V_{OUT}, 50mV/div
C. INDUCTOR CURRENT, 10A/div

VID CODE CHANGE (SLOW = GND)



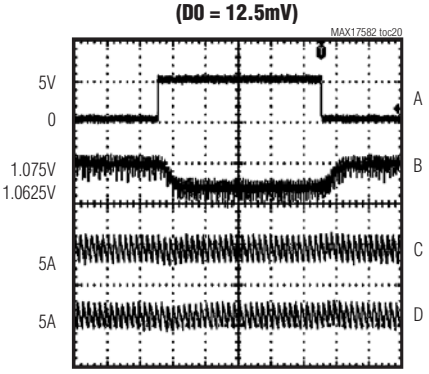
A. VID3, 5V/div
B. V_{OUT}, 50mV/div
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

VID CODE CHANGE (SLOW = V_{DD})



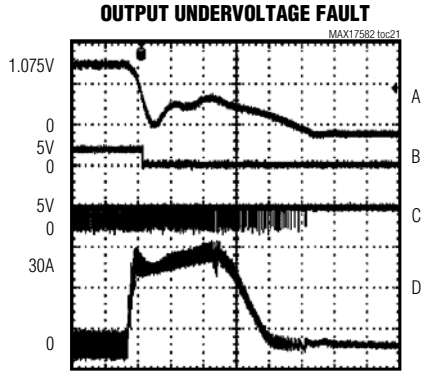
A. VID3, 5V/div
B. V_{OUT}, 50mV/div
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

DYNAMIC VID CODE CHANGE (D0 = 12.5mV)



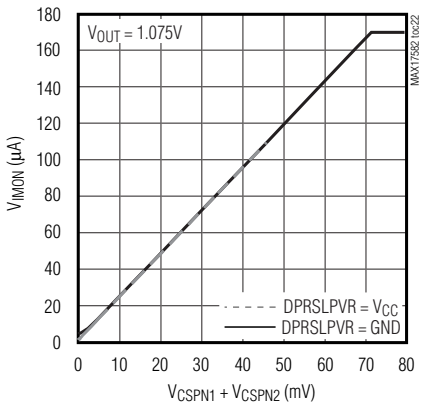
A. D0, 5V/div
B. V_{OUT}, 20mV/div
I_{OUT} = 10A
C. I_{LX1}, 10A/div
D. I_{LX2}, 10A/div

OUTPUT UNDERVOLTAGE FAULT

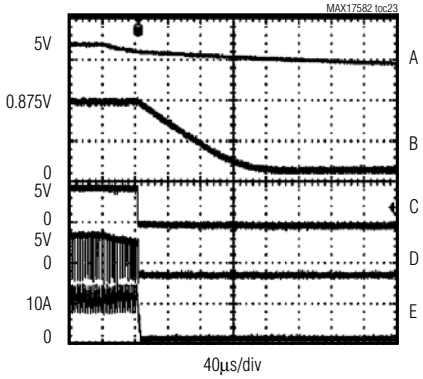


A. V_{OUT}, 500mV/div
B. PWRGD, 10V/div
C. DL_, 10V/div
D. I_{LX1}, 15A/div

V_{IMON} vs. LOAD CURRENT



BIAS SUPPLY REMOVAL (UVLO RESPONSE)



A. 5V BIAS SUPPLY, 5V/div
B. V_{OUT}, 500mV/div
C. PWRGD, 5V/div
D. DL_, 5V/div
E. I_{LX1}, 10A/div
I_{OUT} = 10A

Pin Description

PIN	NAME	FUNCTION
1	PGDIN	System Power-Good Logic Input. PGDIN indicates the power status of other system rails and is used for power-supply sequencing. After power-up to the boot voltage, the output voltage remains at V_{BOOT}, $\overline{CLKEN}$ remains high, and PWRGD remains low as long as PGDIN stays low. When PGDIN is pulled high, the output transitions to the selected VID voltage, and $\overline{CLKEN}$ is pulled low. If the system pulls PGDIN low during normal operation, the MAX17582 immediately drives $\overline{CLKEN}$ high, pulls PWRGD low, and slews the output to the boot voltage (using two-phase pulse-skipping mode). The controller remains at the boot voltage until PGDIN goes high again, $\overline{SHDN}$ is toggled, or the V_{CC} input power supply is cycled.
2	THRM	Input of Internal Comparator. Connect the output of a resistor- and thermistor-divider (between V_{CC} and GND) to THRM. Select the components such that the voltage at THRM falls below 1.5V (30% of V_{CC}) at the desired high temperature.
3	IMON	Current-Monitor Output. The MAX17582 IMON output sources a current that is directly proportional to the current-sense voltage as defined by: $I_{IMON} = G_{m(IMON)} \times (V_{CSP\_} - V_{CSN\_})$ where $G_{m(IMON)}$ = 5mS (typ). The IMON current is unidirectional (sources current out of IMON only) for positive current-sense values. For negative current-sense voltages, the IMON current is zero. Connect an external resistor between IMON and GNDS to create the desired IMON gain based on the following equation: $R_{IMON} = 0.9V/(IMAX \times R_{SENSE(MIN)} \times G_{m(IMON\_MIN)})$ where IMAX is defined in the *Current Monitor* section of the Intel IMVP-6.5 specification and based on discrete increments (20A, 30A, 40A, etc.), $R_{SENSE(MIN)}$ is the minimum effective value of the current-sense element (sense resistor or inductor DCR) that is used to provide the current-sense voltage, and $G_{m(IMON\_MIN)}$ is the minimum transconductance amplifier gain as defined in the *Electrical Characteristics* table. The IMON voltage is internally clamped to a maximum of 1.1V (typ). The transconductance amplifier and voltage clamp are internally compensated, so IMON cannot directly drive large capacitance values. To filter the IMON signal, use an RC filter as shown in Figure 1. IMON is pulled to ground when the MAX17582 is in shutdown.
4	ILIM	Valley Current-Limit Adjustment Input. The valley current-limit threshold voltage at CSP_ to CSN_ equals precisely 1/10 of the differential TIME to ILIM voltage over a 0.1V to 0.5V range (10mV to 50mV current-sense range). The negative current-limit threshold is nominally -125% of the corresponding valley current-limit threshold. Connect ILIM directly to V_{CC} to set the default current-limit threshold setting of 22.5mV (typ) nominal.
5	TIME	Slew-Rate Adjustment. TIME regulates to 2.0V and the load current determines the slew rate of the internal error-amplifier target. The sum of the resistance between TIME and GND (R_{TIME}) determines the nominal slew-rate: SLEW RATE = (12.5mV/µs) x (71.5kΩ/R_{TIME}) The guaranteed R_{TIME} range is between 35.7kΩ and 178kΩ. This “nominal” slew rate applies to VID transitions and to the transition from boot mode to VID. If the VID DAC inputs are clocked, the slew rate for all other VID transitions is set by the rate at which they are clocked, up to a maximum slew rate equal to the nominal slew rate defined above. The startup and shutdown slew rates are always 1/8 of nominal slew rate in order to minimize surge currents. If $\overline{SLOW}$ is low, then the slew rate is reduced to 1/2 of nominal.
6, 14, 47	GND	Analog Ground
7	V_{CC}	Controller Analog Bias Supply Voltage. Connect to a 4.5V to 5.5V source. Bypass to GND with 1µF minimum.
8	CCI	Current-Balance Compensation. Connect a 470pF capacitor between CCI and the positive side of the feedback remote sense. CCI is internally forced low in shutdown.

Dual-Phase, Quick-PWM Controller for IMVP-6.5 CPU Core Power Supplies

Pin Description (continued)

PIN	NAME	FUNCTION
9	FB	Remote Feedback-Sense Input. Normally shorted to FBAC and connected to the VCC_SENSE pin of the CPU socket through the load-line gain resistor (see the FBAC pin description). FB internally connects to the error amplifier and integrator.
10	FBAC	Voltage-Positioning Transconductance Amplifier Output. Connect a resistor R_{FB} between FBAC and the positive side of the feedback remote sense to set the DC steady-state droop based on the voltage-positioning gain requirement: $R_{FB} = R_{DROOP}/(R_{SENSE} \times G_{m(FBAC)})$ where R_{DROOP} is the desired voltage-positioning slope and $G_{m(FBAC)}$ = 600µS (typ). R_{SENSE} is the value of the current-sense resistors that are used to provide the (CSP_, CSN_) current-sense voltages. If lossless sensing is used, $R_{SENSE} = R_L$. In this case, consider making R_{FB} a resistor network that includes an NTC thermistor to minimize the temperature dependence of the voltage-positioning slope. FBAC is high impedance in shutdown.
11	GNDS	Remote Ground-Sense Input. Normally connected to the VSS_SENSE pin of the CPU socket. GNDS internally connects to a transconductance amplifier that fine tunes the output voltage—compensating for voltage drops from the regulator ground to the load ground.
12, 24, 37	N.C.	Internally Not Connected
13	CSN2	Negative Current-Sense Input for Phase 2. Connect CSN2 to the negative terminal of the inductor current-sensing resistor or directly to the negative terminal of the inductor if the lossless DCR sensing method is used (see Figure 3).
15	CSP2	Positive Current-Sense Input for Phase 2. Connect CSP2 to the positive terminal of the inductor current-sensing resistor or directly to the positive terminal of the filtering capacitor used when the lossless DCR sensing method is used (see Figure 3). Short CSP2 to V_{CC} for dedicated 1-phase operation.
16	$\overline{SHDN}$	Shutdown Control Input. This input cannot withstand the battery voltage. Connect to V_{CC} for normal operation. Connect to ground to put the IC into its 1µA max shutdown state. During startup, the output voltage is ramped up to the boot voltage slowly at a slew rate that is 1/8 the slew rate set by the TIME resistor. During the transition from normal operation to shutdown, the output voltage is ramped down at the same slow slew rate. Forcing $\overline{SHDN}$ to 11V~13V disables undervoltage protection, clears the fault latch, disables transient phase overlap, and disables the BST_ charging switches. Do not connect $\overline{SHDN}$ to > 13V.
17	DPRSLPVR	Pulse-Skipping Control Input. This 1.0V logic input signal indicates power usage and sets the operating mode of the MAX17582. When DPRSLPVR is forced high, the controller immediately enters the automatic pulse-skipping mode. The controller returns to forced-PWM mode when DPRSLPVR is forced low and the output is in regulation. The PWRGD upper threshold is blanked during any downward output-voltage transition that occurs when the controller is in pulse-skipping mode, and stays blanked until the transition-related PWRGD blanking period is complete and the output reaches regulation. The MAX17582 is in 2-phase pulse-skipping mode during startup and while in boot mode, but is in forced-PWM mode during the transition from boot mode to VID mode plus 20µs, and during soft-shutdown, irrespective of the DRPSLPVR logic level. DPRSLPVR and $\overline{PSI}$ together determine the operating mode and the number of active phases as shown in the following truth table: **DPRSLPVR** / **$\overline{PSI}$** / **MODE AND PHASES** 1 / 0 / Very low current (1-phase pulse skipping) 1 / 1 / Low current (approximately 3A) (1-phase pulse skipping) 0 / 0 / Intermediate power potential (1-phase PWM) 0 / 1 / Max power potential (2- or 1-phase PWM as configured at CSP2)

Pin Description (continued)

PIN	NAME	FUNCTION
18	$\overline{PSI}$	Power-State Indicator Input. DPRSLPVR and $\overline{PSI}$ together determine the operating mode and the number of active phases as shown in the truth table included under the $\overline{PSI}$ pin description.
19	TON	Switching Frequency Setting Input. An external resistor between the input power source and TON sets the switching period (T_{SW} = 1/f_{SW}) per phase according to the following equation: T_{SW} = 16.3pF x (R_{TON} + 6.5kΩ) TON becomes high impedance in shutdown to reduce the input quiescent current. If the TON current is less than 10µA, the MAX17582 disables the controller, sets the TON open fault latch, and pulls DL_ and DH_ low.
20	V3P3	3.3V CLKEN Input Supply. V3P3 input supplies the $\overline{CLKEN}$ CMOS push-pull logic output. Connect to the system's standard 3.3V supply voltage before $\overline{SHDN}$ is pulled high for proper IMVP-6.5 operation.
21	$\overline{CLKEN}$	Clock Enable Push-Pull Logic Output. This inverted logic output indicates when the output voltage sensed at FB is in regulation. During soft-start, shutdown, and when the FB is out of regulation, the MAX17582 pulls $\overline{CLKEN}$ up to V3P3. During VID transitions, the controller forces $\overline{CLKEN}$ low. Except during the power-up sequence, $\overline{CLKEN}$ is the inverse of PWRGD. See the *Startup Timing Diagram* (Figure 9). When in pulse-skipping mode (DPRSLPVR high), the upper $\overline{CLKEN}$ threshold is disabled.
22	PWRGD	Open-Drain Power-Good Output. After output-voltage transitions, except during power-up and power-down; if FB is in regulation then PWRGD is high impedance. During startup, PWRGD is held low and continues to be low while the part is in boot mode and until 5ms (typ) after $\overline{CLKEN}$ goes low. PWRGD is forced low in shutdown. PWRGD is forced high impedance whenever the slew-rate controller is active (output-voltage transitions). When in pulse-skipping mode (DPRSLPVR high), the upper PWRGD threshold comparator is blanked during downward transitions. A pullup resistor on PWRGD causes additional finite shutdown current.
23	PHASEGD	Phase-Good Current-Balance Open-Drain Output. Used to signal the system that one of the two phases either has a fault condition or is not matched with the other. Detection is done by identifying the need for a large on-time difference between phases in order to achieve or move towards current balance. PHASEGD is low in shutdown. PHASEGD is forced high impedance whenever the slew-rate controller is active (output-voltage transitions). PHASEGD is forced high impedance while in 1-phase operation (DPRSLPVR = high or $\overline{PSI}$ = low).
25	BST2	Boost Flying-Capacitor Connection for Phase 2. BST2 provides the upper supply rail for the DH2 high-side gate driver. An internal switch between V_{DD} and BST2 charges the flying capacitor while the low-side MOSFET is on (DL2 pulled high and LX2 pulled to ground).
26	LX2	Inductor Connection for Phase 2. LX2 is the internal lower supply rail for the DH2 high-side gate driver. Also used as an input to the controller's zero-crossing comparator for phase 2.
27	DH2	High-Side Gate-Driver Output for Phase 2. DH2 swings from LX2 to BST2. The controller pulls DH2 low in shutdown.
28	PGND2	Power Ground
29	DL2	Low-Side Gate-Driver Output for Phase 2. DL2 swings from GND to V_{DD}. DL2 is forced low in skip mode after detecting an inductor current zero crossing. DL2 is forced low during 1-phase operation ($\overline{PSI}$ = GND or CSP2 = V_{CC}).
30	$\overline{VRHOT}$	Open-Drain Output of Internal Comparator. $\overline{VRHOT}$ is pulled low when the voltage at THRM goes below 1.5V (30% of V_{CC}). $\overline{VRHOT}$ is high impedance in shutdown.
31	V_{DD}	Driver Supply Voltage Input. V_{DD} is the supply voltage used to internally power the low-side gate drivers and refresh the BST_ flying capacitors during the off-times. Connect V_{DD} to the 4.5V to 5.5V system supply voltage. Bypass V_{DD} to the system power ground with a 1µF each or greater ceramic capacitor.

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Pin Description (continued)

PIN	NAME	FUNCTION
32	DL1	Low-Side Gate-Driver Output for Phase 1. DL1 swings from GND to V_{DD}. DL1 is forced low after soft-shutdown or in skip mode after detecting an inductor current zero crossing.
33	PGND1	Power Ground
34	DH1	High-Side Gate-Driver Output for Phase 1. DH1 swings from LX1 to BST1. The controller pulls DH1 low in shutdown.
35	LX1	Inductor Connection for Phase 1. LX1 is the internal lower supply rail for the DH1 high-side gate driver. Also used as an input to the controller's zero-crossing comparator for phase 1.
36	BST1	Boost Flying-Capacitor Connection for Phase 1. BST1 provides the upper supply rail for the DH1 high-side gate driver. An internal switch between V_{DD} and BST1 charges the flying capacitor while the low-side MOSFET is on (DL1 is pulled high and LX1 is pulled to ground).
38	$\overline{SLOW}$	IMVP-6.5 Slew-Rate Select Input. This 1.0V logic input signal selects between the nominal and "slow" (half of nominal rate) slew rates. When $\overline{SLOW}$ is forced high, the selected nominal slew rate is set by the TIME resistance as defined above. When $\overline{SLOW}$ is forced low, the slew rate is reduced to half the nominal slew rate.
39–45	D0–D6	Low-Voltage VID DAC Code Input. The D0–D6 inputs do not have internal pullups. These 1.0V logic inputs are designed to interface directly with the CPU. The output voltage is set by the VID code indicated by the logic-level voltages on D0–D6 (see Table 4).
46	CSP1	Positive Current-Sense Input for Phase 1. Connect CSP1 to the positive terminal of the inductor current-sensing resistor or directly to the positive terminal of the filtering capacitor used when the lossless DCR sensing method is used (see Figure 3).
48	CSN1	Negative Current-Sense Input for Phase 1. Connect CSN1 to the negative terminal of the inductor current-sensing resistor or directly to the negative terminal of the inductor if the lossless DCR sensing method is used (see Figure 3). Under V_{CC} UVLO conditions and after soft-shutdown is completed, CSN1 is internally pulled to GND through a 10Ω FET to discharge the output.
—	EP	Exposed Pad. Internally connected to GND. Connect to the ground plane through a thermally enhanced via.

Detailed Description

Table 1 lists the component selection for standard applications. Table 2 lists component suppliers for the MAX17582.

Free-Running, Constant-On-Time PWM Controller with Input Feed-Forward

The Quick-PWM control architecture is a pseudo-fixed-frequency, constant-on-time, current-mode regulator with voltage feed-forward (Figure 2). This architecture relies on the output filter capacitor's ESR to act as the current-sense resistor, so the output ripple voltage provides the PWM ramp signal. The control algorithm is simple: the high-side switch on-time is determined solely by a one-shot whose period is inversely proportional to input voltage and directly proportional to output voltage, or the difference between the main and secondary inductor currents (see the *On-Time One-Shot* section). Another one-shot sets a minimum off-time. The on-time one-shot triggers when the error comparator goes low, the inductor current of the selected phase is below the valley current-limit threshold, and the minimum off-time one-shot times out. The controller maintains 180° out-of-phase operation by alternately triggering the main and secondary phases after the error comparator drops below the output-voltage set point.

Table 1. Component Selection for Standard Applications

DESIGN PARAMETERS	IMVP-6.5 AUBURNDALE SV CORE	IMVP-6.5 AUBURNDALE LV CORE
CIRCUIT	**FIGURE 1**	**FIGURE 1**
Input-Voltage Range	7V to 20V	7V to 20V
Maximum Load Current (TDC Current)	50A (37A)	28A (19A)
Transient Load Current	35A (10A/µs)	23A (10A/µs)
Load Line	-1.9mV/A	-3mV/A
COMPONENTS		
TON Resistance (R_{TON})	200kΩ (f_{SW} = 300kHz)	200kΩ (f_{SW} = 300kHz)
Inductance (L)	NEC/TOKIN MPC1055LR36 0.36µH, 32A, 0.8mΩ	NEC/TOKIN MPC1055LR36 0.36µH, 32A, 0.8mΩ
High-Side MOSFET (N_H)	Siliconix 1x Si4386DY 7.8mΩ/9.5mΩ (typ/max)	Siliconix 1x Si4386DY 7.8mΩ/9.5mΩ (typ/max)
Low-Side MOSFET (N_L)	Siliconix 2x Si4642DY 3.9mΩ/4.7mΩ (typ/max)	Siliconix 2x Si4642DY 3.9mΩ/4.7mΩ (typ/max)
Output Capacitors (C_{OUT})	4x 330µF, 6mΩ, 2.5V Panasonic EEFSX0D0D331XR 28x 10µF, 6V ceramic (0805)	3x 330µF, 6mΩ, 2.5V Panasonic EEFSX0D0D331XR 28x 10µF, 6V ceramic (0805)
Input Capacitors (C_{IN})	4x 10µF, 25V ceramic (1210)	4x 10µF, 25V ceramic (1210)
TIME-ILIM Resistance (R1)	10kΩ	10kΩ
ILIM-GND Resistance (R2)	59kΩ	59kΩ
FB Resistance (R_{FB})	4.02kΩ	6.34kΩ
IMON Resistance	9.09kΩ	18.2kΩ
LX_-CSP_ Resistance (R5)	1.21kΩ	1.21kΩ
CSP_-CSN_ Series Resistance (R6)	1.50kΩ	1.50kΩ
Parallel NTC Resistance	20kΩ	20kΩ
DCR Sense NTC (NTC1)	10kΩ NTC B = 3380 TDK NTCG163JH103F	10kΩ NTC B = 3380 TDK NTCG163JH103F
DCR Sense Capacitance (C_{SENSE})	2x 0.22µF, 6V ceramic (0805)	2x 0.22µF, 6V ceramic (0805)

Table 2. Component Suppliers

SUPPLIER	WEBSITE
AVX Corp.	www.avxcorp.com
BI Technologies	www.bitechnologies.com
Central Semiconductor Corp.	www.centralsemi.com
Fairchild Semiconductor	www.fairchildsemi.com
International Rectifier	www.irf.com
KEMET Corp	www.kemet.com
NEC/TOKIN America, Inc.	www.nec-tokin.com
Panasonic Corp.	www.panasonic.com

SUPPLIER	WEBSITE
Pulse Engineering	www.pulseeng.com
Renesas Technology Corp.	www.renesas.com
SANYO Electric Co, Ltd.	www.sanyodevice.com
Siliconix (Vishay)	www.vishay.com
Sumida Corp.	www.sumida.com
Taiyo Yuden	www.t-yuden.com
TDK Corp.	www.component.tdk.com
TOKO America, Inc.	www.tokoam.com

Dual-Phase, Quick-PWM Controller for IMVP-6.5 CPU Core Power Supplies

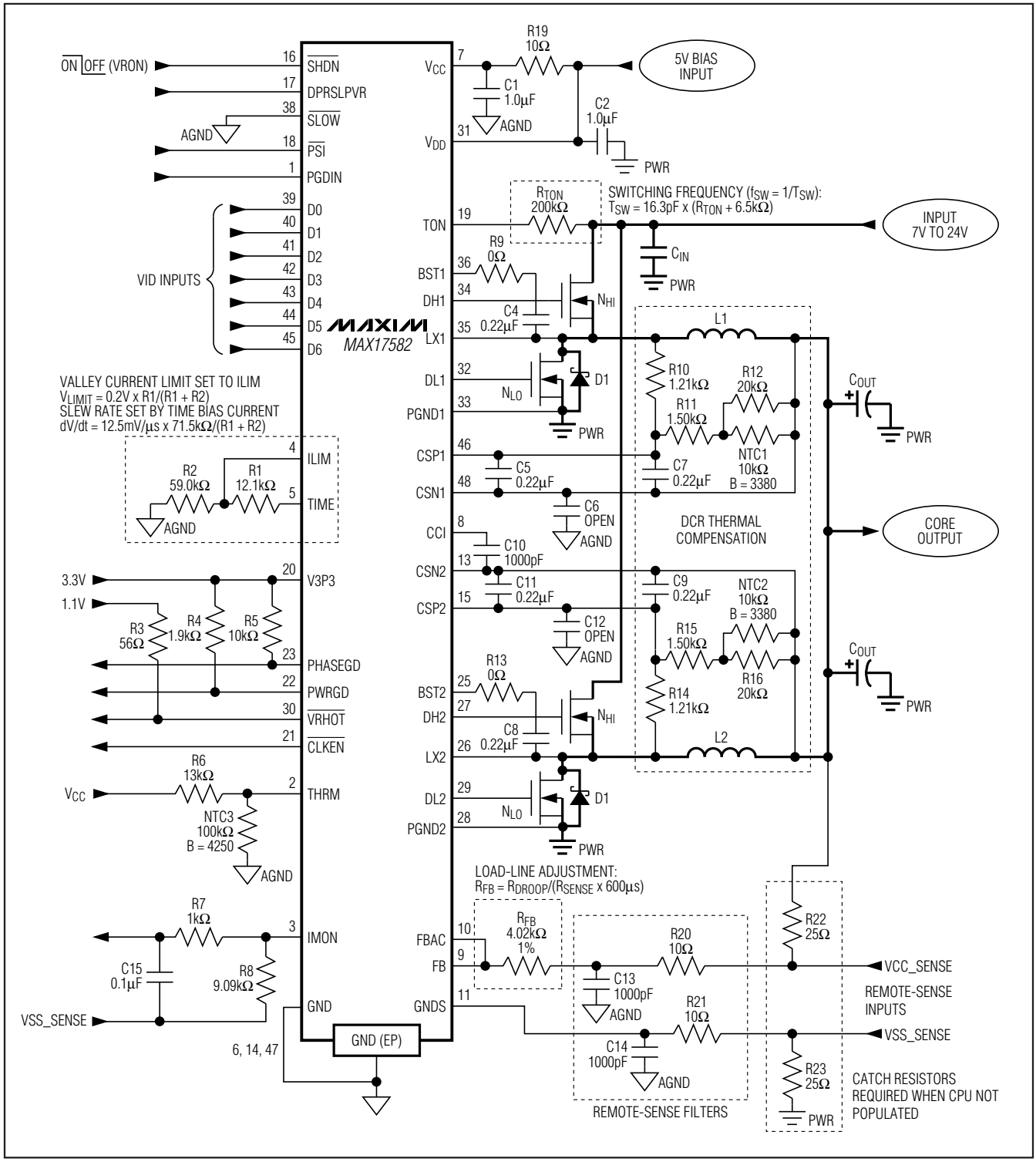

Figure 1. Standard 2-Phase IMVP-6.5 (Calpella) Application Circuit

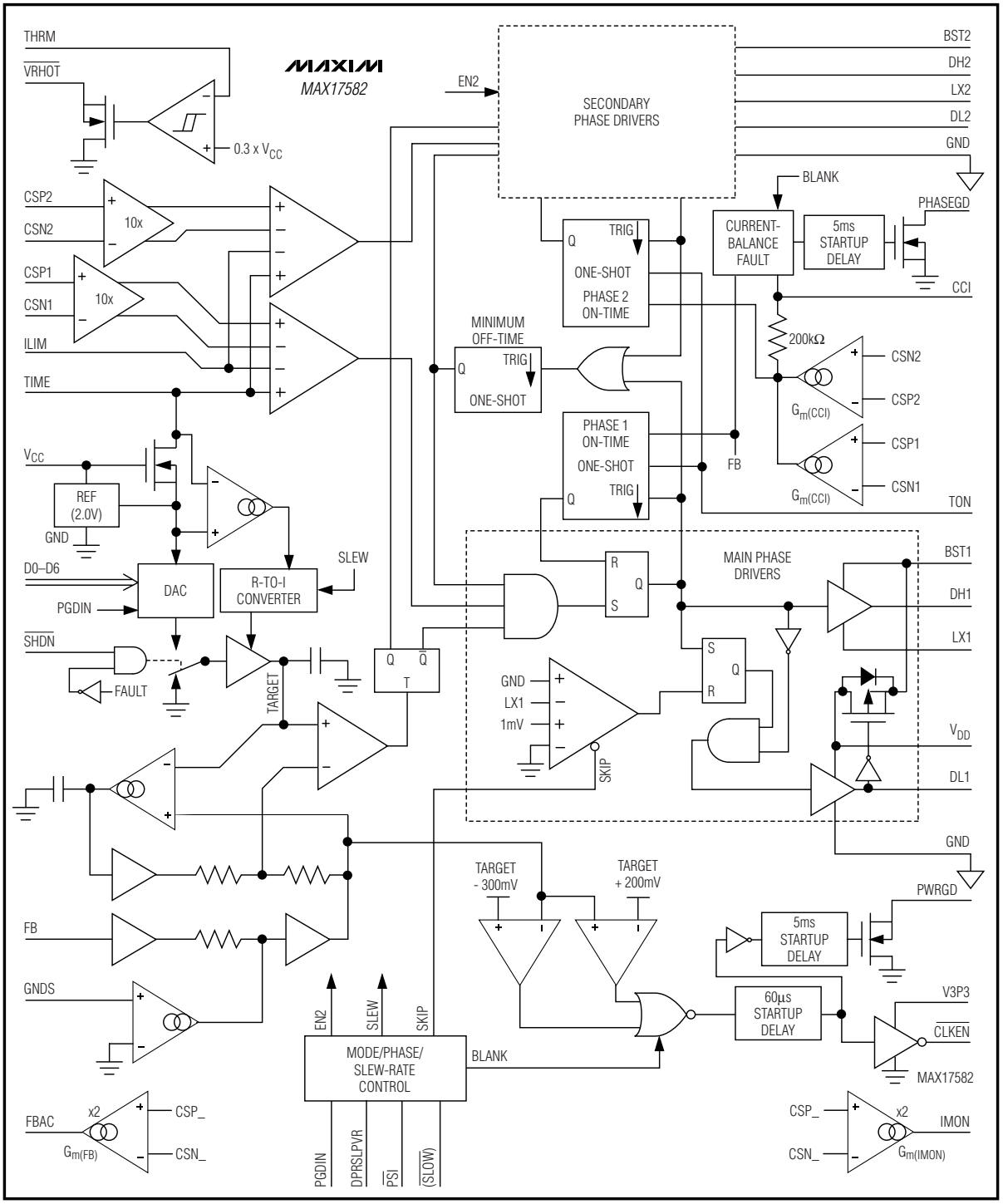

Figure 2. Functional Diagram

Dual-Phase, Quick-PWM Controller for IMVP-6.5 CPU Core Power Supplies

Dual 180° Out-of-Phase Operation

The two phases in the MAX17582 operate 180° out-of-phase to minimize input and output filtering requirements, reduce electromagnetic interference (EMI), and improve efficiency. This effectively lowers component count—reducing cost, board space, and component power requirements—making the MAX17582 ideal for high-power, cost-sensitive applications.

Typically, switching regulators provide power using only one phase instead of dividing the power among several phases. In these applications, the input capacitors must support high instantaneous current requirements. The high RMS ripple current can lower efficiency due to I^2R power loss associated with the input capacitor's effective series resistance (ESR). Therefore, the system typically requires several low-ESR input capacitors in parallel to minimize input-voltage ripple, to reduce ESR-related power losses, and to meet the necessary RMS ripple current rating.

With the MAX17582, the controller shares the current between two phases that operate 180° out-of-phase, so the high-side MOSFETs never turn on simultaneously during normal operation. The instantaneous input current of either phase is effectively halved, resulting in reduced input-voltage ripple, ESR power loss, and RMS ripple current (see the *Input Capacitor Selection* section). Therefore, the same performance can be achieved with fewer or less-expensive input capacitors.

+5V Bias Supply (V_{CC} and V_{DD})

The Quick-PWM controller requires an external +5V bias supply in addition to the battery. Typically, this +5V bias supply is the notebook's 95% efficient +5V system supply. Keeping the bias supply external to the IC improves efficiency and eliminates the cost associated with the +5V linear regulator that would otherwise be needed to supply the PWM circuit and gate drivers. If stand-alone capability is needed, the +5V bias supply can be generated with an external linear regulator.

The +5V bias supply must provide V_{CC} (PWM controller) and V_{DD} (gate-drive power), so the maximum current drawn is:

$$I_{BIAS} = I_{CC} + f_{SW} (Q_{G(LOW)} + Q_{G(HIGH)})$$

where I_{CC} is provided in the *Electrical Characteristics* table, f_{SW} is the switching frequency, and $Q_{G(LOW)}$ and $Q_{G(HIGH)}$ are the MOSFET data sheet's total gate-charge specification limits at V_{GS} = 5V.

V_{IN} and V_{DD} can be connected together if the input power source is a fixed +4.5V to +5.5V supply. If the +5V bias supply is powered up prior to the battery supply, the enable signal ($\overline{SHDN}$ going from low to high) must be delayed until the battery voltage is present to ensure startup.

Switching Frequency (TON)

Connect a resistor (R_{TON}) between TON and V_{IN} to set the switching period $T_{SW} = 1/f_{SW}$, per phase:

$$T_{SW} = 16.3pF \times (R_{TON} + 6.5k\Omega)$$

A 96.75kΩ to 303.25kΩ corresponds to switching periods of 167ns (600kHz) to 500ns (200kHz), respectively. High-frequency (600kHz) operation optimizes the application for the smallest component size, trading off efficiency due to higher switching losses. This might be acceptable in ultra-portable devices where the load currents are lower and the controller is powered from a lower voltage supply. Low-frequency (200kHz) operation offers the best overall efficiency at the expense of component size and board space.

TON Open-Circuit Protection

The TON input includes open-circuit protection to avoid long, uncontrolled on-times that could result in an overvoltage condition on the output. The MAX17582 detects an open-circuit fault if the TON current drops below 10µA for any reason—the TON resistor (R_{TON}) is unpopulated, a high resistance value is used, the input voltage is low, etc. Under these conditions, the MAX17582 stops switching (DH_ and DL_ pulled low) and immediately sets the fault latch. Toggle $\overline{SHDN}$ or cycle the V_{CC} power supply below 0.5V to clear the fault latch and reactivate the controller.

On-Time One-Shot

The core of each phase contains a fast, low-jitter, adjustable one-shot that sets the high-side MOSFETs on-time. The one-shot for the main phase varies the on-time in response to the input and feedback voltages. The main high-side switch on-time is inversely proportional to the input voltage as measured by the TON input, and proportional to the feedback voltage (V_{FB}):

$$t_{ON(MAIN)} = \frac{T_{SW}(V_{FB} + 0.075V)}{V_{IN}}$$

where the switching period ($T_{SW} = 1/f_{SW}$) is set by the resistor at the TON pin, and 0.075V is an approximation to accommodate the expected drop across the low-side MOSFET switch.

The one-shot for the secondary phase varies the on-time in response to the input voltage and the difference between the main and secondary inductor currents. Two identical transconductance amplifiers integrate the difference between the master and slave current-sense signals. The summed output is internally connected to CCI, allowing adjustment of the integration time constant with a compensation network connected between

CCI and FB. The resulting compensation current and voltage are determined by the following equations:

$$I_{CCI} = G_m(V_{CSP1} - V_{CSN1}) - G_m(V_{CSP2} - V_{CSN2})$$

$$V_{CCI} = V_{FB} + I_{CCI}Z_{CCI}$$

where Z_{CCI} is the impedance at the CCI output. The secondary on-time one-shot uses this integrated signal (V_{CCI}) to set the secondary high-side MOSFETs on-time. When the main and secondary current-sense signals ($V_{CM} = V_{CSP1} - V_{CSN1}$ and $V_{CS} = V_{CSP2} - V_{CSN2}$) become unbalanced, the transconductance amplifiers adjust the secondary on-time, which increases or decreases the secondary inductor current until the current-sense signals are properly balanced:

$$t_{ON(SEC)} = T_{SW}\left(\frac{V_{CCI} + 0.075V}{V_{IN}}\right)$$

$$= T_{SW}\left(\frac{V_{FB} + 0.075V}{V_{IN}}\right) + T_{SW}\left(\frac{I_{CCI}Z_{CCI}}{V_{IN}}\right)$$

$$= (\text{Main On-time}) + (\text{Secondary Current Balance Correction})$$

This algorithm results in a nearly constant switching frequency and balanced inductor currents despite the lack of a fixed-frequency clock generator. The benefits of a constant switching frequency are twofold: first, the frequency can be selected to avoid noise-sensitive regions such as the 455kHz IF band; second, the inductor ripple-current operating point remains relatively constant, resulting in easy design methodology and predictable output-voltage ripple. The on-time one-shots have good accuracy at the operating points specified in the *Electrical Characteristics* table. On-times at operating points far removed from the conditions specified in the *Electrical Characteristics* table can vary over a wider range.

On-times translate only roughly to switching frequencies. The on-times guaranteed in the *Electrical Characteristics* table are influenced by switching delays in the external high-side MOSFET. Resistive losses, including the inductor, both MOSFETs, output capacitor ESR, and PCB copper losses in the output and ground tend to raise the switching frequency at higher output currents. Also, the dead-time effect increases the effective on-time, reducing the switching frequency. It occurs only during forced-PWM operation and dynamic output-voltage transitions when the inductor current reverses at light- or negative-load currents. With reversed inductor current, the inductor's EMF causes LX_ to go high earlier than normal, extending the on-time by a period equal to the DH_-rising dead time. For loads above the critical conduction point, where the dead-time effect is no longer a factor, the actual switching frequency (per phase) is:

$$f_{SW} = \frac{(V_{OUT} + V_{DROP1})}{t_{ON}(V_{IN} + V_{DROP1} - V_{DROP2})}$$

where V_{DROP1} is the sum of the parasitic voltage drops in the inductor discharge path, including synchronous rectifier, inductor, and PCB resistances; V_{DROP2} is the sum of the parasitic voltage drops in the inductor charge path, including high-side switch, inductor, and PCB resistances; and t_{ON} is the on-time as determined above.

Current Sense

The output current of each phase is sensed. Low-offset amplifiers are used for current balance, voltage-positioning gain, and current limit. Sensing the current at the output of each phase offers advantages, including less noise sensitivity, more accurate current sharing between phases, and the flexibility of using either a current-sense resistor or the DC resistance of the output inductor.

Using the DC resistance (R_{DCR}) of the output inductor allows higher efficiency. In this configuration, the initial tolerance and temperature coefficient of the inductor's DCR must be accounted for in the output-voltage droop-error budget and power monitor. This current-sense method uses an RC filtering network to extract the current information from the output inductor (see Figure 3). The resistive divider used should provide a current-sense resistance (R_{CS}) low enough to meet the current-limit requirements, and the time constant of the RC network should match the inductor's time constant (L/R_{CS}):

$$R_{CS} = \left(\frac{R2}{R1+R2}\right)R_{DCR}$$

and:

$$R_{CS} = \frac{L}{C_{EQ}}\left[\frac{1}{R1} + \frac{1}{R2}\right]$$

where R_{CS} is the required current-sense resistance and R_{DCR} is the inductor's series DC resistance.

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Use the worst-case inductance and R_{DCR} values provided by the inductor manufacturer, adding some margin for the inductance drop over temperature and load. To minimize the current-sense error due to the current-sense inputs' bias current ($I_{CSP\_}$ and $I_{CSN\_}$), choose R1||R2 to be less than 2kΩ and use the previous equation to determine the sense capacitance (C_{EQ}). Choose capacitors with 5% tolerance and resistors with 1% tolerance specifications. Temperature compensation is recommended for this current-sense method. See the *Voltage Positioning and Loop Compensation* section for detailed information.

When using a current-sense resistor for accurate output-voltage positioning, the circuit requires a differential RC filter to eliminate the AC voltage step caused by the equivalent series inductance (L_{ESL}) of the current-sense resistor (see Figure 3). The ESL induced-voltage step does not affect the average current-sense voltage, but results in a significant peak current-sense voltage error that results in unwanted offsets in the regulation voltage and results in early current-limit detection. Similar to the inductor DCR sensing method above, the RC filter's time constant should match the L/R time constant formed by the current-sense resistor's parasitic inductance:

$$\frac{L_{ESL}}{R_{SENSE}} = C_{EQ}R1$$

where L_{ESL} is the equivalent series inductance of the current-sense resistor, R_{SENSE} is current-sense resistance value, and C_{EQ} and R1 are the time-constant matching components.

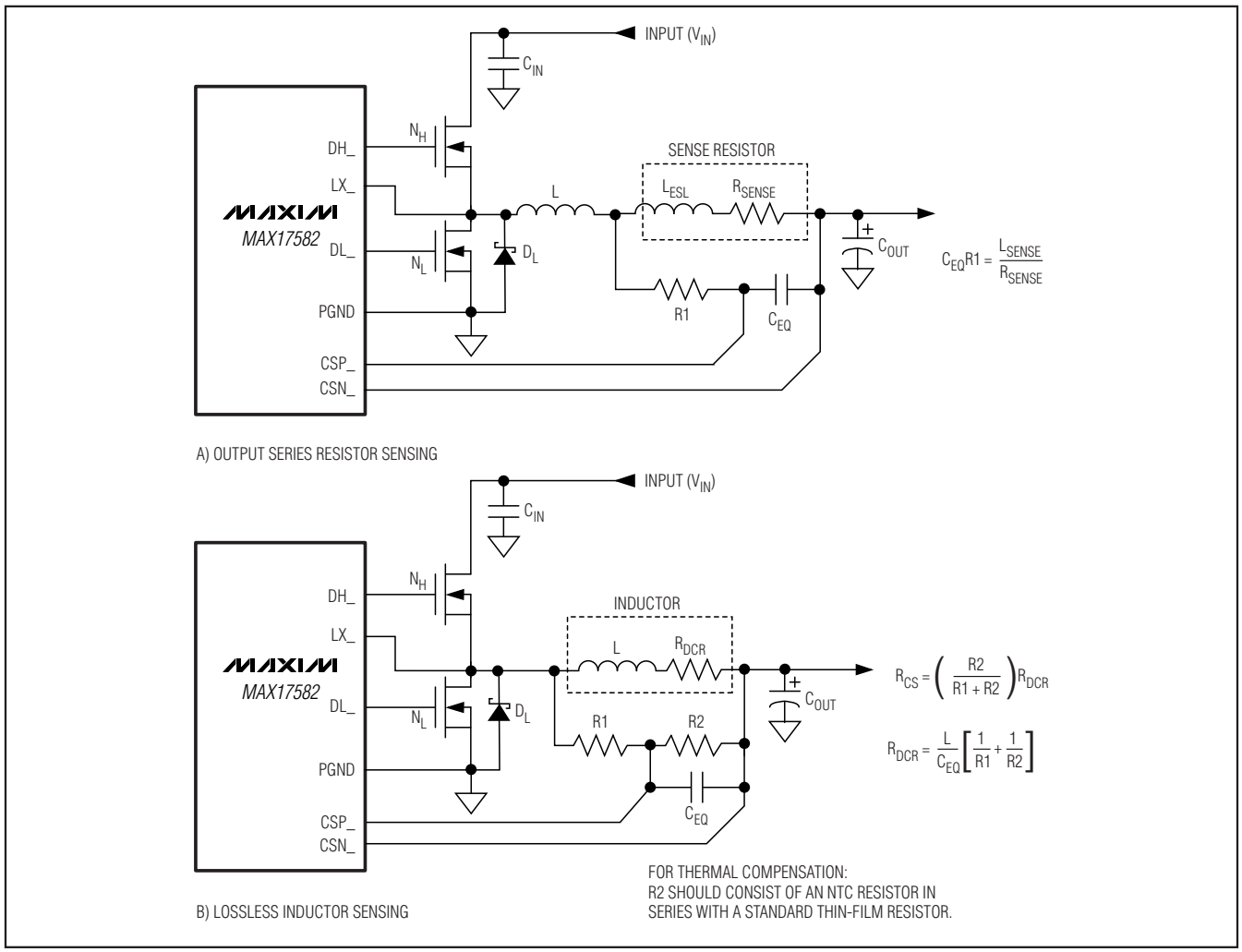

Figure 3. Current-Sense Methods

Current Balance

The MAX17582 integrates the difference between the current-sense voltages and adjusts the on-time of the secondary phase to maintain current balance. The current balance now relies on the accuracy of the current-sense resistors instead of the inaccurate, thermally sensitive on-resistance of the low-side MOSFETs. With active current balancing, the current mismatch is determined by the current-sense resistor values and the offset voltage of the transconductance amplifiers:

$$I_{OS(IBAL)} = I_{LMAIN} - I_{LSEC} = \frac{V_{OS(IBAL)}}{R_{SENSE}}$$

where R_{SENSE} is the effective sense resistance seen at the current-sense pins and $V_{OS(IBAL)}$ is the current-balance offset specification in the *Electrical Characteristics* table.

The worst-case current mismatch occurs immediately after a load transient due to inductor value mismatches resulting in different di/dt for the two phases. The time it takes the current-balance loop to correct the transient imbalance depends on the mismatch between the inductor values and switching frequency.

Current Limit

The current-limit circuit employs a unique "valley" current-sensing algorithm that uses current-sense resistors between the current-sense inputs (CSP_ to CSN_) as the current-sensing elements. If the current-sense signal of the selected phase is above the current-limit threshold, the PWM controller does not initiate a new cycle until the inductor current of the selected phase drops below the valley current-limit threshold. When either phase trips the current limit, both phases are effectively current limited since the interleaved controller does not initiate a cycle with either phase.

Since only the valley current is actively limited, the actual peak current is greater than the current-limit threshold by an amount equal to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are a function of the current-sense resistance, inductor value, and battery voltage. When combined with the undervoltage-protection circuit, this current-limit method is effective in almost every circumstance.

The positive valley current-limit threshold voltage at CSP_ to CSN_ equals precisely 1/10 of the differential TIME to ILIM voltage over a 0.1V to 0.5V range (10mV to 50mV current-sense range). Connect ILIM directly to V_{CC} to set the default current-limit threshold setting of 22.5mV (typ).

The negative current-limit threshold (forced-PWM mode only) is nominally -125% of the corresponding valley current-limit threshold. When the inductor current drops below the negative current limit, the controller immediately activates an on-time pulse—DL_ turns off and DH_ turns on—allowing the inductor current to remain above the negative-current threshold.

Carefully observe the PCB layout guidelines to ensure that noise and DC errors do not corrupt the current-sense signals seen by the current-sense inputs (CSP_, CSN_).

Feedback Adjustment Amplifiers

Voltage-Positioning Amplifier (Steady-State Droop)

The MAX17582 includes a transconductance amplifier for adding gain to the voltage-positioning sense path. The amplifier's input is generated by summing the current-sense inputs, which differentially sense the voltage across either current-sense resistors or the inductor's DCR. The amplifier's output connects directly to the regulator's voltage-positioned feedback input (FB), so the resistance between FB and the output-voltage sense point determines the voltage-positioning gain:

$$V_{OUT} = V_{TARGET} - R_{FB}I_{FB}$$

where the target voltage (V_{TARGET}) is defined in the *Nominal Output-Voltage Selection* section, and the FB amplifier's output current (I_{FB}) is determined by the sum of the current-sense voltages:

$$I_{FB} = G_{m(FB)} \sum_{X=1}^{\eta_{PH}} V_{CSX}$$

where $V_{CS} = V_{CSP\_} - V_{CSN\_}$ is the differential current-sense voltage, and $G_{m(FB)}$ is typically 600µS as defined in the *Electrical Characteristics* table.

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Differential Remote Sense

The MAX17582 includes differential, remote-sense inputs to eliminate the effects of voltage drops along the PCB traces and through the processor's power pins. The feedback-sense node connects to the voltage-positioning resistor (R_{FB}). The ground-sense (GNDS) input connects to an amplifier that adds an offset directly to the target voltage, effectively adjusting the output voltage to counteract the voltage drop in the ground path. Connect the voltage-positioning resistor (R_{FB}) and ground-sense (GNDS) input directly to the processor's remote-sense outputs, as shown in Figure 1.

Integrator Amplifier

An integrator amplifier forces the DC average of the FB voltage to equal the target voltage. This transconductance amplifier integrates the feedback voltage and provides a fine adjustment to the regulation voltage (Figure 2), allowing accurate DC output-voltage regulation regardless of the output ripple voltage. The integrator amplifier can shift the output voltage by ±100mV (typ). The differential input-voltage range is at least ±60mV total, including DC offset and AC ripple.

The MAX17582 disables the integrator by connecting the amplifier inputs together at the beginning of all VID transitions done in pulse-skipping mode (DPRSLPVR = high). The integrator remains disabled until 20µs after the transition is completed (the internal target settles) and the output is in regulation (edge detected on the error comparator).

Transient-Overlap Operation

When a transient occurs, the response time of the controller depends on how quickly it can slew the inductor current. Multiphase controllers that remain 180° out-of-phase when a transient occurs actually respond slower than an equivalent single-phase controller. To provide fast-transient response, the MAX17582 supports a phase-overlap mode, which allows the dual regulators to operate in-phase when heavy load transients are detected, effectively reducing the response time. After either high-side MOSFET turns off, if the output voltage does not exceed the regulation voltage when the minimum off-time expires, the controller simultaneously turns on both high-side MOSFETs during the next on-time cycle. This maximizes the total inductor current slew rate. The phases remain overlapped until the output voltage exceeds the regulation voltage after the minimum off-time expires.

After the phase-overlap mode ends, the controller automatically begins with the opposite phase. For example, if the secondary phase provided the last on-time pulse before overlap operation began, the controller starts switching with the main phase when overlap operation ends. Table 3 is the operating mode truth table.

Nominal Output-Voltage Selection

The nominal no-load output voltage (V_{TARGET}) is defined by the selected voltage reference (VID DAC) plus the remote ground-sense adjustment (V_{GNDS}) as defined in the following equation:

$$V_{TARGET} = V_{FB} = V_{DAC} + V_{GNDS}$$

where V_{DAC} is the selected VID voltage. On startup, the MAX17582 slews the target voltage from ground to the preset boot voltage.

DAC Inputs (D0–D6)

The digital-to-analog converter (DAC) programs the output voltage using the D0–D6 inputs. D0–D6 are low-voltage (1.0V) logic inputs, designed to interface directly with the CPU. Do not leave D0–D6 unconnected. Changing D0–D6 initiates a transition to a new output-voltage level. Change D0–D6 together, avoiding greater than 20ns skew between bits. Otherwise, incorrect DAC readings might cause a partial transition to the wrong voltage level followed by the intended transition to the correct voltage level, lengthening the overall transition time. The available DAC codes and resulting output voltages are compatible with the IMVP-6.5 (Table 4) specifications.

Table 3. Operating Mode Truth Table

INPUTS				PHASE OPERATION*	OPERATING MODE
$\overline{SHDN}$	$\overline{SLOW}$	DPRSLPVR	$\overline{PSI}$		
GND	X	X	X	Disabled	Low-Power Shutdown Mode. DL1 and DL2 forced low, and the controller is disabled. The supply current drops to 1µA (max).
Rising	X	X	X	Multiphase pulse-skipping 1/8 R_{TIME} slew rate	Startup/Boot. When $\overline{SHDN}$ is pulled high, the MAX17582 begins the startup sequence. The controller enables the PWM regulator and ramps the output voltage up to the boot voltage. See Figure 9.
High	High	Low	High	Multiphase forced-PWM nominal R_{TIME} slew rate	Full Power. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4).
High	High	Low	Low	1-phase forced-PWM nominal R_{TIME} slew rate	Intermediate Power. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4). When $\overline{PSI}$ is pulled low, the MAX17582 immediately disables phase 2. DH2 and DL2 are pulled low.
High	High	High	X	1-phase pulse-skipping nominal R_{TIME} slew rate	Deeper Sleep Mode. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4). When DPRSLPVR is pulled high, the MAX17582 immediately enters 1-phase pulse-skipping operation, allowing automatic PWM/PFM switchover under light loads. The PWRGD and $\overline{CLKEN}$ upper thresholds are blanked during downward transitions. DH2 and DL2 are pulled low.
High	Low	High	X	1-phase pulse-skipping	Deeper Sleep Slow Exit Mode. The no-load output voltage is determined by the selected VID DAC code (D0–D6, Table 4). When $\overline{SLOW}$ is pulled low, the MAX17582 reduces its slew rate to 1/2 of normal. The PWRGD and $\overline{CLKEN}$ upper thresholds are blanked. DH2 and DL2 are pulled low.
Falling	X	X	X	Multiphase forced-PWM 1/8 R_{TIME} slew rate	Shutdown. When $\overline{SHDN}$ is pulled low, the MAX17582 immediately pulls PWRGD and PHASEGD low, $\overline{CLKEN}$ becomes high, all enabled phases are activated, and the output voltage is ramped down to ground. Once the output reaches 0V, the controller enters the low-power shutdown state. See Figure 9.
High	X	X	X	Disabled	Fault Mode. The fault latch has been set by the MAX17582 UVP or thermal-shutdown protection. The controller remains in fault mode until V_{CC} power is cycled or $\overline{SHDN}$ toggled.

**Multiphase operation—all enabled phases active.*