Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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19-1795; Rev 1; 9/05

MAXIM

Low-Power Triple-Output TFT LCD DC-DC Converter

General Description

The MAX1779 triple-output DC-DC converter provides highly efficient regulated voltages required by small active matrix, thin-film transistor (TFT) liquid-crystal displays (LCDs). One high-power DC-DC converter and two low-power charge pumps convert the +2.7V to +5.5V input supply voltage into three independent output voltages.

The primary high-power DC-DC converter generates a boosted output voltage (V_{MAIN}) up to 13V that is regulated within ±1%. The low-power BiCMOS control circuitry and the low on-resistance (1Ω) of the integrated power MOSFET allows efficiency up to 91%. The 250kHz current-mode pulse-width modulation (PWM) architecture provides fast transient response and allows the use of ultra-small inductors and ceramic capacitors.

The dual charge pumps independently regulate one positive output (V_{POS}) and one negative output (V_{NEG}). These low-power outputs use external diode and capacitor stages (as many stages as required) to regulate output voltages up to +40V and down to -40V. A proprietary regulation algorithm minimizes output ripple, as well as capacitor sizes for both charge pumps.

The MAX1779 is available in the ultra-thin TSSOP package (1.1mm max height).

Applications

TFT Active-Matrix LCD Displays

Passive-Matrix LCD Displays

PDAs

Digital-Still Cameras

Camcorders

Typical Operating Circuit appears at end of data sheet.

Features

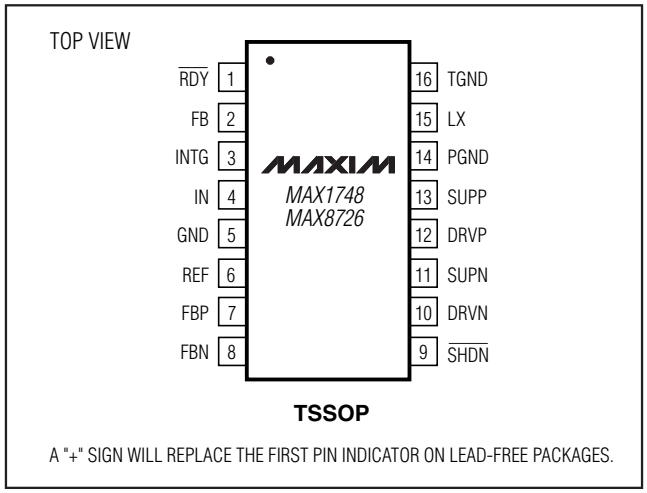
- **Three Integrated DC-DC Converters**
- **250kHz Current-Mode PWM Boost Regulator**
  - **Up to +13V Main High-Power Output**
  - **±1% Accuracy**
  - **High Efficiency (91%)**
- **Dual Charge-Pump Outputs**
  - **Up to +40V Positive Charge-Pump Output**
  - **Down to -40V Negative Charge-Pump Output**
- **Internal Supply Sequencing**
- **Internal Power MOSFETs**
- **+2.7V to +5.5V Input Supply**
- **0.1µA Shutdown Current**
- **0.5mA Quiescent Current**
- **Internal Soft-Start**
- **Power-Ready Output**
- **Ultra-Small External Components**
- **Thin TSSOP Package (1.1mm max)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1779EUE	-40°C to +85°C	16 TSSOP
MAX1779EUE+	-40°C to +85°C	16 TSSOP

+ Denotes lead-free package.

Pin Configuration



TSSOP

A "+" SIGN WILL REPLACE THE FIRST PIN INDICATOR ON LEAD-FREE PACKAGES.

Low-Power Triple-Output TFT LCD DC-DC Converter

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, TGND to GND .....-0.3V to +6V
DRVN to GND .....-0.3V to (V_{SUPN} + 0.3V)
DRVP to GND .....-0.3V to (V_{SUPP} + 0.3V)
PGND to GND .....±0.3V
$\overline{RDY}$ to GND .....-0.3V to +14V
LX, SUPP, SUPN to PGND .....-0.3V to +14V
INTG, REF, FB, FBN, FBP to GND .....-0.3V to (V_{IN} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
16-Pin TSSOP (derate 9.4mW/°C above +70°C) 755mW
Operating Temperature Range
MAX1779EUE .....-40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = +10V, TGND = PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 2200pF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Range	V_{IN}		2.7		5.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} rising, 40mV hysteresis (typ)	2.2	2.4	2.6	V
IN Quiescent Supply Current	I_{IN}	V_{FB} = V_{FBP} = +1.5V, V_{FBN} = -0.2V		0.5	1	mA
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = +1.5V		0.25	0.55	mA
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.1V		0.25	0.55	mA
IN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{IN} = +5V		0.1	10	µA
SUPP Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPP} = +13V		0.1	10	µA
SUPN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPN} = +13V		0.1	10	µA
MAIN BOOST CONVERTER						
Output Voltage Range	V_{MAIN}		V_{IN}		13	V
FB Regulation Voltage	V_{FB}		1.235	1.248	1.261	V
FB Input Bias Current	I_{FB}	V_{FB} = +1.25V, INTG = GND	-50		50	nA
Operating Frequency	f_{OSC}		212	250	288	kHz
Oscillator Maximum Duty Cycle			79	85	92	%
Load Regulation		I_{MAIN} = 0 to 50mA, V_{MAIN} = +5V		0.1		%
Line Regulation				0.1		%/V
Integrator Gm				320		µs
LX Switch On-Resistance	$R_{LX(ON)}$	I_{LX} = 100mA		1.0	2.0	Ω
LX Leakage Current	I_{LX}	V_{LX} = +13V		0.01	20	µA
LX Current Limit	I_{LIM}		350	450	650	mA
Maximum RMS LX Current				250		mA
FB Fault Trip Level		Falling edge	1.07	1.1	1.14	V
POSITIVE CHARGE PUMP						
V_{SUPP} Input Supply Range	V_{SUPP}		2.7		13	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = +10V, TGND = PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 2200pF, **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Frequency				0.5 × f_{OSC}		Hz
FBP Regulation Voltage	V_{FBP}		1.20	1.25	1.30	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = +1.5V	-50		50	nA
DRVP PCH On-Resistance				3	10	Ω
DRVP NCH On-Resistance		V_{FBP} = +1.200V		1.5	5	Ω
		V_{FBP} = +1.300V	20			kΩ
FBP Power-Ready Trip Level		Rising edge	1.09	1.13	1.16	V
FBP Fault Trip Level		Falling edge		1.11		V
Maximum RMS DRVP Current				0.1		A
NEGATIVE CHARGE PUMP						
V_{SUPN} Input Supply Range	V_{SUPN}		2.7		13	V
Operating Frequency				0.5 × f_{OSC}		Hz
FBN Regulation Voltage	V_{FBN}		-50	0	50	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = -0.05V	-50		50	nA
DRVN PCH On-Resistance				3	10	Ω
DRVN NCH On-Resistance		V_{FBN} = +0.050V		1.5	5	Ω
		V_{FBN} = -0.050V	20			kΩ
FBN Power-Ready Trip Level		Falling edge	80	120	165	mV
FBN Fault Trip Level		Rising edge		140		mV
Maximum RMS DRVN Current				0.1		A
REFERENCE						
Reference Voltage	V_{REF}	-2µA < I_{REF} < 50µA	1.231	1.25	1.269	V
Reference Undervoltage Threshold		V_{REF} rising	0.9	1.05	1.2	V
LOGIC SIGNALS						
$\overline{SHDN}$ Input Low Voltage		0.25V hysteresis (typ)			0.9	V
$\overline{SHDN}$ Input High Voltage			2.1			V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$			0.01	1	µA
$\overline{RDY}$ Output Low Voltage		I_{SINK} = 2mA		0.25	0.5	V
$\overline{RDY}$ Output High Voltage		$V_{\overline{RDY}}$ = +13V		0.01	1	µA

Low-Power Triple-Output TFT LCD DC-DC Converter

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = +10V, TGND = PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 2200pF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input Supply Range	V_{IN}		2.7	5.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} rising, 40mV hysteresis (typ)	2.2	2.6	V
IN Quiescent Supply Current	I_{IN}	V_{FB} = V_{FBP} = +1.5V, V_{FBN} = -0.2V		1	mA
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = +1.5V		0.55	mA
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.1V		0.55	mA
IN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{IN} = +5V		10	µA
SUPP Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPP} = +13V		10	µA
SUPN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPN} = +13V		10	µA
MAIN BOOST CONVERTER					
Output Voltage Range	V_{MAIN}		V_{IN}	13	V
FB Regulation Voltage	V_{FB}		1.225	1.271	V
FB Input Bias Current	I_{FB}	V_{FB} = +1.25V, INTG = GND	-50	50	nA
Operating Frequency	f_{OSC}		195	305	kHz
Oscillator Maximum Duty Cycle			79	92	%
LX Switch On-Resistance	$R_{LX(ON)}$	I_{LX} = 100mA		2.0	Ω
LX Leakage Current	I_{LX}	V_{LX} = +13V		20	µA
LX Current Limit	I_{LIM}		350	700	mA
FB Fault Trip Level		Falling edge	1.07	1.14	V
POSITIVE CHARGE PUMP					
SUPP Input Supply Range	V_{SUPP}		2.7	13	V
FBP Regulation Voltage	V_{FBP}		1.20	1.30	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = +1.5V	-50	50	nA
DRVP PCH On-Resistance				10	Ω
DRVP NCH On-Resistance		V_{FBP} = +1.200V		5	Ω
		V_{FBP} = +1.300V	20		kΩ
FBP Power-Ready Trip Level		Rising edge	1.09	1.16	V
NEGATIVE CHARGE PUMP					
SUPN Input Supply Range	V_{SUPN}		2.7	13	V
FBN Regulation Voltage	V_{FBN}		-50	50	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = -0.05V	-50	50	nA
DRVN PCH On-Resistance				10	Ω
DRVN NCH On-Resistance		V_{FBN} = +0.050V		5	Ω
		V_{FBN} = -0.050V	20		kΩ
FBN Power-Ready Trip Level		Falling edge	80	165	mV
REFERENCE					
Reference Voltage	V_{REF}	-2µA < I_{REF} < 50µA	1.223	1.269	V
Reference Undervoltage		V_{REF} rising	0.9	1.2	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = +10V, TGND = PGND = GND, C_{REF} = 0.22µF, C_{INTG} = 2200pF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 1)

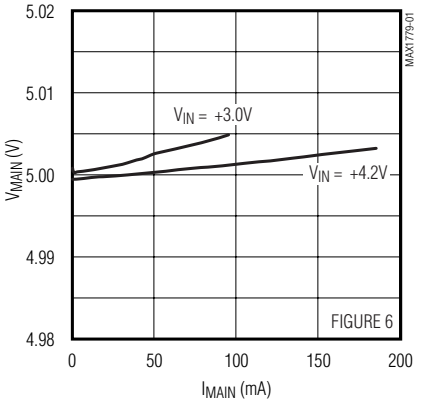
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
LOGIC SIGNALS					
$\overline{SHDN}$ Input Low Voltage		0.25V hysteresis (typ)		0.9	V
$\overline{SHDN}$ Input High Voltage			2.1		V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$			1	µA
$\overline{RDY}$ Output Low Voltage		I_{SINK} = 2mA		0.5	V
$\overline{RDY}$ Output High Leakage		$V_{\overline{RDY}}$ = +13V		1	µA

Note 1: Specifications to -40°C are guaranteed by design, not production tested.

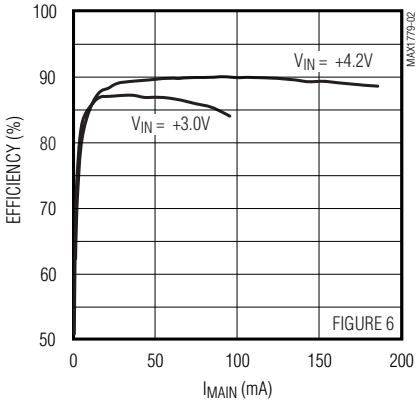
Typical Operating Characteristics

(Circuit of Figure 5, V_{IN} = +3.3V, T_A = +25°C, unless otherwise noted.)

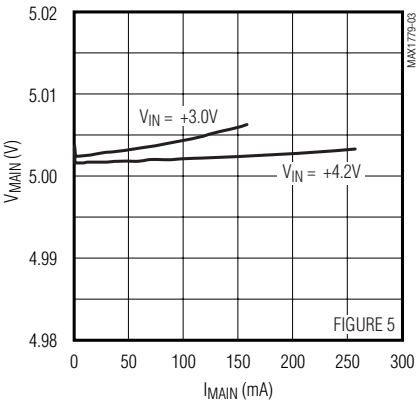
MAIN OUTPUT VOLTAGE vs. LOAD CURRENT (L = 10µH, 5V OUTPUT)



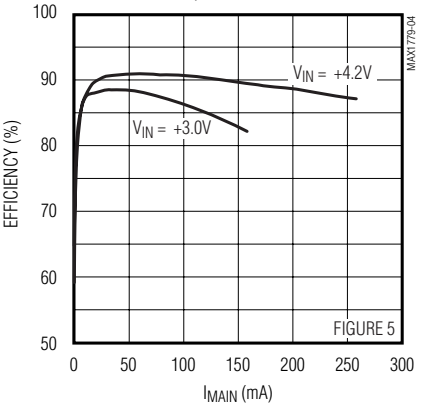
MAIN STEP-UP CONVERTER EFFICIENCY vs. LOAD CURRENT (L = 10µH, 5V OUTPUT)



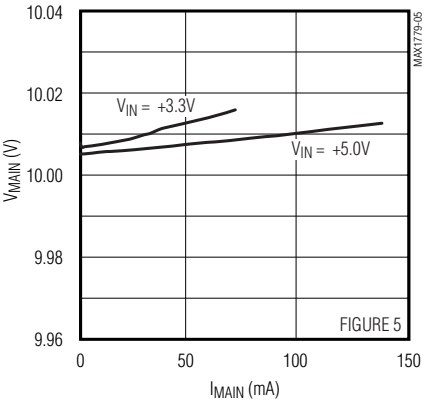
MAIN OUTPUT VOLTAGE vs. LOAD CURRENT (L = 33µH, 5V OUTPUT)



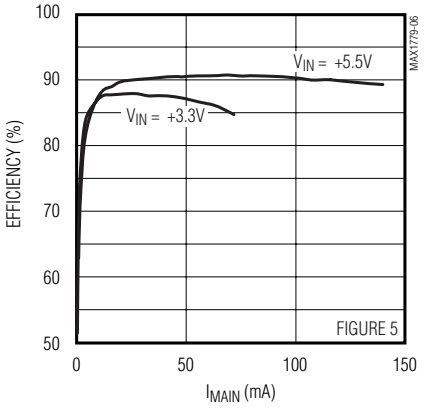
MAIN STEP-UP CONVERTER EFFICIENCY vs. LOAD CURRENT (L = 33µH, 5V OUTPUT)



MAIN OUTPUT VOLTAGE vs. LOAD CURRENT (L = 33µH, 10V OUTPUT)



MAIN STEP-UP CONVERTER EFFICIENCY vs. LOAD CURRENT (L = 33µH, 10V OUTPUT)

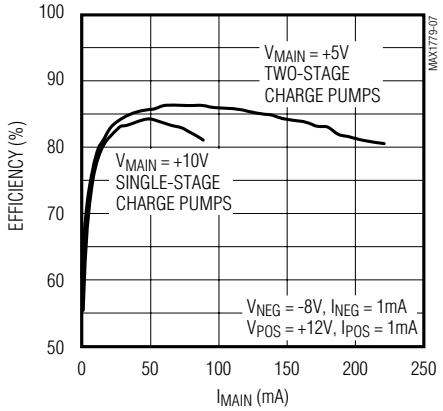


Low-Power Triple-Output TFT LCD DC-DC Converter

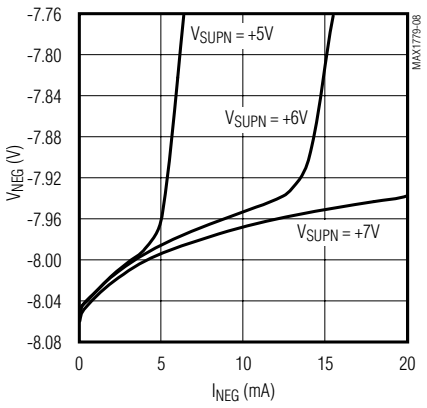
Typical Operating Characteristics (continued)

(Circuit of Figure 5, V_{IN} = +3.3V, T_A = +25°C, unless otherwise noted.)

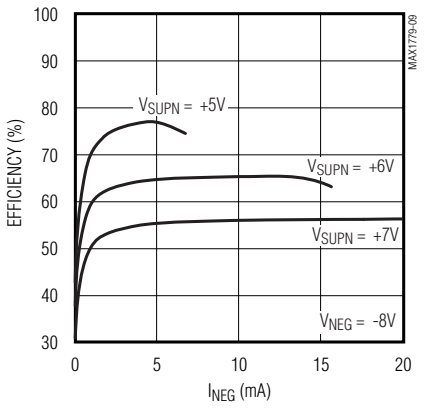
EFFICIENCY vs. LOAD CURRENT (BOOST CONVERTER AND CHARGE PUMPS)



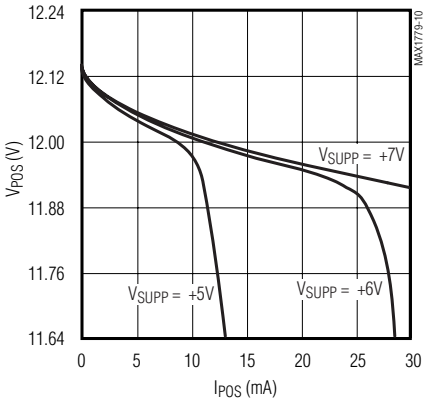
NEGATIVE CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT



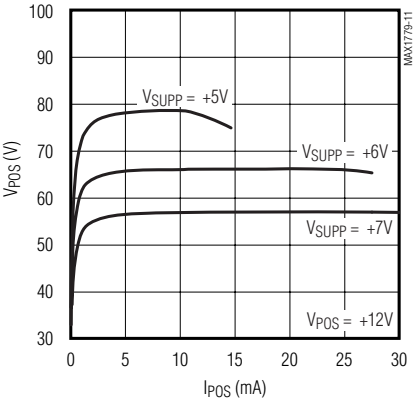
NEGATIVE CHARGE-PUMP EFFICIENCY vs. LOAD CURRENT



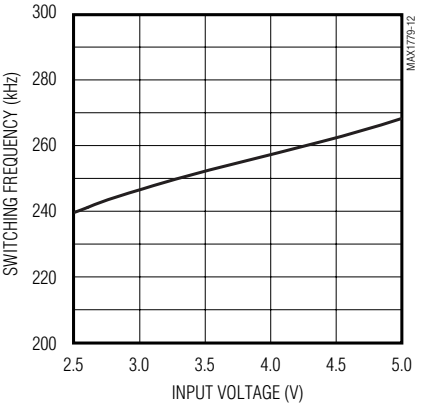
POSITIVE CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT



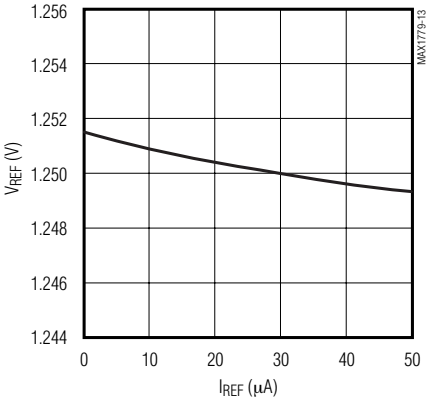
POSITIVE CHARGE-PUMP EFFICIENCY vs. LOAD CURRENT



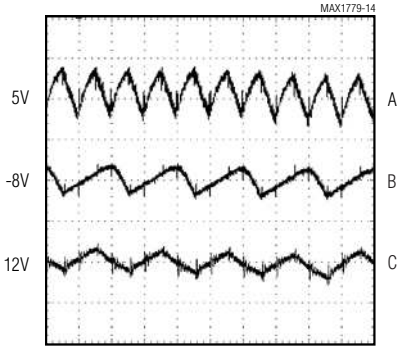
SWITCHING FREQUENCY vs. INPUT VOLTAGE



REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT

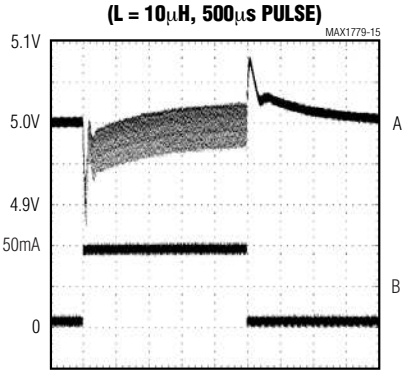


RIPPLE WAVEFORMS



A. V_{MAIN} = 5V, I_{MAIN} = 100mA, 10mV/div
B. V_{NEG} = -8V, I_{NEG} = 1mA, 5mV/div
C. V_{POS} = 12V, I_{POS} = 1mA, 5mV/div, FIGURE 5

LOAD TRANSIENT (L = 10µH, 500µs PULSE)

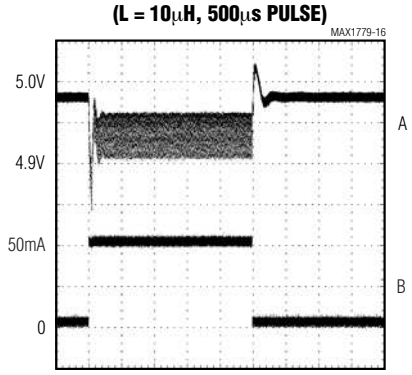


A. V_{MAIN} = 5V, 50mV/div
B. V_{MAIN} = 5mA to 50mA, 25mA/div
FIGURE 6

Typical Operating Characteristics (continued)

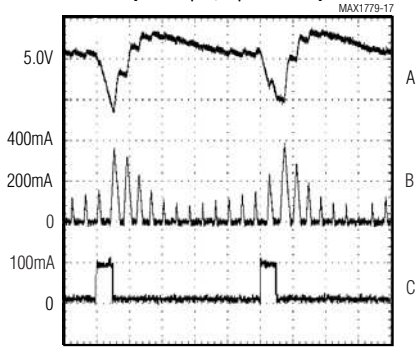
(Circuit of Figure 5, V_{IN} = +3.3V, T_A = +25°C, unless otherwise noted.)

LOAD TRANSIENT WITHOUT INTEGRATOR (L = 10µH, 500µs PULSE)



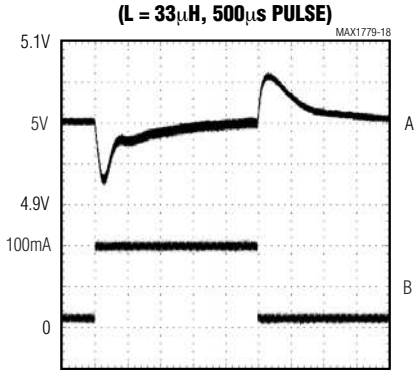
100µs/div
A. V_{MAIN} = 5V, 50mV/div
B. V_{MAIN} = 5mA to 50mA, 25mA/div
INTG = REF, FIGURE 6

LOAD TRANSIENT WITHOUT INTEGRATOR (L = 10µH, 5µs PULSE)



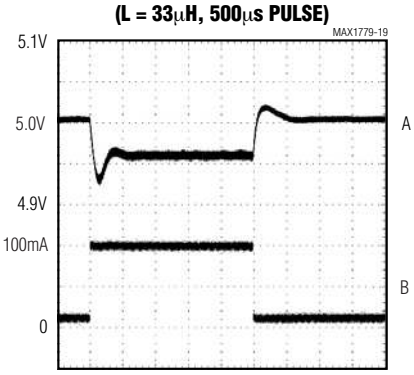
10µs/div
A. V_{MAIN} = 5V, 100mV/div
B. I_L, 200mA/div
C. I_{MAIN} = 10mA to 100mA, 100mA/div
INTG = REF, FIGURE 6

LOAD TRANSIENT (L = 33µH, 500µs PULSE)



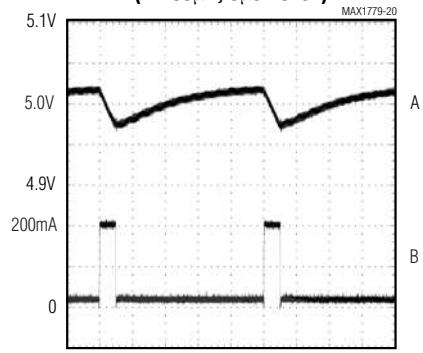
100µs/div
A. V_{MAIN} = 5V, 50mV/div
B. I_{MAIN} = 10mA to 100mA, 50mA/div
FIGURE 5

LOAD TRANSIENT WITHOUT INTEGRATOR (L = 33µH, 500µs PULSE)



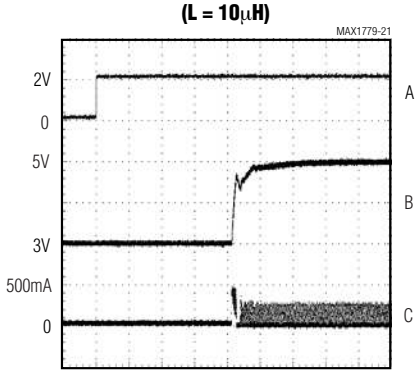
100µs/div
A. V_{MAIN} = 5V, 50mV/div
B. I_{MAIN} = 10mA to 100mA, 50mA/div
INTG = REF, FIGURE 5

LOAD TRANSIENT (L = 33µH, 5µs PULSE)



10µs/div
A. V_{MAIN} = 5V, 50mV/div
B. I_{MAIN} = 20mA to 200mA, 100mA/div
FIGURE 5

STARTUP WAVEFORM (L = 10µH)



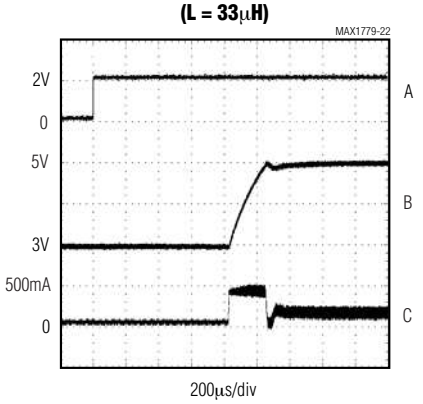
200µs/div
A. $V_{\overline{SHDN}}$ = 0 to 2V, 2V/div
B. V_{MAIN} = 5V, 1V/div
C. I_L, 500 mA/div
FIGURE 6, R_{MAIN} = 100Ω

Low-Power Triple-Output TFT LCD DC-DC Converter

Typical Operating Characteristics (continued)

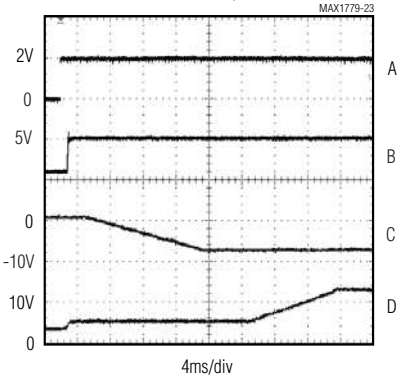
(Circuit of Figure 5, V_{IN} = +3.3V, T_A = +25°C, unless otherwise noted.)

STARTUP WAVEFORM
(L = 33µH)



A. $V_{\overline{SHDN}}$ = 0 to 2V, 2V/div
B. V_{MAIN} = 5V, 1V/div
C. I_L, 500mA/div
R_{MAIN} = 50Ω

POWER-UP SEQUENCING



A. $V_{\overline{SHDN}}$ = 0 to 2V, 2V/div
B. V_{MAIN} = 5V, R_{MAIN} = 50Ω, 2.5V/div
C. V_{NEG} = -8V, R_{NEG} = 8kΩ, 10V/div
D. V_{POS} = +12V, R_{POS} = 12kΩ, 10V/div

Pin Description

PIN	NAME	FUNCTION
1	$\overline{RDY}$	Active-Low Open-Drain Output. Indicates all outputs are ready. The on-resistance is 125Ω (typ).
2	FB	Main Boost Regulator Feedback Input. Regulates to 1.25V nominal. Connect feedback resistive divider to analog ground (GND).
3	INTG	Main Boost Integrator Output. If used, connect 2200pF to analog ground (GND). To disable integrator, connect to REF.
4	IN	Supply Input. +2.7V to +5.5V input range. Bypass with a 0.1µF capacitor between IN and GND, as close to the pins as possible.
5	GND	Analog Ground. Connect to power ground (PGND) underneath the IC.
6	REF	Internal Reference Bypass Terminal. Connect a 0.22µF capacitor from this terminal to analog ground (GND). External load capability to 50µA.
7	FBP	Positive Charge-Pump Regulator Feedback Input. Regulates to 1.25V nominal. Connect feedback resistive divider to analog ground (GND).
8	FBN	Negative Charge-Pump Regulator Feedback Input. Regulates to 0V nominal.
9	$\overline{SHDN}$	Active-Low Logic-Level Shutdown Input. Connect $\overline{SHDN}$ to IN for normal operation.

Pin Description (continued)

PIN	NAME	FUNCTION
10	DRVN	Negative Charge-Pump Driver Output. Output high level is V_{SUPN}, and low level is PGND.
11	SUPN	Negative Charge-Pump Driver Supply Voltage. Bypass to PGND with a 0.1µF capacitor.
12	DRVP	Positive Charge-Pump Driver Output. Output high level is V_{SUPP}, and low level is PGND.
13	SUPP	Positive Charge-Pump Driver Supply Voltage. Bypass to PGND with a 0.1µF capacitor.
14	PGND	Power Ground. Connect to GND underneath the IC.
15	LX	Main Boost Regulator Power MOSFET N-Channel Drain. Connect output diode and output capacitor as close to PGND as possible.
16	TGND	Must be connected to ground.

Detailed Description

The MAX1779 is a highly efficient triple-output power supply for TFT LCD applications. The device contains one high-power step-up converter and two low-power charge pumps. The primary boost converter uses an internal N-channel MOSFET to provide maximum efficiency and to minimize the number of external components. The output voltage of the main boost converter (V_{MAIN}) can be set from V_{IN} to 13V with external resistors.

The dual charge pumps independently regulate a positive output (V_{POS}) and a negative output (V_{NEG}). These low-power outputs use external diode and capacitor stages (as many stages as required) to regulate output voltages up to +40V and down to -40V. A proprietary regulation algorithm minimizes output ripple as well as capacitor sizes for both charge pumps.

Also included in the MAX1779 are a precision 1.25V reference that sources up to 50µA, logic shutdown, soft-start, power-up sequencing, fault detection, and an active-low open-drain ready output.

Main Boost Converter

The MAX1779 main step-up converter switches at a constant 250kHz internal oscillator frequency to allow the use of small inductors and output capacitors. The MOSFET switch pulse width is modulated to control the power transferred on each switching cycle and to regulate the output voltage.

During PWM operation, the internal clock's rising edge sets a flip-flop, which turns on the N-channel MOSFET (Figure 1). The switch turns off when the voltage-error, slope-compensation, and current-feedback signals trip the comparators and reset the flip-flop. The switch remains off for the rest of the clock cycle. Changes in the output voltage error signal shift the switch current trip level, consequently modulating the MOSFET duty cycle.

Dual Charge-Pump Regulator

The MAX1779 contains two individual low-power charge pumps. One charge pump inverts the supply voltage (SUPN) and provides a regulated negative output voltage. The second charge pump doubles the supply voltage (SUPP) and provides a regulated positive output voltage. The MAX1779 contains internal P-channel and N-channel MOSFETs to control the power transfer. The internal MOSFETs switch at a constant 125kHz ($0.5 \times f_{OSC}$).

Negative Charge Pump

During the first half-cycle, the P-channel MOSFET turns on and the flying capacitor C5 charges to V_{SUPN} minus a diode drop (Figure 2). During the second half-cycle, the P-channel MOSFET turns off, and the N-channel MOSFET turns on, level shifting C5. This connects C5 in parallel with the reservoir capacitor C6. If the voltage across C6 minus a diode drop is lower than the voltage across C5, charge flows from C5 to C6 until the diode (D5) turns off. The amount of charge transferred to the output is controlled by the variable N-channel on-resistance.

Positive Charge Pump

During the first half-cycle, the N-channel MOSFET turns on and charges the flying capacitor C3 (Figure 3). This initial charge is controlled by the variable N-channel on-resistance. During the second half-cycle, the N-channel MOSFET turns off and the P-channel MOSFET turns on, level shifting C3 by V_{SUPP} volts. This connects C3 in parallel with the reservoir capacitor C4. If the voltage across C4 plus a diode drop ($V_{POS} + V_{DIODE}$) is smaller than the level-shifted flying capacitor voltage

Low-Power Triple-Output TFT LCD DC-DC Converter

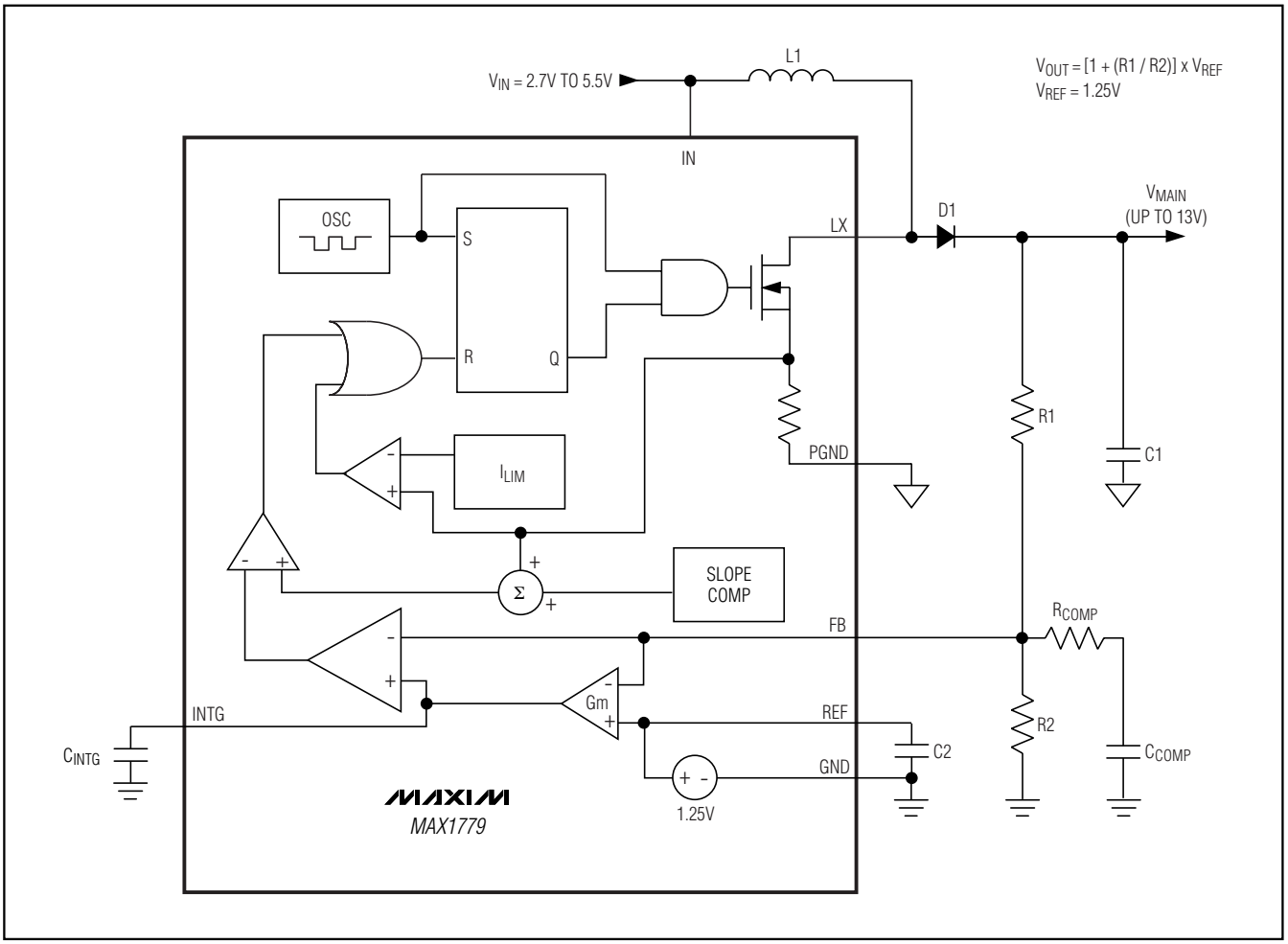


Figure 1. PWM Boost Converter Block Diagram

(V_{C3} + V_{SUPP}), charge flows from C3 to C4 until the diode (D3) turns off.

Soft-Start

The main boost regulator does not have soft-start.

For the charge pumps, soft-start is achieved by controlling the rise rate of the output voltage. The output voltage regulates within 16ms, regardless of output capacitance and load, limited only by the regulator's output impedance (see the Startup Waveforms in the *Typical Operating Characteristics*).

Shutdown

A logic-low level on $\overline{SHDN}$ disables all three MAX1779 converters and the reference. When shut down, the supply current drops to 0.1µA to maximize battery life and the reference is pulled to ground. The output capacitance and load current determine the rate at which each output voltage will decay. A logic-level high on $\overline{SHDN}$ activates the MAX1779 (see *Power-Up Sequencing*). Do not leave $\overline{SHDN}$ floating. If unused, connect $\overline{SHDN}$ to IN.

Power-Up Sequencing

Upon power-up or exiting shutdown, the MAX1779 starts a power-up sequence. First, the reference powers up. Then the main DC-DC step-up converter powers up. Once the main boost converter reaches regulation, the negative charge pump turns on. When the negative output voltage reaches approximately 90% of its nominal value (V_{FBN} < 120mV), the positive charge pump starts up. Finally, when the positive output voltage reaches 90% of its nominal value (V_{FBP} >

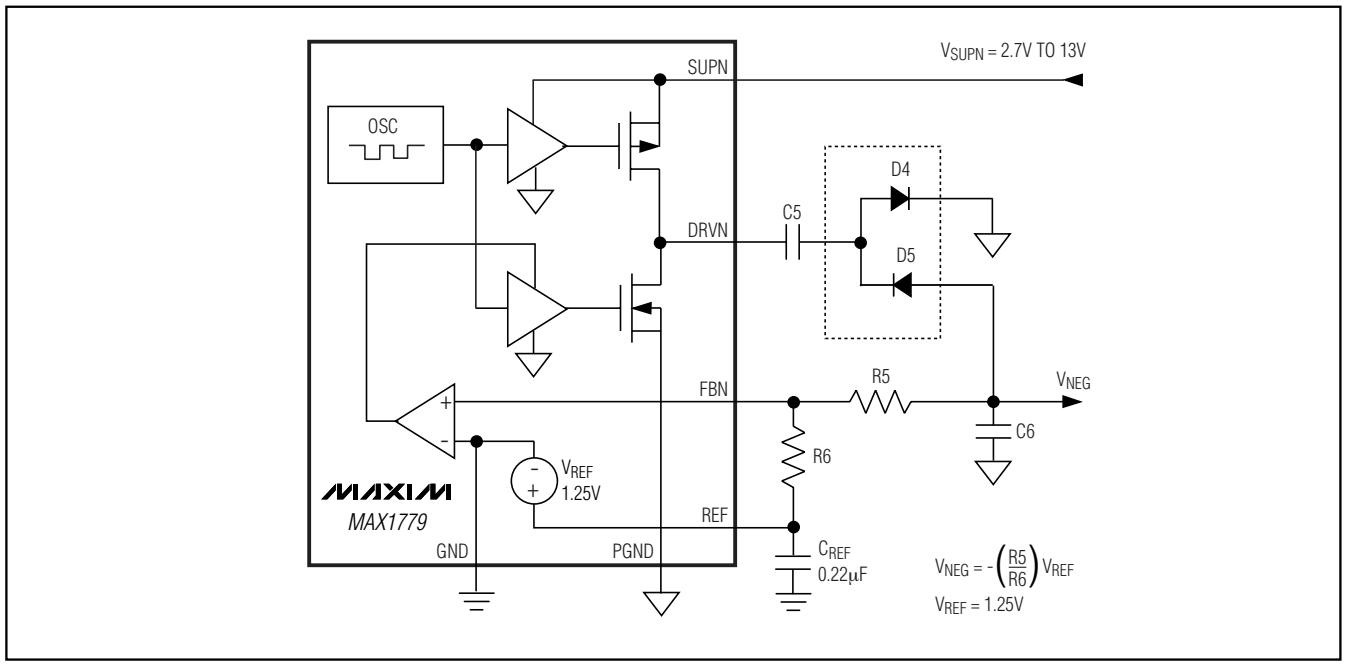


Figure 2. Negative Charge-Pump Block Diagram

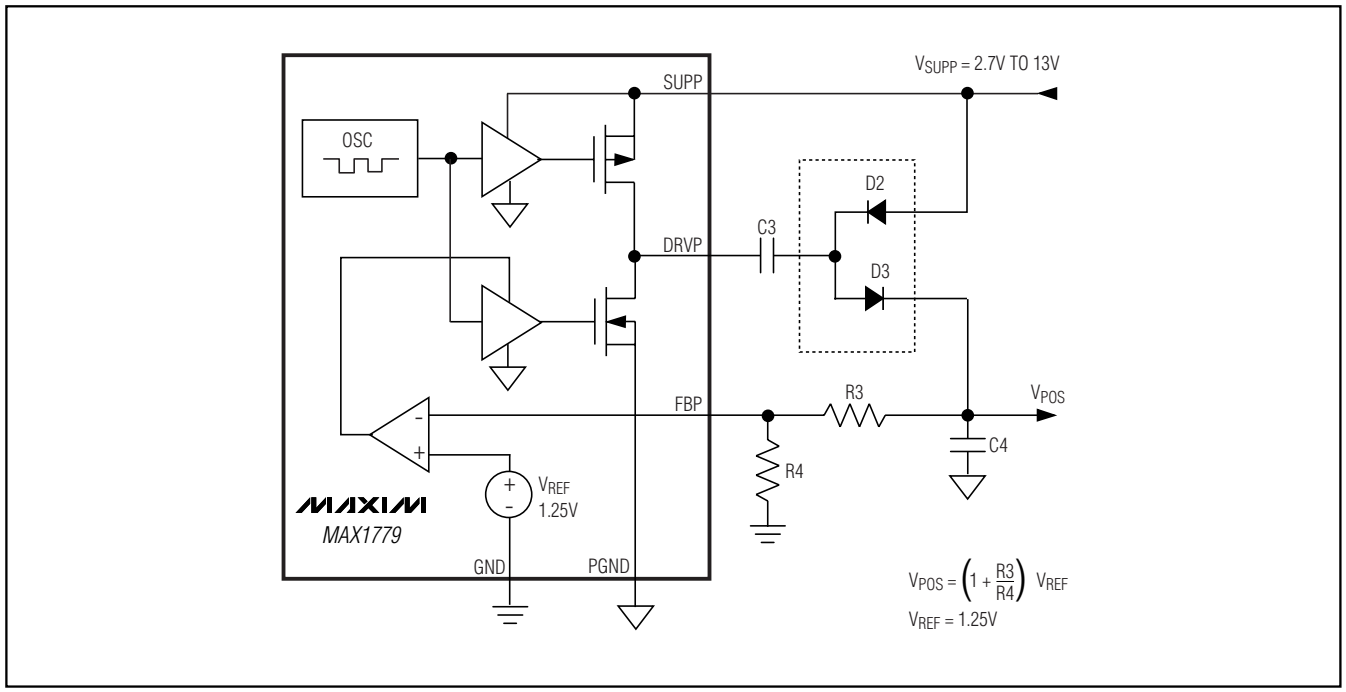


Figure 3. Positive Charge-Pump Block Diagram

Low-Power Triple-Output TFT LCD DC-DC Converter

1.125V), the active-low ready signal ($\overline{RDY}$) is pulled low (see *Power Ready* section).

Power Ready

Power ready is an open-drain output. When the power-up sequence is properly completed, the MOSFET turns on and pulls $\overline{RDY}$ low with a typical 125Ω on-resistance. If a fault is detected, the internal open-drain MOSFET appears as a high impedance. Connect a 100kΩ pullup resistor between $\overline{RDY}$ and IN for a logic-level output.

Fault Detection

Once $\overline{RDY}$ is low, if any output falls below its fault-detection threshold, then $\overline{RDY}$ becomes high impedance.

For the reference, the fault threshold is 1.05V. For the main boost converter, the fault threshold is 88% of its nominal value (V_{FB} < 1.1V). For the negative charge pump, the fault threshold is approximately 88% of its nominal value (V_{FBN} < 140mV). For the positive charge pump, the fault threshold is 88% of its nominal value (V_{FBP} < 1.11V).

Once an output faults, all outputs later in the power sequence shut down until the faulted output rises above its power-up threshold. For example, if the negative charge-pump output voltage falls below the fault detection threshold, the main boost converter remains active while the positive charge pump stops switching and its output voltage decays, depending on output capacitance and load. The positive charge-pump output will not power up until the negative charge-pump output voltage rises above its power-up threshold (see the *Power-Up Sequencing* section).

Voltage Reference

The voltage at REF is nominally 1.25V. The reference can source up to 50µA with good load regulation (see *Typical Operating Characteristics*). Connect a 0.22µF bypass capacitor between REF and GND.

Design Procedure

Main Boost Converter

Inductor Selection

Inductor selection depends upon the minimum required inductance value, saturation rating, series resistance, and size. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output voltage ripple. For most applications, values between 10µH and 33µH work best with the controller's switching frequency.

The inductor value depends on the maximum output load the application must support, input voltage, and output voltage. With high inductor values, the MAX1779 sources higher output currents, has less output ripple, and enters continuous-conduction operation with lighter loads; however, the circuit's transient response time is slower. On the other hand, low-value inductors respond faster to transients, remain in discontinuous-conduction operation, and typically offer smaller physical size. The maximum output current an inductor value will support may be calculated by the following equations:

A. Continuous-conduction: if

$$I_{MAIN(MAX)} \geq \frac{1}{2}\left(\frac{V_{IN(MIN)}}{V_{MAIN}}\right) I_{LIM(MIN)}$$

then

$$L \geq \frac{1}{2}\left(\frac{1}{f}\right)\left(\frac{V_{IN(MIN)}}{V_{MAIN}}\right)^2 \left[\frac{V_{MAIN} - V_{IN(MIN)}}{\left(\left(\frac{V_{IN(MIN)}}{V_{MAIN}}\right) I_{LIM(MIN)}\right) - I_{MAIN(MAX)}}\right]$$

B. Discontinuous-conduction: if

$$I_{MAIN(MAX)} < \frac{1}{2}\left(\frac{V_{IN(MIN)}}{V_{MAIN}}\right) I_{LIM(MIN)}$$

then

$$L \geq 2\left(\frac{1}{f}\right)\left[\frac{I_{MAIN(MAX)}\left(V_{MAIN} - V_{IN(MIN)}\right)}{I_{LIM(MIN)}^2}\right]$$

where $I_{LIM(MIN)}$ = 350mA and f = 250kHz (see the *Electrical Characteristics*).

The inductor's saturation current rating should exceed peak inductor current throughout the normal operating range. Under fault conditions, the inductor current may reach up to 600mA ($I_{LIM(MAX)}$, see the *Electrical Characteristics*). However, the MAX1779's fast current-limit circuitry allows the use of soft-saturation inductors while still protecting the IC.

The inductor's DC resistance significantly affects efficiency due to the power loss in the inductor. The power loss due to the inductor's series resistance (P_{LR}) may be approximated by the following equation:

$$P_{LR} \cong \left(\frac{I_{MAIN} \times V_{MAIN}}{V_{IN}}\right)^2 \times R_L$$

where R_L is the inductor's series resistance. For best performance, select inductors with resistance less than the internal N-channel MOSFET on-resistance (1Ω typ).

Output Capacitor

The output capacitor selection depends on circuit stability and output voltage ripple. In order to deliver the maximum output current capability of the MAX1779, the inductor must run in continuous-conduction mode (see *Inductor Selection*). The minimum recommended output capacitance is:

$$C_{OUT} > \frac{60 \times L \times I_{MAIN(MAX)}}{V_{MAIN} \times V_{IN(MIN)}}$$

For configurations that need less output current, the MAX1779 allows lower output capacitance when operating in discontinuous-conduction mode throughout the load range. Under these conditions, at least 10µF is recommended, as shown in Figure 6. In both discontinuous and continuous operation, additional feedback compensation is required (see the *Feedback Compensation* section) to increase the margin for stability by reducing the bandwidth further. In cases where the output capacitance is sufficiently large, additional feedback compensation will not be necessary. However, in certain applications that require benign load transients and constantly operate in discontinuous-conduction mode, output capacitance less than 10µF may be used.

Output voltage ripple has two components: variations in the charge stored in the output capacitor with each LX pulse, and the voltage drop across the capacitor's equivalent series resistance (ESR) caused by the current into and out of the capacitor:

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

For low-value ceramic capacitors, the output voltage ripple is dominated by $V_{RIPPLE(C)}$.

Integrator Capacitor

The MAX1779 contains an internal current integrator that improves the DC load regulation but increases the peak-to-peak transient voltage (see the Load Transient Waveforms in the *Typical Operating Characteristics*). For highly accurate DC load regulation, enable the integrator by connecting a capacitor to INTG. The minimum capacitor value should be C_{OUT}/10k or 1nF, whichever is greater. Alternatively, to minimize the peak-to-peak transient voltage at the expense of DC load regulation, disable the integrator by connecting INTG to REF and adding a 100kΩ resistor to GND.

Feedback Compensation

Compensation on the feedback node is required to have enough margin for stability. Add a pole-zero pair from FB to GND in the form of a compensation resistor (R_{COMP} in Figures 5 and 6) in series with a compensation capacitor (C_{COMP} in Figures 5 and 6). For continuous conduction operation, select R_{COMP} to be 1/2 the value of R2, the low-side feedback resistor. For discontinuous-conduction operation, select R_{COMP} to be 1/5th the value of R2.

Start with a compensation capacitor value of (220pF × R_{COMP})/10kΩ. Increase this value to improve the DC stability as necessary. Larger compensation values slow down the converter's response time. Check the startup waveform for excessive overshoot each time the compensation capacitor value is increased.

Charge Pump

Efficiency Considerations

The efficiency characteristics of the MAX1779 regulated charge pumps are similar to a linear regulator. They are dominated by quiescent current at low output currents and by the input voltage at higher output currents (see *Typical Operating Characteristics*). So the maximum efficiency may be approximated by:

$$\text{Efficiency} \cong |V_{NEG}| / [V_{IN} \times N];$$
for the negative charge pump

$$\text{Efficiency} \cong V_{POS} / [V_{IN} \times (N + 1)];$$
for the positive charge pump

where N is the number of charge-pump stages.

Output Voltage Selection

Adjust the positive output voltage by connecting a voltage-divider from the output (V_{POS}) to FBP to GND (see *Typical Operating Circuit*). Adjust the negative output voltage by connecting a voltage-divider from the output (V_{NEG}) to FBN to REF. Select R4 and R6 in the 50kΩ to 100kΩ range. Higher resistor values improve efficiency at low output current but increase output voltage error due to the feedback input bias current. Calculate the remaining resistors with the following equations:

$$R3 = R4 [(V_{POS} / V_{REF}) - 1]$$

$$R5 = R6 (|V_{NEG} / V_{REF}|)$$

where V_{REF} = 1.25V. V_{POS} may range from V_{SUPP} to +40V, and V_{NEG} may range from 0 to -40V.

Flying Capacitor

Increasing the flying capacitor's value increases the output current capability. Above a certain point, increasing the capacitance has a negligible effect because the output current capability becomes domi-

Low-Power Triple-Output TFT LCD DC-DC Converter

nated by the internal switch resistance and the diode impedance. Start with 0.1µF ceramic capacitors. Smaller values may be used for low-current applications.

Charge-Pump Output Capacitor

Increasing the output capacitance or decreasing the ESR reduces the output ripple voltage and the peak-to-peak transient voltage. Use the following equation to approximate the required capacitor value:

$$C_{PUMP} \geq [I_{PUMP} / (125kHz \times V_{RIPPLE})]$$

Charge-Pump Input Capacitor

Use a bypass capacitor with a value equal to or greater than the flying capacitor. Place the capacitor as close to the IC as possible. Connect directly to PGND.

Rectifier Diode

Use Schottky diodes with a current rating equal to or greater than 4 times the average output current, and a voltage rating at least 1.5 times V_{SUPP} for the positive charge pump and V_{SUPN} for the negative charge pump.

PC Board Layout and Grounding

Carefully printed circuit layout is extremely important to minimize ground bounce and noise. First, place the main boost converter output diode and output capacitor less than 0.2in (5mm) from the LX and PGND pins with wide traces and no vias. Then place 0.1µF ceramic bypass capacitors near the charge-pump input pins (SUPP and SUPN) to the PGND pin. Keep the charge-pump circuitry as close to the IC as possible, using wide traces and avoiding vias when possible. Locate all feedback resistive dividers as close to their respective feedback pins as possible. The PC board should feature separate GND and PGND areas connected at only one point under the IC. To maximize output power and efficiency and to minimize output power ripple voltage, use extra wide power ground traces and solder the IC's power ground pin directly to it. Avoid having sensitive traces near the switching nodes and high-current lines.

Refer to the MAX1779 evaluation kit for an example of proper board layout.

Applications Information

LX Charge Pump

Some applications require multiple charge-pump stages due to low supply voltages. In order to reduce the circuit's size and component count, an unregulated charge pump may be added onto the LX switching node. The configuration shown in Figure 4 works well for most applications. The maximum output current of the low-power charge pumps depends on the maximum load current that the LX charge pump can provide and is limited by the following formula:

$$I_{LXPUMP} = ((N + 1) \times I_{POS}) + (M + I_{NEG}) \leq 5mA$$

where N is the number of stages in the positive low-power charge pump, and M is the number of stages in the negative charge pump. Applications requiring more output current should not use the LX charge pump, so they will require extra stages on both low-power charge pumps. The output capacitor of this unregulated charge pump needs to be stacked on top of the main output in order to keep the main regulator stable. Increasing the integrator capacitor may also be required to compensate for the additional charge-pump capacitance on the main regulator loop.

The output capacitor of this unregulated charge pump needs to be stacked on top of the main output in order to keep the main regulator stable. Increasing the integrator capacitor may also be required to compensate for the additional charge-pump capacitance on the main regulator loop.

Table 1. Component Suppliers

SUPPLIER	PHONE	FAX
INDUCTORS		
Coilcraft	847-639-6400	847-639-1469
Coiltronics	561-241-7876	561-241-9339
Sumida USA	847-956-0666	847-956-0702
Toko	847-297-0070	847-699-1194
CAPACITORS		
AVX	803-946-0690	803-626-3123
Kemet	408-986-0424	408-986-1442
Sanyo	619-661-6835	619-661-1055
Taiyo Yuden	408-573-4150	408-573-4159
DIODES		
Central Semiconductor	516-435-1110	516-435-1824
International Rectifier	310-322-3331	310-322-3332
Motorola	602-303-5454	602-994-6430
Nihon	847-843-7500	847-843-2798
Zetex	516-543-7100	516-864-7630

Chip Information

TRANSISTOR COUNT: 2846

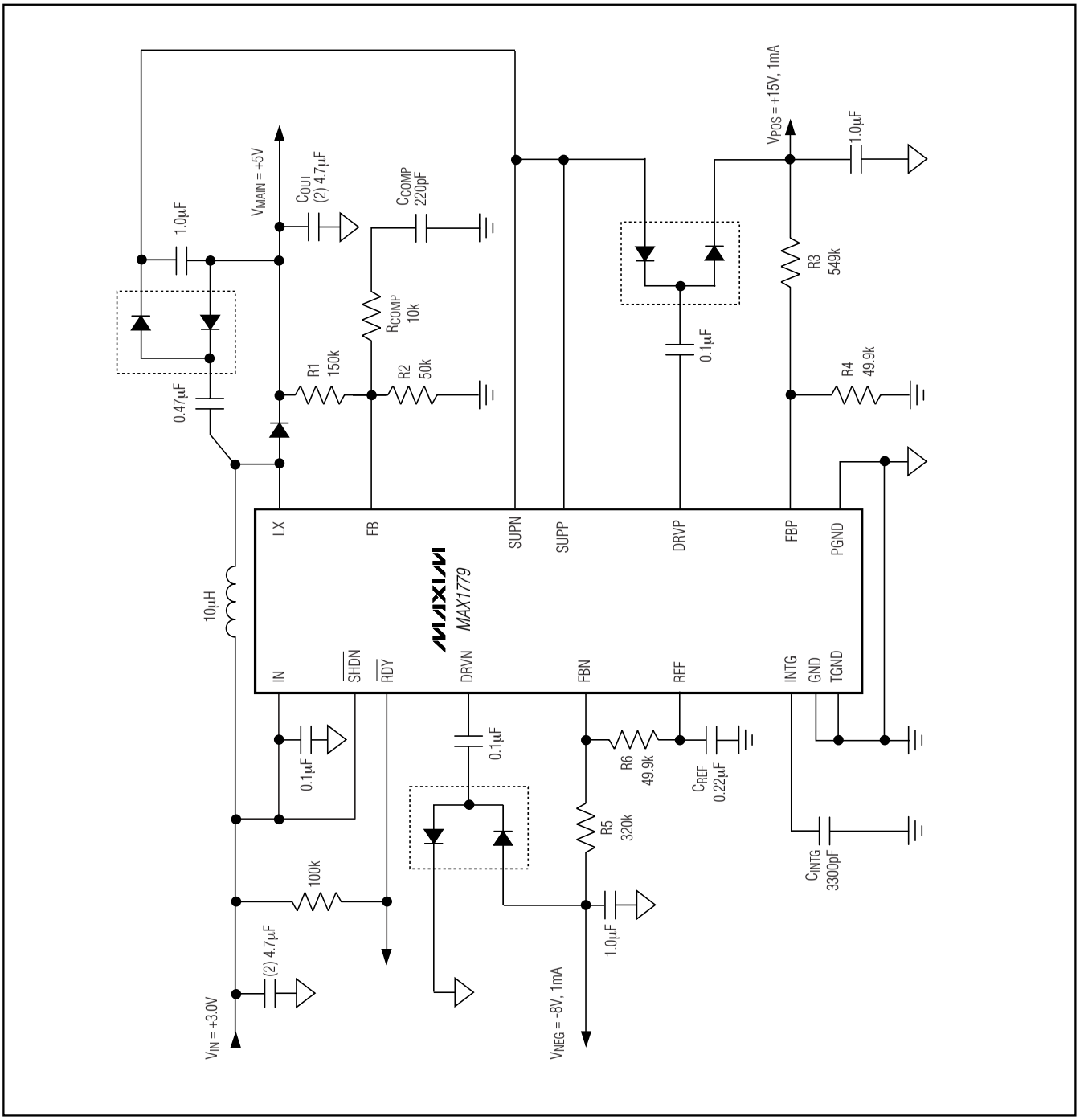


Figure 4. Minimizing the Number of Charge-Pump Stages

Low-Power Triple-Output TFT LCD DC-DC Converter

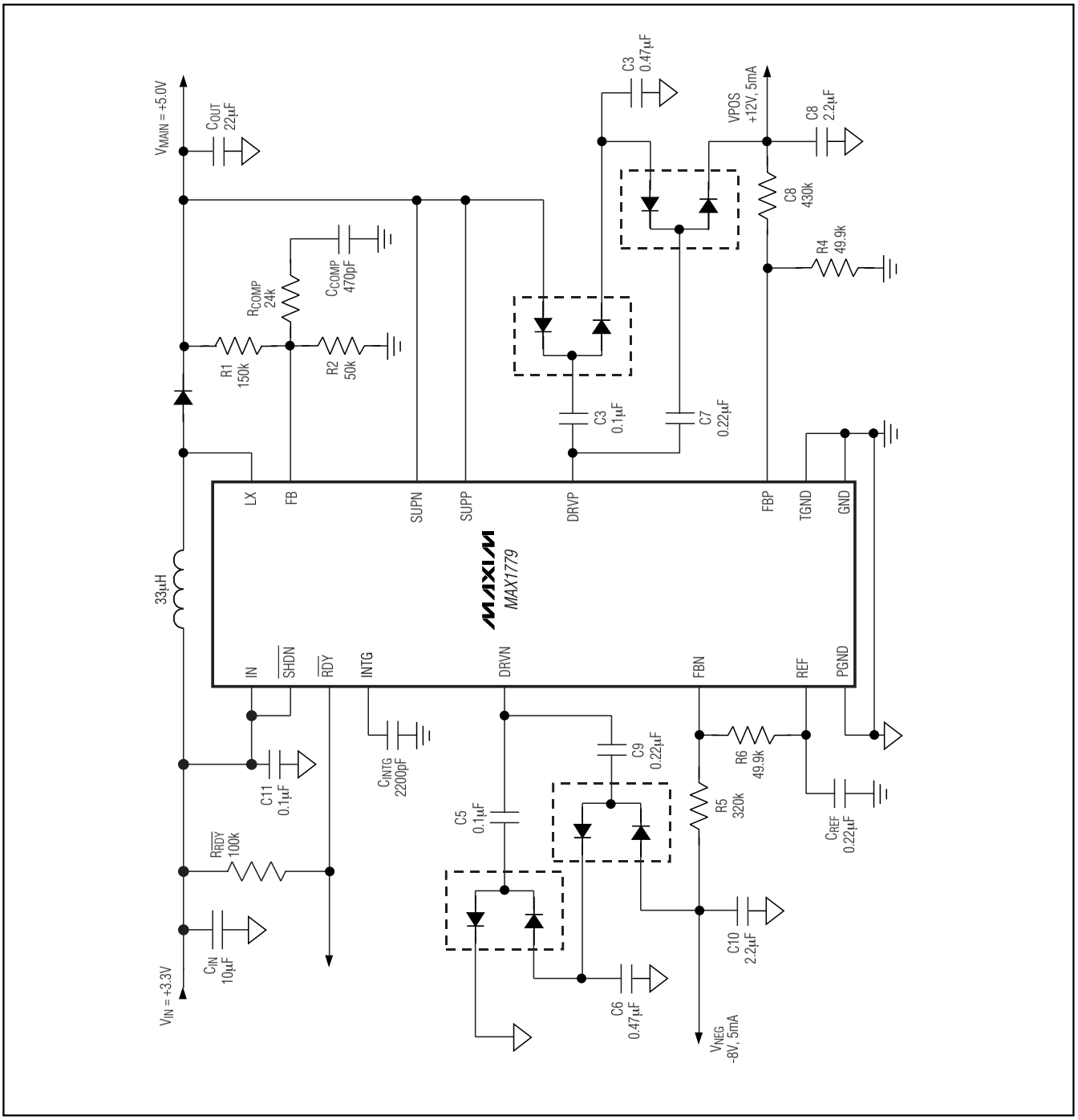


Figure 5. Typical Operating Circuit (L = 33µH)

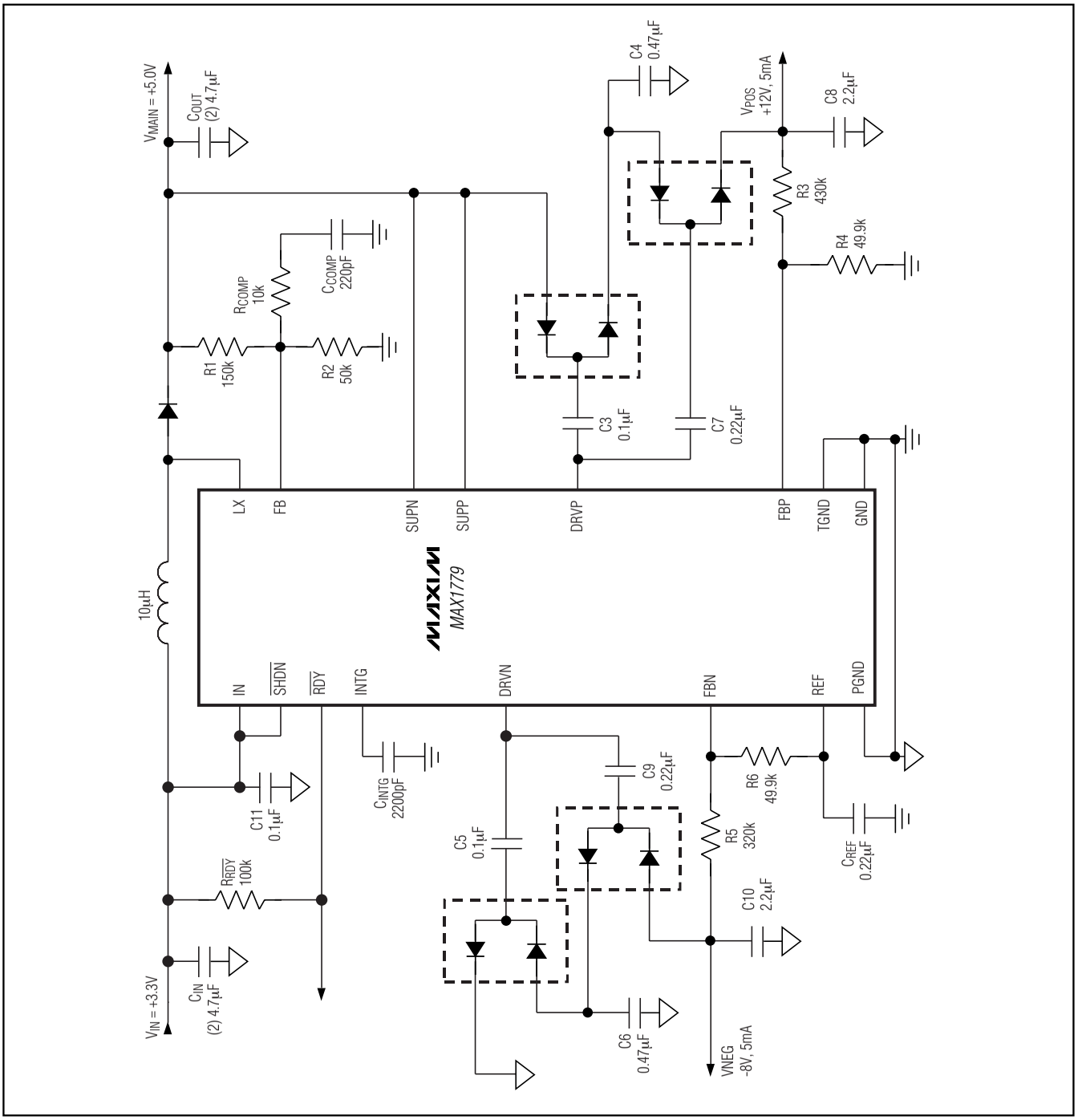


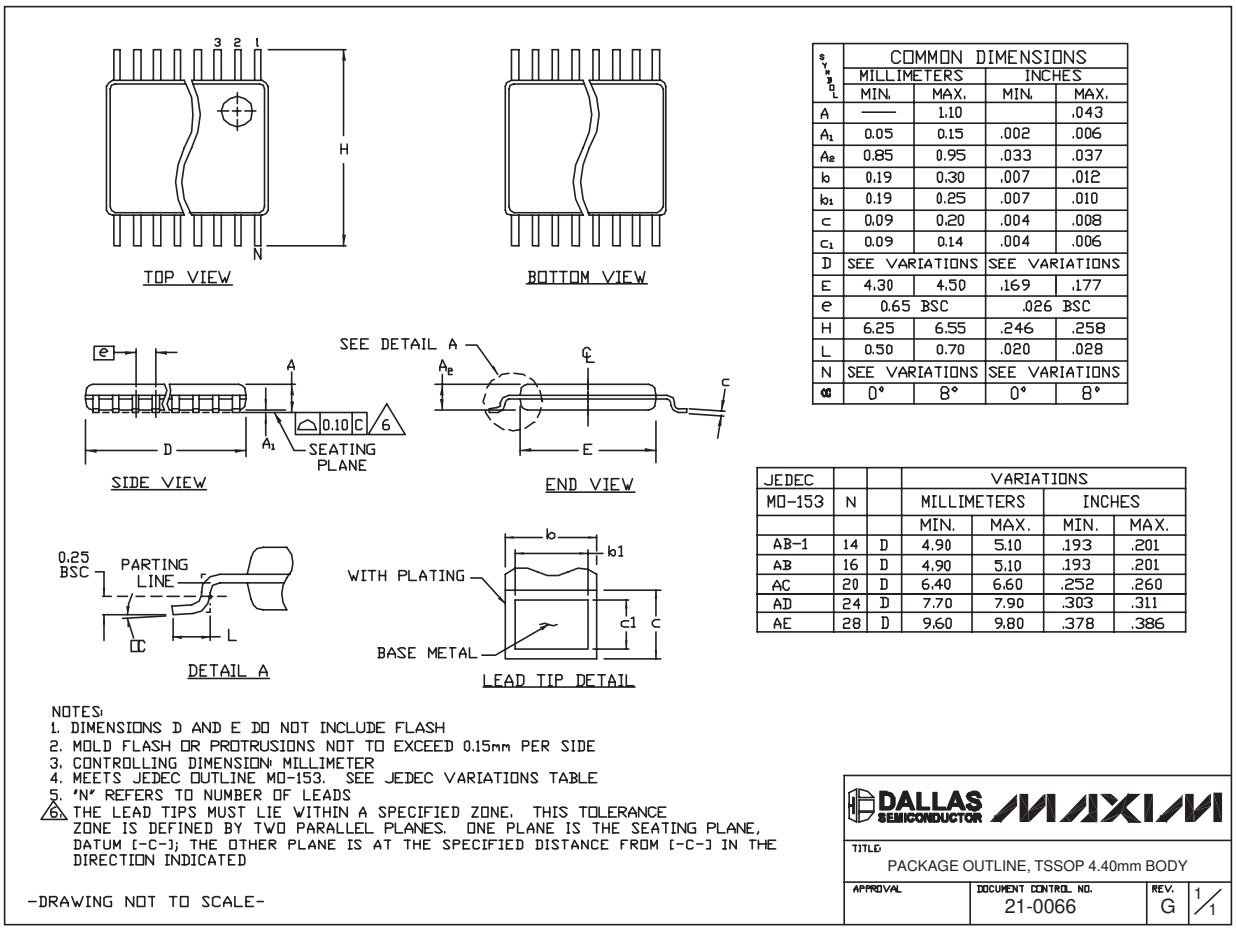
Figure 6. Typical Operating Circuit (L = 10µH)

Low-Power Triple-Output TFT LCD DC-DC Converter

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_e	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	G	1/1

Note: *The MAX1779 16-pin TSSOP package does not have an exposed pad.*