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MAX1778/ MAX1880–MAX1885
Quad-Output TFT LCD DC-DC Converters with Buffer

General Description

The MAX1778/MAX1880–MAX1885 multiple-output DC-DC converters provide the regulated voltages required by active matrix thin-film transistor (TFT) liquid crystal displays (LCD) in a low-profile TSSOP package. One high-power step-up converter and two low-power charge pumps convert the 2.7V to 5.5V input voltage into three independent output voltages. A built-in linear regulator and VCOM buffer complete the power-supply requirements.

The main step-up converter accurately generates an externally set output voltage up to 13V that can supply the display's row/column drivers. The converter's high switching frequency and current-mode PWM architecture provide fast transient response and allow the use of small low-profile inductors and ceramic capacitors. The low-power BiCMOS control circuitry and internal 14V switch (0.35Ω N-channel MOSFET) enable efficiencies up to 91%.

The dual low-power charge pumps (MAX1778/ MAX1880/MAX1881/MAX1882 only) independently regulate one positive output (V_{POS}) and one negative output (V_{NEG}). These low-power outputs use external diode and capacitor stages (as many stages as required) to regulate output voltages up to +40V and -40V. A unique control scheme minimizes output ripple as well as capacitor sizes for both charge pumps.

A resistor-programmable, 40mA, low-dropout linear regulator (MAX1778/MAX1881/MAX1883/MAX1884 only) provides preregulation or postregulation for any of the supplies. For higher current applications, an external transistor can be added. Additionally, the VCOM buffer provides a high current output that is ideal for driving the capacitive backplane of TFT LCD panels. The VCOM buffer's output voltage is preset with an internal 50% resistive-divider or can be externally adjusted for other voltages.

The MAX1778/MAX1880–MAX1885 are protected against output undervoltage and thermal overload conditions by a latched fault detection circuit that shuts down the device. All devices are available in the ultrathin TSSOP package (1.1mm max height).

Applications

TFT LCD Notebook Displays

TFT LCD Desktop Monitor Panels

Features

♦ **500kHz/1MHz Current-Mode PWM Step-Up Regulator**
    Up to +13V Main High-Power Output
    ±1% Accurate
    High Efficiency (91%)

♦ **Dual Regulated Charge-Pump Outputs (MAX1778/MAX1880–MAX1882 only)**
    Up to +40V Positive Charge-Pump Output
    Up to -40V Negative Charge-Pump Output

♦ **Low-Dropout 40mA Linear Regulator (MAX1778/MAX1881/MAX1883/MAX1884 only)**
    Up to +15V LDO Input

♦ **Optional Higher Current with External Transistor**

♦ **2.7V to 5.5V Input Supply**

♦ **Internal Supply Sequencing and Soft-Start**

♦ **Power-Ready Output**

♦ **Adjustable Fault-Detection Latch**

♦ **Thermal Protection (+160°C)**

♦ **0.1µA Shutdown Current**

♦ **0.7mA IN Quiescent Current**

♦ **Ultra-Small External Components**

♦ **Thin TSSOP Package (1.1mm max height)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1778EUG	-40°C to +85°C	24 TSSOP
MAX1778EUG+	-40°C to +85°C	24 TSSOP
MAX1880EUG	-40°C to +85°C	24 TSSOP
MAX1880EUG/V+	-40°C to +85°C	24 TSSOP
MAX1881EUG	-40°C to +85°C	24 TSSOP
MAX1882EUG	-40°C to +85°C	24 TSSOP
MAX1883EUP	-40°C to +85°C	20 TSSOP
MAX1884EUP	-40°C to +85°C	20 TSSOP
MAX1885EUP	-40°C to +85°C	20 TSSOP

+Denotes a lead(Pb)-free/RoHS-compliant package.
/V denotes an automotive qualified part.

Typical Operating Circuit appears at end of data sheet.

Pin Configurations and Selector Guide appear at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-1979; Rev 2; 10/12

MAX1778/MAX1880–MAX1885

Quad-Output TFT LCD DC/DC Converters with Buffer

ABSOLUTE MAXIMUM RATINGS

IN, $\overline{SHDN}$, TGND, FLTSET to GND............................-0.3V to +6V
DRVN to GND...-0.3V to (V_{SUPN} + 0.3V)
DRVP to GND...-0.3V to (V_{SUPP} + 0.3V)
PGND to GND...±0.3V
$\overline{RDY}$, SUPB to GND..-0.3V to +14V
LX, SUPP, SUPN to PGND ....-0.3V to +14V
SUPL to GND..-0.3V to +18V
LDOOUT to GND ....-0.3V to (V_{SUPL} + 0.3V)
INTG, REF, FB, FBN, FBP to GND...............-0.3V to (V_{IN} + 0.3V)
FBL to GND ....-0.3V to the lower of (V_{SUPL} + 0.3V) or +6V

BUFOUT, BUF+, BUF- to GND ....-0.3V to (V_{SUPB} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
   20-Pin TSSOP (derate 10.9mW/°C above +70°C) 879mW
   24-Pin TSSOP (derate 12.2mW/°C above +70°C) 975mW
Operating Temperature Range
   MAX1778EUG, MAX1883EUP ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply Range	V_{IN}			2.7		5.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} rising, 40mV hysteresis (typ)		2.2	2.4	2.6	V
IN Quiescent Supply Current	I_{IN}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V	MAX1778/MAX1880/ MAX1883 (f_{OSC} = 1MHz)		0.7	1	mA
			MAX1881/MAX1882/ MAX1884/MAX1885 (f_{OSC} = 500kHz)		0.6	1	
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = 1.5V	MAX1778/MAX1880 (f_{OSC} = 1MHz)		0.4	0.7	mA
			MAX1881/MAX1882 (f_{OSC} = 500kHz)		0.3	0.5	
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.2V	MAX1778/MAX1880 (f_{OSC} = 1MHz)		0.4	0.7	mA
			MAX1881/MAX1882 (f_{OSC} = 500kHz)		0.3	0.5	
IN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{IN} = 5V			0.1	10	µA
SUPP Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPP} = 13V, MAX1778/MAX1880/MAX1881/MAX1882			0.1	10	µA
SUPN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPN} = 13V, MAX1778/MAX1880/MAX1881/MAX1882			0.1	10	µA
SUPL Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPL} = 13V MAX1778/MAX1881/MAX1883/MAX1884			0.1	10	µA
SUPB Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPB} = 13V			6	13	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
MAIN STEP-UP CONVERTER							
Main Output Voltage Range	V_{MAIN}			V_{IN}		13	V
FB Regulation Voltage	V_{FB}	Integrator enabled, C_{INTG} = 1000pF		1.234	1.247	1.260	V
		Integrator disabled (INTG = REF)		1.220		1.280	
FB Input Bias Current	I_{FB}	V_{FB} = 1.25V, INTG = GND		-50		+50	nA
Operating Frequency	f_{OSC}	MAX1778/MAX1880/MAX1883		0.85	1	1.15	MHz
		MAX1881/MAX1882/MAX1884/MAX1885		425	500	575	kHz
Oscillator Maximum Duty Cycle				80	85	91	%
Load Regulation		I_{LX} = 0 to 200mA, V_{MAIN} = 10V	Integrator enabled, C_{INTG} = 1000pF		0.01		%
			Integrator disabled (INTG = REF)		0.2		
Line Regulation					0.1		%/V
Integrator Transconductance					317		µS
LX Switch On-Resistance	$R_{LX(ON)}$	I_{LX} = 100mA			0.35	0.7	Ω
LX Leakage Current	I_{LX}	V_{LX} = 13V			0.01	20	µA
LX Current Limit	I_{LIM}	Phase I = soft-start (1024/f_{OSC})		0.275	0.38	0.5	A
		Phase II = soft-start (1024/f_{OSC})			0.75		
		Phase III = soft-start (1024/f_{OSC})			1.12		
		Phase IV = fully on (after 3072/f_{OSC})		1.15	1.5	1.85	
Maximum RMS LX Current					1		A
Soft-Start Period	t_{SS}	Power-up to the end of Phase III			3072 / f_{OSC}		s
FB Fault Trip Level		Falling edge, FLTSET = GND		1.07	1.1	1.14	V
		Falling edge, FLTSET = 1V		0.955	0.99	1.025	
POSITIVE CHARGE PUMP (MAX1778/MAX1880/MAX1881/MAX1882 only)							
SUPP Input Supply Range	V_{SUPP}			2.7		13	V
Operating Frequency	f_{CHP}				0.5 x f_{OSC}		Hz
FBP Regulation Voltage	V_{FBP}			1.2	1.25	1.3	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.5V		-50		+50	nA
DRVP PCH On-Resistance	$R_{PCH(ON)}$				5	10	Ω
DRVP NCH On-Resistance	$R_{NCH(ON)}$	V_{FBP} = 1.2V			2	4	Ω
		V_{FBP} = 1.3V		20			kΩ
Maximum RMS DRVP Current					0.1		A
FBP Power-Ready Trip Level		Rising edge		1.09	1.125	1.16	V
FBP Fault Trip Level		Falling edge, FLTSET = GND		1.08	1.11	1.16	V
		Falling edge, FLTSET = 1V		0.955	0.99	1.025	

MAX1778/MAX1880–MAX1885

Quad-Output TFT LCD DC/DC Converters with Buffer

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
NEGATIVE CHARGE PUMP (MAX1778/MAX1880/MAX1881/MAX1882 only)							
SUPN Input Supply Range	V_{SUPN}			2.7		13	V
Operating Frequency	f_{CHP}				0.5 x f_{OSC}		Hz
FBN Regulation Voltage	V_{FBN}			-50	0	+50	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = 0		-50		+50	nA
DRVN PCH On-Resistance	$R_{PCH(ON)}$				5	10	Ω
DRVN NCH On-Resistance	$R_{NCH(ON)}$	V_{FBN} = +50mV			2	4	Ω
		V_{FBN} = -50mV		20			kΩ
Maximum RMS DRVN Current					0.1		A
FBN Power-Ready Trip Level		Falling edge		80	125	165	mV
FBN Fault Trip Level		Rising edge		80	140	190	mV
LOW-DROPOUT LINEAR REGULATOR (MAX1778/MAX1881/MAX1883/MAX1884 only)							
SUPL Input Supply Range	V_{SUPL}			4.5		15	V
SUPL Undervoltage Lockout		Rising edge, 50mV hysteresis (typ)		3.8	4	4.3	V
SUPL Quiescent Current	I_{SUPL}	I_{LDO} = 100µA			120	220	µA
Dropout Voltage (Note 1)	V_{DROP}	LDO is set to regulate at 9V	I_{LDO} = 40mA		130	300	mV
			I_{LDO} = 5mA		70		
FBL Regulation Voltage	V_{FBL}	V_{SUPL} = 10V, LDO regulating at 9V, I_{LDO} = 15mA		1.235	1.25	1.265	V
LDO Load Regulation		V_{SUPL} = 10V, LDO regulating at 9V, I_{LDO} = 100µA to 40mA				1.2	%
LDO Line Regulation		V_{SUPL} = 4.5V to 15V, FBL = LDOOUT, I_{LDO} = 15mA				0.02	%/V
FBL Input Bias Current	I_{FBL}	V_{FBL} = 1.25V		-0.8		+0.8	µA
LDO Current Limit	I_{LDOLIM}	V_{SUPL} = 10V, V_{LDOOUT} = 9V, V_{FBL} = 1.2V		40	130	220	mA
VCOM BUFFER							
SUPB Input Supply Range	V_{SUPB}			4.5		13	V
SUPB Quiescent Current	I_{SUPB}	V_{SUPB} = 13V			420	850	µA
BUFOUT Leakage Current				-10		+10	µA
Power-Supply Rejection Ratio	PSRR	V_{SUPB} = 4.5V to 13V, V_{CM} = 2.25V		85	98		dB
Input Common-Mode Voltage Range	V_{CM}	$|V_{OS}|$ < 10mV		1.2		8.8	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 1.2V to 8.8V		75			dB
Input Bias Current	I_{BIAS}	V_{CM} = 5V		-100	-10	+100	nA
Input Offset Current	I_{OS}	V_{CM} = 5V		-100		+100	nA
Gain Bandwidth Product	GBW	C_{BUF} = 1µF			13		kHz

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = 0°C to +85°C**. Typical values are at T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage	V_{BUFOUT}	BUF+ = GND	I_{BUFOUT} = 0	4.99		5.01	V
			I_{BUFOUT} = ±5mA	4.97		5.03	
			I_{BUFOUT} = ±45mA	4.93		5.07	
Input Offset Voltage	V_{OS}	V_{SUPB} = 4.5V to 13V, V_{CM} = 1.2V to (V_{SUPB} - 1.2V)	I_{BUFOUT} = ±5mA	-30		+30	mV
			I_{BUFOUT} = ±45mA	-70		+70	
Output Voltage Swing High	V_{OH}	I_{BUFOUT} = -45mA, ΔV_{OS} = 1V	9	9.6		V
Output Voltage Swing Low	V_{OL}	I_{BUFOUT} = +45mA, ΔV_{OS} = 1V		0.4	1	V
Peak Buffer Output Current					±150		mA
BUF+ Dual Mode™ Threshold Voltage		Falling edge, 20mV hysteresis (typ)		80	125	170	mV
REFERENCE							
Reference Voltage	V_{REF}	-2µA < I_{REF} < 50µA		1.231	1.25	1.269	V
Reference Undervoltage Threshold				0.9	1.05	1.2	V
LOGIC SIGNALS							
$\overline{SHDN}$ Input Low Voltage						0.9	V
$\overline{SHDN}$ Input High Voltage				2.1			V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$				0.01	1	µA
FLTSET Input Voltage Range				0.67 x V_{REF}		0.85 x V_{REF}	V
FLTSET Threshold Voltage		Rising edge, 25mV hysteresis (typ)		80	125	170	mV
FLTSET Input Current		V_{FLTSET} = 1V			0.1	50	nA
$\overline{RDY}$ Output Low Voltage		I_{SINK} = 2mA			0.25	0.5	V
$\overline{RDY}$ Output High Leakage		$V_{\overline{RDY}}$ = 13V			0.01	1	µA
Thermal Shutdown		Rising temperature			160		°C

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MAX1778/MAX1880–MAX1885

Quad-Output TFT LCD DC/DC Converters with Buffer

ELECTRICAL CHARACTERISTICS

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Input Supply Range	V_{IN}			2.7	5.5	V
Input Undervoltage Threshold	V_{UVLO}	V_{IN} Rising, 40mV hysteresis (typ)		2.2	2.6	V
IN Quiescent Supply Current	I_{IN}	V_{FB} = V_{FBP} = 1.5V, V_{FBN} = -0.2V	MAX1778/MAX1880/ MAX1883 (f_{OSC} = 1MHz)		1	mA
			MAX1881/MAX1882/MAX1884/ MAX1885 (f_{OSC} = 500kHz)		1	
SUPP Quiescent Current	I_{SUPP}	V_{FBP} = 1.5V	MAX1778/MAX1880 (f_{OSC} = 1MHz)		0.7	mA
			MAX1881/MAX1882 (f_{OSC} = 500kHz)		0.5	
SUPN Quiescent Current	I_{SUPN}	V_{FBN} = -0.2V	MAX1778/MAX1880 (f_{OSC} = 1MHz)		0.7	mA
			MAX1881/MAX1882 (f_{OSC} = 500kHz)		0.5	
IN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{IN} = 5V			10	µA
SUPP Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPP} = 13V, MAX1778/MAX1880/MAX1881/MAX1882			10	µA
SUPN Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPN} = 13V, MAX1778/MAX1880/MAX1881/MAX1882			10	µA
SUPL Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPL} = 13V, MAX1778/MAX1881/MAX1883/MAX1884			10	µA
SUPB Shutdown Current		$V_{\overline{SHDN}}$ = 0, V_{SUPB} = 13V			13	µA
MAIN STEP-UP CONVERTER						
Main Output Voltage Range	V_{MAIN}			V_{IN}	13	V
FB Regulation Voltage	V_{FB}	Integrator enabled, C_{INTG} = 1000pF		1.223	1.269	V
		Integrator disabled (INTG = REF)		1.21	1.29	
FB Input Bias Current	I_{FB}	V_{FB} = 1.25V, INTG = GND		-50	+50	nA
Operating Frequency	F_{OSC}	MAX1778/MAX1880/MAX1883		0.75	1.25	MHz
		MAX1881/MAX1882/MAX1884/MAX1885		375	625	kHz
Oscillator Maximum Duty Cycle				79	91	%
LX Switch On-Resistance	$R_{LX(ON)}$	I_{LX} = 100mA			0.7	Ω
LX Leakage Current	I_{LX}	V_{LX} = 13V			20	µA
LX Current Limit	I_{LIM}	Phase I = soft-start (1024/f_{OSC})		0.275	0.525	A
		Phase IV = fully on (after 3072/f_{OSC})		1.1	2.05	
FB Fault Trip Level		Falling edge, FLTSET = GND		1.07	1.14	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
POSITIVE CHARGE PUMP (MAX1778/MAX1880/MAX1881/MAX1882 only)					
SUPP Input Supply Range	V_{SUPP}		2.7	13	V
FBP Regulation Voltage	V_{FBP}		1.2	1.3	V
FBP Input Bias Current	I_{FBP}	V_{FBP} = 1.5V	-50	+50	nA
DRVP PCH On-Resistance	$R_{PCH(ON)}$			10	Ω
DRVP NCH On-Resistance	$R_{NCH(ON)}$	V_{FBP} = 1.2V		4	Ω
		V_{FBP} = 1.3V	20		kΩ
FBP Power-Ready Trip Level		Rising edge	1.09	1.16	V
NEGATIVE CHARGE PUMP (MAX1778/MAX1880/MAX1881/MAX1882 only)					
SUPN Input Supply Range	V_{SUPN}		2.7	13	V
FBN Regulation Voltage	V_{FBN}		-50	+50	mV
FBN Input Bias Current	I_{FBN}	V_{FBN} = 0	-50	+50	nA
DRVN PCH On-Resistance	$R_{PCH(ON)}$			10	Ω
DRVN NCH On-Resistance	$R_{NCH(ON)}$	V_{FBN} = +50mV		4	Ω
		V_{FBN} = -50mV	20		kΩ
FBN Power-Ready Trip Level		Falling edge	80	165	mV
LOW DROPOUT LINEAR REGULATOR (MAX1778/MAX1881/MAX1883/MAX1884 only)					
SUPL Input Supply Range	V_{SUPL}		4.5	15	V
SUPL Undervoltage Lockout		Rising edge, 50mV hysteresis (typ)	3.8	4.3	V
SUPL Quiescent Current	I_{SUPL}	I_{LDO} = 100µA		240	µA
Dropout Voltage (Note 1)	V_{DROP}	LDO regulating to 9V, I_{LDO} = 40mA		330	mV
FBL Regulation Voltage	V_{FBL}	V_{SUPL} = 10V, LDO regulating to 9V, I_{LDO} = 15mA	1.222	1.265	V
LDO Load Regulation		V_{SUPL} = 10V, LDO regulating to 9V, I_{LDO} = 100µA to 40mA		1.2	%
LDO Line Regulation		V_{SUPL} = 4.5V to 15V, FBL = LDOOUT, I_{LDO} = 15mA		0.02	%/V
FBL Input Bias Current	I_{FBL}	V_{FBL} = 1.25V	-1.2	+1.2	µA
LDO Current Limit	I_{LDOLIM}	V_{SUPL} = 10V, V_{LDOOUT} = 9V, V_{FBL} = 1.2V	40	260	mA
VCOM BUFFER					
SUPB Input Supply Range	V_{SUPB}		4.5	13	V
SUPB Quiescent Current	I_{SUPB}	V_{SUPB} = 13V		850	µA
BUFOUT Leakage Current			-10	+10	µA
Input Common-Mode Voltage	V_{CM}	$|V_{OS}|$ < 10mV	1.2	8.8	V

Quad-Output TFT LCD DC/DC Converters with Buffer

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = +3.0V, $\overline{SHDN}$ = IN, V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 10V, LDOOUT = FBL, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, C_{REF} = 0.22µF, C_{BUF} = 1µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	MAX	UNITS
Input Bias Current	I_{BIAS}	V_{CM} = 5V		-500	+500	nA
Input Offset Current	I_{OS}	V_{CM} = 5V		-500	+500	nA
Output Voltage	V_{BUFOUT}	BUF+ = GND	I_{BUFOUT} = 0	4.988	5.012	V
			I_{BUFOUT} = ±5mA	4.97	5.03	
			I_{BUFOUT} = ±45mA	4.93	5.07	
Input Offset Voltage	V_{OS}	V_{SUPB} = 4.5V to 13V V_{CM} = 1.2V to (V_{SUPB} - 1.2V)	I_{BUFOUT} = ±5mA	-30	+30	mV
			I_{BUFOUT} = ±45mA	-70	+70	
Output Voltage Swing High	V_{OH}	I_{BUFOUT} = -45mA, ΔV_{OS} = 1V		9		V
Output Voltage Swing Low	V_{OL}	I_{BUFOUT} = +45mA, ΔV_{OS} = 1V			1	V
BUF+ Dual-Mode Threshold Voltage		Falling edge, 20mV hysteresis (typ)		80	170	mV
REFERENCE						
Reference Voltage	V_{REF}	-2µA < I_{REF} < 50µA		1.223	1.269	V
Reference Undervoltage Threshold				0.9	1.2	V
LOGIC SIGNALS						
$\overline{SHDN}$ Input Low Voltage					0.9	V
$\overline{SHDN}$ Input High Voltage				2.1		V
$\overline{SHDN}$ Input Current	$I_{\overline{SHDN}}$				1	µA
FLTSET Input Voltage Range				0.74 x V_{REF}	0.85 x V_{REF}	V
FLTSET Threshold Voltage		Rising edge, 25mV hysteresis (typ)		80	170	mV
FLTSET Input Current		V_{FLTSET} = 1V			50	nA
$\overline{RDY}$ Output Low Voltage		I_{SINK} = 2mA			0.5	V
$\overline{RDY}$ Output High Leakage		$V_{\overline{RDY}}$ = 13V			1	µA

Note 1: Dropout voltage is defined as the V_{SUPL} - V_{LDOOUT}, when V_{SUPL} is 100mV below the set value of V_{LDOOUT}.
Note 2: Specifications to -40°C are guaranteed by design, not production tested.

Typical Operating Characteristics

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)


MAIN 8V OUTPUT VOLTAGE vs. LOAD CURRENT
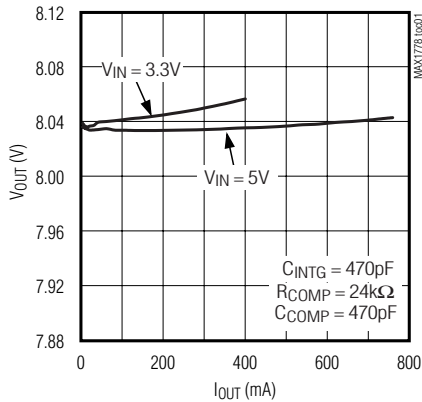
MAIN 8V OUTPUT EFFICIENCY vs. LOAD CURRENT
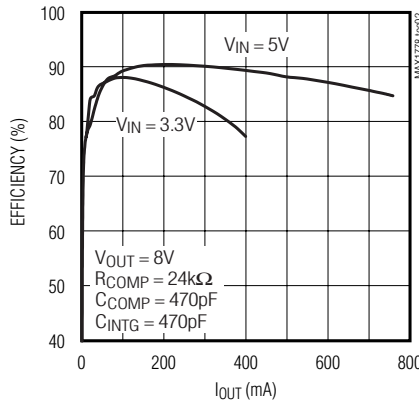
MAIN 12V OUTPUT VOLTAGE vs. LOAD CURRENT
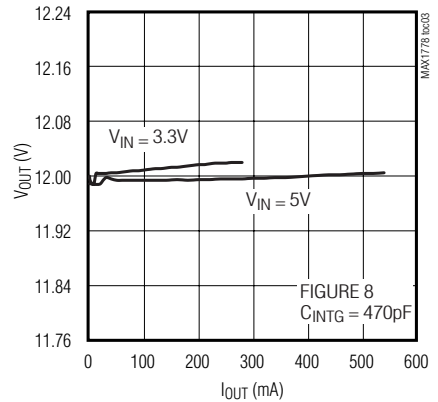
MAIN 12V OUTPUT EFFICIENCY vs. LOAD CURRENT
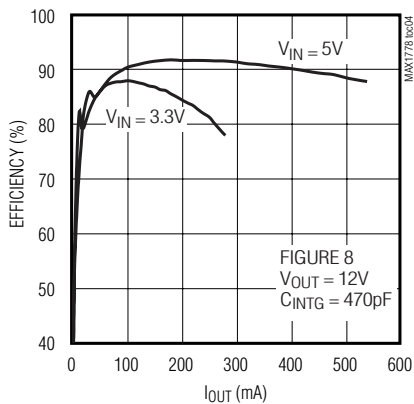
STEP UP CONVERTERS SWITCHING FREQUENCY vs. INPUT VOLTAGE
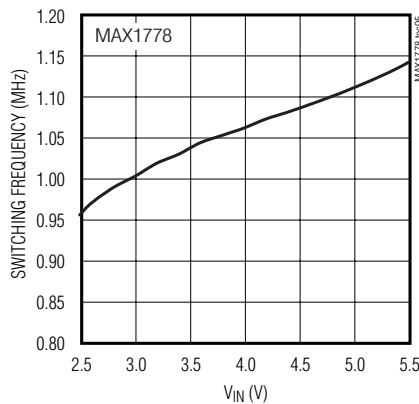
POSITIVE CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT
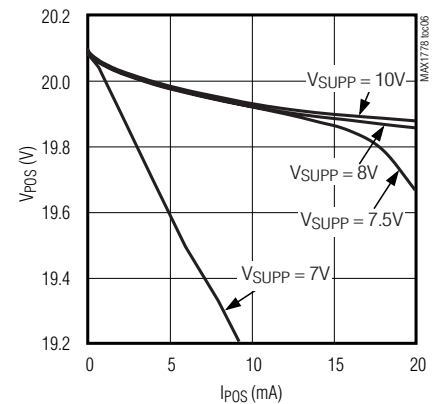
POSITIVE CHARGE-PUMP EFFICIENCY vs. LOAD CURRENT
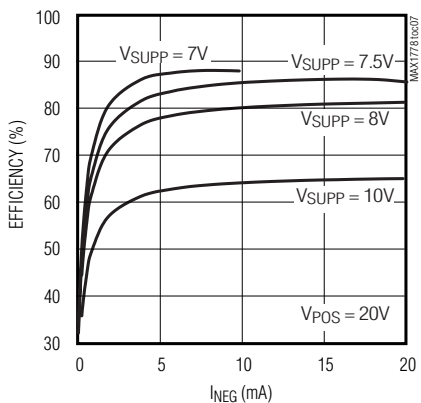
MAXIMUM POSITIVE CHARGE-PUMP OUTPUT VOLTAGE vs. SUPPLY VOLTAGE
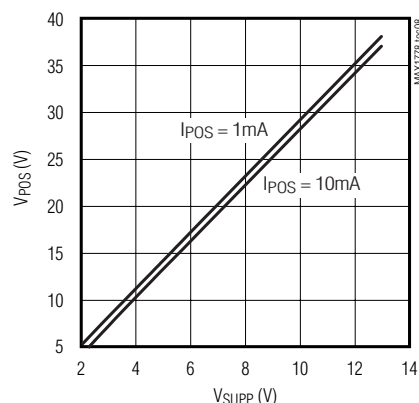
NEGATIVE CHARGE-PUMP OUTPUT VOLTAGE vs. LOAD CURRENT
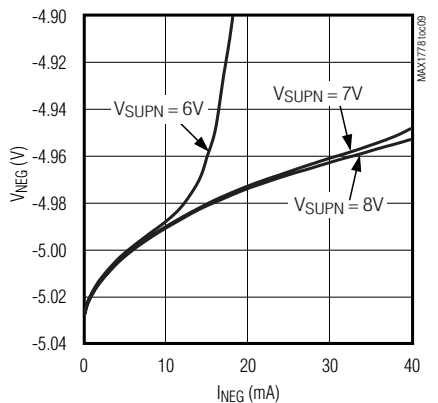
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Quad-Output TFT LCD DC/DC Converters with Buffer

_____Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)

NEGATIVE CHARGE-PUMP EFFICIENCY vs. LOAD CURRENT
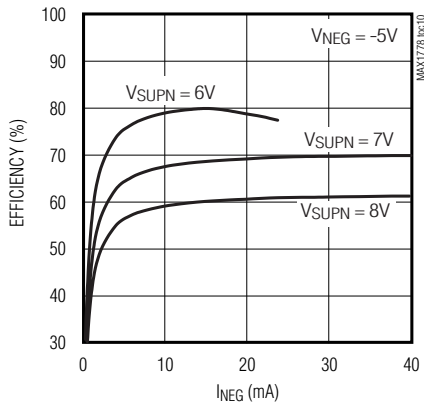
MAXIMUM NEGATIVE CHARGE-PUMP OUTPUT VOLTAGE vs. SUPPLY VOLTAGE
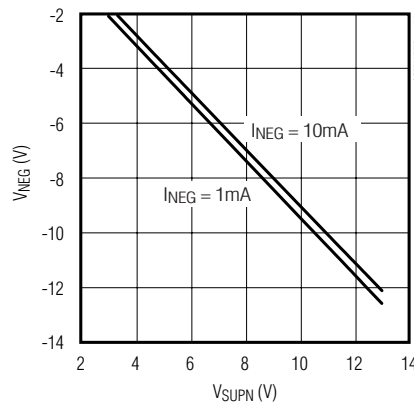
REFERENCE VOLTAGE vs. REFERENCE LOAD CURRENT
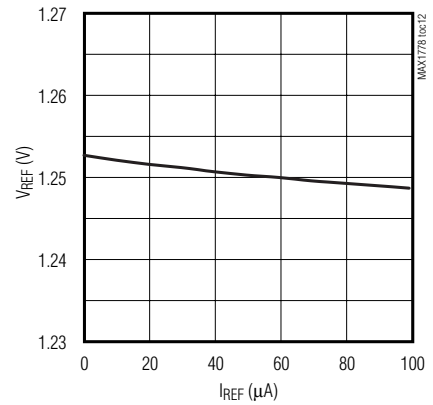
STEP-UP CONVERTER LOAD-TRANSIENT RESPONSE
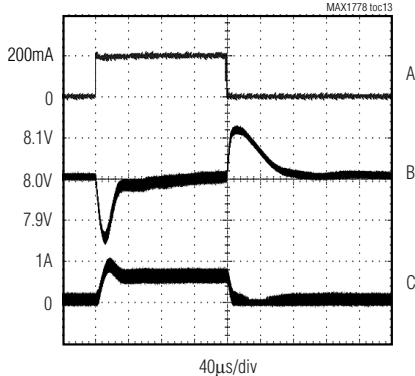
A. I_{MAIN} = 20mA to 200mA, 200mA/div
B. V_{MAIN} = 8V, 100mV/div
C. INDUCTOR CURRENT, 1A/div
C_{INTG} = 1000pF

STEP-UP CONVERTER LOAD-TRANSIENT RESPONSE WITHOUT INTEGRATOR
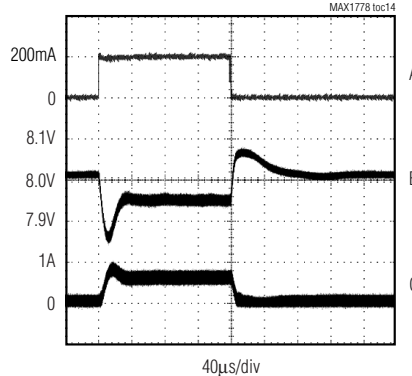
A. I_{MAIN} = 20mA to 200mA, 200mA/div
B. V_{MAIN} = 8V, 100mV/div
C. INDUCTOR CURRENT, 1A/div
INTG = REF

STEP-UP CONVERTER LOAD-TRANSIENT RESPONSE (1µs PULSES)
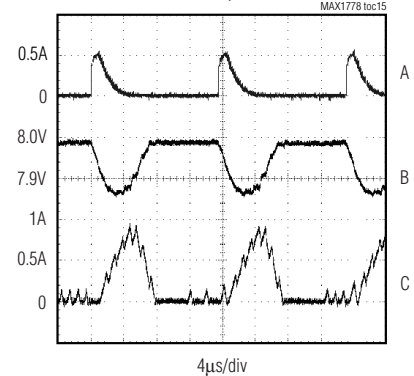
A. I_{MAIN} = 0 to 500mA, 500mA/div
B. V_{MAIN} = 8V, 100mV/div
C. INDUCTOR CURRENT, 500mA/div

Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_IN = +3.3V, $\overline{SHDN}$ = IN, V_MAIN = V_SUPP = V_SUPN = V_SUPB = V_SUPL = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)
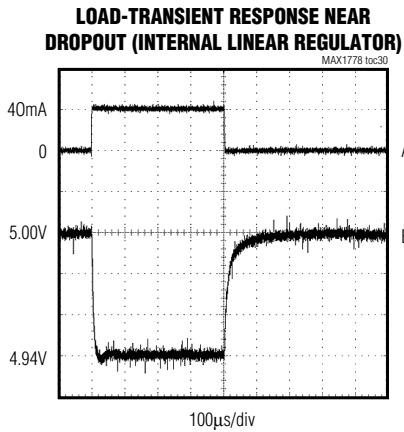
RIPPLE VOLTAGE WAVEFORMS
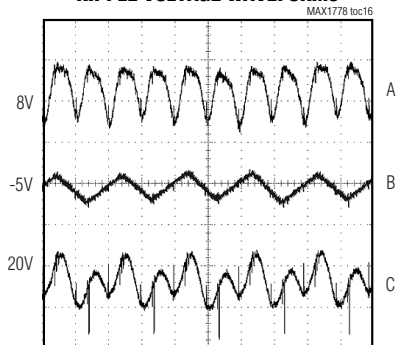
A. V_MAIN = 8V, I_MAIN = 200mA, 10mV/div
B. V_NEG = -5V, I_NEG = 10mA, 20mV/div
C. V_POS = 20V, I_POS = 5mA, 20mV/div

STEP-UP CONVERTER SOFT-START (LIGHT LOAD)
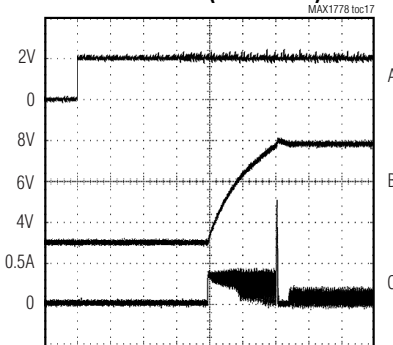
A. V$\overline{SHDN}$ = 0 TO 2V, 2V/div
B. V_MAIN = 8V, 2V/div
C. INDUCTOR CURRENT, 500mA/div
R_LOAD = 400Ω

STEP-UP CONVERTER SOFT-START (HEAVY LOAD)
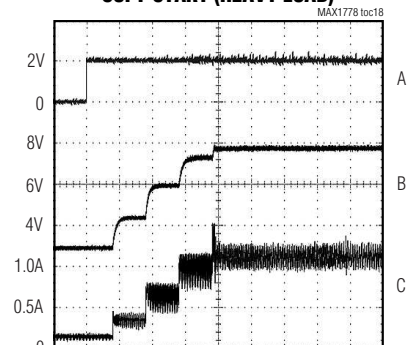
A. V$\overline{SHDN}$ = 0 TO 2V, 2V/div
B. V_MAIN = 8V, 2V/div
C. INDUCTOR CURRENT, 500mA/div
R_LOAD = 20Ω
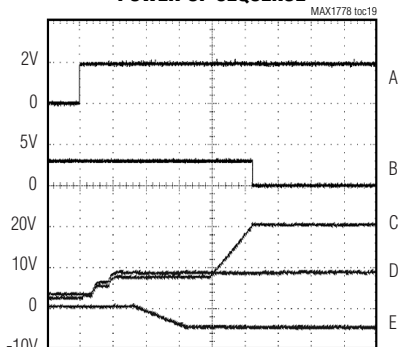
POWER-UP SEQUENCE

A. V$\overline{SHDN}$ = 0 TO 2V, 2V/div
B. $\overline{RDY}$, 5V/div
C. POSITIVE CHARGE PUMP = V_POS = 20V, R_LOAD = 4kΩ, 10V/div
D. STEP-UP CONVERTER: V_MAIN = 8V, R_LOAD = 40Ω, 10V/div
E. NEGATIVE CHARGE PUMP: V_NEG = -5V, R_LOAD = 500Ω, 10V/div

POWER-UP SEQUENCE (CIRCUIT OF FIGURE 10)
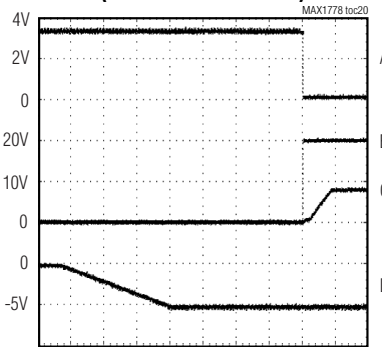
A. $\overline{RDY}$, 2V/div
B. POSITIVE CHARGE PUMP, V_POS(SYS) = 20V, 10V/div
C. STEP-UP CONVERTER: V_MAIN(SYS) = 8V, 10V/div
D. NEGATIVE CHARGE PUMP, V_NEG = -5V, -5V/div

POWER-UP INTO SHORT-CIRCUIT (CIRCUIT OF FIGURE 10)
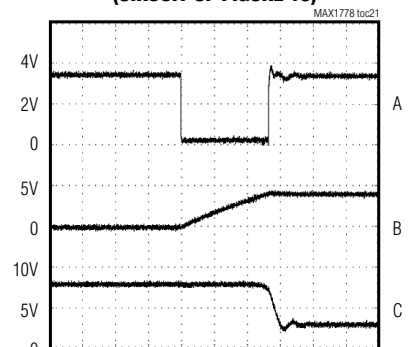
A. $\overline{RDY}$, 2V/div
B. GATE OF N-CH MOSFET, 5V/div
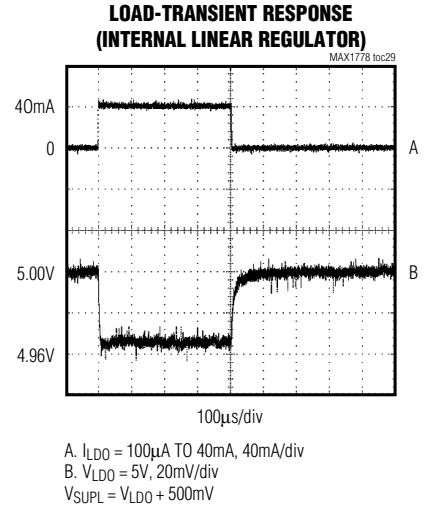C. STEP-UP CONVERTER, V_MAIN(START) = 8V, 5V/div
V_MAIN(SYS) = GND

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Quad-Output TFT LCD DC/DC Converters with Buffer

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)
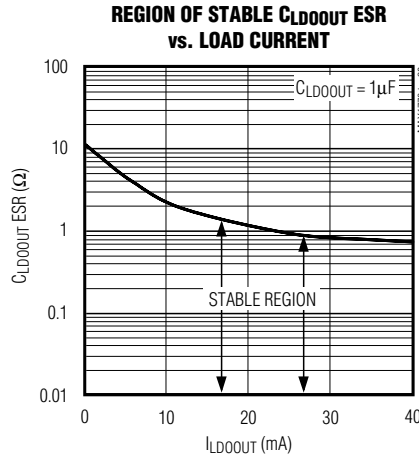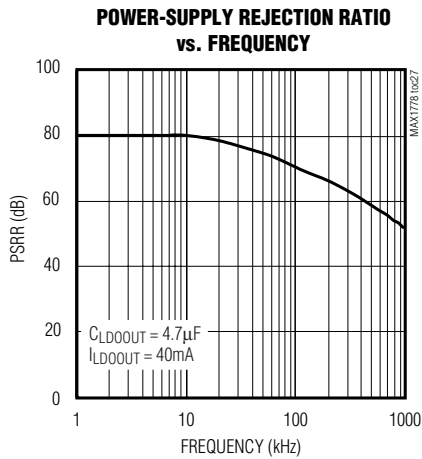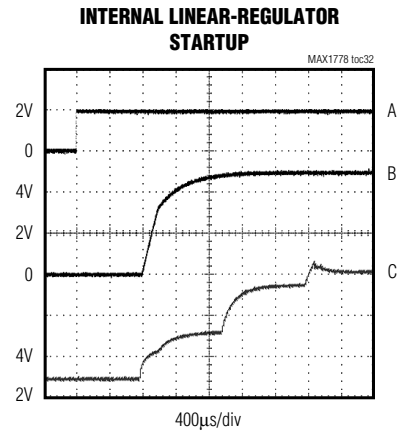

LDO OUTPUT VOLTAGE
vs. LDO INPUT VOLTAGE
(INTERNAL LINEAR REGULATOR)

LDO OUTPUT VOLTAGE
vs. LDO OUTPUT CURRENT
(INTERNAL LINEAR REGULATOR)

LDO OUTPUT VOLTAGE vs. TEMPERATURE
(INTERNAL LINEAR REGULATOR)

DROPOUT VOLTAGE
vs. LDO LOAD CURRENT
(INTERNAL LINEAR REGULATOR)

LDO SUPPLY CURRENT
vs. LDO OUTPUT CURRENT
(INTERNAL LINEAR REGULATOR)

Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)

POWER-SUPPLY REJECTION RATIO vs. FREQUENCY

REGION OF STABLE C_{LDOOUT} ESR vs. LOAD CURRENT

LOAD-TRANSIENT RESPONSE (INTERNAL LINEAR REGULATOR)

A. I_{LDO} = 100µA TO 40mA, 40mA/div
B. V_{LDO} = 5V, 20mV/div
V_{SUPL} = V_{LDO} + 500mV

LOAD-TRANSIENT RESPONSE NEAR DROPOUT (INTERNAL LINEAR REGULATOR)
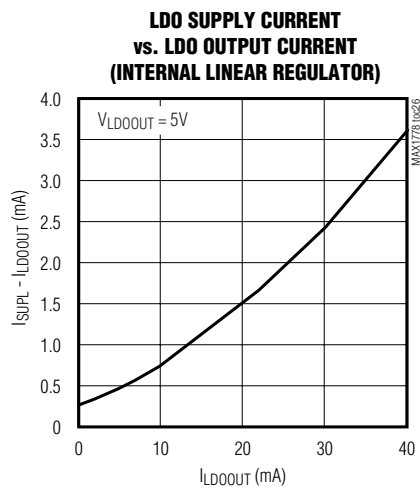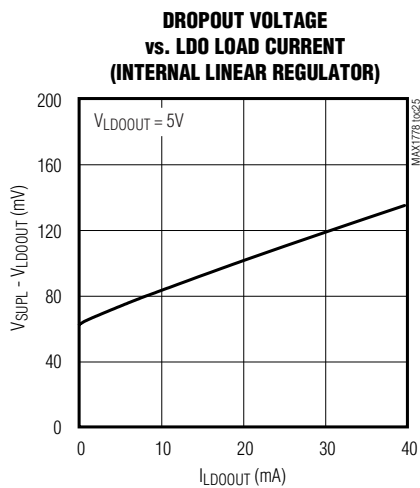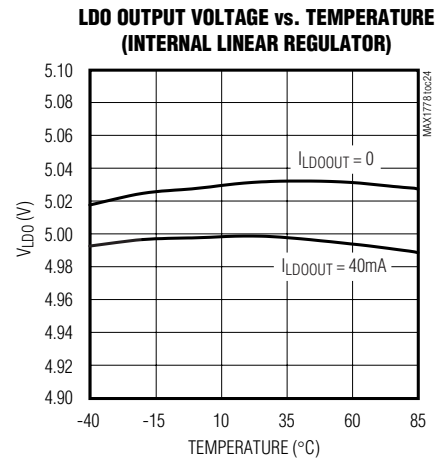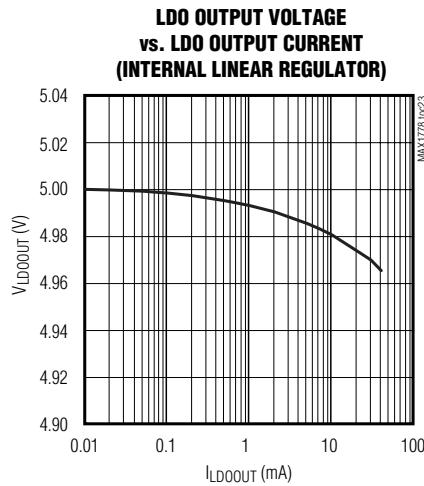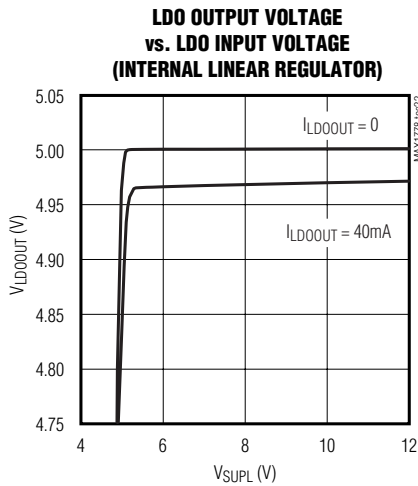
A. I_{LDO} = 100µA TO 40mA, 40mA/div
B. V_{LDO} = 5V, 20mV/div
V_{IN} = V_{LDO} + 100mV

INTERNAL LINEAR-REGULATOR RIPPLE REJECTION
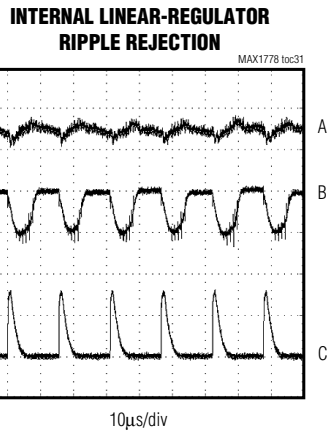
A. V_{LDOOUT} = 5V, I_{LDOOUT} = 40mA, 10mV/div
B. V_{MAIN} = V_{SUPL} = 8V, 200mV/div
C. I_{MAIN} = 0 TO 750mA, 500mA/div

INTERNAL LINEAR-REGULATOR STARTUP

A. $V_{\overline{SHDN}}$ = 0 TO 2V, 2V/div
B. V_{LDOOUT} = 5V, R_{LDOOUT} = 125Ω, 2V/div
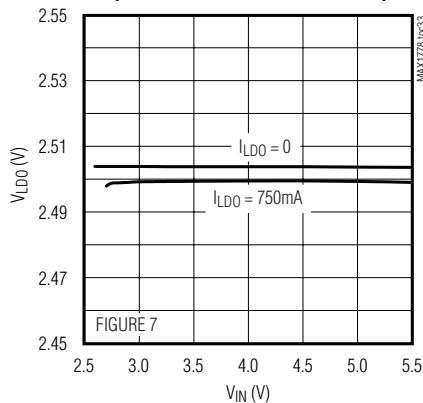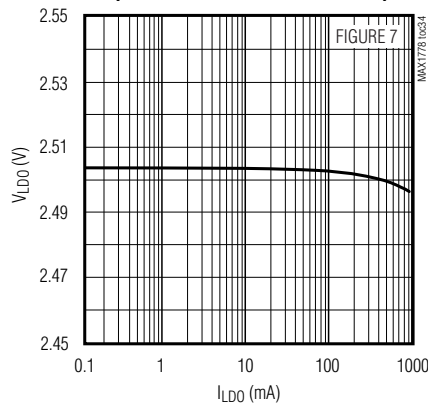C. V_{MAIN} = 8V, R_{MAIN} = 40Ω, 2V/div

Quad-Output TFT LCD DC/DC Converters with Buffer

_____Typical Operating Characteristics (continued)_

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)
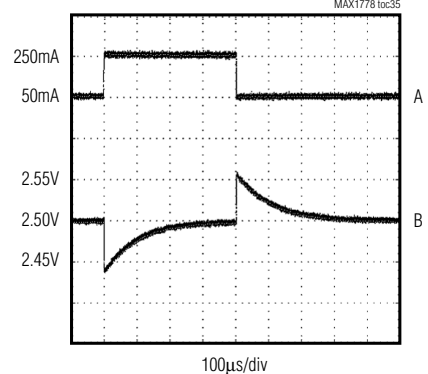
LINEAR-REGULATOR OUTPUT VOLTAGE vs. INPUT VOLTAGE (EXTERNAL LINEAR REGULATOR)

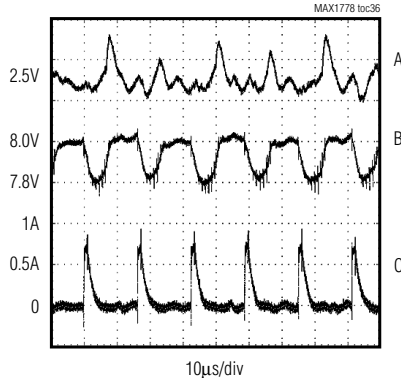### LINEAR-REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT (EXTERNAL LINEAR REGULATOR)
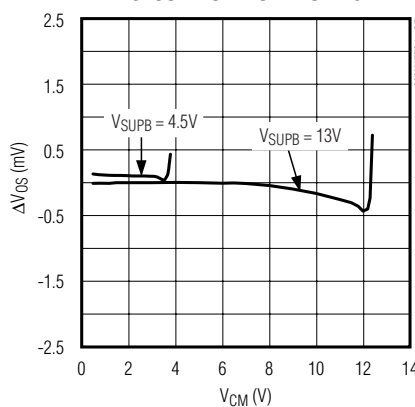

EXTERNAL LINEAR-REGULATOR LOAD-TRANSIENT RESPONSE

A. I_{LDO} = 50mA TO 250mA, 200mA/div
B. V_{LDO} = 2.5V, 50mV/div
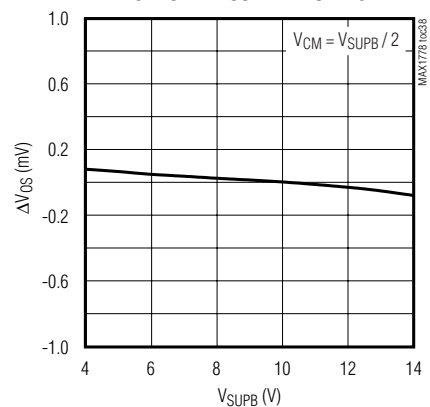FIGURE 7

EXTERNAL LINEAR-REGULATOR RIPPLE REJECTION

A. V_{LDO} = 2.5V, I_{LDO} = 200mA, 10mV/div
B. V_{MAIN} = V_{SUPL} = 8V, 200mV/div
C. I_{MAIN} = 0 TO 750mA, 500mA/div
FIGURE 7

INPUT OFFSET VOLTAGE DEVIATION vs. COMMON-MODE VOLTAGE

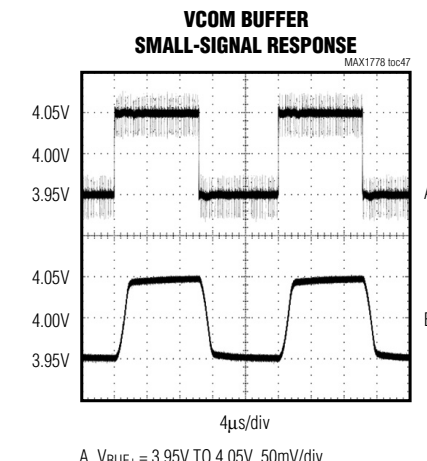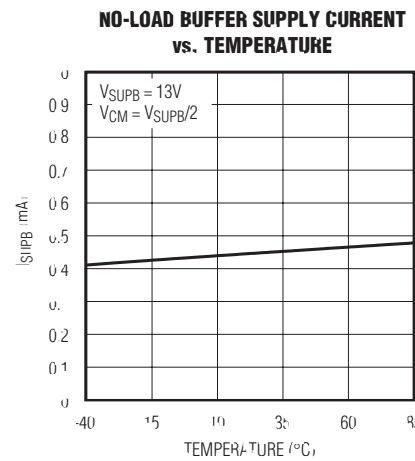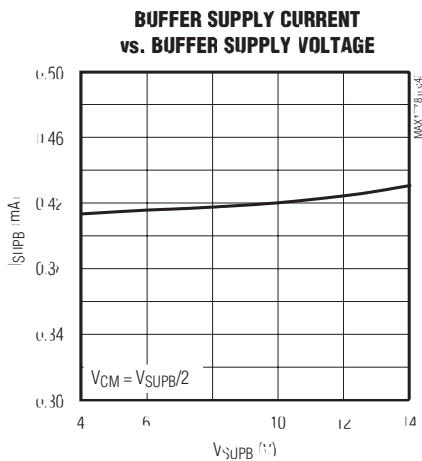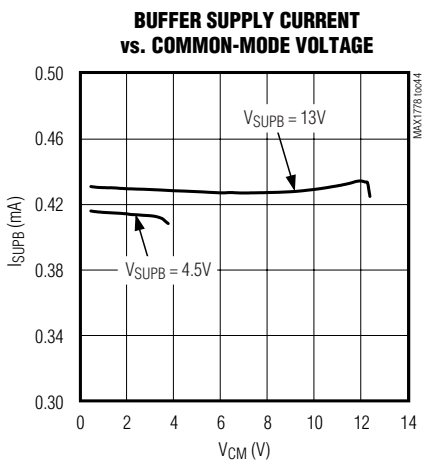### INPUT OFFSET VOLTAGE DEVIATION vs. BUFFER SUPPLY VOLTAGE

Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)

INPUT OFFSET VOLTAGE DEVIATION vs. TEMPERATURE

INPUT OFFSET VOLTAGE DEVIATION vs. TEMPERATURE

BUFFER INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE

BUFFER INPUT BIAS CURRENT vs. BUFFER SUPPLY VOLTAGE

BUFFER INPUT BIAS CURRENT vs. TEMPERATURE

BUFFER SUPPLY CURRENT vs. COMMON-MODE VOLTAGE

BUFFER SUPPLY CURRENT vs. BUFFER SUPPLY VOLTAGE

NO-LOAD BUFFER SUPPLY CURRENT vs. TEMPERATURE

VCOM BUFFER SMALL-SIGNAL RESPONSE

A. V_{BUF+} = 3.95V TO 4.05V, 50mV/div
B. BUFOUT = BUF-, 50mV/div
C_{BUF} = 1µF, V_{SUPB} = 8V
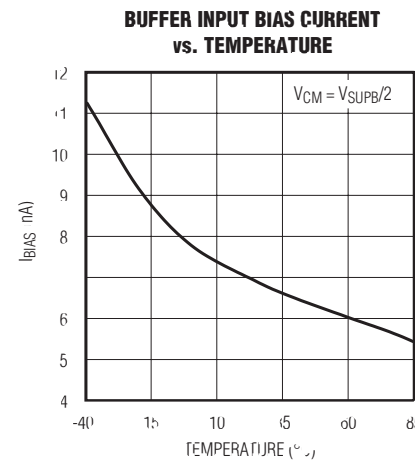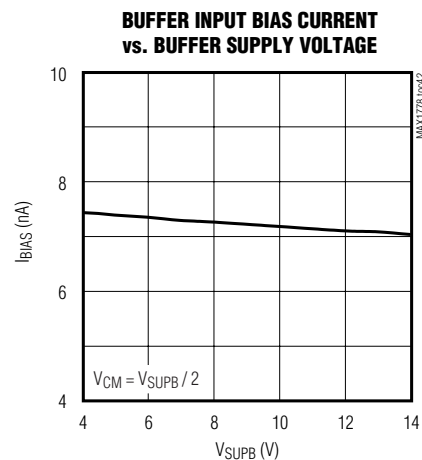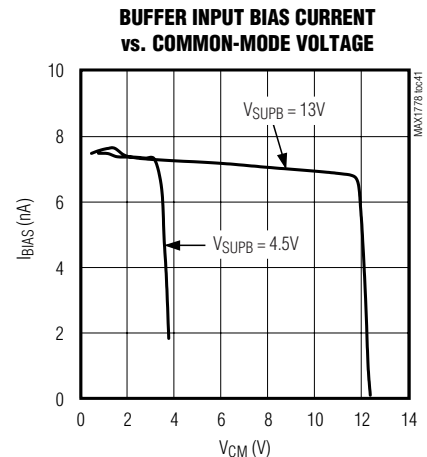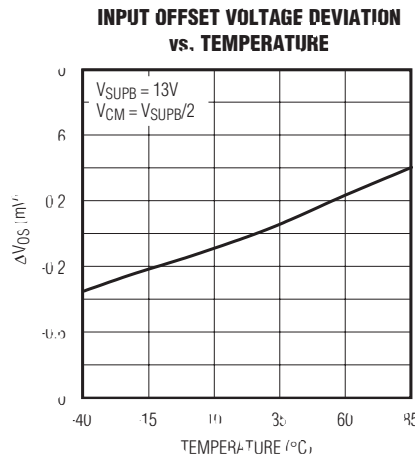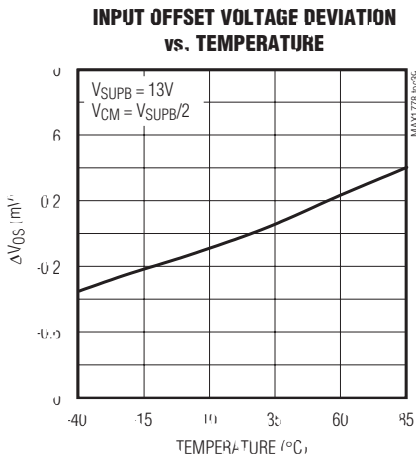
Quad-Output TFT LCD DC/DC Converters with Buffer

Typical Operating Characteristics (continued)

(Circuit of Figure 1, V_{IN} = +3.3V, $\overline{SHDN}$ = IN, V_{MAIN} = V_{SUPP} = V_{SUPN} = V_{SUPB} = V_{SUPL} = 8V, BUF- = BUFOUT, BUF+ = FLTSET = TGND = PGND = GND, T_A = +25°C.)
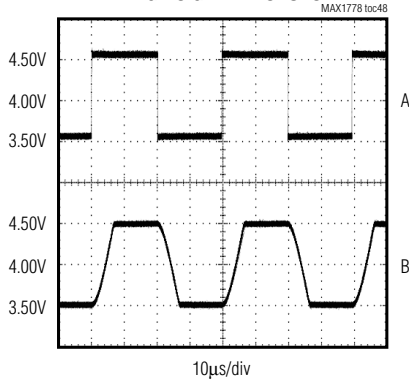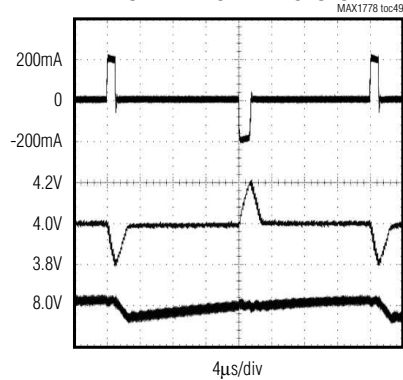

VCOM BUFFER LARGE-SIGNAL RESPONSE

MAX1778 toc48

A. V_{BUF+} = 3.50V TO 4.50V, 0.5V/div
B. BUFOUT = BUF-, 0.5V/div
C_{BUF} = 1µF, V_{SUPB} = 8V

VCOM BUFFER LOAD-TRANSIENT RESPONSE

MAX1778 toc49

A. I_{BUFOUT} = 200mA PULSES, 200mA/div
B. BUFOUT = BUF-, 200mV/div
C. V_{MAIN} = 8V, 50mV/div
V_{SUPB} = V_{MAIN}, BUF+ = GND, C_{BUF} = 1µF

VCOM BUFFER LOAD-TRANSIENT RESPONSE

MAX1778 toc50
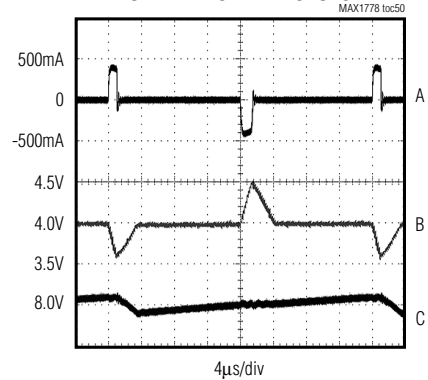
A. I_{BUFOUT} = 400mA PULSES, 500mA/div
B. BUFOUT = BUF-, 0.5V/div
C. V_{MAIN} = 8V, 100mV/div
V_{SUPB} = V_{MAIN}, BUF+ = GND, C_{BUF} = 1µF

VCOM BUFFER STARTUP

MAX1778 toc51
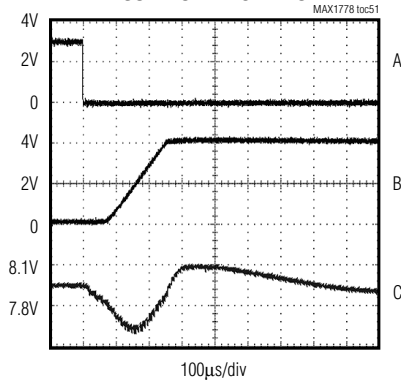
A. $\overline{RDY}$, 2V/div
B. BUFOUT = BUF-, C_{BUF} = 1µF, 2V/div
C. V_{SUPB} = V_{MAIN} = 8V, I_{MAIN} = 20mA, 200mV/div
BUF+ = GND

VCOM BUFFER STARTUP
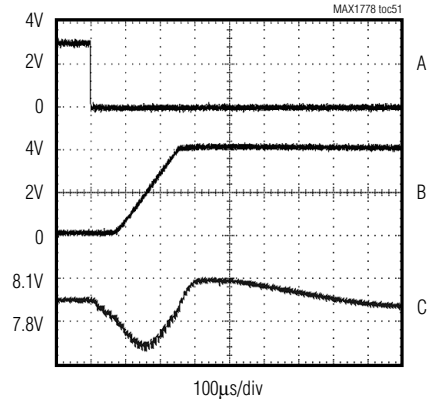
MAX1778 toc51

A. $\overline{RDY}$, 2V/div
B. BUFOUT = BUF-, C_{BUF} = 1µF, 2V/div
C. V_{SUPB} = V_{MAIN} = 8V, I_{MAIN} = 20mA, 200mV/div
BUF+ = GND

Pin Description

PIN				NAME	FUNCTION
MAX1778 MAX1881	MAX1880 MAX1882	MAX1883 MAX1884	MAX1885		
1	1	1	1	FB	Main Step-Up Regulator Feedback Input. Regulates to 1.25V nominal. Connect a resistive divider from the output (V_{MAIN}) to FB to analog ground (GND).
2	2	2	2	INTG	Main Step-Up Integrator Output. When using the integrator, connect 1000pF to analog ground (GND). To disable the integrator, connect INTG to REF.
3	3	3	3	IN	Main Supply Voltage. The supply voltage powers the control circuitry for all the regulators and can range from 2.7V to 5.5V. Bypass with a 0.1µF capacitor between IN and GND, as close to the pins as possible.
4	4	4	4	BUF+	VCOM Buffer (Operational Transconductance Amplifier) Positive Feedback Input. Connect to GND to select the internal resistive divider that sets the positive input to half the amplifier's supply voltage ($V_{BUF+} = V_{SUPB}/2$).
5	5	5	5	BUF-	VCOM Buffer (Operational Transconductance Amplifier) Negative Feedback Input
6	6	6	6	SUPB	VCOM Buffer (Operational Transconductance Amplifier) Supply Voltage
7	7	7	7	BUFOUT	VCOM Buffer (Operational Transconductance Amplifier) Output
8	8	8	8	GND	Analog Ground. Connect to power ground (PGND) underneath the IC.
9	9	9	9	REF	Internal Reference Bypass Terminal. Connect a 0.22µF ceramic capacitor from REF to analog ground (GND). External load capability up to 50µA.
10	10	—	—	FBP	Positive Charge-Pump Regulator Feedback Input. Regulates to 1.25V nominal. Connect a resistive divider from the positive charge-pump output (V_{POS}) to FBP to analog ground (GND).
11	11	—	—	FBN	Negative Charge-Pump Regulator Feedback Input. Regulates to 0V nominal. Connect a resistive divider from the negative charge-pump output (V_{NEG}) to FBN to the reference (REF).
12	12	10	10	$\overline{SHDN}$	Active-Low Shutdown Control Input. Pull $\overline{SHDN}$ low to force the controller into shutdown. If unused, connect $\overline{SHDN}$ to IN for normal operation. A rising edge on $\overline{SHDN}$ clears the fault latch.
13	—	11	—	SUPL	Low-Dropout Linear Regulator Input Voltage. Can range from 4.5V to 15V. Bypass with a 1µF capacitor to GND (see *Capacitor Selection and Regulator Stability*). Connect both input pins together externally.

Quad-Output TFT LCD DC/DC Converters with Buffer

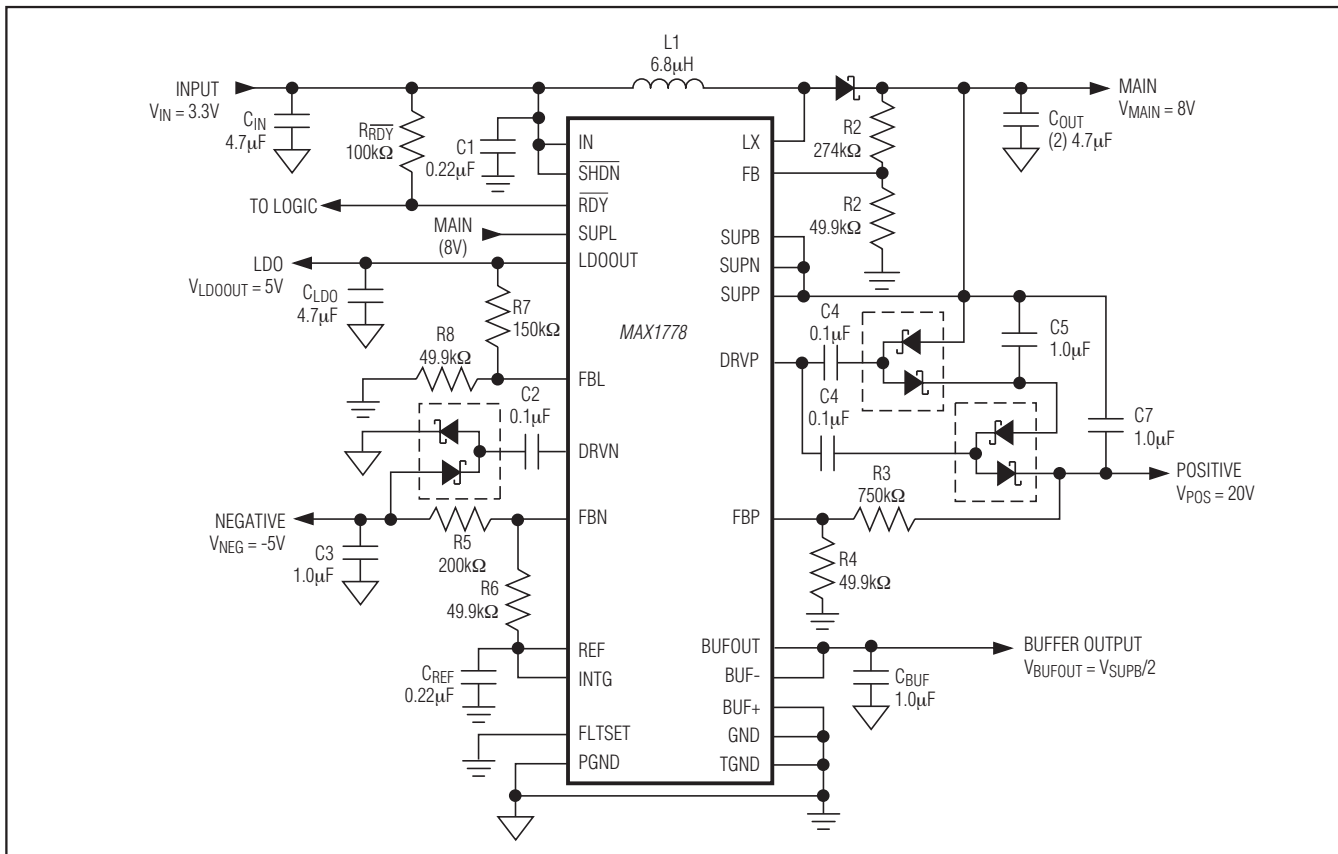| PIN				NAME	FUNCTION
MAX1778 MAX1881	MAX1880 MAX1882	MAX1883 MAX1884	MAX1885		
14	—	12	—	LDOOUT	Linear Regulator Output. Sources up to 40mA. Bypass to GND with a ceramic capacitor determined by: $$C_{LDOOUT} \geq 0.5ms \times \left(\frac{I_{LDOOUT(MAX)}}{V_{LDOOUT}} \right)$$
15	—	13	—	FBL	Voltage Setting Input. Connect a resistive divider from the linear regulator output (V_{LDOOUT}) to FBL to analog ground (GND).
16	16	14	14	FLTSET	Fault Trip-Level Set Input. Connect to a resistive divider between REF and GND to set the main step-up converter's and positive charge pump's fault thresholds between 0.67 x V_{REF} and 0.85 x V_{REF}. Connect to GND for the preset fault threshold (0.9 x V_{REF}).
17	17	—	—	SUPN	Negative Charge-Pump Driver Supply Voltage. Bypass to power ground (PGND) with a 0.1µF capacitor.
18	18	—	—	DRVN	Negative Charge-Pump Driver Output. Output high level is V_{SUPN} and low level is PGND.
19	19	—	—	SUPP	Positive Charge-Pump Driver Supply Voltage. Bypass to power ground (PGND) with a 0.1µF capacitor.
20	20	—	—	DRVP	Positive Charge-Pump Driver Output. Output high level is V_{SUPP} and low level is PGND
21	21	17	17	PGND	Power Ground. Connect to analog ground (GND) underneath the IC.
22	22	18	18	LX	Main Step-Up Regulator Power MOSFET N-Channel Drain. Place output diode and output capacitor as close as possible to PGND.
23	23	19	19	TGND	Must be connected to ground.
24	24	20	20	$\overline{RDY}$	Active-Low, Open-Drain Output. Indicates all outputs are ready. On-resistance is 125Ω (typ).
—	13–15	15, 16	11–13, 15, 16	N.C.	No Connection. Not internally connected.

Figure 1. Typical Application Circuit

Detailed Description

The MAX1778/MAX1880–MAX1885 are highly efficient multiple-output power supplies for thin-film transistor (TFT) liquid crystal display (LCD) applications. The devices contain one high-power step-up converter, two low-power charge pumps, an operational transconductance amplifier (VCOM buffer), and a low-dropout linear regulator. The primary step-up converter uses an internal N-channel MOSFET to provide maximum efficiency and to minimize the number of external components. The output voltage of the main step-up converter (V_{MAIN}) can be set from V_{IN} to 13V with external resistors.

The dual charge pumps (MAX1778/MAX1880–MAX1882 only) independently regulate a positive output (V_{POS}) and a negative output (V_{NEG}). These low-power outputs use external diode and capacitor stages (as many stages as required) to regulate output voltages from -40V to +40V. A unique control scheme minimizes output ripple as well as capacitor sizes for both charge pumps.

A resistor-programmable 40mA linear regulator (MAX1778/MAX1881/MAX1883/MAX1884 only) can provide preregulation or postregulation for any of the supplies. For higher current applications, an external transistor can be added.

Additionally, the VCOM buffer provides a high current output that is ideal for driving capacitive loads, such as the backplane of a TFT LCD panel. The positive feedback input features dual-mode operation, allowing this input to be connected to an internal 50% resistive-divider between the buffer's supply voltage and ground, or externally adjusted for other voltages.

Also included in the MAX1778/MAX1880–MAX1885 is a precision 1.25V reference that sources up to 50µA, logic shutdown, soft-start, power-up sequencing, adjustable fault detection, thermal shutdown, and an active-low, open-drain ready output.

Quad-Output TFT LCD DC/DC Converters with Buffer

Main Step-up Controller

During normal pulse-width modulation (PWM) operation, the MAX1778/MAX1880–MAX1885 main step-up controllers switch at a constant frequency of 500kHz or 1MHz (see the *Selector Guide*), allowing the use of low-profile inductors and output capacitors. Depending on the input-to-output voltage ratio, the controller regulates the output voltage and controls the power transfer by modulating the duty cycle (D) of each switching cycle:

$$D \approx \frac{V_{MAIN} - V_{IN}}{V_{MAIN}}$$

On the rising edge of the internal clock, the controller sets a flip-flop when the output voltage is too low, which turns on the n-channel MOSFET (Figure 2). The inductor current ramps up linearly, storing energy in a magnetic field. Once the sum of the feedback voltage error amplifier, slope-compensation, and current-feedback signals trip the multi-input comparator, the MOSFET turns off, the flip-flop resets, and the diode (D1) turns on. This forces the current through the inductor to ramp back down, transferring the energy stored in the magnetic field to the output capacitor and load. The MOSFET remains off for the rest of the clock cycle.

Changes in the feedback voltage-error signal shift the switch-current trip level, consequently modulating the MOSFET duty cycle.

Under very light loads, an inherent switchover to pulse-skipping takes place (Figure 3). When this occurs, the controller skips most of the oscillator pulses in order to reduce the switching frequency and gate charge losses. When pulse-skipping, the step-up controller initiates a new switching cycle only when the output voltage drops too low. The n-channel MOSFET turns on, allowing the inductor current to ramp up until the multi-input comparator trips. Then, the MOSFET turns off and the diode turns on, forcing the inductor current to ramp down. When the inductor current reaches zero, the diode turns off, so the inductor stops conducting current. This forces the threshold between pulse-skipping and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation:

$$I_{LOAD(CROSSOVER)} \approx \frac{1}{2} \left(\frac{V_{IN}}{V_{MAIN}} \right)^2 \left(\frac{V_{MAIN} - V_{IN}}{f_{OSC}L} \right)$$
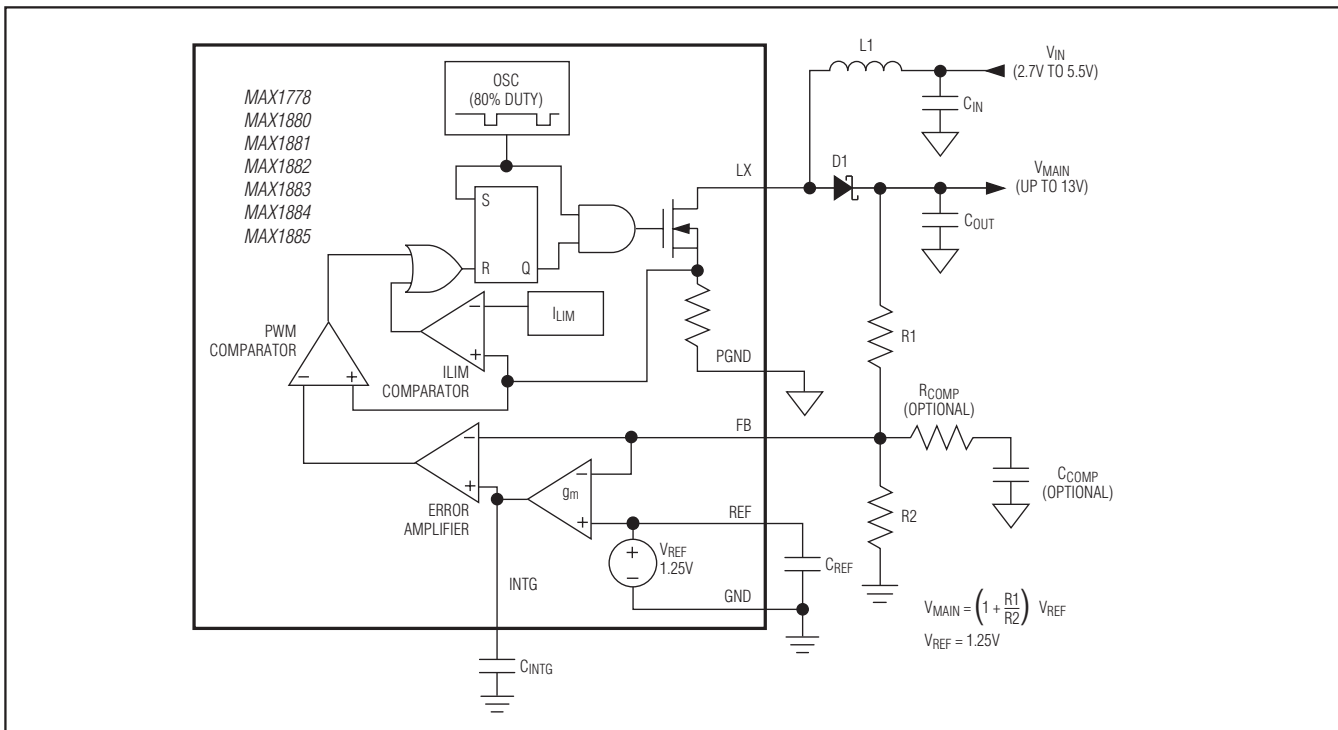

Figure 2. Main Step-Up Converter Block Diagram

Maxim Integrated

The switching waveforms appear noisy and asynchronous when light loading causes pulse-skipping operation; this is a normal operating condition that improves light-load efficiency.
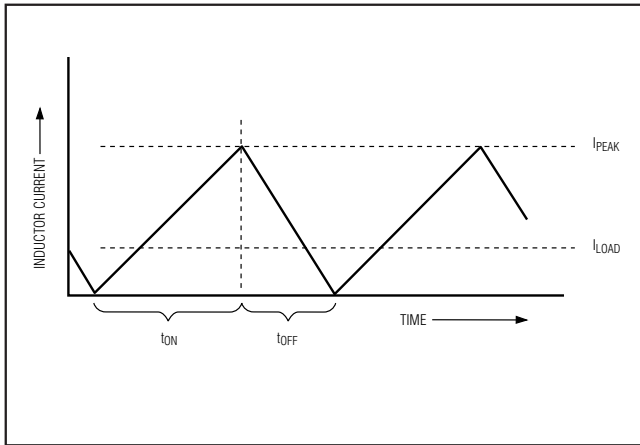

Figure 3. Discontinuous-to-Continuous Conduction Crossover Point

Dual Charge-Pump Regulator (MAX1778/MAX1880–MAX1882 Only)

The MAX1778/MAX1880–MAX1882 controllers contain two independent low-power charge pumps (Figure 4). One charge pump inverts the input voltage and provides a regulated negative output voltage. The second charge pump doubles the input voltage and provides a regulated positive output voltage. The controllers contain internal p-channel and n-channel MOSFETs to control the power transfer. The internal MOSFETs switch at a constant frequency ($f_{CHP} = f_{OSC}/2$).

Positive Charge Pump

During the first half-cycle, the n-channel MOSFET turns on and charges flying capacitor $C_{X(POS)}$ (Figure 4). This initial charge is controlled by the variable n-channel on-resistance. During the second half-cycle, the n-channel MOSFET turns off and the p-channel MOSFET turns on, level shifting $C_{X(POS)}$ by V_{SUPP} volts. This connects $C_{X(POS)}$ in parallel with the reservoir capacitor $C_{OUT(POS)}$. If the voltage across $C_{OUT(POS)}$ plus a diode drop ($V_{POS} + V_{DIODE}$) is smaller than the level-shifted flying capacitor voltage ($V_{CX(POS)} + V_{SUPP}$), charge flows from $C_{X(POS)}$ to $C_{OUT(POS)}$ until the diode (D3) turns off.
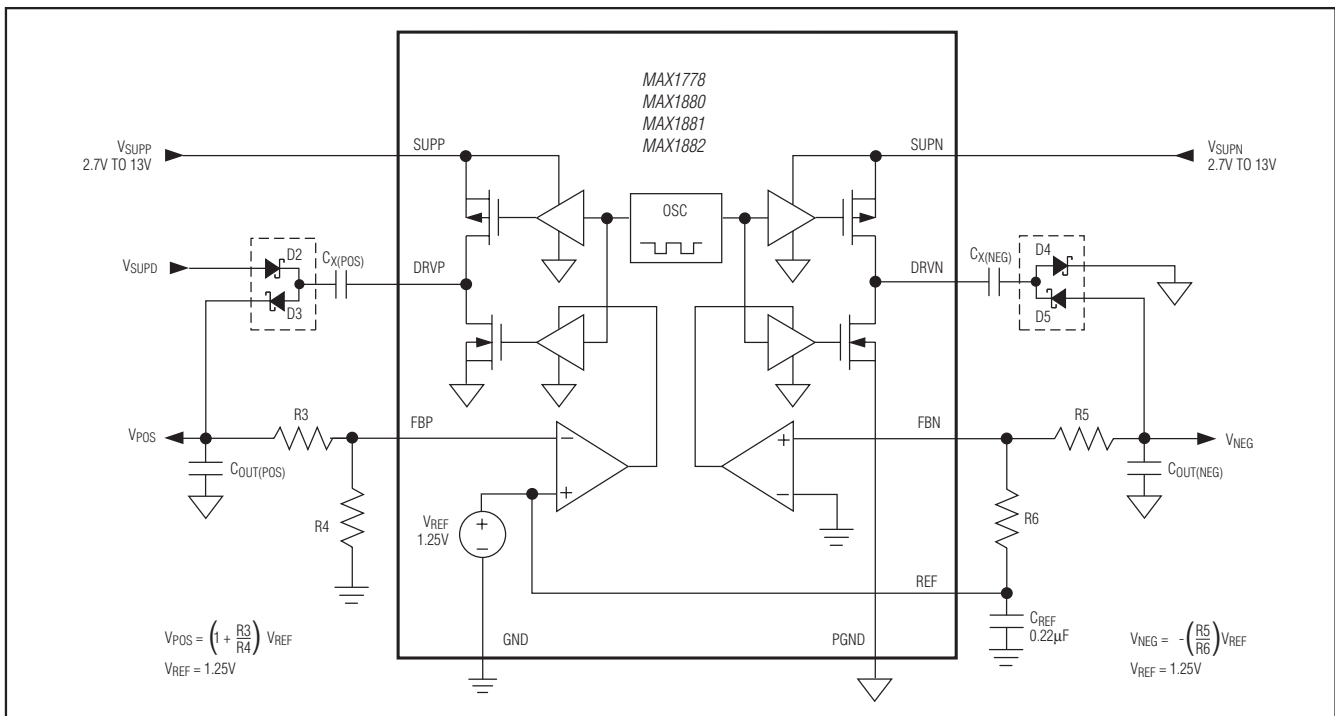

Figure 4. Low-Power Charge Pump Block Diagram

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Negative Charge Pump

During the first half-cycle, the p-channel MOSFET turns on, and flying capacitor $C_{X(NEG)}$ charges to V_{SUPN} minus a diode drop (Figure 4). During the second half-cycle, the p-channel MOSFET turns off, and the n-channel MOSFET turns on, level shifting $C_{X(NEG)}$. This connects $C_{X(NEG)}$ in parallel with reservoir capacitor $C_{OUT(NEG)}$. If the voltage across $C_{OUT(NEG)}$ minus a diode drop is greater than the voltage across $C_{X(NEG)}$, charge flows from $C_{OUT(NEG)}$ to $C_{X(NEG)}$ until the diode (D5) turns off. The amount of charge transferred to the output is controlled by the variable n-channel on-resistance.

Low-Dropout Linear Regulator (MAX1778/MAX1881/MAX1883/MAX1884 Only)

The MAX1778/MAX1881/MAX1883/MAX1884 contain a low-dropout linear regulator (Figure 5) that uses an internal PNP pass transistor (Q_P) to supply loads up to 40mA. As illustrated in Figure 5, the 1.25V reference is connected to the error amplifier, which compares this reference with the feedback voltage and amplifies the difference. If the feedback voltage is higher than the reference voltage, the controller lowers the base current of Q_P, which reduces the amount of current to the output. If the feedback voltage is too low, the device increases the pass transistor base current, which allows more current to pass to the output and increases the output voltage. However, the linear regulator also includes an output current limit to protect the internal pass transistor against short circuits.

The low-dropout linear regulator monitors and controls the pass transistor's base current, limiting the output current to 130mA (typ). In conjunction with the thermal overload protection, this current limit protects the output, allowing it to be shorted to ground for an indefinite period of time without damaging the part.

VCOM Buffer

The MAX1778/MAX1880–MAX1885 include a VCOM buffer, which uses an operational transconductance amplifier (OTA) to provide a current output that is ideal for driving capacitive loads, such as the backplane of a TFT LCD panel. The unity-gain bandwidth of this current-output buffer is:

$$GBW = g_m/C_{OUT}$$

where g_m is the amplifier's transconductance. The bandwidth is inversely proportional to the output capacitor, so large capacitive loads improve stability; however, lower bandwidth decreases the buffer's transient response time. To improve the transient response
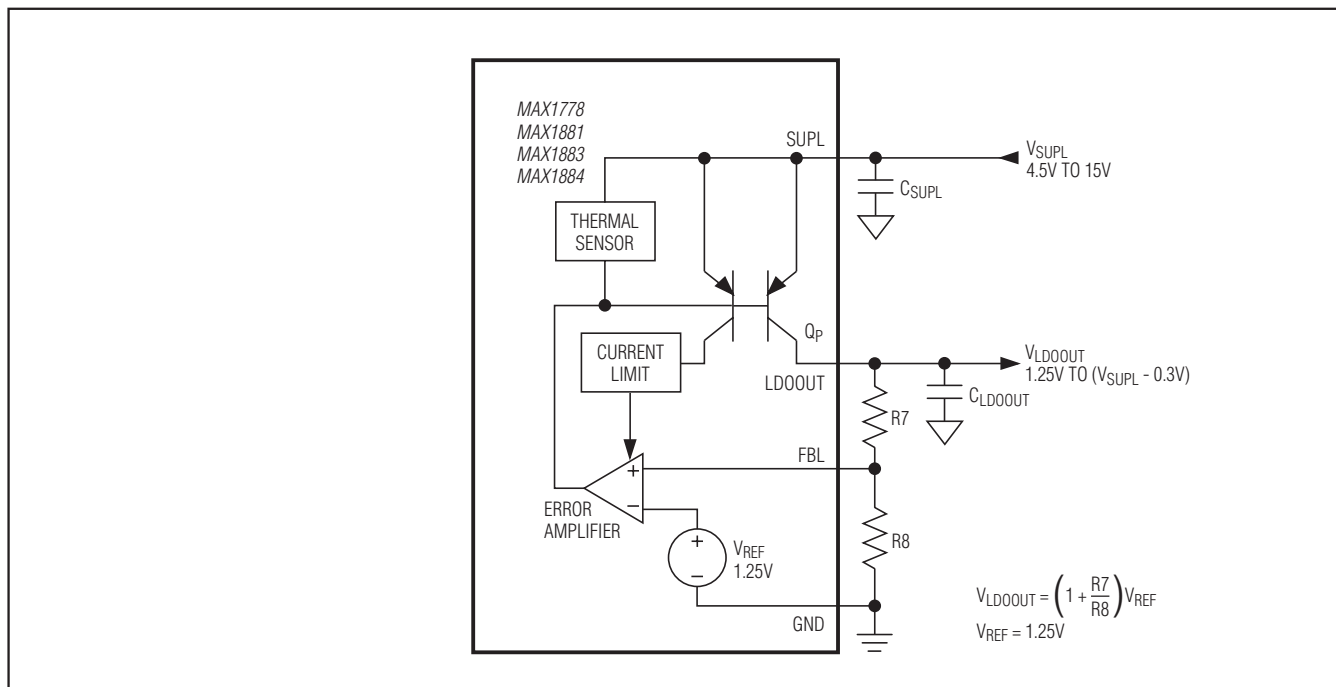

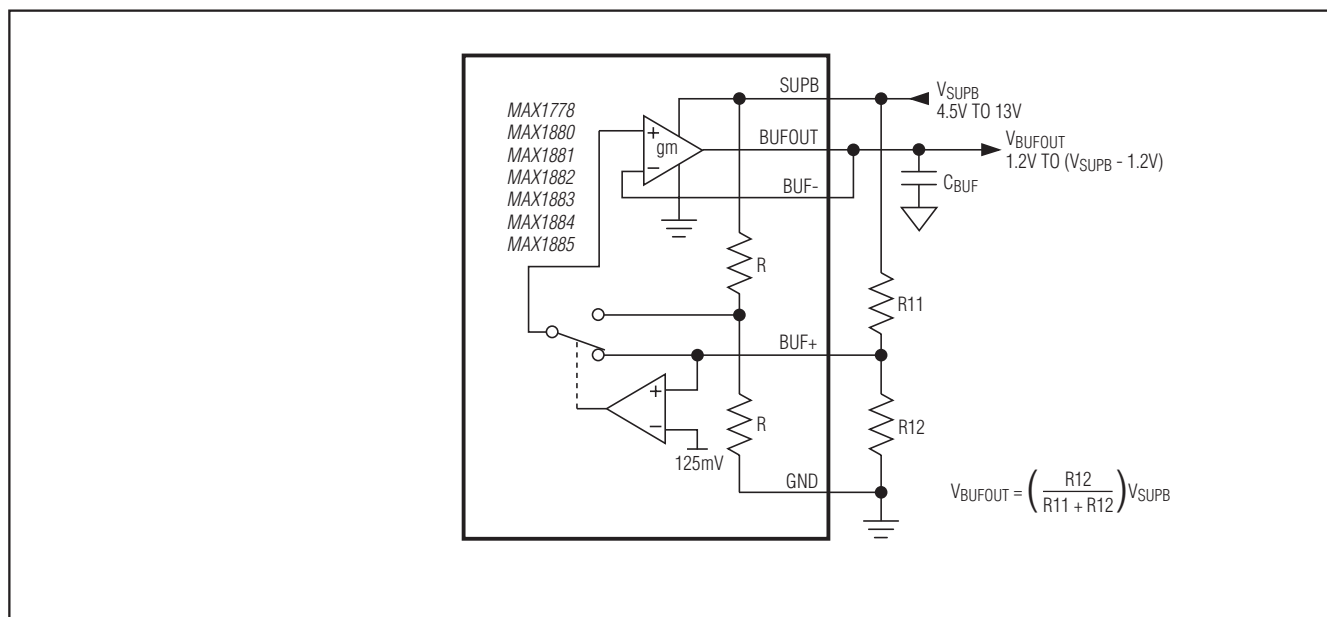Figure 5. Low-Dropout Linear Regulator Block Diagram

Figure 6. VCOM Buffer Block Diagram

times, the amplifier's transconductance increases as the output current increases (see the *Typical Operating Characteristics*).

The VCOM buffer's positive feedback input features dual mode operation. The buffer's output voltage can be internally set by a 50% resistive divider connected to the buffer's supply voltage (SUPB), or the output voltage can be externally adjusted for other voltages.

Shutdown ($\overline{SHDN}$)

A logic-low level on $\overline{SHDN}$ shuts down all of the converters and the reference. When shut down, the supply current drops to 0.1µA to maximize battery life, and the reference is pulled to ground. The output capacitance, feedback resistors, and load current determine the rate at which each output voltage decays. A logic-level high on $\overline{SHDN}$ power activates the MAX1778/ MAX1880–MAX1885 (see the *Power-Up Sequencing* section). Do not leave $\overline{SHDN}$ floating. If unused, connect $\overline{SHDN}$ to IN. A logic-level transition on $\overline{SHDN}$ clears the fault latch.

Power-Up Sequencing

Upon power-up or exiting shutdown, the MAX1778/ MAX1880–MAX1885 start a power-up sequence. First, the reference powers up. Then, the main DC-DC step-up converter powers up with soft-start enabled. The linear regulator powers up at the same time as the main step-up converter; however, the power sequence and

ready output signal are not affected by the regulation of the linear regulator. While the main step-up converter powers up, the output of the PWM comparator remains low (Figure 2), and the step-up converter charges the output capacitors, limited only by the maximum duty cycle and current-limit comparator. When the step-up converter approaches its nominal regulation value and the PWM comparator's output changes states for the first time, the negative charge pump turns on. When the negative output voltage reaches approximately 90% of its nominal value ($V_{FBN} < 110mV$), the positive charge pump starts up. Finally, when the positive output voltage reaches 90% of its nominal value ($V_{FBP} > 1.125V$), the active-low ready signal ($\overline{RDY}$) goes low (see the *Power Ready* section), and the VCOM buffer powers up. The MAX1883–MAX1885 do not contain the charge pumps, but the power-up sequence still contains the charge pumps' startup logic, which appears as a delay ($2 \times 4096/f_{OSC}$) between the step-up converter reaching regulation and when the ready signal and VCOM buffer are activated.

Soft-Start

For the main step-up regulator, soft-start allows a gradual increase of the current-limit level during startup to reduce input surge currents. The MAX1778/MAX1880–MAX1885 divide the soft-start period into four phases. During the first phase, the controller limits the current limit to only 0.38A (see the *Electrical Characteristics*), approximately a quarter of the maximum current limit

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($I_{LX(MAX)}$). If the output does not reach regulation within 1ms, soft-start enters phase II, and the current limit is increased by another 25%. This process is repeated for phase III. The maximum 1.5A (typ) current limit is reached within 3072 clock cycles or when the output reaches regulation, whichever occurs first (see the startup waveforms in the *Typical Operating Characteristics*).

For the charge pumps (MAX1778/MAX1880–MAX1882 only), soft-start is achieved by controlling the rate of rise of the output voltage. Both charge-pump output voltages are controlled to be in regulation within 4096 clock cycles, irregardless of output capacitance and load, limited only by the charge pump's output impedance. Although the MAX1883–MAX1885 controllers do not include the charge pumps, the soft-start logic still contains the 4096 clock cycle startup periods for both charge pumps.

Fault Trip Level (FLTSET)

The MAX1778/MAX1880–MAX1885 feature dual-mode operation to allow operation with either a preset fault trip level or an adjustable trip level for the step-up converter and positive charge-pump outputs. Connect FLTSET to GND to select the preset 0.9 × V_{REF} fault threshold. The fault trip level can also be adjusted by connecting a voltage-divider from REF to FLTSET (Figure 8). For greatest accuracy, the total load on the reference (including current through the negative charge-pump feedback resistors) should not exceed 50µA so that V_{REF} is guaranteed to be in regulation (see the *Electrical Characteristics*). Therefore, select R10 in the 100kΩ to 1MΩ range, and calculate R9 with the following equation:

$$R9 = R10\ [(V_{REF}/V_{FLTSET}) - 1]$$

where V_{REF} = 1.25V, and V_{FLTSET} can range from 0.67 x V_{REF} to 0.85 x V_{REF}. FLTSET's input bias current has a maximum value of 50nA. For 1% error, the current through R10 should be at least 100 times the FLTSET input bias current (I_{FLTSET}).

Fault Condition

Once $\overline{RDY}$ is low, if the output of the main regulator or either low-power charge pump falls below its fault detection threshold, or if the input drops below its undervoltage threshold, then $\overline{RDY}$ goes high impedance and all outputs shut down; however, the reference remains active. After removing the fault condition, toggle shutdown (below 0.8V) or cycle the input voltage (below 0.2V) to clear the fault latch and reactivate the device.

The reference fault threshold is 1.05V. For the step-up converter and positive charge-pump, the fault trip level is set by FLTSET (see the *Fault Trip Level (FLTSET)* section). For the negative charge pump, the fault threshold measured at the charge-pump's feedback input (FBN) is 140mV (typ).

Power Ready ($\overline{RDY}$)

$\overline{RDY}$ is an open-drain output. When the power-up sequence for the main step-up converter and low-power charge pumps has properly completed, the 14V MOSFET turns on and pulls $\overline{RDY}$ low with a 125Ω (typ) on-resistance. If a fault is detected on any of these three outputs, the internal open-drain MOSFET appears as a high impedance. Connect a 100kΩ pullup resistor between $\overline{RDY}$ and IN for a logic-level output.

Voltage Reference (REF)

The voltage at REF is nominally 1.25V. The reference can source up to 50µA with good load regulation (see the *Typical Operating Characteristics*). Connect a 0.22µF ceramic bypass capacitor between REF and GND.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX1778/MAX1880–MAX1885. When the junction temperature exceeds T_J = +160°C, a thermal sensor activates the fault protection, which shuts down the controller, allowing the IC to cool. Once the device cools down by 15°C, toggle shutdown (below 0.8V) or cycle the input voltage (below 0.2V) to clear the fault latch and reactivate the controller. Thermal-overload protection protects the controller in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction-temperature rating of T_J = +150°C.

Operating Region and Power Dissipation

The MAX1778/MAX1880–MAX1885s' maximum power dissipation depends on the thermal resistance of the IC package and circuit board, the temperature difference between the die junction and ambient air, and the rate of any airflow. The power dissipated in the device depends on the operating conditions of each regulator and the buffer.

The step-up controller dissipates power across the internal n-channel MOSFET as the controller ramps up the inductor current. In continuous conduction, the power dissipated internally can be approximated by:

$$P_{STEP-UP} \approx \left[\left(\frac{I_{MAIN}V_{MAIN}}{V_{IN}} \right)^2 + \frac{1}{12} \left(\frac{V_{IN}D}{f_{OSC}L} \right)^2 \right] \times R_{DS(ON)}D$$

where I_{MAIN} includes the primary load current and the input supply currents for the charge pumps (see the *Charge-Pump Input Power and Efficiency Considerations* section), linear regulator, and VCOM buffer.

The linear regulator generates an output voltage by dissipating power across an internal pass transistor, so the power dissipation is simply the load current times the input-to-output voltage differential:

$$P_{LDO(INT)} = I_{LDO}(V_{SUPL} - V_{LDO})$$

When driving an external transistor, the internal linear regulator provides the base drive current. Depending on the external transistor's current gain (β) and the maximum load current, the power dissipated by the internal linear regulator can still be significant:

$$P_{LDO(INT)} = \frac{I_{LDO}}{\beta}\left[V_{SUPL} - (V_{LDO} + 0.7V)\right]$$

$$= I_{LDOOUT}(V_{SUPL} - V_{LDOOUT})$$

The charge pumps provide regulated output voltages by dissipating power in the low-side n-channel MOSFET, so they could be modeled as linear regulators followed by unregulated charge pumps. Therefore, their power dissipation is similar to a linear regulator:

$$P_{NEG} = I_{NEG}\left[(V_{SUPN} - 2V_{DIODE})N - V_{NEG}\right]$$

$$P_{POS} = I_{POS}\left[(V_{SUPP} - 2V_{DIODE})N + V_{SUPD} - V_{POS}\right]$$

where N is the number of charge-pump stages, V_{DIODE} is the diodes' forward voltage, and V_{SUPD} is the positive charge-pump diode supply (Figure 4).

The VCOM buffer's power dissipation depends on the capacitive load (C_{LOAD}) being driven, the peak-to-peak voltage change (V_{P-P}) across the load, and the load's switching rate:

$$P_{BUF} = V_{P-P}C_{LOAD}f_{LOAD}V_{SUPB}$$

To find the total power dissipated in the device, the power dissipated by each regulator and the buffer must be added together:

$$P_{TOTAL} = P_{STEP-UP} + P_{LDO(INT)}$$
$$+ P_{NEG} + P_{POS} + P_{BUF}$$

The maximum allowed power dissipation is 975mW (24-pin TSSOP)/879mW (20-pin TSSOP) or:

$$P_{MAX} = (T_{J(MAX)} - T_A)/(\theta_{JB} + \theta_{BA})$$

where $T_J - T_A$ is the temperature difference between the controller's junction and the surrounding air, θ_{JB} (or θ_{JC}) is the thermal resistance of the package to the board, and θ_{BA} is the thermal resistance from the PCB to the surrounding air.

Design Procedure

Main Step-Up Converter

Output-Voltage Selection
Adjust the output voltage by connecting a voltage-divider from the output (V_{MAIN}) to FB to GND (see the *Typical Operating Circuit*). Select R2 in the 10kΩ to 50kΩ range. Calculate R1 with the following equations:

$$R1 = R2\left[(V_{MAIN}/V_{REF}) - 1\right]$$

where $V_{REF} = 1.25V$. V_{MAIN} can range from V_{IN} to 13V.

Inductor Selection
Inductor selection depends upon the minimum required inductance value, saturation rating, series resistance, and size. These factors influence the converter's efficiency, maximum output load capability, transient response time, and output-voltage ripple. For most applications, values between 4.7μH and 22μH work best with the controller's switching frequency (Tables 1 and 2).

The inductor value depends on the maximum output load the application must support, input voltage, output voltage, and switching frequency. With high inductor values, the MAX1778/MAX1880–MAX1885 source higher output currents, have less output ripple, and enter continuous conduction operation with lighter loads; however, the circuit's transient response time is slower. On the other hand, low-value inductors respond faster to transients, remain in discontinuous conduction operation, and typically offer smaller physical size for a given series resistance and current rating. The equations provided here include a constant LIR, which is the ratio of the peak-to-peak AC inductor current to the average DC inductor current. For a good compromise between the size of the inductor, power loss, and output-voltage ripple, select an LIR of 0.3 to 0.5. The inductance value is then given by:

$$L_{MIN} = \left(\frac{V_{IN(MIN)}}{V_{MAIN}}\right)^2\left(\frac{V_{MAIN} - V_{IN(MIN)}}{I_{MAIN(MAX)}f_{OSC}}\right)\left(\frac{1}{LIR}\right)\eta$$