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MAX19005

Quad, Ultra-Low-Power, 200Mbps ATE Drivers/Comparators

General Description

The MAX19005 four-channel, ultra-low-power, pin-electronics IC includes a two-level pin driver, a window comparator, a passive load, and force-and-sense Kelvin-switched parametric measurement unit (PMU) connections for each channel. The driver features a -1V to +5.2V voltage range, includes high-impedance modes, and is highly linear even at low voltage swings. The window comparator features 240MHz equivalent input bandwidth and programmable output voltage levels. The passive load provides pullup and pulldown voltages to the device-under-test (DUT).

Low leakage and high impedance are operational configurations that are programmed through a 3-wire, low-voltage, CMOS-compatible serial interface. High-speed PMU switching is realized through dedicated digital control inputs.

This device is available in an 80-pin, 12mm x 12mm body, 0.5mm pitch TQFP with an exposed 6mm x 6mm die pad on the bottom of the package for efficient heat removal. The device is specified to operate over the 0°C to +70°C commercial temperature range and features a die temperature monitor output.

***Ordering Information* appears at end of data sheet.**

Features

- ♦ **Small Footprint: Four Channels in 0.3in^2**
- ♦ **Low-Power Dissipation: 340mW/Channel (typ)**
- ♦ **High Speed: 200Mbps at 3V_{P-P}**
- ♦ **-1V to +5.2V Operating Range**
- ♦ **Integrated Pin Switch (with -1V to +24V Off Range)**
- ♦ **Integrated PMU Switches with -1V to +24V Operating Range**
- ♦ **Passive Load**
- ♦ **Low-Leakage Mode by Pin Switch Off: 10nA (max)**
- ♦ **Low Gain and Offset Error**

Applications

NAND Flash Testers

DRAM Probe Testers

Low-Cost Mixed-Signal/System-on-Chip (SoC) Testers

Active Burn-In Systems

Structural Testers

For related parts and recommended products to use with this part, refer to: www.maxim-ic.com/MAX19005.related

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .... -0.3V to +9.4V
V_{SS} to GND .... -6.25V to +0.3V
V_{DD} - V_{SS} .... +15.65V
V_L to GND .... -0.3V to +5V
DHV_, DLV_ to GND with
Integrated Pin Switch Off .... V_{SS} - 0.3V to V_{DD} + 0.3V
DHV_, DLV_ to GND with
Integrated Pin Switch On .... V_{SSSW} - 0.3V to V_{DD} + 0.3V
DATA_, RCV_, V_{BBI} to GND .... -0.3V to +5V
LDV_ to GND .... V_{SSSW} - 0.3V to V_{DD} + 0.3V
CHV_, CLV_ COMPHI, COMPLO
to GND .... V_{SS} - 0.3V to V_{DD} + 0.3V
CMPH_, CMPL_, V_{BBO} to GND .... -0.3V to V_{DD}
$\overline{LD}$, DIN, SCLK, $\overline{CS}$, SWEN to GND. .... -0.3V to +V_L
CHV_, CLV_ to DUT_ with Integrated Pin Switch On.............8V
DUT_ to GND with Integrated Pin Switch Off…V_{SSSW} to V_{DDSW}
DUT_ to GND with Integrated Pin Switch On…… V_{SSSW} to V_{DD}
FORCE, SENSE, PMU_ to GND .... V_{SSSW} to V_{DDSW}
V_{DDSW} to V_{SSSW} .... +27V
V_{DDSW} to V_{SS} .... +31.35V
V_{DDSW} to GND .... -0.3V to +26.1V
V_{SSSW} to GND .... -2.4V to +0.3V
DUT_, CMPH_, CMPL_ Short-Circuit Duration..........Continuous
DOUT to GND .... -0.3V to +V_L
TEMP to GND .... -0.3V to V_{DD}
TEMP Short-Circuit Duration ....Continuous
PMU Force Switch Continuous Current .... ±35mA
PMU Force Switch Peak Current.................................. ±160mA
PMU Sense Switch Continuous Current.......................... ±1mA
PMU Sense Switch Peak Current................................... ±30mA
All Digital Inputs .... ±30mA
Continuous Power Dissipation (T_A = +70°C)
TQFP (derate 35.7mW/°C above +70°C) 2857mW
Storage Temperature Range........................... -65°C to +150°C
Junction Temperature ....+150°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{DDSW} = +24.6V, V_{SSSW} = -1.25V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$= 0V, LOAD EN LOW_ = LOAD EN HIGH_ = 0, SWEN = 1, T_J = +70°C with an accuracy of ±15°C. Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DRIVER (all specifications apply when DUT_ = DHV_ or DUT_ = DLV_)						
DC CHARACTERISTICS ($R_{DUT\_}$ ≥ 10MΩ, unless otherwise noted)						
Voltage Range			-1.0		+5.2	V
Gain		Measured at 0V and +3V	0.995	1	1.005	V/V
Gain Temperature Coefficient				50		ppm/°C
Offset		$V_{DHV\_}$ = +2V, $V_{DLV\_}$ = 0V			±10	mV
Offset Temperature Coefficient		$V_{DHV\_}$ = +1.5V		±250		µV/°C
Power-Supply Rejection Ratio	PSRR	V_{DD}, V_{SS} independently varied over full range, $V_{DHV\_}$ = +1.5V			±18	mV/V
		V_{DDSW}, V_{SSSW} independently varied over full range, $V_{DHV\_}$ = +1.5V			±10	mV/V
Maximum DC Drive Current	$I_{DUT\_}$		±40			mA
DC Output Resistance		$I_{DUT\_}$ = ±10mA, DATA_ = 1, trim condition, target = 49.5Ω	47.5	49.5	51.5	Ω
DC Output Resistance (V_{DDSW} = + 15V)		$I_{DUT\_}$ = ±10mA, DATA_ = 1	49.0	52.0	55.0	Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{DDSW} = +24.6V, V_{SSSW} = -1.25V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$= 0V, LOAD EN LOW_ = LOAD EN HIGH_ = 0, SWEN = 1, T_J = +70°C with an accuracy of ±15°C. Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC Output Resistance Variation		$I_{DUT\_}$ = -40mA to +40mA, DATA_ = 1 (Note 2)				5.0	Ω
DC Output Resistance Variation (V_{DDSW} = +15V)		$I_{DUT\_}$ = -40mA to +40mA, DATA_ = 1 (Note 2)				8.0	Ω
DC Crosstalk, DHV_ to DLV_, DLV_ to DHV_		$V_{DLV\_}$ = +1.5V, $V_{DHV\_}$ = -1V, +5.2V				±5	mV
		$V_{DHV\_}$ = +1.5V, $V_{DLV\_}$ = -1V, +5.2V				±5	
Linearity Error		+1.5V (Note 3)				±5	mV
		-1V and +5.2V (Note 3)				±15	
AC CHARACTERISTICS ($R_{DUT\_}$ = 50Ω to GND, unless otherwise noted) (Note 4)							
Dynamic Output Current		(Note 5)			±60		mA
Drive Mode Overshoot, Undershoot, and Preshoot		+0.2V to $4V_{P-P}$ swing (Note 6)			5% + 10		mV
High-Impedance Mode Spike		DHV_/high-Z, $V_{DLV\_}$ = -1V, $V_{DHV\_}$ = 0V			25		mV
		DLV_/high-Z, $V_{DLV\_}$ = 0V, $V_{DHV\_}$ = +1V			25		
Propagation Delay, Data to Output		$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, average of t_{LH} and t_{HL}		2.5	3.5	5.1	ns
Propagation Delay Temperature Coefficient		$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V			1		ps/°C
Propagation Delay Match, t_{LH} vs. t_{HL}		$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V			70		ps
Propagation Delay Skew, Drivers Within Package		$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V			100		ps
Propagation Delay Change vs. Pulse Width		Relative to 12.5ns pulse	$3V_{P-P}$, 40MHz, PW = 4ns to 21ns		±40		ps
			$1V_{P-P}$, 40MHz, PW = 2.5ns to 22.5ns		±90		
Propagation Delay Change vs. Common-Mode Voltage		$1V_{P-P}$, $V_{DLV\_}$ = 0V to +3V, relative to delay at $V_{DLV\_}$ = +1V			±80		ps
Propagation Delay, Drive to High Impedance, High Impedance to Drive		$V_{DHV\_}$ = +1.5V, $V_{DLV\_}$ = -1V, average of both directions of t_{LH} and t_{HL}			3.9		ns
Minimum Voltage Swing		(Note 7)			100		mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{DDSW} = +24.6V, V_{SSSW} = -1.25V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$= 0V, LOAD EN LOW_ = LOAD EN HIGH_ = 0, SWEN = 1, T_J = +70°C with an accuracy of ±15°C. Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise/Fall Time (Average Rise/Fall Time)		$V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V, 20% to 80%		0.8		ns
		$V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0, 20% to 80%		0.8		
		$V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, 10% to 90%	1.4	2.0	2.7	
		$V_{DHV\_}$ = +4V, $V_{DLV\_}$ = 0V, $R_{DUT\_}$ = 500Ω, 10% to 90%		2.5		
		$V_{DHV\_}$ = +5V, $V_{DLV\_}$ = 0V, $R_{DUT\_}$ = 500Ω, 10% to 90%		3.1		
Rise/Fall Time Matching		$V_{DHV\_}$ = +0.2V; $V_{DLV\_}$ = 0V		±50		%
		$V_{DHV\_}$ = +1V; $V_{DLV\_}$ = 0V		±15		
		$V_{DHV\_}$ = +3V and +5V; $V_{DLV\_}$ = 0V		±5		
Minimum Pulse Width (Average Positive/Negative Pulse) (Note 8)		$0.2V_{P-P}$, $V_{DHV\_}$ = +0.2V, $V_{DLV\_}$ = 0V		1.8		ns
		$1V_{P-P}$, $V_{DHV\_}$ = +1V, $V_{DLV\_}$ = 0V		2.0		
		$3V_{P-P}$, $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V		2.6		
COMPARATOR (driver in high-impedance mode) (Note 9)						
DC CHARACTERISTICS						
Input Voltage Range			-1.0		+5.2	V
Differential Input Voltage		$V_{DUT\_}$ - $V_{CHV\_}$, $V_{DUT\_}$ - $V_{CLV\_}$	-6.2		+6.2	V
Hysteresis		$V_{CHV\_}$ = $V_{CLV\_}$ = +1.5V		8		mV
Input Offset Voltage		$V_{DUT\_}$ = +1.5V, V_{COMPHI} = +0.8V, V_{COMPLO} = +0.2V (Note 10)			±10	mV
Input Offset Temperature Coefficient		(Note 10)		±25		µV/°C
Common-Mode Rejection Ratio	CMRR	$V_{DUT\_}$ = 0V and +3V (Note 10)	60			dB
Linearity Error		$V_{DUT\_}$ = +1.5V (Notes 3, 10)			±5	mV
		$V_{DUT\_}$ = -1V, +5.2V (Notes 3, 10)			±10	
Power-Supply Rejection Ratio	PSRR	$V_{DUT\_}$ = +1.5V, V_{DD}, V_{SS}, V_{DDSW}, V_{SSSW} supplies independently varied over full range (Note 10)			±5	mV/V
AC CHARACTERISTICS (Note 11)						
Equivalent Input Bandwidth		$V_{DLV\_}$ = 0V termination mode, $V_{DUT\_}$ = $1V_{P-P}$, t_R = t_F = 500ps input, calculated from 10% to 90% redigitization waveform		300		MHz
Prop Delay		$V_{DUT\_}$= $1V_{P-P}$, $V_{CHV\_}$ or $V_{CLV\_}$ = +0.5V	1.1	2.0	3.3	ns
Prop-Delay Temperature Coefficient		$V_{DUT\_}$= $1V_{P-P}$, $V_{CHV\_}$ or $V_{CLV\_}$ = +0.5V		2		ps/°C
Prop-Delay Match, t_{LH} to t_{HL}		Absolute value of delta for each comparator, $V_{DUT\_}$ = $1V_{P-P}$		±250		ps

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{DDSW} = +24.6V, V_{SSSW} = -1.25V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$= 0V, LOAD EN LOW_ = LOAD EN HIGH_ = 0, SWEN = 1, T_J = +70°C with an accuracy of ±15°C. Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Prop-Delay Skew, Comparators Within Package		Same edges (LH and HL), $V_{DUT\_}$ = 1V_{P-P}		±100		ps
Prop-Delay Dispersions vs. Common-Mode Voltage (Note 12)		$V_{CHV\_}$ or $V_{CLV\_}$ = 0 to +4.9V, $V_{DUT\_}$= 0.2V_{P-P}		±20		ps
		$V_{CHV\_}$ or $V_{CLV\_}$ = -0.9 to +4.9V, $V_{DUT\_}$= 0.2V_{P-P}		±30		
Prop-Delay Dispersions vs. Overdrive		$V_{DLV\_}$ = 0V termination mode, $V_{DUT\_}$ = 1V_{P-P}, t_R = t_F = 500ps input, 90% (rising edge) and 10% (falling edge) relative to timing at 50% point		±600		ps
Prop-Delay Dispersions vs. Pulse Width		2ns to 23ns pulse width, relative to 12.5ns pulse width		±60		ps
Prop-Delay Dispersions vs. Slew Rate		+0.5V/ns to +2V/ns		±50		ps
LOGIC INPUTS AND OUTPUTS (COMPHI, COMPLO, CMPH_, CMPL_, V_{BBO})						
Input Voltage Range, V_{COMPHI} and V_{COMPLO}			0		3.6	V
Differential Input Voltage, V_{COMPHI} - V_{COMPLO}		$V_{COMPHI} \geq V_{COMPLO}$, CMPH_ and CMPL_ with no load	0		3.6	V
Differential Input Voltage, V_{COMPHI} - V_{COMPLO}		$V_{COMPHI} \geq V_{COMPLO}$, CMPH_ and CMPL_ with 50Ω to V_{TTCMP}, $V_{COMPHI} \geq V_{TTCMP} \geq V_{COMPLO}$	0		1.0	V
Reference Output, V_{BBO}		Relative to (V_{COMPHI} + V_{COMPLO})/2 at V_{COMPHI} = +1V and V_{COMPLO} = 0V			±50	mV
Output High-Voltage Offset		I_{OUT} = 0mA, relative to V_{COMPHI} at V_{COMPHI} = +1V			±65	mV
Output Low-Voltage Offset		I_{OUT} = 0mA, relative to V_{COMPLO} at $V_{COMPLO\_}$ = 0V			±65	mV
Output Resistance, CMPH_ and CMPL_		$I_{CMPH\_}$ = $I_{CMPL\_}$ = ±10mA, V_{COMPHI} = +1V, V_{COMPLO} = 0V, CMPH_, CMPL_ at high-level output	40	50	60	Ω
Maximum Current Limit, CMPH_ and CMPL_		V_{COMPHI} = +1.8V, V_{COMPLO} = 0V, CMPH_, CMPL_ at high-level output, V_{FORCE} = 0V, +3.6V	-15		+15	mA
Maximum Current Limit, V_{BBO}		V_{COMPHI} = +1V, V_{COMPLO} = 0V, at V_{BBO} = +0.5V output	-1		+1	mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{DDSW} = +24.6V, V_{SSSW} = -1.25V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$= 0V, LOAD EN LOW_ = LOAD EN HIGH_ = 0, SWEN = 1, T_J = +70°C with an accuracy of ±15°C. Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rise/Fall Time, CMPH_ and CMPL_		20% to 80%, $V_{COMPHI\_}$ = +1V, V_{COMPLO} = 0V, load = T-line, 50Ω > 1ns, 50Ω to GND		0.7		ns
PASSIVE LOAD (driver in high-impedance mode) (Note 13)						
DC CHARACTERISTICS $R_{DUT\_}$ ≥ 10MΩ, unless otherwise noted)						
LDV_ Voltage Range			-1.0		+5.2	V
Gain		Measured at 0V and +3V	0.99		1.01	V/V
Gain Temperature Coefficient		Measured at 0V and +3V		50		ppm/°C
Offset		$V_{LDV\_}$ = +1.5V			±100	mV
Offset Temperature Coefficient				0.02		mV/°C
Power-Supply Rejection Ratio	PSRR	V_{DD} and V_{SS} independently varied over full range, $V_{LDV\_}$ = +1.5V	-18		+18	mV/V
		V_{DDSW} and V_{SSSW} independently varied over full range, $V_{LDV\_}$ = +1.5V	-10		+10	mV/V
Output Resistance Tolerance—High Value		$I_{DUT\_}$ = ±2mA, $V_{LDV\_}$ = +1.5V	710	750	790	Ω
Output Resistance Tolerance—Low Value		$I_{DUT\_}$ = ±4mA, $V_{LDV\_}$ = +1.5V	335	375	415	Ω
Output Resistance, Tolerance—High Value (V_{DDSW} = +15V)		$I_{DUT\_}$ = ±2mA, $V_{LDV\_}$ = +1.5V	735	800	865	Ω
Output Resistance, Tolerance—Low Value (V_{DDSW} = +15V)		$I_{DUT\_}$ = ±4mA, $V_{LDV\_}$ = +1.5V	360	425	490	Ω
Switch Resistance Variation		0 to +3V (relative to +1.5V)		±10		%
		Full range (relative to +1.5V)		±30		
Switch Resistance Variation (V_{DDSW} = +15V)		0 to +3V (relative to +1.5V)		±10		%
		Full range (relative to +1.5V)		±30		
Maximum Output Current		$V_{LDV\_}$ = -1V, $V_{DUT\_}$ = +5V	-4			mA
		$V_{LDV\_}$ = +5V, $V_{DUT\_}$ = -1V			+4	
Linearity Error, Full Range		Measured at -1V, +1.5V, and +5.2V (Notes 3, 14)			±25	mV
AC CHARACTERISTICS						
Settling Time, LDV_ to Output		$V_{LDV\_}$ = -1V to +5V step, $R_{DUT\_}$ = 100kΩ (Note 15)		0.5		µs
Output Transient Response		$V_{LDV\_}$ = +1.5V, $V_{DUT\_}$ = -1V to +5V square wave at 1MHz, $R_{DUT\_}$ = 50kΩ		20		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{DDSW} = +24.6V, V_{SSSW} = -1.25V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_\_}$= 0V, LOAD EN LOW_ = LOAD EN HIGH_ = 0, SWEN = 1, T_J = +70°C with an accuracy of ±15°C. Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
PMU SWITCHES (FORCE, SENSE, PMU_) (Note 13)						
Voltage Range			-1.0		+24	V
Voltage Range (V_{DDSW} = +15V)			-1.0		+10	V
Force Switch Resistance		V_{FORCE} = +1.5V, $I_{PMU\_}$ = ±10mA			40	Ω
Force Switch Resistance (V_{DDSW} = +15V)		V_{FORCE} = +1.5V, $I_{PMU\_}$ = ±10mA			47	Ω
Force Path Current		$V_{PMU\_}$ = -1V to +24V, V_{FORCE} = -1V to +24V			±30	mA
Force Path Current (V_{DDSW} = +15V)		$V_{PMU\_}$ = -1V to +10V, V_{FORCE} = -1V to +10V			±30	mA
Force Switch Resistance Variation		0V to +3V (relative to V_{FORCE} = +1.5V)		±10		%
		Full range (Note 16)		±40		
Force Switch Resistance Variation (V_{DDSW} = +15V)		0V to +3V (relative to V_{FORCE} = +1.5V)		±15		%
		Full range (Note 16)		±45		
Sense Switch Resistance		V_{SENSE} = +1.5V, $I_{PMU\_}$ = ±0.4mA	650	1000	1350	Ω
Sense Switch Resistance (V_{DDSW} = +15V)		V_{SENSE} = +1.5V, $I_{PMU\_}$ = ±0.4mA	850	1250	1800	Ω
Sense Switch Resistance Variation		Relative to +11.5V, full range		±40		%
Sense Switch Resistance Variation (V_{DDSW} = +15V)		Relative to +4.5V, full range		±40		%
PMU_ Capacitance		Force and sense switches open		6		pF
FORCE Capacitance		All channels of force and sense switches open		36		pF
SENSE Capacitance		All channels of force and sense switches open		8		pF
FORCE External Capacitance		Allowable external capacitance		2		nF
SENSE External Capacitance		Allowable external capacitance		1		nF
FORCE and SENSE Switching Speed		Connect, PMU_ = +5V, FORCE or SENSE 10MΩ ll 8pF		10		µs
		Disconnect, PMU_ = +5V, FORCE or SENSE 10MΩ ll 8pF		100		
PMU_ Leakage		SWEN = 0, or PMU EN_ = 0, $V_{FORCE\_}$ = $V_{SENSE\_}$ = -1V to +24V		±0.5	±5	nA
PMU_ Leakage (V_{DDSW} = +15V)		SWEN = 0, or PMU EN_ = 0, $V_{FORCE\_}$ = $V_{SENSE\_}$ = -1V to +10V		±0.5	±5	nA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{DDSW} = +24.6V, V_{SSSW} = -1.25V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$= 0V, LOAD EN LOW_ = LOAD EN HIGH_ = 0, SWEN = 1, T_J = +70°C with an accuracy of ±15°C. Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TOTAL FUNCTION						
DUT_						
Leakage, High-Impedance Mode		Passive load switches open, pin switch short, $V_{DUT\_}$ = +5.2V, $V_{CLV\_}$ = $V_{CHV\_}$ = -1V, $V_{DUT\_}$ = -1V, $V_{CLV\_}$ = $V_{CHV\_}$ = +5.2V, full range			2	µA
Low-Leakage Recovery Time		Confirmed simulation only (Note 17)		10		µs
Combined Capacitance		High-impedance mode, passive load switches open, pin switch short		10		pF
Load Resistance Range		(Note 18)		1		GΩ
Load Capacitance Range		(Note 18)		12		nF
Leakage, Pin Switch Off Mode		-1V to +24V, pin switch open		±1	±10	nA
Leakage, Pin Switch Off Mode (V_{DDSW} = +15V)		-1V to +10V, pin switch open		±1	±10	nA
Pin Switch Switching Speed		Connect or disconnect, $V_{DH\_}$ = +5V, DUT_ = 10MΩ ll 8pF		10		µs
VOLTAGE REFERENCE INPUTS (DHV_, DLV_, CHV_, CLV_, LDV_, COMPHI, COMPLO)						
Input Bias Current					±100	µA
SINGLE-ENDED CONTROL INPUTS (DATA_, RCV_)						
Input High Voltage			V_{BBI} + 0.2		3.2	V
Input Low Voltage			0		V_{BBI} - 0.2	V
Voltage Between Inputs and V_{BBI}			V_{BBI} - 1.6		V_{BBI} + 1.6	V
Input Offset Voltage					±50	mV
Input Bias Current					±100	µA
REFERENCE INPUT (V_{BBI})						
Input Voltage Range			0.2		3.0	V
Input Bias Current					±100	µA
DIGITAL INPUTS ($\overline{LD}$, DIN, SCLK, $\overline{CS}$)						
Input High Voltage		(Note 19)	2/3 (V_L)		V_L	V
Input Low Voltage		(Note 19)	-0.1		1/3 (V_L)	V
Input Bias Current					±1	µA
SERIAL-DATA OUTPUT (DOUT)						
Output High Voltage		I_{OH} = -1mA	V_L - 0.4		V_L + 0.1	V
Output Low Voltage		I_{OL} = +1mA	V_{DGND} - 0.1		V_{DGND} + 0.4	V
Output Rise-and-Fall Time		C_L = 10pF		5.0		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{DDSW} = +24.6V, V_{SSSW} = -1.25V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_\_}$ = 0V, LOAD EN LOW_ = LOAD EN HIGH_ = 0, SWEN = 1, T_J = +70°C with an accuracy of ±15°C. Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Low to DOUT Delay		C_L = 10pF	4		45	ns
SERIAL-INTERFACE TIMING						
SCLK Frequency					20	MHz
SCLK Pulse-Width High	t_{CH}		20			ns
SCLK Pulse-Width Low	t_{CL}		20			ns
$\overline{CS}$ Low to SCLK High Setup	t_{CSS0}		5			ns
SCLK High to $\overline{CS}$ Low Hold	t_{CSH0}		0			ns
$\overline{CS}$ High to SCLK High Setup	t_{CSS1}		20			ns
SCLK High to $\overline{CS}$ High Hold	t_{CSH1}		20			ns
DIN to SCLK High Setup	t_{DS}		10			ns
DIN to SCLK High Hold	t_{DH}		10			ns
$\overline{CS}$ High to $\overline{LD}$ Low Hold	t_{CSHLD}		20			ns
$\overline{CS}$ High Pulse Width	t_{CSWH}		20			ns
$\overline{LD}$ Low Pulse Width	t_{LDW}		20			ns
V_L Rising to $\overline{CS}$ Low		Power-on delay		2		µs
TEMPERATURE SENSOR						
Nominal Voltage		T_J = +70°C, $R_L \geq$ 10MΩ		3.43		V
Temperature Coefficient				+10		mV/°C
Output Resistance				17		kΩ
POWER SUPPLIES						
Positive Supply Voltage	V_{DD}	(Note 20)	7.6	8	8.4	V
Negative Supply Voltage	V_{SS}	(Note 20)	-5.25	-5	-4.75	V
Logic Supply Voltage	V_L		2.3	3	3.6	V
Switch Positive Supply Voltage	V_{DDSW}	(Notes 20, 21)	24.1	24.6	25.1	V
Switch Positive Supply Voltage	V_{DDSW}	(Notes 20, 22)	14.5	15	15.5	V
Switch Negative Supply Voltage	V_{SSSW}	(Note 20)	-1.4	-1.25	-1.1	V
Positive Supply Current	I_{DD}	f_{OUT} = 0MHz		105	120	mA
Negative Supply Current	I_{SS}	f_{OUT} = 0MHz		105	120	mA
Logic Supply Current	I_L	f_{OUT} = 0MHz		1	4	mA
Switch Positive Supply Current	I_{DDSW}	f_{OUT} = 0MHz		2	6	mA
Switch Negative Supply Current	I_{SSSW}	f_{OUT} = 0MHz		1.5	5	mA
Static Power Dissipation		f_{OUT} = 0MHz		1.35	1.56	W
Operating Power Dissipation		f_{OUT} = 100Mbps (Note 23)		1.45		W

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +8V, V_{SS} = -5V, V_L = +3V, V_{DDSW} = +24.6V, V_{SSSW} = -1.25V, V_{COMPHI} = +1V, V_{COMPLO} = 0V, $V_{LDV\_}$= 0V, LOAD EN LOW_ = LOAD EN HIGH_ = 0, SWEN = 1, T_J = +70°C with an accuracy of ±15°C. Specification compliance with supply and temperature variations is verified by guard-banding mean shifts of characterization data, unless otherwise noted. All temperature coefficients measured at T_J = +50°C to +90°C, unless otherwise noted.) (Note 1)

Note 1: All minimum and maximum DC, rise/fall time at +3V swing tests are 100% production tested. The propagation-delay data to output and propagation-delay comparator tests are guaranteed by design. All specifications are with DUT_ and PMU_ electrically isolated, unless otherwise noted.

Note 2: Resistance measurements are made using ±2.5mA current changes in the loading instrument about the noted value. Absolute value of the difference in measured resistance over the specified range, tested separately for each current polarity. Test conditions are at $I_{DUT\_}$ = ±1mA, ±12mA, and ±40mA, respectively.

Note 3: Relative to a straight line through 0V and +3V.

Note 4: $V_{DHV\_}$ = +3V, $V_{DLV\_}$ = 0V, unless otherwise specified. DATA_ and RCV_ V_{HIGH} = +2V, V_{LOW} = 1V, V_{BBI} = +1.5V.

Note 5: Current supplied for a minimum of 10ns. Verified to be greater than or equal to DC drive current by design and characterization.

Note 6: Undershoot is any reflection of the signal back towards its starting voltage after it has reached 90% of its swing. Preshoot is any aberration in the signal before it reaches 10% of its swing.

Note 7: At the minimum voltage swing, undershoot is less than 20%. DHV_ and DLV_ references are adjusted to result in the specified swing.

Note 8: At this pulse width, the output reaches at least 90% of its nominal (DC) amplitude. The pulse width is measured at DATA_.

Note 9: With the exception of offset and gain/CMRR tests, reference input values are calibrated for offset and gain.

Note 10: Measured by using a servo to locate comparator thresholds.

Note 11: Unless otherwise noted, all propagation delays are measured at 40MHz, $V_{DUT\_}$ = 0 to +1V, $V_{CHV\_}$ = $V_{CLV\_}$ = +0.5V, t_R = t_F = 500ps, Z_S = 50Ω, driver in high-impedance mode. Comparator outputs are terminated with 50Ω to GND. Measured from $V_{DUT\_}$ crossing calibrated CHV_/CLV_ threshold to midpoint of nominal comparator output swing.

Note 12: $V_{DUT\_}$ = 200mV_{P-P}. Propagation delay is compared to a reference time at +2V.

Note 13: Operating output voltage/current range of passive load and PMU force switch at +24.6V supply. See Figure 1.

Note 14: LOAD EN LOW_ = LOAD EN HIGH_ = 1.

Note 15: Waveform settles to within 5% of final value into 100kΩ load.

Note 16: $I_{PMU\_}$ = ±2mA at V_{FORCE} = -1V, +11.5V, and +24V. Percent variation relative to value calculated at V_{FORCE} = +11.5V.

Note 17: Time to return to the specified maximum leakage after a +3V, +4V/ns step at DUT_.

Note 18: Load at end of 2ns transmission line; for stability only, AC performance could be degraded.

Note 19: The driver meets all of its timing specifications at the specified digital input voltages.

Note 20: Specifications are simulated and characterized over the full power-supply range. Production tests are performed with power supplies at typical values.

Note 21: DUT_ (pin switch off), PMU_ maximum voltage is +24V.

Note 22: DUT_ (pin switch off), PMU_ maximum voltage is +10V.

Note 23: All channels driven at 3V_{P-P}, load = 2ns, 50Ω transmission line terminated with 3pF.

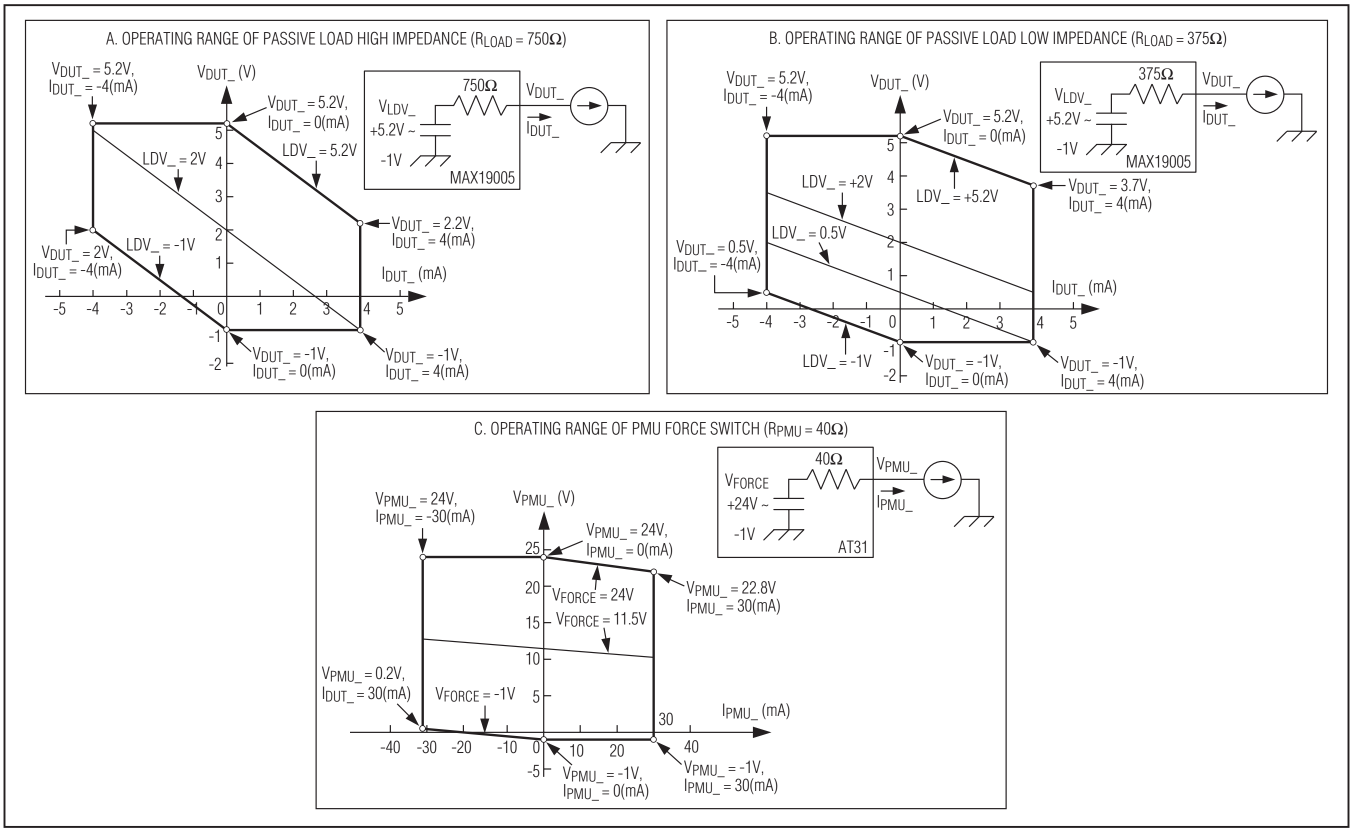
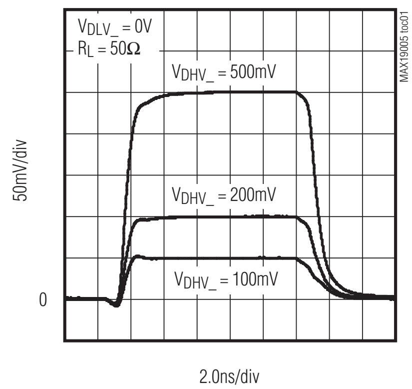


Figure 1. Operating Ranges

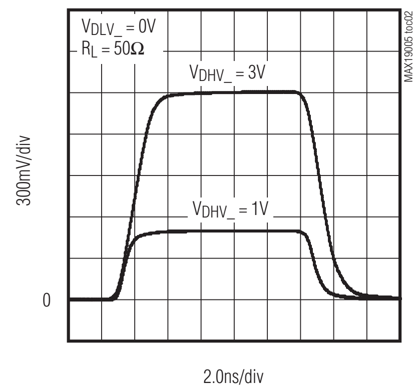
Typical Operating Characteristics

(V_{DD} = 8V, V_{SS} = -5V, V_L = 3V, V_{DDSW} = 24.6V, V_{SSSW} = 1.25V, V_{COMPHI} = 1V, V_{COMPLO} = 0V, $V_{LDV\_}$ = 0V, LOAD EN LOW = LOAD EN HIGH = 0, SWEN = 1, temperature coefficients T_J = +70°C are measured at T_J = +50°C to +90°C, unless otherwise noted.)

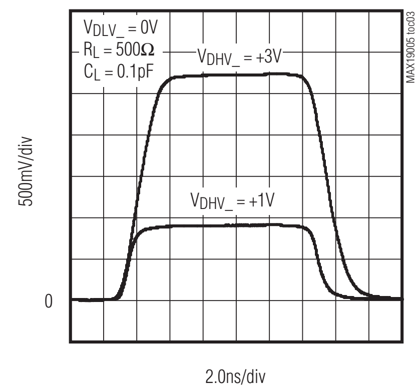
DRIVER SMALL-SIGNAL RESPONSE



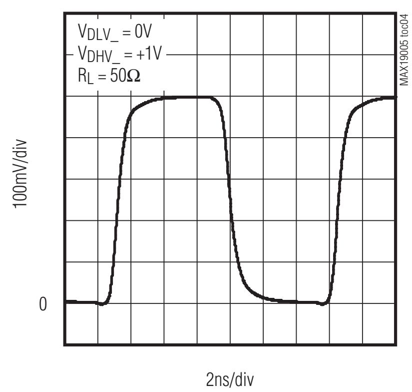
DRIVER LARGE-SIGNAL RESPONSE



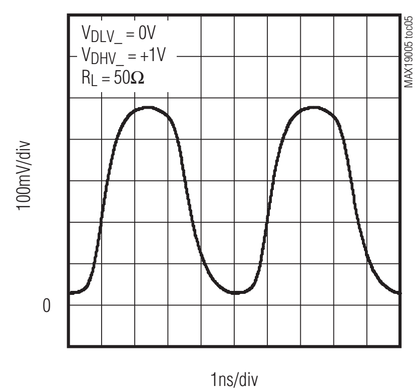
DRIVER LARGE-SIGNAL RESPONSE INTO 500Ω



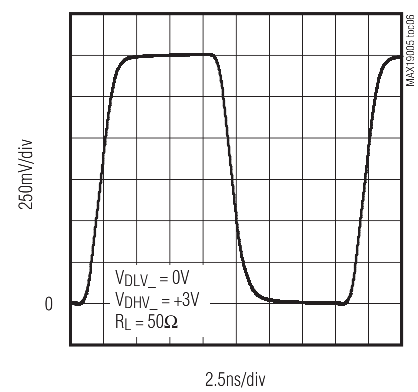
DRIVER 1VP-P, 150Mbps SIGNAL RESPONSE



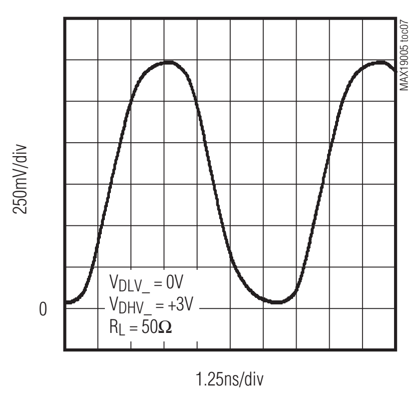
DRIVER 1VP-P, 400Mbps SIGNAL RESPONSE



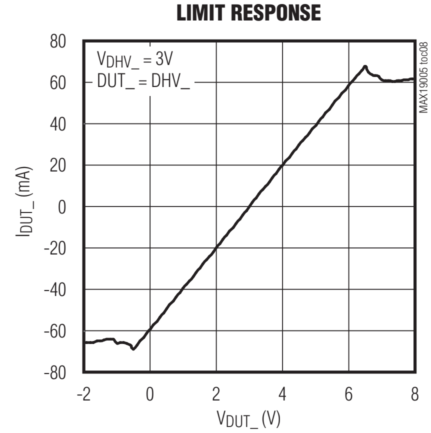
DRIVER 3VP-P, 100Mbps SIGNAL RESPONSE



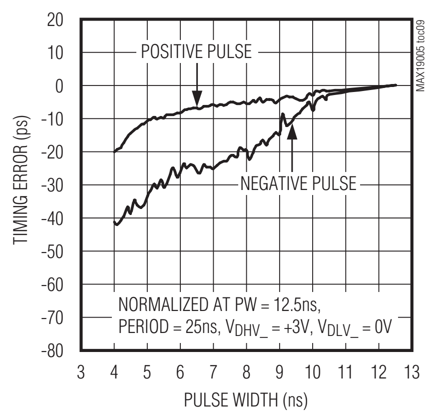
DRIVER 3VP-P, 250Mbps SIGNAL RESPONSE



DRIVER DC CURRENT—LIMIT RESPONSE



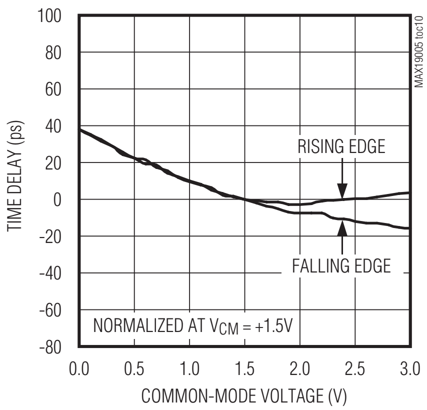
DRIVER 3V TRAILING-EDGE TIMING ERROR vs. PULSE WIDTH



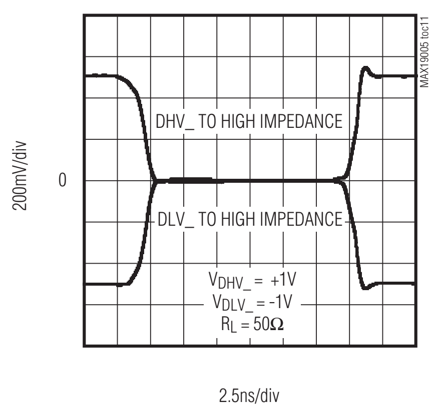
Typical Operating Characteristics (continued)

(V_{DD} = 8V, V_{SS} = -5V, V_L = 3V, V_{DDSW} = 24.6V, V_{SSSW} = 1.25V, V_{COMPHI} = 1V, V_{COMPLO} = 0V, $V_{LDV\_}$ = 0V, LOAD EN LOW = LOAD EN HIGH = 0, SWEN = 1, temperature coefficients T_J = +70°C are measured at T_J = +50°C, to +90°C unless otherwise noted.)

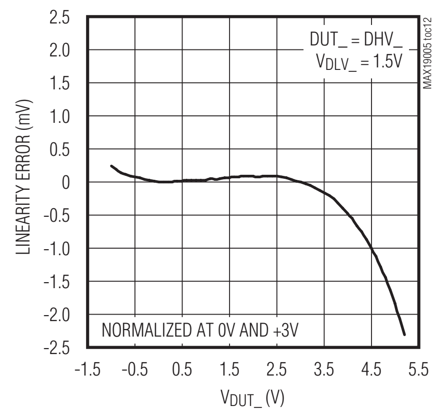
DRIVER TIME DELAY vs. COMMON-MODE VOLTAGE



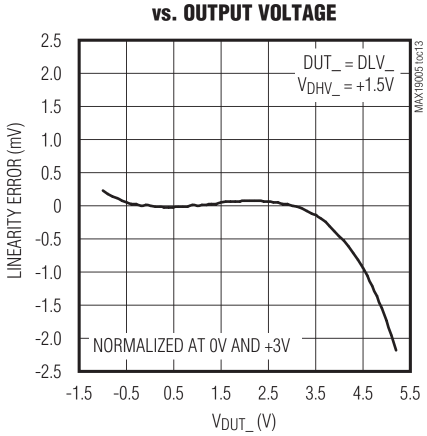
DRIVE-TO-HIGH-IMPEDANCE TRANSITION



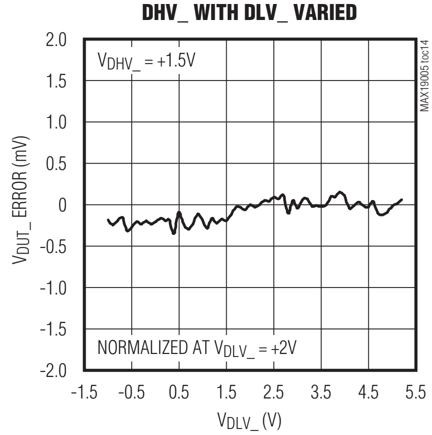
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



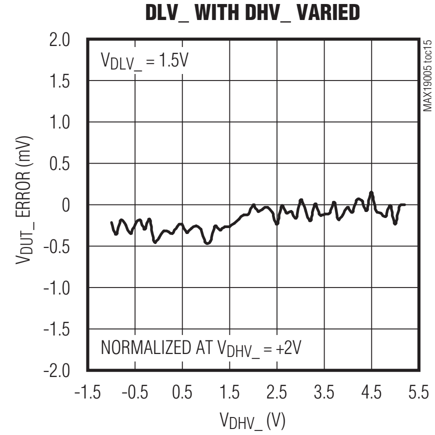
DRIVER LINEARITY ERROR vs. OUTPUT VOLTAGE



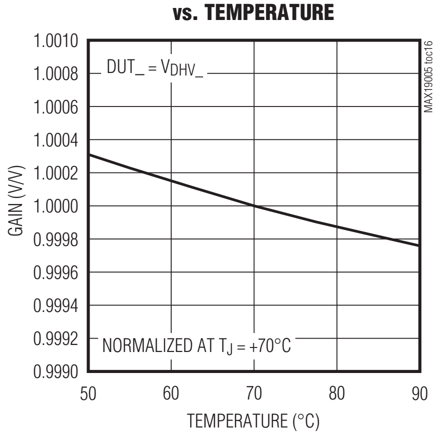
CROSSTALK, DUT_ DRIVEN BY DHV_ WITH DLV_ VARIED



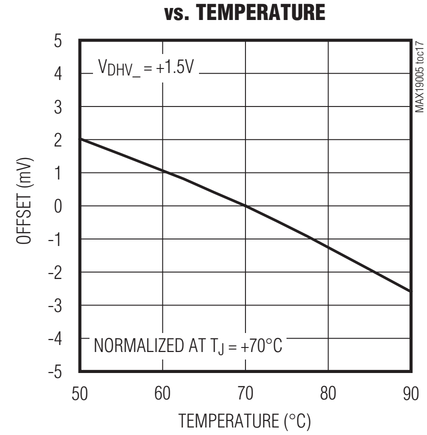
CROSSTALK, DUT_ DRIVEN BY DLV_ WITH DHV_ VARIED



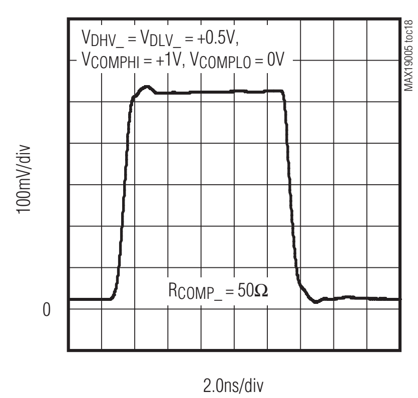
DRIVER GAIN vs. TEMPERATURE



DRIVER OFFSET vs. TEMPERATURE



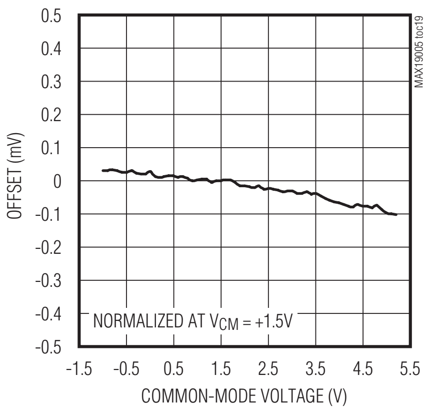
COMPARATOR OUTPUT RESPONSE



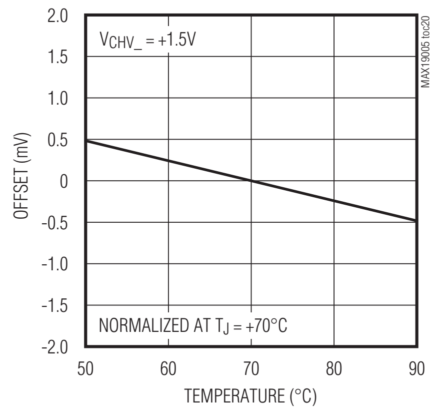
Typical Operating Characteristics (continued)

(V_{DD} = 8V, V_{SS} = -5V, V_L = 3V, V_{DDSW} = 24.6V, V_{SSSW} = 1.25V, V_{COMPHI} = 1V, V_{COMPLO} = 0V, $V_{LDV\_}$ = 0V, LOAD EN LOW = LOAD EN HIGH = 0, SWEN = 1, temperature coefficients T_J = +70°C are measured at T_J = +50°C, to +90°C unless otherwise noted.)

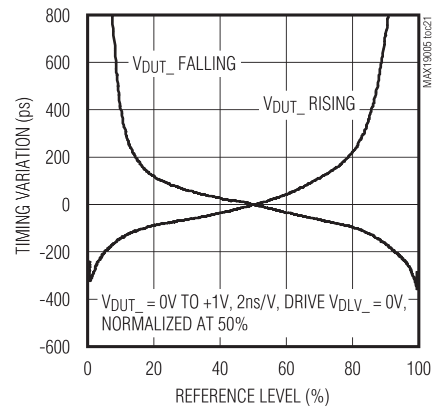
COMPARATOR OFFSET vs. COMMON-MODE VOLTAGE



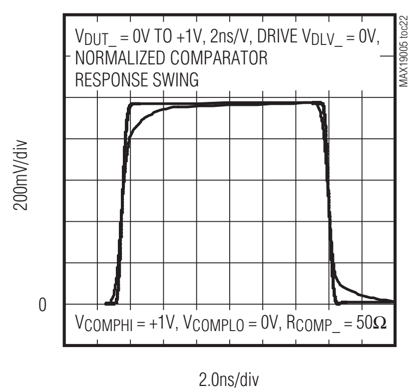
COMPARATOR OFFSET vs. TEMPERATURE



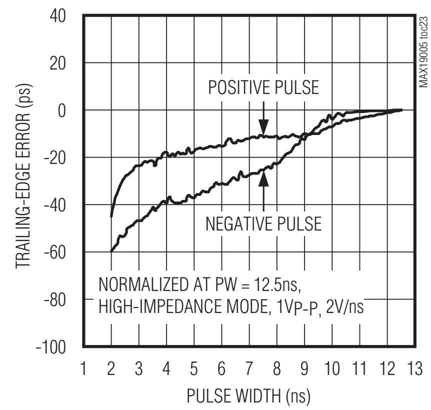
COMPARATOR WAVEFORM TRACKING



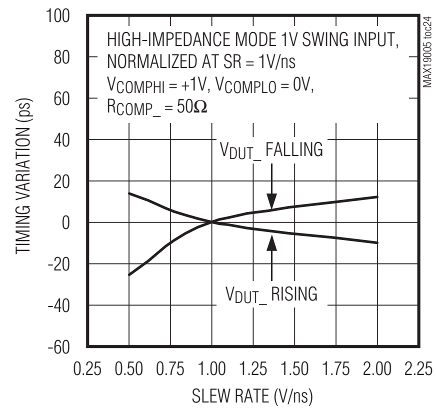
COMPARATOR RESPONSE vs. HIGH SLEW-RATE OVERDRIVE



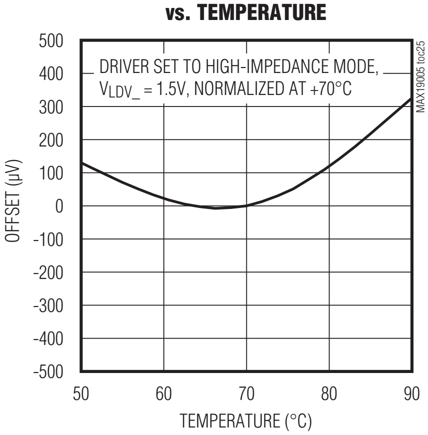
COMPARATOR TIMING VARIATION vs. PULSE WIDTH



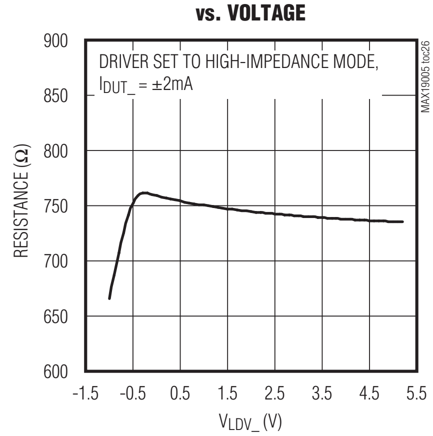
COMPARATOR TIMING VARIATION vs. INPUT SLEW RATE



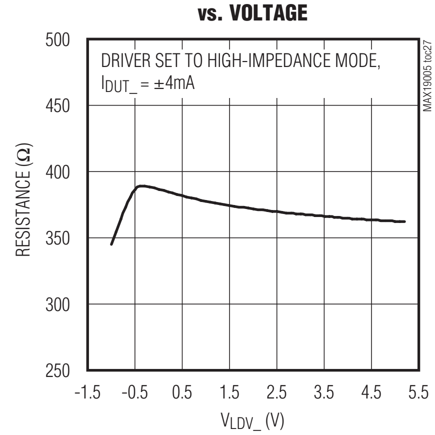
PASSIVE LOAD OFFSET vs. TEMPERATURE



PASSIVE LOAD HIGH RESISTOR vs. VOLTAGE



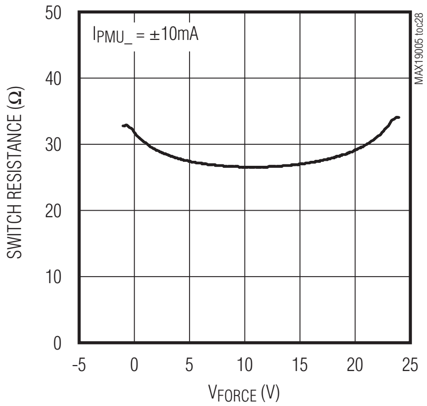
PASSIVE LOAD LOW RESISTOR vs. VOLTAGE



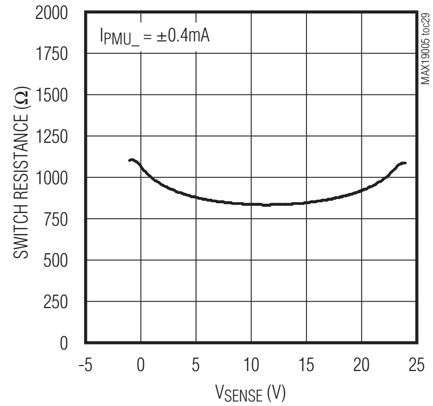
Typical Operating Characteristics (continued)

(V_{DD} = 8V, V_{SS} = -5V, V_L = 3V, V_{DDSW} = 24.6V, V_{SSSW} = 1.25V, V_{COMPHI} = 1V, V_{COMPLO} = 0V, $V_{LDV\_}$ = 0V, LOAD EN LOW = LOAD EN HIGH = 0, SWEN = 1, temperature coefficients T_J = +70°C are measured at T_J = +50°C, to +90°C unless otherwise noted.)

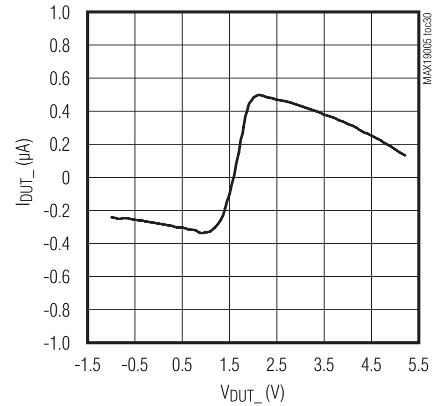
PMU_ FORCE SWITCH RESISTANCE vs. FORCE VOLTAGE



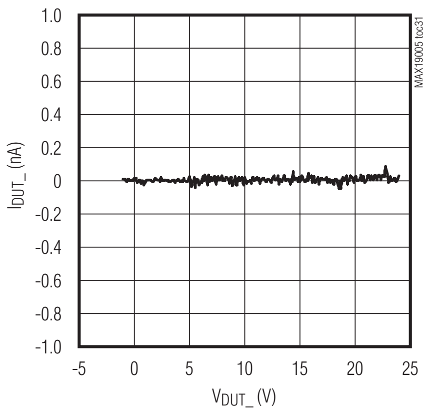
PMU_ SENSE SWITCH RESISTANCE vs. SENSE VOLTAGE



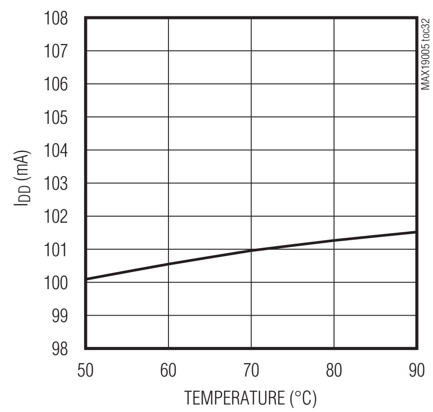
HIGH-IMPEDANCE LEAKAGE AT DUT_ vs. DUT_ VOLTAGE



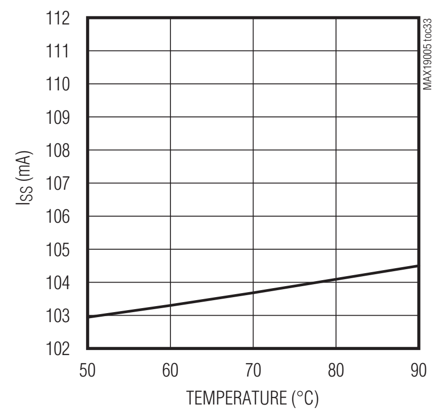
LOW-LEAKAGE CURRENT vs. DUT_ VOLTAGE



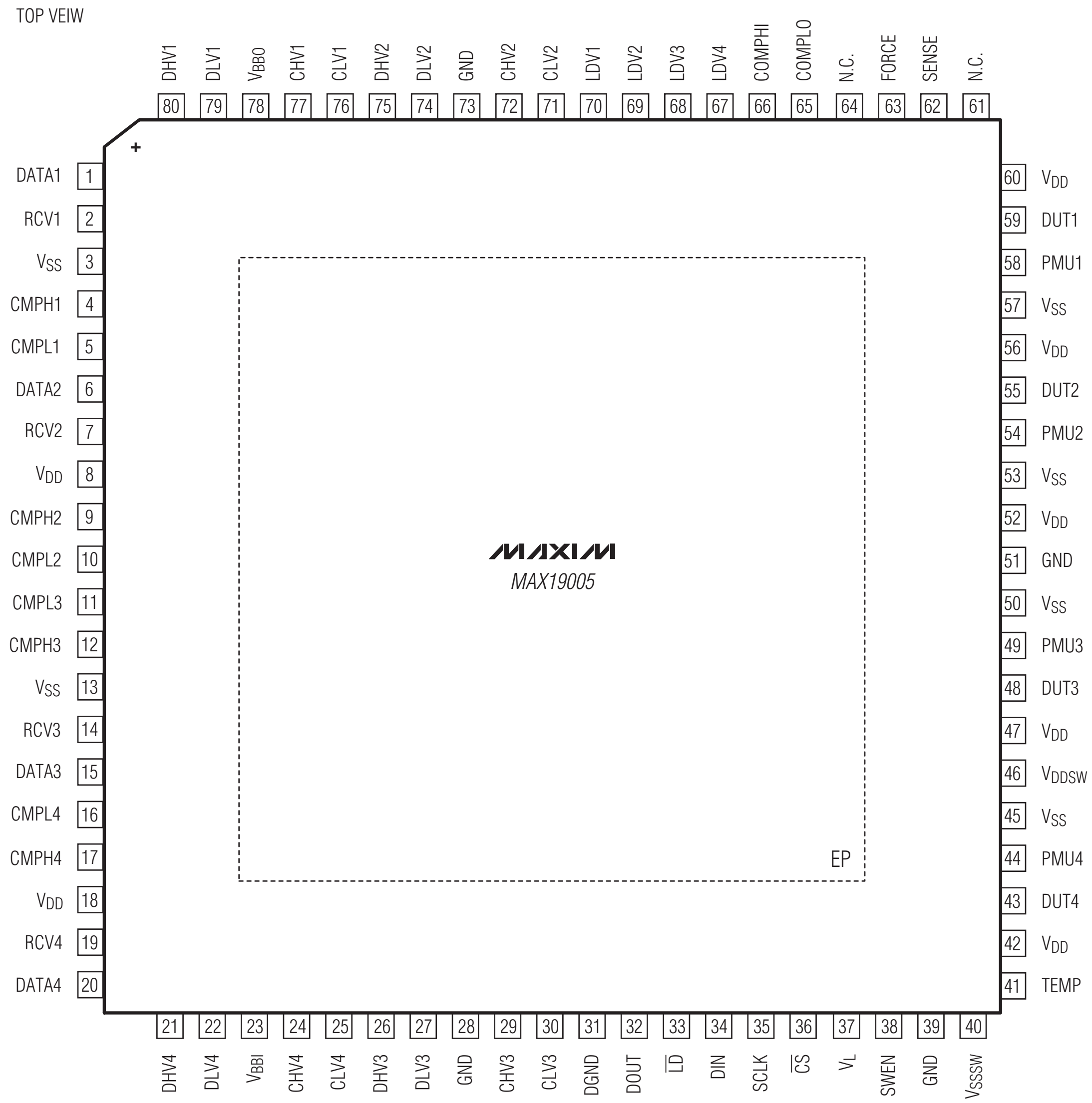
I_{DD} SUPPLY CURRENT vs. TEMPERATURE



I_{SS} SUPPLY CURRENT vs. TEMPERATURE



Pin Configuration



TQFP

Pin Description

PIN	NAME	FUNCTION
1	DATA1	Channel 1 Multiplexer Control Input. Selects the driver 1 input from DHV1 or DLV1 in drive mode. See Table 1 and Figure 2.
2	RCV1	Channel 1 Multiplexer Control Input. Sets the channel 1 mode to drive or receive. See Table 1 and Figure 2.
3, 13, 45, 50, 53, 57	V_{SS}	Negative Power-Supply Input
4	CMPH1	Channel 1 High-Side Comparator Output
5	CMPL1	Channel 1 Low-Side Comparator Output
6	DATA2	Channel 2 Multiplexer Control Input. Selects the driver 2 input from DHV2 or DLV2 in drive mode. See Table 1 and Figure 2.
7	RCV2	Channel 2 Multiplexer Control Input. Sets the channel 2 mode to drive or receive. See Table 1 and Figure 2.
8, 18, 42, 47, 52, 56, 60	V_{DD}	Positive Power-Supply Input
9	CMPH2	Channel 2 High-Side Comparator Output
10	CMPL2	Channel 2 Low-Side Comparator Output
11	CMPL3	Channel 3 Low-Side Comparator Output
12	CMPH3	Channel 3 High-Side Comparator Output
14	RCV3	Channel 3 Multiplexer Control Input. Sets the channel 3 mode to drive or receive. See Table 1 and Figure 2.
15	DATA3	Channel 3 Multiplexer Control Input. Selects the driver 3 input from DHV3 or DLV3 in drive mode. See Table 1 and Figure 2.
16	CMPL4	Channel 4 Low-Side Comparator Output
17	CMPH4	Channel 4 High-Side Comparator Output
19	RCV4	Channel 4 Multiplexer Control Input. Sets the channel 4 mode to drive or receive. See Table 1 and Figure 2.
20	DATA4	Channel 4 Multiplexer Control Input. Selects driver 4 input from DHV4 or DLV4 in drive mode. See Table 1 and Figure 2.
21	DHV4	Channel 4 Driver High-Voltage Input
22	DLV4	Channel 4 Driver Low-Voltage Input
23	V_{BBI}	DATA_/RCV_ Threshold Voltage Input
24	CHV4	Channel 4 High-Side Comparator Threshold Voltage Input
25	CLV4	Channel 4 Low-Side Comparator Threshold Voltage Input
26	DHV3	Channel 3 Driver High-Voltage Input
27	DLV3	Channel 3 Driver Low-Voltage Input
28, 39, 51, 73	GND	Analog Ground
29	CHV3	Channel 3 High-Side Comparator Threshold Voltage Input
30	CLV3	Channel 3 Low-Side Comparator Threshold Voltage Input
31	DGND	Digital Ground Connection

Pin Description (continued)

PIN	NAME	FUNCTION
32	DOUT	Serial-Interface Data Output
33	$\overline{LD}$	Load Input. Latches data from the serial input register to the control register on rising edge. Transparent when low.
34	DIN	Serial-Interface Data Input
35	SCLK	Serial Clock
36	$\overline{CS}$	Chip Select
37	V_L	Logic Power-Supply Input
38	SWEN	PMU Switch and Pin Switch Enable Input
40	V_{SSSW}	PMU Switch and Pin Switch Negative Power-Supply Input
41	TEMP	Temperature Sensor Output
43	DUT4	Channel 4 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 4.
44	PMU4	Channel 4 Parametric Measurement Unit Connection. PMU switch I/O node for channel 4.
46	V_{DDSW}	Positive PMU Switch and Pin Switch Power-Supply Input
48	DUT3	Channel 3 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 3.
49	PMU3	Channel 3 Parametric Measurement Unit Connection. PMU switch I/O node for channel 3.
54	PMU2	Channel 2 Parametric Measurement Unit Connection. PMU switch I/O node for channel 2.
55	DUT2	Channel 2 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 2.
58	PMU1	Channel 1 Parametric Measurement Unit Connection. PMU switch I/O node for channel 1.
59	DUT1	Channel 1 Device-Under-Test Connection. Driver, comparator, and load I/O node for channel 1.
61, 64	N.C.	No Connection. Not internally connected.
62	SENSE	PMU Sense Connection
63	FORCE	PMU Force Connection
65	COMPLO	Comparator Output Low-Voltage Reference Input
66	COMPHI	Comparator Output High-Voltage Reference Input
67	LDV4	Channel 4 Load Voltage Input
68	LDV3	Channel 3 Load Voltage Input
69	LDV2	Channel 2 Load Voltage Input
70	LDV1	Channel 1 Load Voltage Input
71	CLV2	Channel 2 Low-Side Comparator Threshold Voltage Input
72	CHV2	Channel 2 High-Side Comparator Threshold Voltage Input
74	DLV2	Channel 2 Driver Low-Voltage Input
75	DHV2	Channel 2 Driver High-Voltage Input
76	CLV1	Channel 1 Low-Side Comparator Threshold Voltage Input
77	CHV1	Channel 1 High-Side Comparator Threshold Voltage Input
78	V_{BBO}	Comparator Output Threshold Voltage Output
79	DLV1	Channel 1 Driver Low-Voltage Input
80	DHV1	Channel 1 Driver High-Voltage Input
—	EP	Exposed Pad. Leave unconnected or connect to GND.

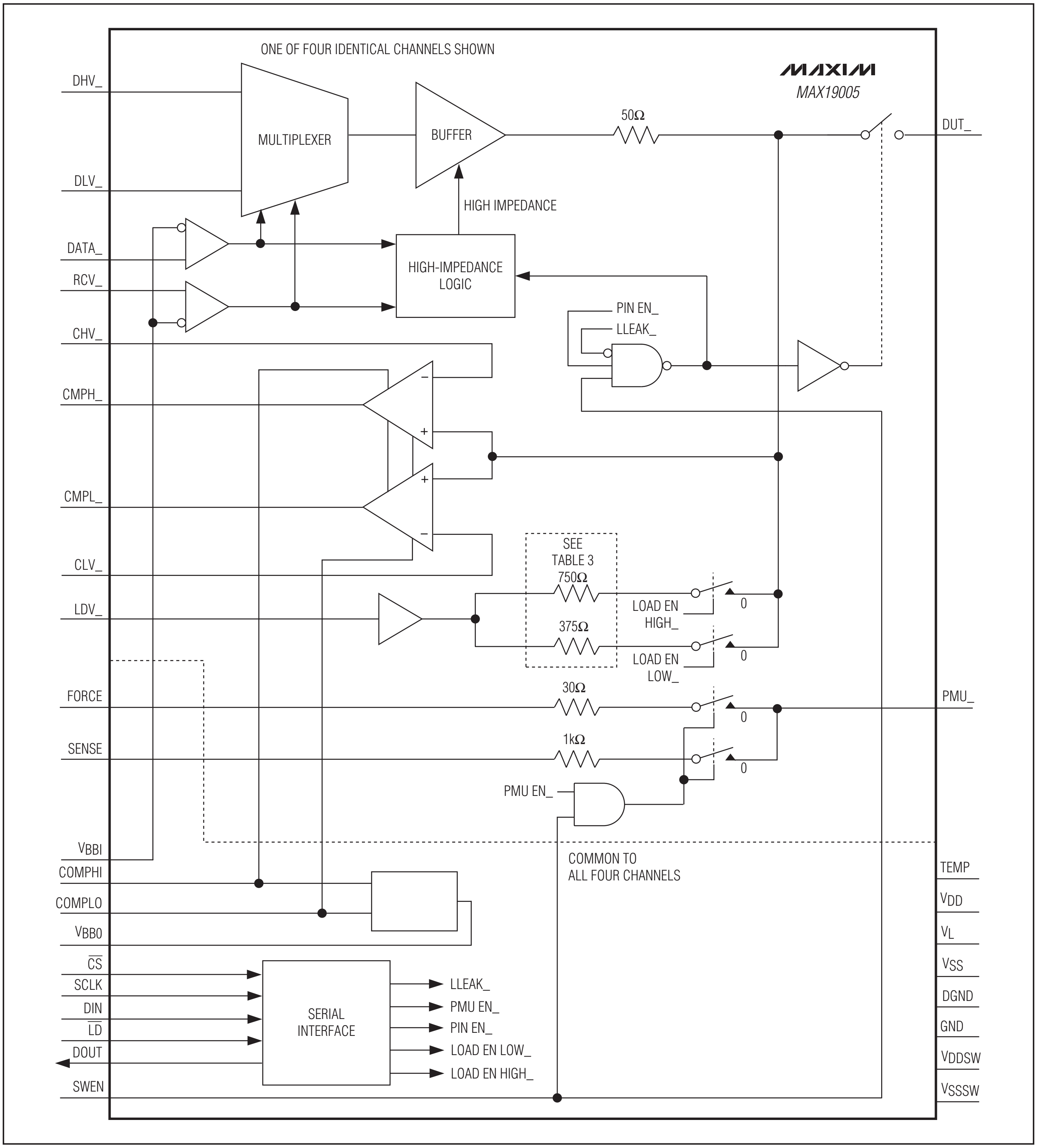


Figure 2. Block Diagram

Detailed Description

The MAX19005 is a four-channel, ultra-low-power, pin-electronics IC for automated test equipment that includes, for each channel, a two-level pin driver, a window comparator, a passive load, and a Kelvin instrument connection (Figure 2). All functions feature a -1V to +5.2V operating range and the drivers include a high-impedance mode. The comparators feature programmable output voltages, allowing optimization for different CMOS interface standards. The loads have selectable output resistance for optimizing DUT_ current loading. The Kelvin paths allow accurate connection of an instrument with ±25mA source/sink capability. Additionally, the IC offers a low-leakage mode that reduces DUT_ leakage current to less than 20nA.

Each of the four channels feature single-ended CMOS-compatible inputs (DATA_ and RCV_) for control of the driver signal path (Figure 3). The IC mode operations are programmed through a 3-wire, low-voltage CMOS-compatible serial interface.

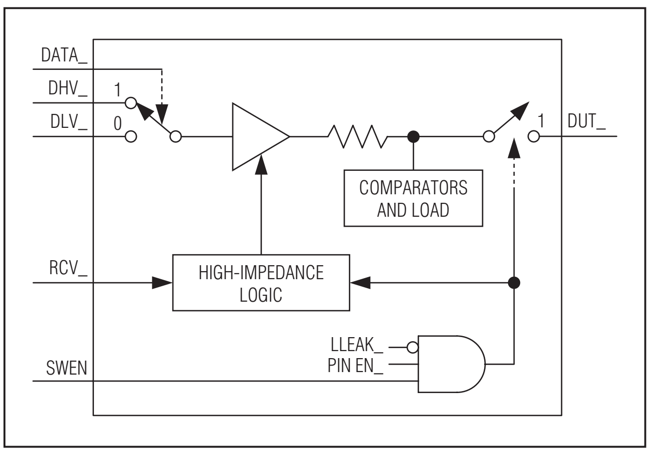


Figure 3. Multiplexer and Driver Channel

The driver input is a high-speed multiplexer that selects one of two voltage inputs: DHV_ and DLV_. This switching is controlled by high-speed inputs DATA_ and RCV_. DATA_ and RCV_ are single-ended inputs with threshold levels (V_{BBI}). Each channel's threshold levels are independently buffered to minimize crosstalk.

DUT_ can be toggled at high speed between the buffer output and high-impedance mode, or it can be placed into low-leakage mode (Figure 3, Table 1). High-speed input RCV_ and mode-control bit LLEAK_ control these modes. In high-impedance mode, the bias current at DUT_ is less than 2µA over the -1V to +5.2V range, while the node maintains its ability to track high-speed signals. In low-leakage mode, the bias current at DUT_ is further reduced to less than 20nA, and signal tracking slows.

The nominal driver output resistance is 49.5Ω.

Comparators

The IC provides two independent high-speed comparators for each channel. Each comparator has one input connected internally to DUT_ and the other input connected to either CHV_ or CLV_ (Figure 2). Comparator outputs are a logical result of the input conditions, as indicated in Table 2.

The comparator output voltages are easily interfaced to a wide variety of logic standards. Use buffered inputs COMPHI and COMPLO to set the high and low output voltages. For correct operation, COMPHI should be greater than or equal to COMPLO. The comparator 50Ω output impedance provides source termination (Figure 4). V_{BBO} output voltage is provided, (COMPHI + COMPLO)/2.

Table 1. Component List

EXTERNAL PIN CONNECTIONS			INTERNAL REGISTER CONTROL BITS		DRIVER STATUS	PIN SWITCH STATUS
RCV_	DATA_	SWEN	PIN EN_	LLEAK_		
0	0	1	1	0	DUT_ = DLV_	Short
0	1	1	1	0	DUT_ = DHV_	Short
1	X	1	1	0	High impedance	Short
X	X	0	X	0	0V	Open
X	X	X	0	0	0V	Open
X	X	X	X	1	0V (low power)	Open

X = Don't care.

Table 2. Comparator Logic

CONDITION		CMPH_	CMPL_
DUT_ < CHV_	DUT_ < CLV_	0	0
DUT_ < CHV_	DUT_ > CLV_	0	1
DUT_ > CHV_	DUT_ < CLV_	1	0
DUT_ > CHV_	DUT_ > CLV_	1	1

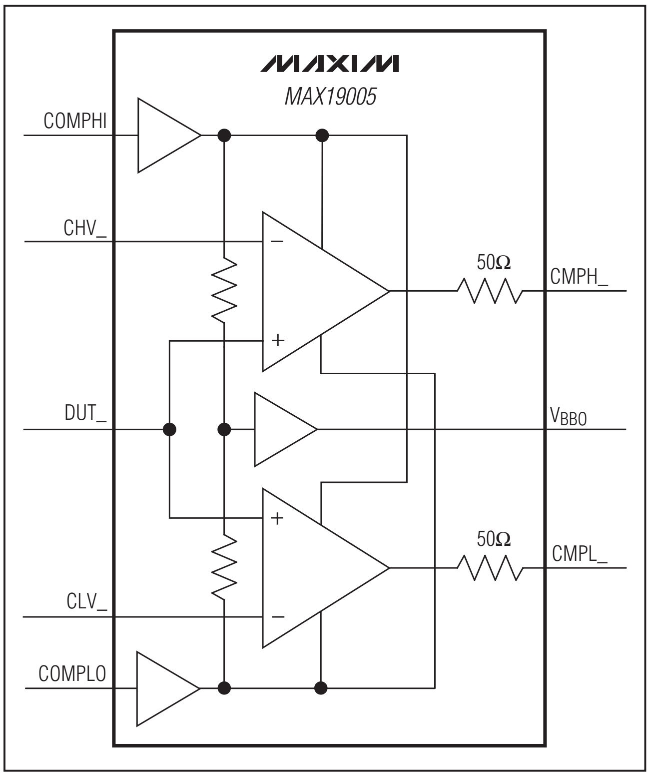


Figure 4. Complementary 50Ω Comparator Outputs

Passive Load

The IC channels each feature a passive load consisting of a buffered input voltage (LDV_) connected to DUT_ through two resistive paths (Figure 2). Each path connects to DUT_ individually by a switch controlled through the serial interface. Programming options include none (load disconnected), either, or both paths connected. The loads facilitate fast open/short testing in conjunction with the comparator, and pullup of open-drain DUT_ outputs. See Table 3.

Table 3. Passive Load Logic

INTERNAL CONTROL BITS		PASSIVE LOAD STATUS
LOAD EN HIGH_	LOAD EN LOW_	
0	0	Disconnect
0	1	375Ω load connect
1	0	750Ω load connect
1	1	750Ω ll 375Ω load connect

Table 4. PMU Switch Logic

EXTERNAL CONNECTION	INTERNAL CONTROL BIT	PMU SWITCH STATUS
SWEN	PMU EN_	
0	X	Open
1	0	Open
1	1	Short

X = *Don't care.*

Parametric Switches

Each of the four IC channels provide force-and-sense paths for connection of a PMU or other DC resource to the device-under-test (Figure 2). Both force and sense switches are simultaneously controlled through the serial interface providing maximum application flexibility. PMU_ and DUT_ are provided on separate pins, allowing designs that do not require the parametric switch feature to avoid the added capacitance of PMU_. It also allows PMU_ to connect to DUT_, either directly or with an impedance-matching network. See Table 4.

Low-Leakage Mode (LLEAK_)

Asserting LLEAK_ through the serial port places the IC into a very-low-leakage state. See the *Electrical Characteristics* section. This mode is convenient for making IDDQ and PMU measurements without the need for an output disconnect relay. LLEAK_ control is independent for each channel.

When DUT_ is driven with a high-speed signal while LLEAK_ is asserted, the leakage current momentarily increases beyond the limits specified for normal operation. The low-leakage recovery specification in the *Electrical Characteristics* section indicates device behavior under this condition.

Temperature Monitor

Each device supplies a single temperature output signal (TEMP) that asserts a nominal +3.43V output voltage at a +70°C (343K) die temperature. The output voltage increases proportionately with temperature at a rate of 10mV/°C. The temperature sensor output impedance is 17kΩ (typ).

Serial Interface and Device Control

A CMOS-compatible serial interface controls the IC modes (Figure 5). Control data flow into a 12-bit shift register (LSB first) and are latched when $\overline{\text{CS}}$ is taken high. Data from the shift register are then loaded to the per-channel control latches, as determined by bits D[8:11] (Figure 5 and Table 5). The latches contain the five mode bits for each channel of the device. The mode bits, in conjunction with external inputs DATA_ and RCV_, manage the features of each channel. Transfer data asynchronously from the input registers to the channel registers by forcing $\overline{\text{LD}}$ low. With $\overline{\text{LD}}$ always low, data transfer on the rising edge of $\overline{\text{CS}}$.

Heat Removal

With adequate airflow, no external heat sinking is needed under most operating conditions. If excess heat must be dissipated through the exposed pad, solder it to circuit-board copper. The exposed pad must be either left unconnected, isolated, or connected to GND.

Power Minimization

To minimize power consumption, activate only the needed channels. Each channel placed in low-leakage mode saves approximately 240mW.

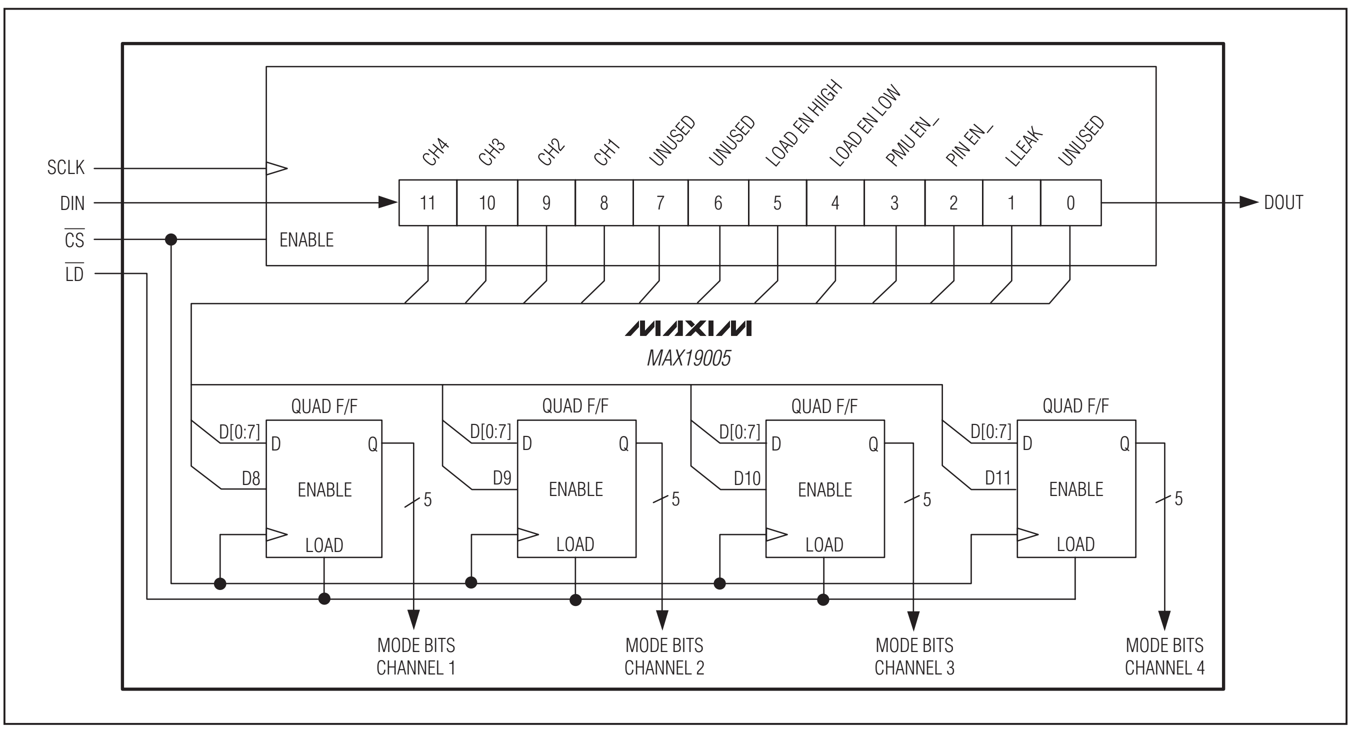


Figure 5. Serial Interface

Table 5. Control Register Bits

BIT	NAME	FUNCTION	BIT STATE		POWER-UP STATE
			0	1	
D0	—	Unused	X	X	0
D1	LLEAK	Assert low-leakage mode	Active	Low leakage	0
D2	PIN EN	Enable pin switch	Disabled	Enabled	0
D3	PMU EN	Enable PMU switch	Disabled	Enabled	0
D4	LOAD EN LOW	Enable low load resistor	Disabled	Enabled	0
D5	LOAD EN HIGH	Enable high load resistor	Disabled	Enabled	0
D6	—	Unused	X	X	0
D7	—	Unused	X	X	0
D8	CH1	Update channel 1 control register	Disabled	Enabled	1
D9	CH2	Update channel 2 control register	Disabled	Enabled	1
D10	CH3	Update channel 3 control register	Disabled	Enabled	1
D11	CH4	Update channel 4 control register	Disabled	Enabled	1

X = Don't care.

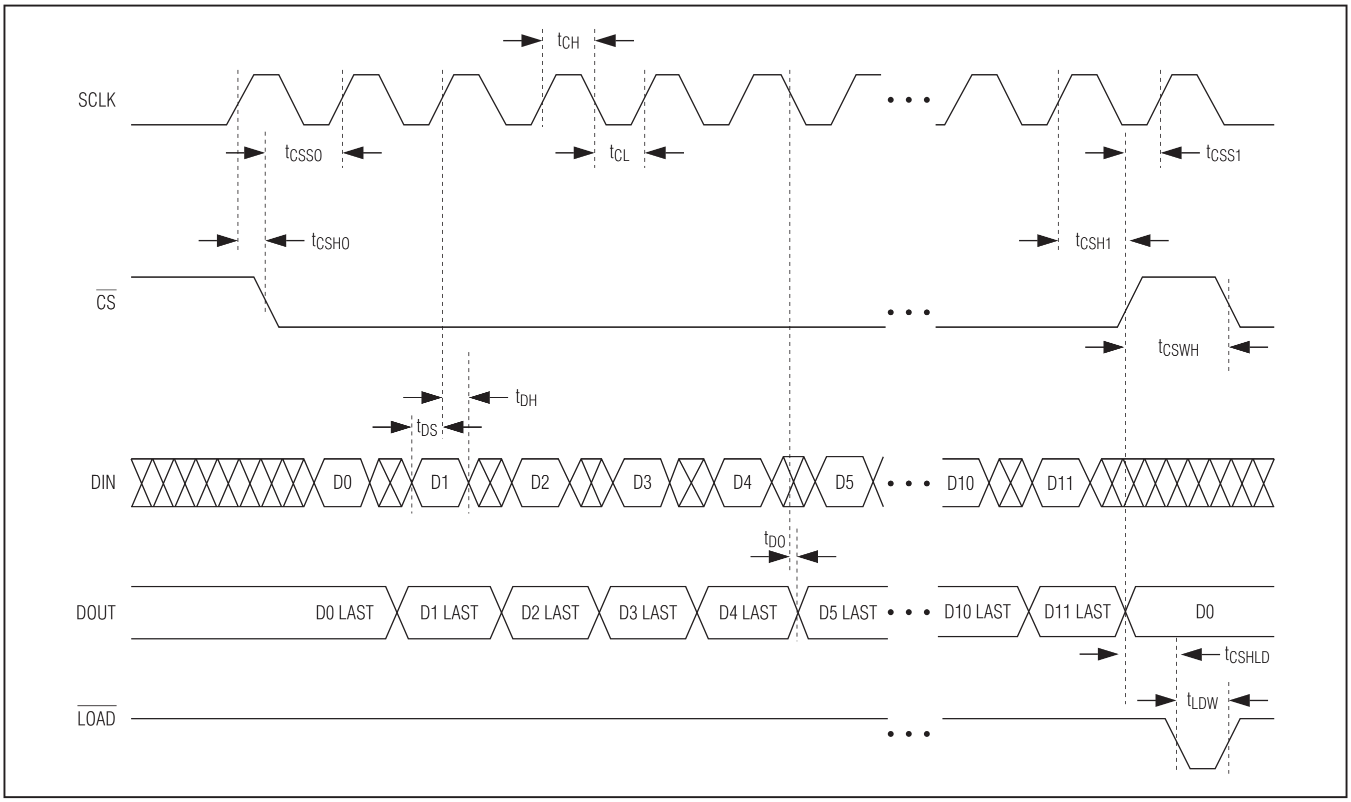


Figure 6. Serial-Interface Timing

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	HEAT EXTRACTION
MAX19005CCS+	0°C to +70°C	80 TQFP-EP*	Bottom

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
80 TQFP-EP	C80E+4	**21-0115**	**90-0152**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	—