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MAX19505–MAX19507/ MAX19515–MAX19517 Evaluation Kits

General Description

The MAX19505–MAX19507/MAX19515–MAX19517 evaluation kits (EV kits) are fully assembled and tested circuit boards that contain all the components necessary to evaluate the performance of this family of 8-bit and 10-bit analog-to-digital converters (ADCs). The EV kits also include Windows® 2000-, Windows XP®-, and Windows Vista®-compatible software that provides a simple graphical user interface (GUI) for exercising the programmable features of the MAX19505–MAX19507/ MAX19515–MAX19517.

The MAX19505–MAX19507/MAX19515–MAX19517 EV kits accept a single-ended analog input from an analog signal source. The EV kits provide an on-board circuit that transforms this analog single-ended signal into a differential signal. The ADC digital output can be captured easily with Maxim's data converter evaluation platform (DCEP). The EV kits operate from a single 5V power supply and provide on-board regulation for the analog, clock, digital, and logic circuitry.

Part Selection Table

PART	RESOLUTION (Bits)	SPEED (Msps)
MAX19505ETM+	8	65
MAX19506ETM+	8	100
MAX19507ETM+	8	130
MAX19515ETM+	10	65
MAX19516ETM+	10	100
MAX19517ETM+	10	130

Features

♦ **Single Power-Supply Operation**
♦ **Direct Interface with Maxim DCEP Data Source Board Using QSH Connectors**
♦ **Low-Voltage and Low-Power Operation**
♦ **On-Board Single-Ended to Differential Transformer Circuitry**
♦ **Differential or Single-Ended Clock Configuration**
♦ **On-Board Clock-Shaping Circuit with Adjustable Duty Cycle**
♦ **On-Board SPI™ Interface Circuit**
♦ **User-Selectable Supply Voltages**
♦ **Data Source (FPGA) Board Available (Order DCEP)**
♦ **Lead(Pb)-Free and RoHS Compliant**
♦ **Fully Assembled and Tested**

Ordering Information

PART	TYPE
MAX19505EVKIT+	EV Kit
MAX19506EVKIT+	EV Kit
MAX19507EVKIT+	EV Kit
MAX19515EVKIT+	EV Kit
MAX19516EVKIT+	EV Kit
MAX19517EVKIT+	EV Kit
DCEP	Data Converter Evaluation Platform

+Denotes lead(Pb)-free and RoHS compliant.

Component List

DESIGNATION	QTY	DESCRIPTION
CLK, SYNC, VINA, VINB,	4	SMA PCB vertical-mount connectors
C1, C4, C9, C10, C11, C14, C15, C17–C21, C23–C26	16	0.1µF ±10%, 50V X5R ceramic capacitors (0603) Murata GRM188R61H104K TDK C1608X7R1H104K
C2, C3	2	10pF ±5%, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H100J TDK C1005C0G1H100J
C5, C7, C22, C27, C28, C74, C76, C77	8	10µF ±20%, 6.3V X5R ceramic capacitors (0805) Murata GRM21BR60J106K TDK C2012X5R0J106M

DESIGNATION	QTY	DESCRIPTION
C6, C8, C60	3	1µF ±10%, 16V X7R ceramic capacitors (0603) TDK C1608X7R1C105K Murata GRM188R71C105K
C12, C13	2	22pF ±5%, 50V C0G ceramic capacitors (0603) TDK C1608C0G1H220J
C16	1	3300pF ±10%, 50V X7R ceramic capacitor (0603) TDK C1608X7R1H332K
C29, C48–C53, C65–C68, C70–C73	15	0.1µF ±20%, 10V X5R ceramic capacitors (0402) TDK C1005X5R1A104M

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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

Component List (continued)

DESIGNATION	QTY	DESCRIPTION
C30, C31	2	100pF ±5%, 50V C0G ceramic capacitors (0402) Murata GRM1555C1H101J TDK C1005C0G1H101J
C32–C35	0	Not installed, ceramic capacitors (0402)
C54, C55, C75, C78	4	0.01µF ±10%, X7R 25V ceramic capacitors (0603) Murata GRM188R71E103K Taiyo Yuden UMK107B103KZ
D1	1	Green surface-mount LED (0603)
D2	1	Dual Schottky diode (SOT23) Central Semi CMPD6263S+ Diodes, Inc. BAS70-04
FB1	1	Not installed, ferrite bead—short by PC trace (0603) TDK MMZ1608R301A
H1	0	Not installed, 2 x 5-pin JTAG header
J1	0	Not installed, dual-row (2 x 5) 10-pin header (0.1in centers)
J2, J3, J4, JU6, JU7, JU9, JU10	7	2-pin headers (cut to fit)
J5	1	120-position, high-speed connector Samtec QSH-060-01-L-D-A
J7	1	Dual-row (2 x 5) 10-pin header
JU1, JU2, JU3	3	4-pin headers (cut to fit)
P1	1	USB type-B right-angle female receptacle
RA1–RA4	4	47Ω ±5% resistor arrays Panasonic EXB-2HV-470J
R1, R13–R18, R50–R53	0	Not installed, resistors (0603)
R2, R43, R44	3	100kΩ ±5% resistors (0603)
R6	1	10kΩ ±5% resistor (0603)
R7	1	2.2kΩ ±5% resistor (0603)
R8	1	1.5kΩ ±5% resistor (0603)
R9, R10	2	27Ω ±5% resistors (0603)
R11	1	0Ω ±5% resistor (0603)
R12	1	220Ω ±5% resistor (0603)

DESIGNATION	QTY	DESCRIPTION
R19–R22	4	75Ω ±0.5% resistors (0603) Susumu RR0816Q-750-D IRC PFC-W0603LF-03-75R0-B or equivalent
R23–R26	4	121Ω ±0.5% resistors (0603) IRC PFC-W0603LF-03-1210-D or equivalent Susumu RR0816P-1210-D
R27–R34, R39, R40, R41, R47, R48, R49	0	Not installed, resistors—short by PC trace (0603)
R35–R38	0	Not installed, resistors—short by PC trace (0402)
R42, R54, R55	3	49.9Ω ±1% resistors (0603)
R46	1	10kΩ potentiometer, 19-turn, 3/8in
R56, R57	2	100Ω ±1% resistors (0603)
SW1, SW2	2	2-position, low-profile DIP switches
T1–T4	4	1:1 RF transformers Mini-Circuits ADT1-1WT+
T5	1	1:2 RF transformer Coilcraft TTWB-2-B
TP1, TP2	0	Not installed, test points
U1	1	See the *EV Kit-Specific Component List*
U2	1	Microcontroller (68 QFN-EP*) Maxim MAXQ2000-RAX+
U3	1	UART-to-USB converter (32 TQFP) FTDI FT232BL
U4	1	2.5V regulator (5 SC70) Maxim MAX8511EXK25+T (Top Mark: ADV)
U5	1	3.3V regulator (5 SC70) Maxim MAX8511EXK33+T (Top Mark: AEI)
U6	1	Single 1.8V to 5V level translator (6 SOT23) TI SN74LVC1T45DBVT (Top Mark: CT1_) TI SN74LVC1T45DBVR (Top Mark: CT1_)

EP = Exposed pad.

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Component List (continued)

DESIGNATION	QTY	DESCRIPTION
U7	1	Dual 1.8V to 5V level translator (8 SSOP) TI SN74LVC2T45DCTT (Top Mark: CT2_) TI SN74LVC2T45DCTR (Top Mark: CT2_)
U8	1	93C46 type 3-wire EEPROM (8 SO) 16-bit architecture Atmel AT93C46A-10SU-2.7
U10	1	TinyLogic ULP-A inverter (6 SC70) Fairchild NC7WV04P6X
U11, U12	2	Low-voltage 16-bit registers (48 TSSOP) TI SN74AUC16244DGGR

DESIGNATION	QTY	DESCRIPTION
U13	1	1.8V regulator (5 SC70) Maxim MAX8511EXK18+T (Top Mark: AEF)
U14, U15	2	Pin-selectable LDO regulators (8 TDFN) Maxim MAX8902AATA+ (Top Mark: ABG)
Y1	1	16MHz crystal
Y2	1	6MHz crystal
—	1	PCB: MAX19505/06/07/15/16/17 EVALUATION KIT+

EV Kit-Specific Component List

PART	DESIGNATION	DESCRIPTION
MAX19505EVKIT+		8-bit 65Msps dual ADC (48 TQFN) Maxim MAX19505ETM+
MAX19506EVKIT+		8-bit 100Msps dual ADC (48 TQFN) Maxim MAX19506ETM+
MAX19507EVKIT+		8-bit 130Msps dual ADC (48 TQFN) Maxim MAX19507ETM+
MAX19515EVKIT+	U1	10-bit 65Msps dual ADC (48 TQFN) Maxim MAX19515ETM+
MAX19516EVKIT+		10-bit 100Msps dual ADC (48 TQFN) Maxim MAX19516ETM+
MAX19517EVKIT+		10-bit 130Msps dual ADC (48 TQFN) Maxim MAX19517ETM+

Evaluate: MAX19505–MAX19507/MAX19515–MAX19517

Component Suppliers

SUPPLIER	PHONE	WEBSITE
Central Semiconductor Corp.	631-435-1110	www.centralsemi.com
Coilcraft, Inc.	847-639-6400	www.coilcraft.com
Diodes, Inc.	805-446-4800	www.diodes.com
Fairchild Semiconductor	888-522-5372	www.fairchildsemi.com
Future Technology Devices International Ltd.	—	www.ftdichip.com
IRC, Inc.	361-992-7900	www.irctt.com
Mini-Circuits	718-934-4500	www.minicircuits.com
Murata Electronics North America, Inc.	770-436-1300	www.murata-northamerica.com
Panasonic Corp.	800-344-2112	www.panasonic.com
Samtec, Inc.	800-726-8329	www.samtec.com
Susumu International USA	208-328-0307	www.susumu-usa.com
Taiyo Yuden	800-348-2496	www.t-yuden.com
TDK Corp.	847-803-6100	www.component.tdk.com
Texas Instruments Inc.	972-644-5580	www.ti.com

Note: _Indicate that you are using the MAX19505, MAX19506, MAX19507, MAX19515, MAX19516, or MAX19517 when contacting these component suppliers._

MAX19505–MAX19507/MAX19515–MAX19517 EV Kit Files

FILE	DESCRIPTION
INSTALL.EXE	Installs the EV kit files on your computer
MAX19505.EXE	
MAX19506.EXE	
MAX19507.EXE	Application program
MAX19515.EXE	
MAX19516.EXE	
MAX19517.EXE	
FTD2XX.INF	USB device driver file
UNINST.INI	Uninstalls the EV kit software
TROUBLESHOOTING_USB.PDF	USB driver installation help file

**MAXIM**

Quick Start

Recommended Equipment

- Single 5V, 1A DC power supply
- Signal generator with low phase noise and low jitter for clock input (e.g., HP 8644B)
- Signal generator for analog signal input (e.g., HP 8644B)
- Maxim DCEP (Data Converter Evaluation Platform)
- Analog bandpass filters (e.g., K&L Microwave) for input and clock signal
- User-supplied Windows 2000, Windows XP, or Windows Vista PC with two spare USB ports

Note: In the following sections, software-related items are identified by bolding. Text in **bold** refers to items from the EV kit software. Text in **bold and underlined** refers to items from the Windows operating system.

Procedure

The MAX19505–MAX19507/MAX19515–MAX19517 EV kits are fully assembled and tested surface-mount boards. Follow the steps below to verify board operation. **Caution: Do not turn on power supplies or enable signal generators until all connections are completed.**

1) Verify that shunts are installed across pins 1-3 of jumpers JU1, JU2, and JU3 (SPI connected).

2) Verify that no shunts are installed across jumpers JU6 (device enabled) and JU7 (SPI enabled).

3) Verify that shunts are installed across jumpers JU9 (AVDD connected) and JU10 (OVDD connected).

4) Set SW1 (1, 4) to the on position and SW1 (2, 3) to the off position (AVDD = 1.8V).

5) Set SW2 (1, 4) to the on position and SW2 (2, 3) to the off position (OVDD = 1.8V).

6) Connect the clock generator output to the clock bandpass filter input.

7) Connect the output of the clock bandpass filter to the CLK SMA connector.

8) Connect the output of the analog signal generator to the input of the signal bandpass filter. Keep the cable connection between the signal generators, filters, and EV kit board as short as possible for optimum dynamic performance.

9) Connect the output of the signal bandpass filter to the VINA SMA connector. Note: It is recommended that a 3dB or 6dB attenuation pad be used to reduce reflections and distortion from the bandpass filter.

10) Apply power to the DCEP at J4 using the provided supply connector.

11) Carefully connect the boards by aligning J5 on the DCEP to J5 on the EV kit. Gently press them together.

12) Connect the USB cable from the computer's type-A USB port to the DCEP board's type-B USB port.

13) Connect the 5V, 1A power supply to VIN. Connect the ground terminal of this supply to the corresponding GND pad.

14) Connect the USB cable from the computer's type-A USB port to the EV kit board's type-B USB port.

15) Visit **www.maxim-ic.com/evkitsoftware** to download the latest version of the MAX19517 EV kit software and install it on your computer by running the INSTALL.EXE program. The program files are copied and icons are created in the Windows **Start** menu.

16) Start the MAX19517 program by opening its icon in the **Start** menu.

17) Turn on the 5V power supply.

18) Enable the signal generators.

19) Set the clock signal generator for an output amplitude of 2V$_{P-P}$ or higher (recommended +16dBm to +19dBm for optimum AC performance for input frequencies > 100MHz) and the frequency (f$_{CLK}$) as appropriate.

20) Set the analog input signal generators for an output amplitude of less than or equal to 2V$_{P-P}$ and to the desired frequency.

21) Verify that the two signal generators are phase locked to each other. Adjust the output power level of the signal generators to overcome cable, bandpass filter, and attenuation pad losses at the input.

22) Download the DCEP software from the included CD-ROM and install it on your computer by running the DCEP Installation XX MMM YY.EXE file. Note that XX MMM YY indicates the day, month, and year of the available software build. The program files are copied and icons are created in the Windows **Start** menu.

23) Start the DCEP program by opening its icon in the **Start** menu.

24) Collect data using the DCEP software.

__Detailed Description of Software

User-Interface Panel

The program's main window contains two tabs, **Input/Output/Clock** (Figure 1) and **Power Management** (Figure 2), that provide controls for the MAX19517 software-configurable features. The **Input/Output/Clock** tab sheet provides controls for **Output Format**, **Input Common Mode**, **Output CMOS Termination**, **Output Timing Control**, and **Clock Controls**. The **Power Management** tab sheet provides controls for **Power Management** and **Output Driver Power Mgmt. Controls**. Changes to the controls result in a write operation that updates the appropriate registers of the ADC. A status bar is also provided at the bottom of the program's main window and is used to verify command module and device connectivity. For reference, a list of registers and their content is provided in a column on the right side of the program's main window.
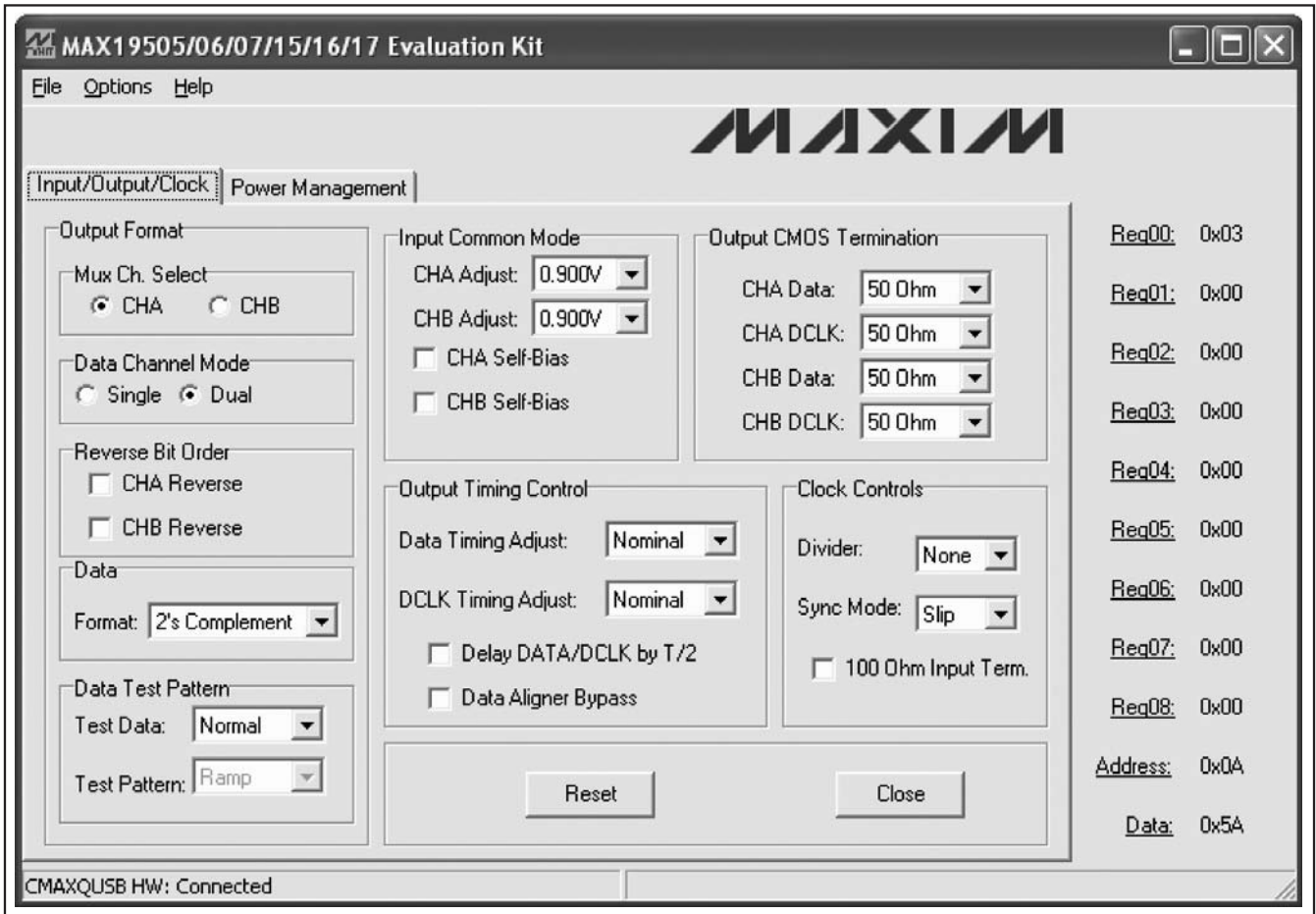
Figure 1. MAX19517 EV Kit Software (Input/Output/Clock Tab)
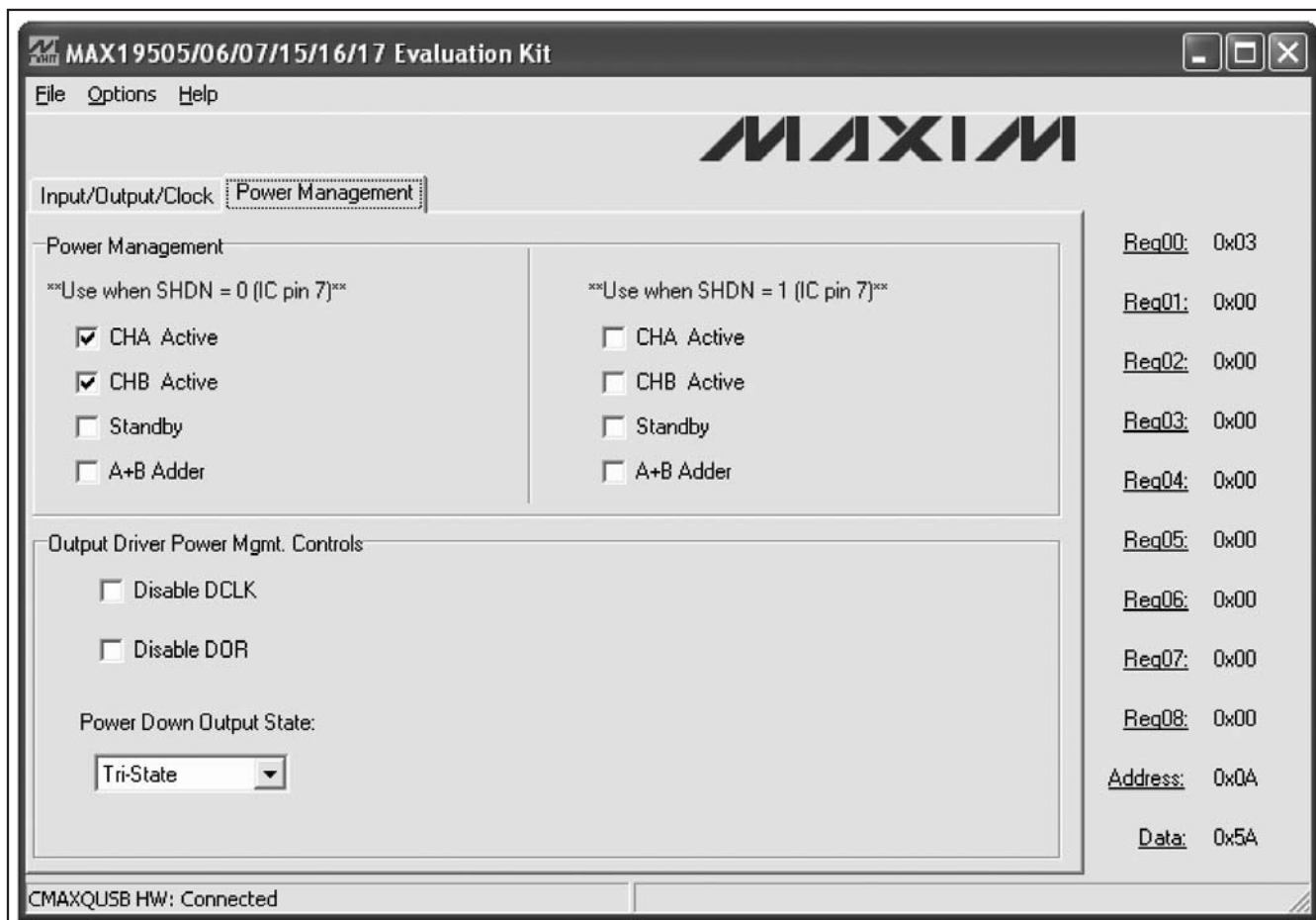
Figure 2. MAX19517 EV Kit Software (Power Management Tab)

Input/Output/Clock Tab

Output Format

The **Output Format** group box contains several functions that format the output data. The option to select between single or dual data channels or set the multiplexer between channels A or B is available through proper selection of the radio buttons in the **Data Channel Mode** and **Mux Ch. Select** group boxes. The **CHA Reverse** and **CHB Reverse** checkboxes in the **Reverse Bit Order** group box allow the user to reverse the bit order of channels A and B, respectively.

The **Format** drop-down list in the **Data** group box configures the output data to two's complement, offset binary, or gray code. The **Test Data** drop-down list in the **Data Test Pattern** group box gives the user the option to choose between normal and test data modes. When **Test Data mode** is selected, the **Test Pattern** drop-down list becomes active. The **Test Pattern** drop-down list allows the user to choose between ramping or alternating test pattern data.

Input Common Mode

The **CHA Adjust** and **CHB Adjust** drop-down lists set the input common-mode voltage according to the value selected. The **CHA Self-Bias** and **CHB Self-Bias** checkboxes apply common-mode voltages to input pins when checked, and disable common-mode inputs when unchecked.

Output CMOS Termination

The **Output CMOS Termination** group box contains independent controls to set the CMOS back termination of **CHA Data** and **CHB Data** and **CHA DCLK** and **CHB DCLK**. The **CHA Data** and **CHB Data** drop-down lists set the data termination, while the **CHA DCLK** and **CHB DCLK** drop-down lists sets the DCLK termination.

MAX19505–MAX19507/
MAX19515–MAX19517 Evaluation Kits

Output Timing Control

The **Output Timing Control** group box contains controls to make adjustments to data and DCLK timing. The **Data Timing Adjust** drop-down list adjusts DATA timing by the selected value. The **DCLK Timing Adjust** drop-down list adjusts DCLK timing by the selected value. By checking the **Delay DATA/DCLK by T/2** checkbox, DATA and DCLK outputs are delayed by a factor of T/2. The **Data Aligner Bypass** checkbox bypasses the data aligner delay line when checked. For more details on output timing control, refer to the respective IC data sheet.

Clock Controls

The **Clock Controls** group box contains controls for manipulating the clock. The **Divider** drop-down list sets the clock divider. The **Sync Mode** drop-down list sets clock synchronization to either slip or edge mode. In slip mode, the divided output is forced to skip a state transition on the third rising edge of the input clock (CLK) after the rising edge of SYNC. In edge mode, the divided output is forced to state 0 on the third rising edge of CLK. The **100 Ohm Input Term.** checkbox switches 100Ω across differential clock inputs when checked. For more details on clock synchronization and control, refer to the respective IC data sheet.

Power Management Tab

Power Management Controls

The **Power Management** group box contains two sets of controls. The first set is used only when the SHDN pin on the EV kit is set low; the second set is used only when the SHDN pin on the EV kit is set high. When checked, the **CHA Active** and **CHB Active** checkboxes activate channel A and channel B, respectively, and power down/standby channel A and channel B when

unchecked. The **Standby** checkbox toggles between standby mode when checked and full power-down mode when unchecked, as long as **CHA Active** or **CHB Active** checkboxes are unchecked. The **A+B Adder** mode checkbox toggles between A+B adder mode when checked and normal dual mode when unchecked. For more details on power management, refer to the respective IC data sheet.

Output Driver Power Management Controls

The **Output Driver Power Mgmt. Controls** group box contains controls to disable the digital clock (DCLK) and out-of-range indicator (DOR). The **Disable DCLK** checkbox disables the DCLK when checked and the **Disable DOR** checkbox disables DOR. Note: Disable DCLK and disable DOR applies to CMOS modes only. The **Power Down Output State** drop-down list sets the digital output high, low, or to tri-state during power-down. For more details on output driver power management control, refer to the respective IC data sheet.

Simple SPI/SMBus Commands

There are two methods for communicating with the MAX19505–MAX19507/MAX19515–MAX19517: through the normal user-interface windows (Figures 1 and 2) or through the SMBus commands available by selecting the **Interface (Advanced Users)** menu item from the **Options** menu bar. The **Maxim Command Module Interface** window pops up and includes a **3-wire interface** tab that allows data to be written to each individual register.

The SMBus dialog boxes accept numeric data in binary, decimal, or hexadecimal. Hexadecimal numbers should be prefixed by $ or 0x. Binary numbers must be exactly eight digits. See Figure 3 for an illustration of this tool.

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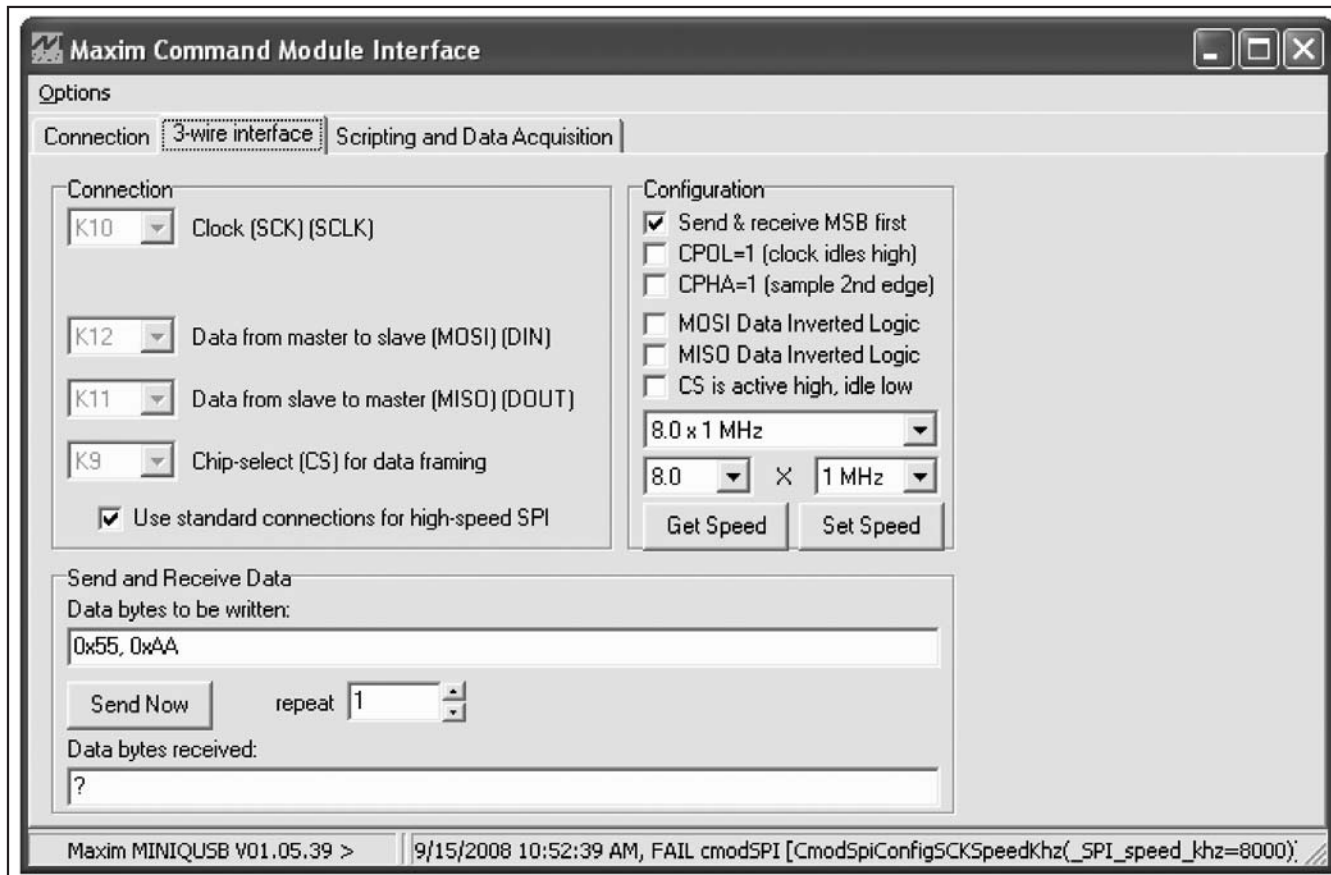Evaluate: MAX19505–MAX19507/MAX19515–MAX19517

Figure 3. Interface Diagnostic Window (3-Wire Interface Tab)

_Detailed Description of Hardware

The MAX19505–MAX19507/MAX19515–MAX19517 evaluation kits (EV kits) are fully assembled and tested circuit boards that contain all the components necessary to evaluate the performance of this family of 8-bit and 10-bit analog-to-digital converters (ADCs).

The ADCs accept differential input signals; however, on-board transformers (T1–T4) convert a readily available single-ended source output to the required differential signal. The input signals of the ADCs can be measured using a differential oscilloscope probe at headers J2 and J3.

Output drivers (U11 and U12) buffer the output signals of the data converter. The digital outputs of each EV kit are accessible at header J5.

Each EV kit is designed as a four-layer PCB to optimize the performance of this family of ADCs. Separate analog,

digital, clock, and buffer power planes minimize noise coupling between analog and digital signals. The 100Ω differential microstrip transmission lines are used for analog and clock inputs. The 50Ω microstrip transmission lines are used for all digital outputs. The trace lengths of the 100Ω differential input lines are matched to within a few thousandths of an inch to minimize layout-dependent input-signal skew.

Using the DCEP with the EV Kit

The data converter evaluation platform (DCEP) is required for evaluation of this particular family of evaluation kits. EV kit-specific database files are required to configure the DCEP software and can be downloaded from the included CD-ROM. When loading the DCEP database files, select the appropriate .dsm file for the specific kit used.

Connecting the DCEP to the EV Kit

The DCEP and the EV kit boards can be connected using the specified on-board connectors. J5 on the EV kit mates with J5 on the DCEP board. Alternatively, the two boards can be connected with coaxial ribbon cables (Samtec, part no. HQCD-060.00-STR-TBR-1). Note that it is necessary to use either the on-board connectors or cables to obtain a reliable electrical connection between the two boards.

Power Supplies

The MAX19505–MAX19507/MAX19515–MAX19517 EV kits operate from a single 5V DC power supply (VIN) and provide on-board regulation to power the analog, digital, and clock-shaping circuit blocks. The analog and clock (AVDD) are regulated to 1.8V through the MAX8902A (U14), a pin-selectable linear regulator. The digital output is regulated to 1.8V through the MAX8902A (U15) as well. SW1 and SW2 are provided to select the desired output of U14 and U15. See Tables 1 and 2 for AVDD and OVDD supply options. The MAX8511 (U13) regulates VIN to provide a 1.8V DC to power the logic circuitry (VLOGIC). Jumpers JU9 and JU10 are provided to either disconnect or measure current through AVDD and OVDD, respectively.

Table 1. MAX8902A Output Voltage for AVDD (SW1)

SW1 POSITION 1 (SELB)	SW1 POSITION 2 (SELA)	AVDD (V)
Off (unconnected)	Off (unconnected)	2.5
Off (unconnected)	On (GND)	3.3
On (GND)	Off (unconnected)	1.8*
On (GND)	On (GND)	3.0

*Default.

Table 2. MAX8902A Output Voltage for OVDD (SW2)

SW1 POSITION 1 (SELB)	SW1 POSITION 2 (SELA)	OVDD (V)
Off (unconnected)	Off (unconnected)	2.5
Off (unconnected)	On (GND)	3.3
On (GND)	Off (unconnected)	1.8*
On (GND)	On (GND)	3.0

*Default.

Clock Input

The data converter allows for either differential or single-ended signals to drive the clock inputs. The MAX19505–MAX19507/MAX19515–MAX19517 EV kits support both methods.

In single-ended operation, the clock signal is applied to the ADC through a buffer (U10). In differential mode, an on-board transformer converts a user-supplied single-ended analog input and generates a differential analog signal, which is then applied to the ADC's input pins.

Configuring the EV Kits for Single-Ended Clock Operation

To configure the MAX19505–MAX19507/MAX19515–MAX19517 EV kits for single-ended clock operation, the following modifications must be made to the clock circuit:

1) Cut the traces at locations R47, R48, and R49.

2) Install 0Ω resistors at locations R51 and R52.

3) Install a 49.9Ω ±1% resistor at location R50.

In single-ended clock configuration, potentiometer R46 can be utilized to control the duty cycle of the clock input signal. Measure the clock input at J4 and adjust R46 until the desired duty cycle is achieved.

Input Signal

Although this family of ADCs accepts differential analog input signals, the EV kits only require single-ended analog input signals. Insertion losses due to a series-connected filter and the interconnecting cables decrease the amount of power seen at the EV kit input. Account for these losses when setting the signal generator amplitude. On-board transformers (T1–T4) convert the single-ended analog input signals and generate the recommended differential analog signals at the ADCs' differential input pins. The input circuit supports input frequencies from 1MHz to 400MHz.

Output Signal

The MAX19505, MAX19506, and MAX19507 feature two 8-bit, parallel, CMOS-compatible digital outputs that transmit the converted analog input signals. The higher resolution MAX19515, MAX19516, and MAX19517 feature two 10-bit, parallel, CMOS-compatible digital outputs that transmit the converted analog input signals. Each set of 8-bit or 10-bit digital outputs also includes a clock bit (DCLKA/B) and overrange bit (DORA/B) to accommodate data synchronization and error detection. See the *Output Bit Locations* section for more details on how to configure these 8-bit and 10-bit converter outputs.

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Output Bit Locations

Two drivers (U11 and U12) buffer the digital outputs of the individual ADCs. These drivers are able to drive large capacitive loads, which may be present at the logic analyzer connection. The outputs of the buffers are connected to J5. See Table 3 (10-bit ADCs) and Table 4 (8-bit ADCs) for bit locations of header J5.

Serial Port Enable (SPEN)

The SPEN pin selects the means of programming the internal registers of the MAX19505–MAX19507/ MAX19515–MAX19517 ADCs. SPEN is set high or low based on the settings of jumper JU7, shown in Table 5. When a shunt on JU7 is installed, the 3-wire serial port is disabled and the part can be programmed through jumpers JU1, JU2, and JU3 in parallel mode. When JU7 is left open, SPEN is pulled to GND through R44. Refer to the respective IC data sheet for more information on SPEN and parallel programming. Note that when the serial port is enabled, jumpers JU1, JU2, and JU3 must be set to pins 1-3 for proper operation.

Shutdown (SHDN)

The MAX19505–MAX19507/MAX19515–MAX19517 ADCs can also be placed in a low-power shutdown mode through jumper JU6. This pin has different effects depending on the state of SPEN. When in SPI programming mode, SHDN can select between two power-management states. When in parallel programming mode, SHDN can enable/disable the IC.

When SPI programming is enabled (SPEN = 0), the SHDN pin is a toggle switch between two power-management states, shown in Figure 2 under the **Power Management** group box of the software interface. When a shunt is installed on JU6, SHDN is connected to AVDD and the user can select the appropriate settings for **CHA Active**, **CHB Active**, **Standby**, and **A+B Adder** mode under the label ****Use when SHDN = 1 (IC pin 7)****. When no shunt is installed on JU6, SHDN is connected to GND through R43 and the user can select the appropriate settings for **CHA Active**, **CHB Active**, **Standby**, and **A+B Adder** mode under the label ****Use when SHDN = 0 (IC pin 7)****.

Table 3. Output Bit Locations (MAX19515, MAX19516, MAX19517—10-Bit, Dual ADCs)

SIGNAL	CHANNEL		DESCRIPTION
	A	B	
D0	J5-44	J5-110	Data bit 0 (LSB)
D1	J5-38	J5-106	Data bit 1
D2	J5-36	J5-104	Data bit 2
D3	J5-32	J5-98	Data bit 3
D4	J5-30	J5-96	Data bit 4
D5	J5-26	J5-92	Data bit 5
D6	J5-24	J5-90	Data bit 6
D7	J5-18	J5-86	Data bit 7
D8	J5-16	J5-84	Data bit 8
D9	J5-12	J5-78	Data bit 9
DOR_	J5-10	J5-112	Overrange bit
DCLK_	J5-4	J5-118	Clock bit

Note: See the EV kit schematic for all other nondata connections.

Table 4. Output Bit Locations (MAX19505, MAX19506, MAX19507—8-Bit, Dual ADCs)

SIGNAL	CHANNEL		DESCRIPTION
	A	B	
D0	J5-36	J5-104	Data bit 0 (LSB)
D1	J5-32	J5-98	Data bit 1
D2	J5-30	J5-96	Data bit 2
D3	J5-26	J5-92	Data bit 3
D4	J5-24	J5-90	Data bit 4
D5	J5-18	J5-86	Data bit 5
D6	J5-16	J5-84	Data bit 6
D7	J5-12	J5-78	Data bit 7
DOR_	J5-10	J5-112	Overrange bit
DCLK_	J5-4	J5-118	Clock bit

Note: See the EV kit schematic for all other nondata connections.

Table 5. Jumper JU7 Functions

SHUNT POSITION	SPEN PIN	3-WIRE SERIAL PORT
Installed	Connected to AVDD	Disabled (parallel programming mode)
Not installed*	Connected to GND though a 100kΩ pulldown resistor	Enabled (SPI programming)

*Default position.

When parallel programming mode is enabled ($\overline{SPEN}$ = 1), the SHDN pin enables/disables the IC according to the settings in Table 6.

Parallel Programming

Limited feature selection is available as an alternative to full programmability through the serial port. If the serial port is disabled by setting the $\overline{SPEN}$ pin high, the serial port pins ($\overline{CS}$, SCLK, SDIN) become feature selection pins (OUTSEL, DIV, FORMAT) that require an analog control network.

Jumpers JU1, JU2, JU3, and JU7 control the feature selection when the serial port is disabled (parallel programming is enabled). See Table 7 for functionality.

Table 6. Jumper JU6 Functions ($\overline{SPEN}$ = AVDD)

SHUNT POSITION	SHDN PIN	POWER STATE ($\overline{SPEN}$ = AVDD)
Installed	Connected to AVDD	Complete power-down
Not installed*	Connected to GND through a 100kΩ pulldown resistor	CHA + CHB active

*Default position.

Table 7. Parallel Programming Feature Selection

SCLK/DIV (JU1)	SDIN/FORMAT (JU2)	$\overline{CS}$/OUTSEL (JU3)	$\overline{SPEN}$ (JU7)	DESCRIPTION
SCLK	SDIN	$\overline{CS}$	0	Serial port active. Features are programmed through the serial port.
X	0	X	1	Two's complement
X	VDD	X	1	Offset binary
X	(Unconnected pin)	X	1	Gray code
0	X	X	1	Clock divide-by-1
VDD	X	X	1	Clock divide-by-2
(Unconnected pin)	X	X	1	Clock divide-by-4
X	X	0	1	CMOS (dual bus)
X	X	VDD	1	MUX CMOS (channel A data bus)
X	X	(Unconnected pin)	1	MUX CMOS (channel B data bus)

X = Don't care.

Evaluate: MAX19505–MAX19507/MAX19515–MAX19517
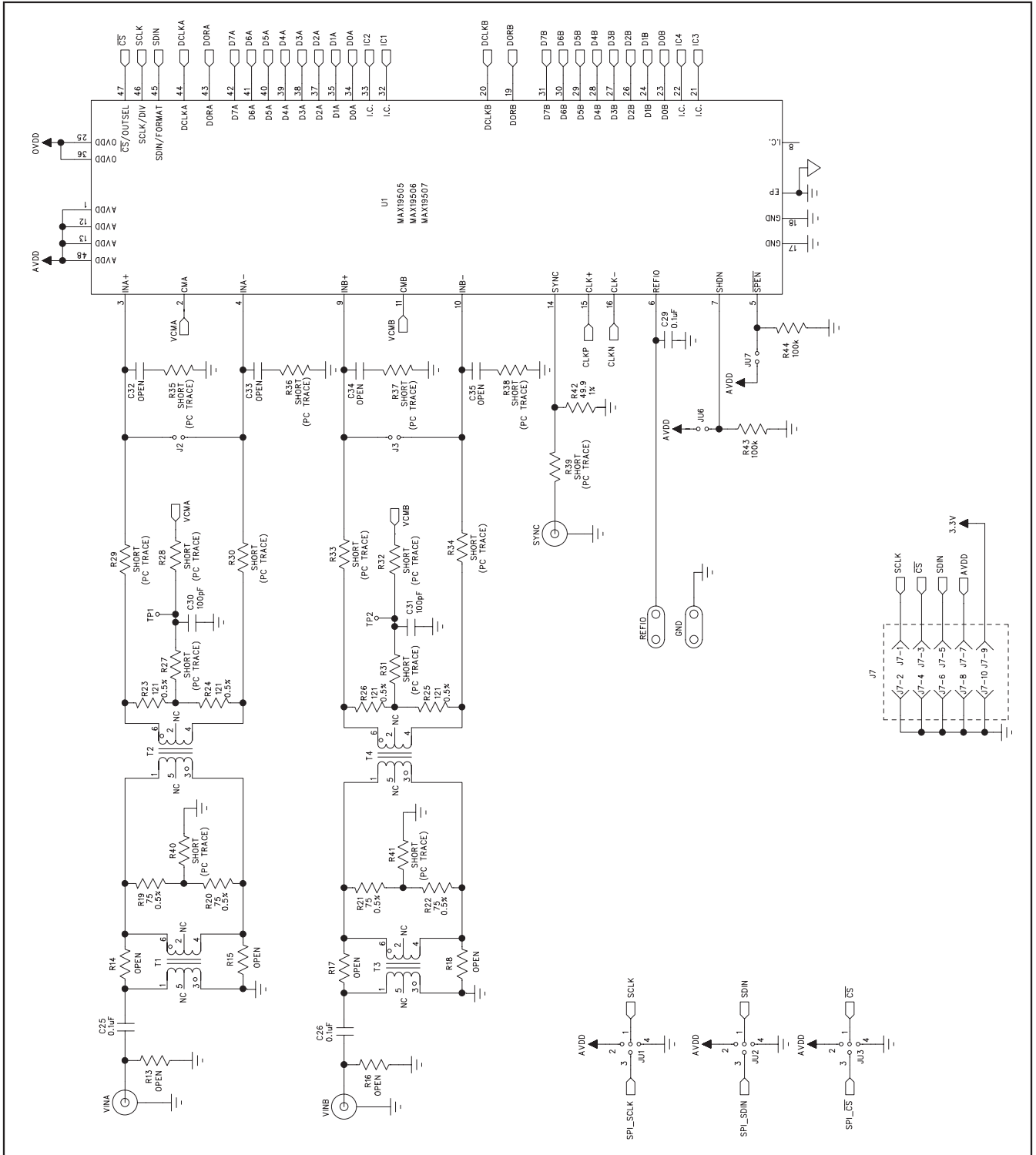
Figure 4a. MAX19505/MAX19506/MAX19507 EV Kits Schematic (Sheet 1 of 2)
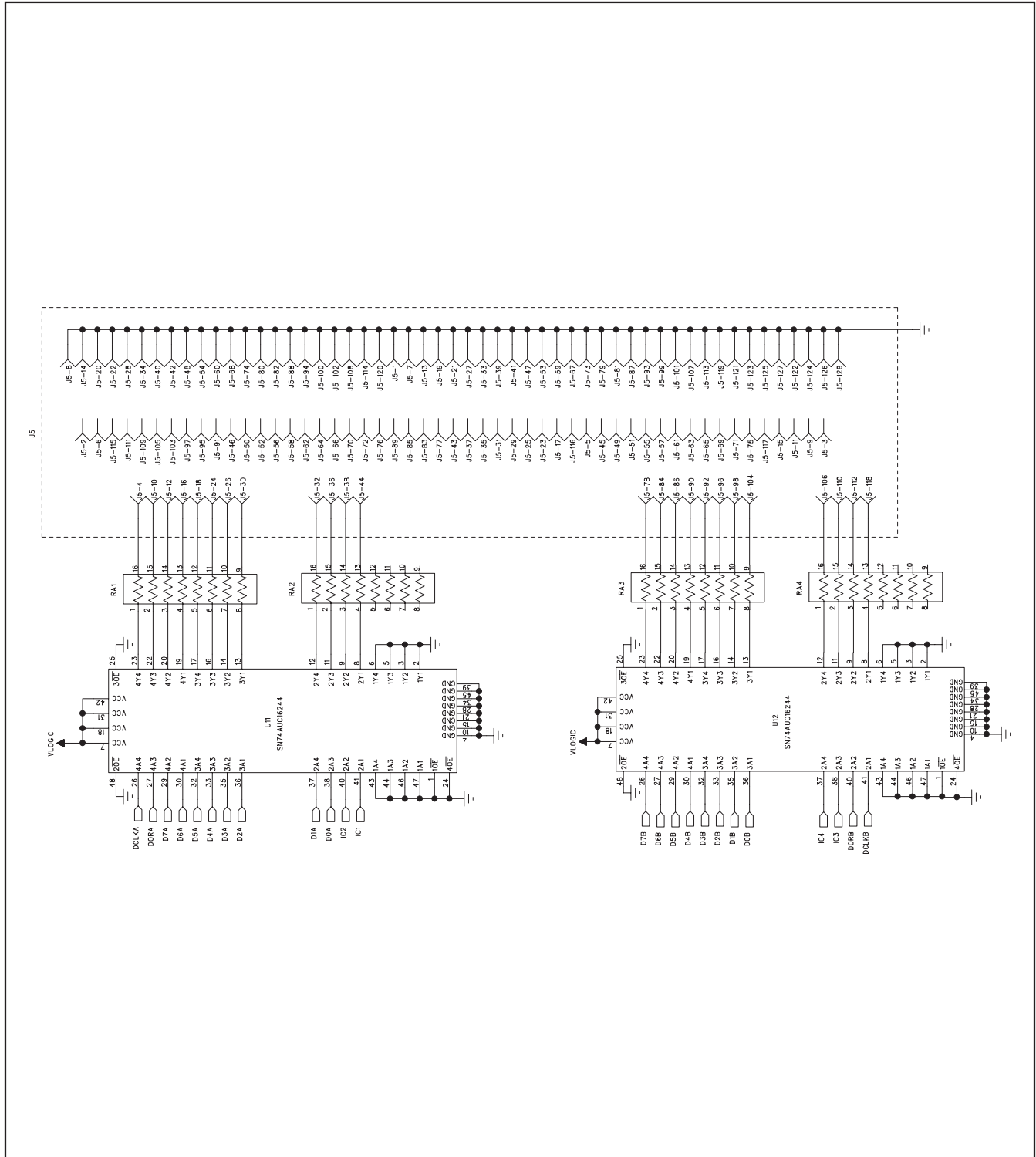
Figure 4b. MAX19505/MAX19506/MAX19507 EV Kits Schematic (Sheet 2 of 2)

/MAXIM
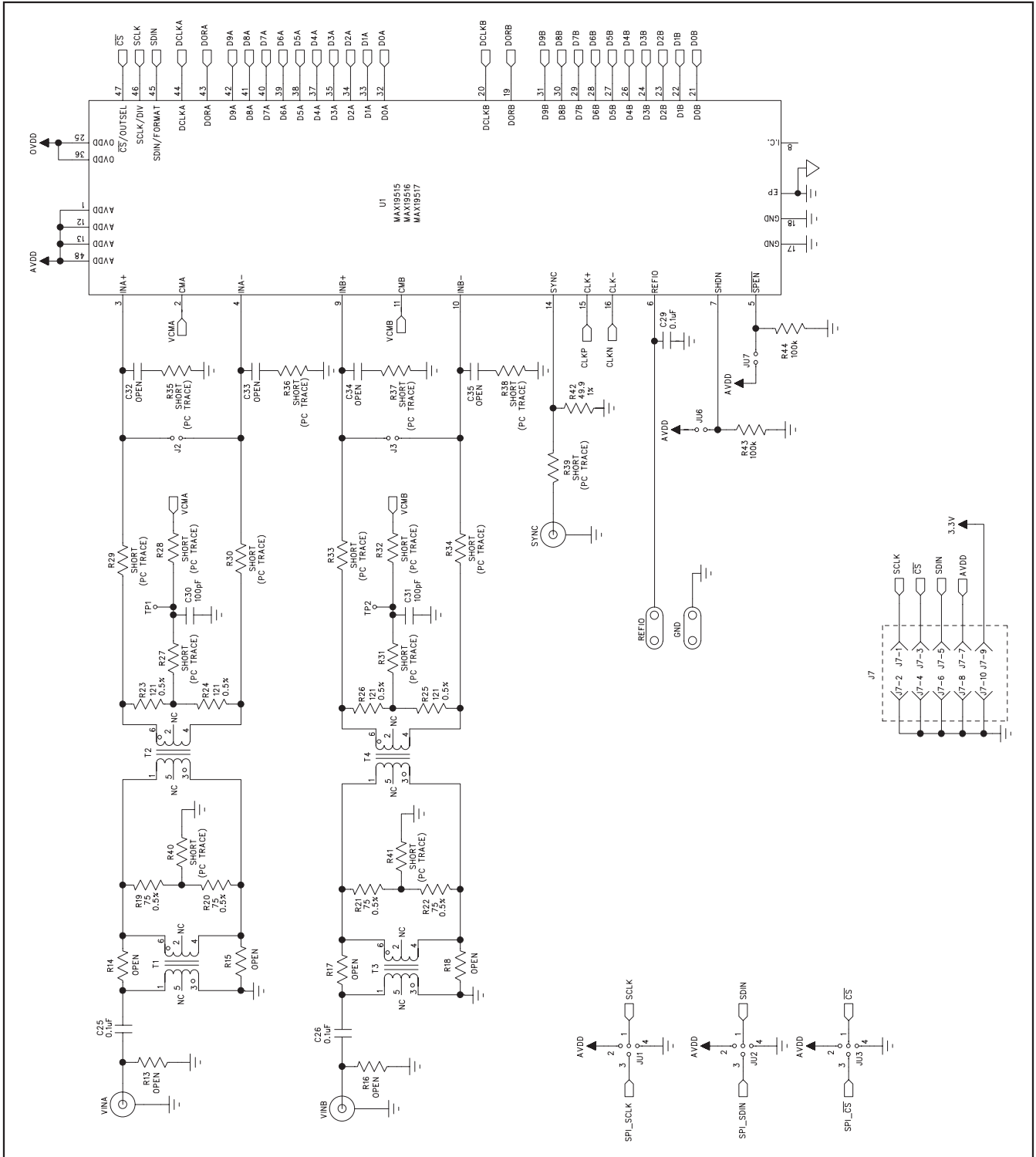
Figure 5a. MAX19515/MAX19516/MAX19517 EV Kits Schematic (Sheet 1 of 2)

_/W/XI/W_
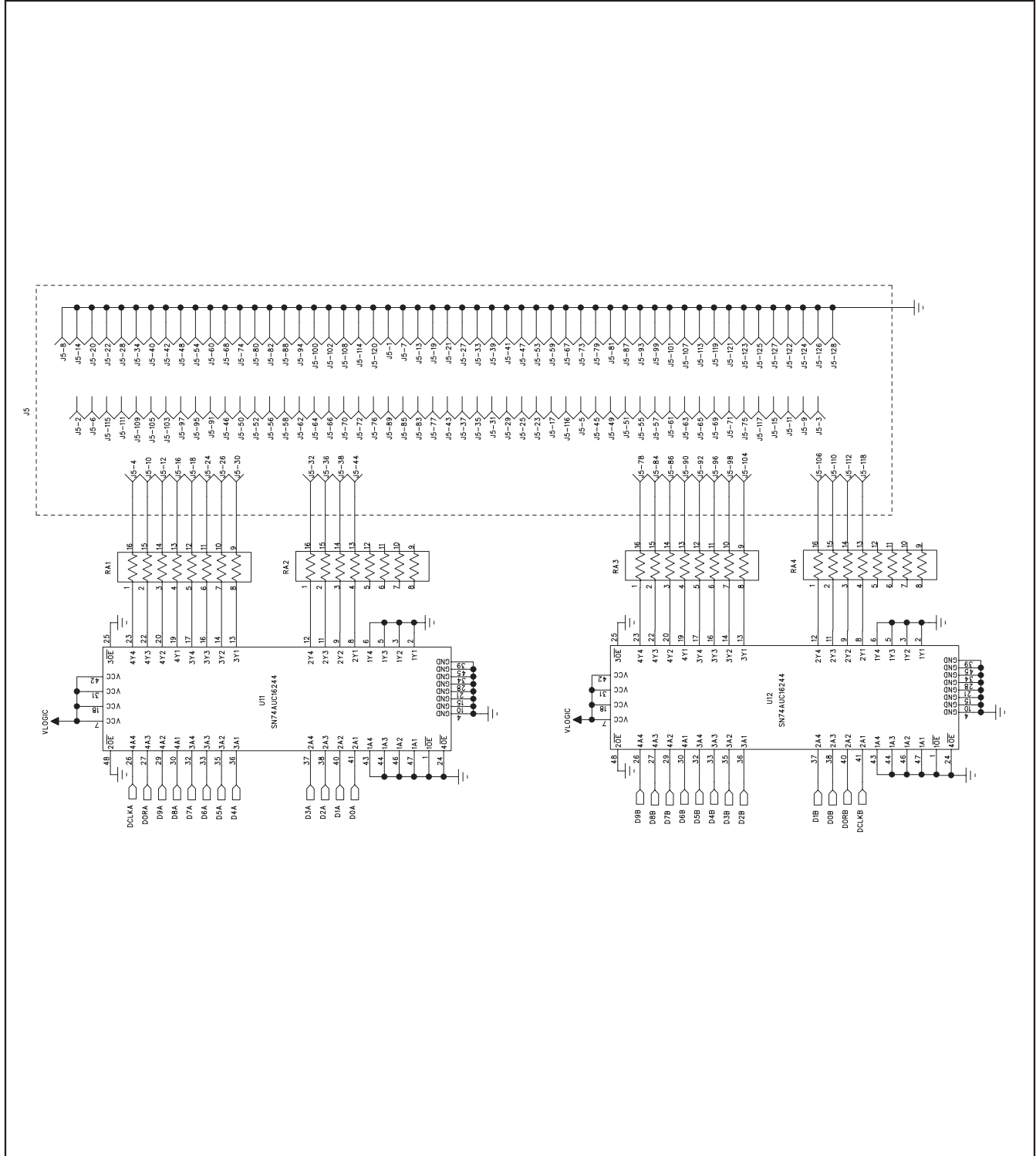
Figure 5b. MAX19515/MAX19516/MAX19517 EV Kits Schematic (Sheet 2 of 2)

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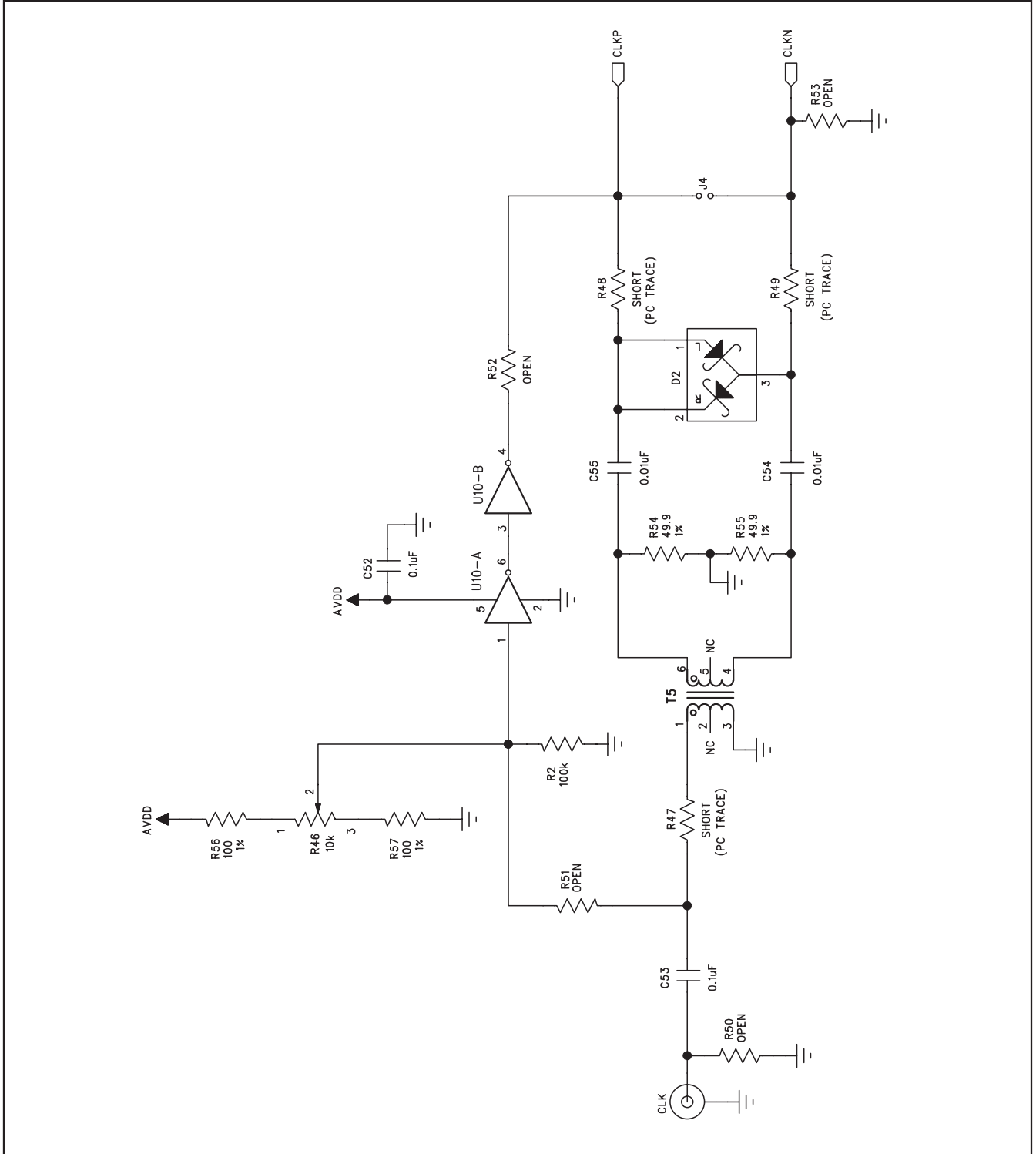
Figure 6a. MAX19505–MAX19507/MAX19515–MAX19517 EV Kits Schematic (Sheet 1 of 3)
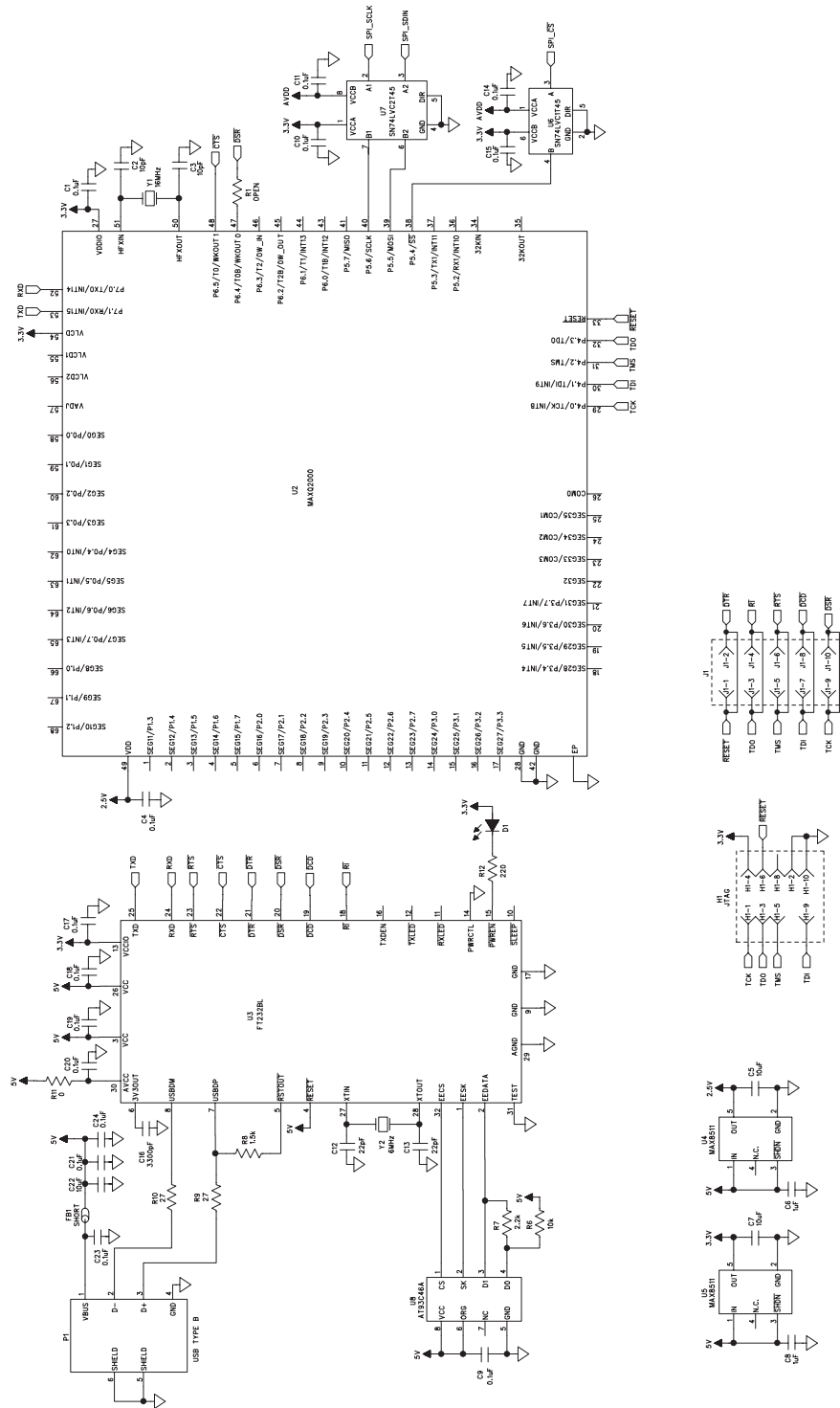
Figure 6b. MAX19505–MAX19507/MAX19515–MAX19517 EV Kits Schematic (Sheet 2 of 3)

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Evaluate: MAX19505–MAX19507/MAX19515–MAX19517
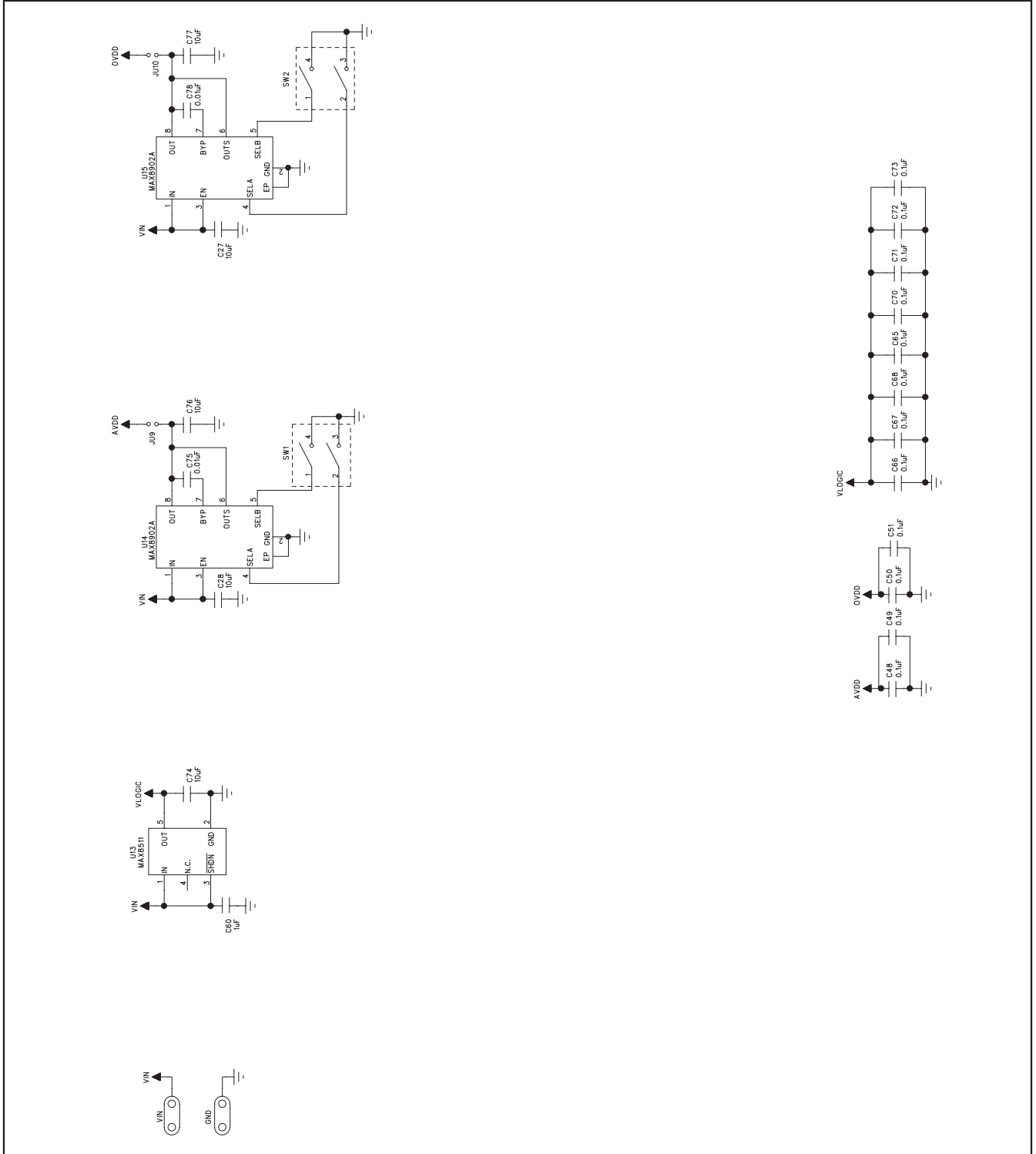
Figure 6c. MAX19505–MAX19507/MAX19515–MAX19517 EV Kits Schematic (Sheet 3 of 3)
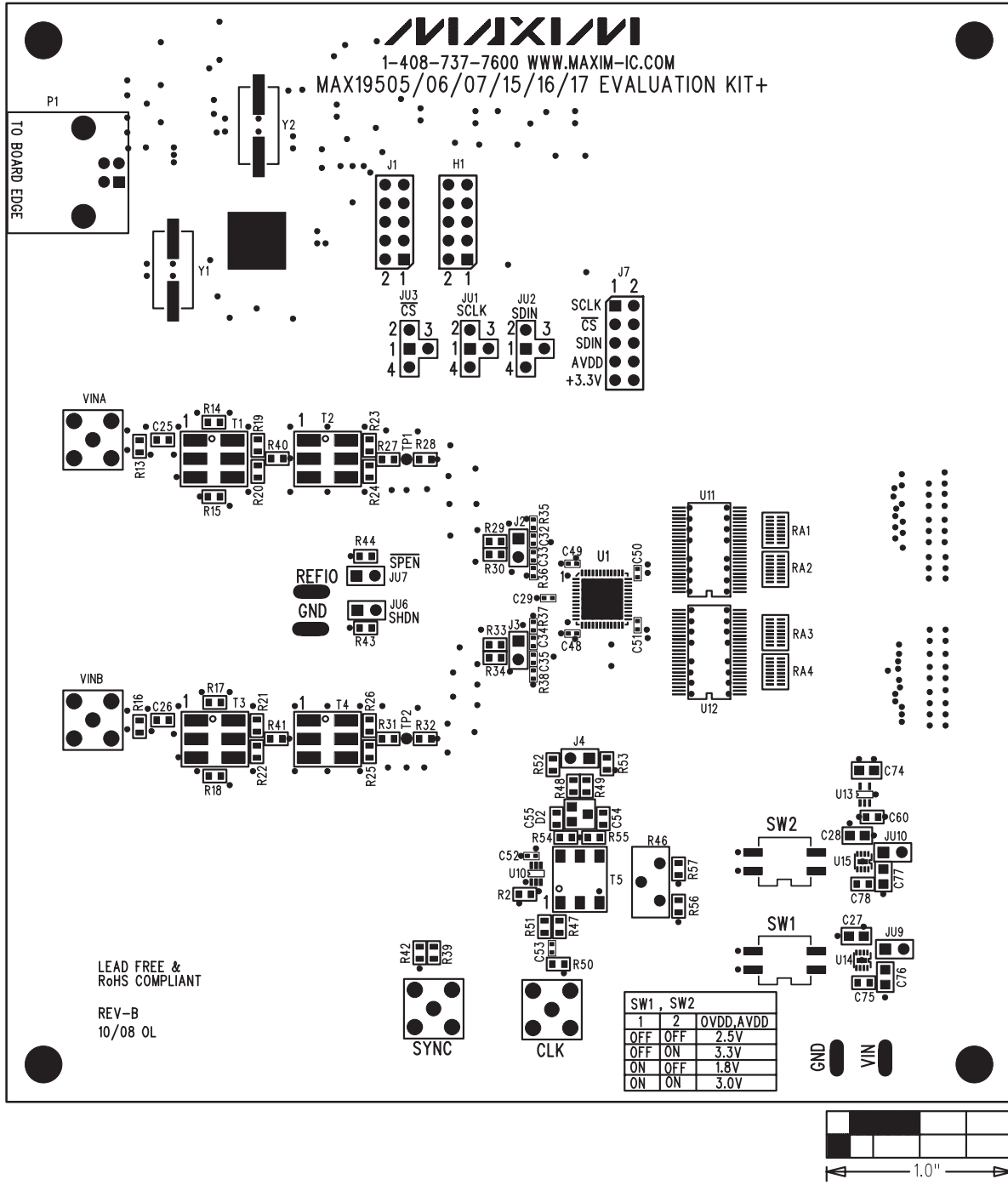
Figure 7. MAX19505–MAX19507/MAX19515–MAX19517 EV Kits Component Placement Guide—Component Side

/VI/XI/VI
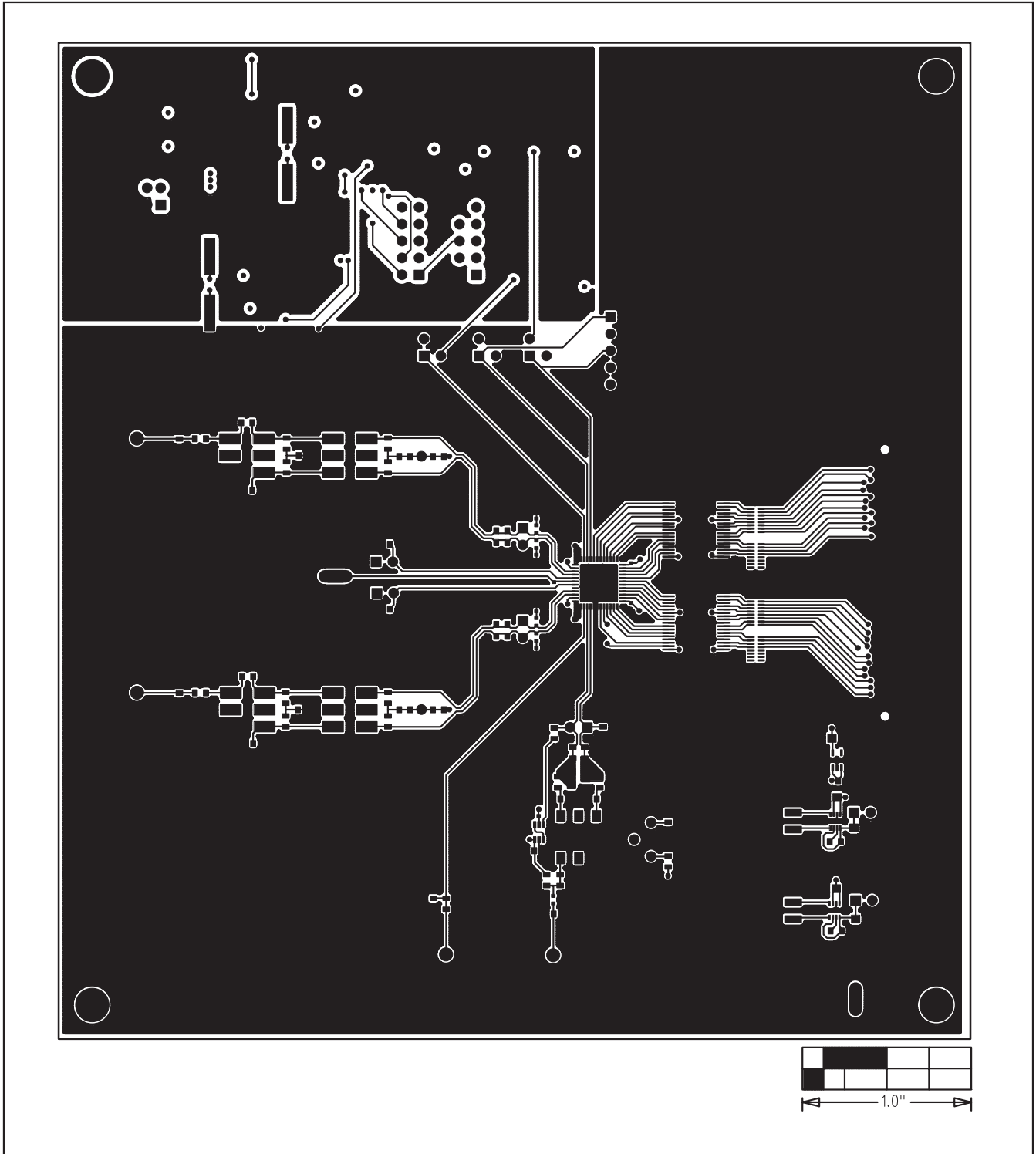
Figure 8. MAX19505–MAX19507/MAX19515–MAX19517 EV Kits PCB Layout—Component Side
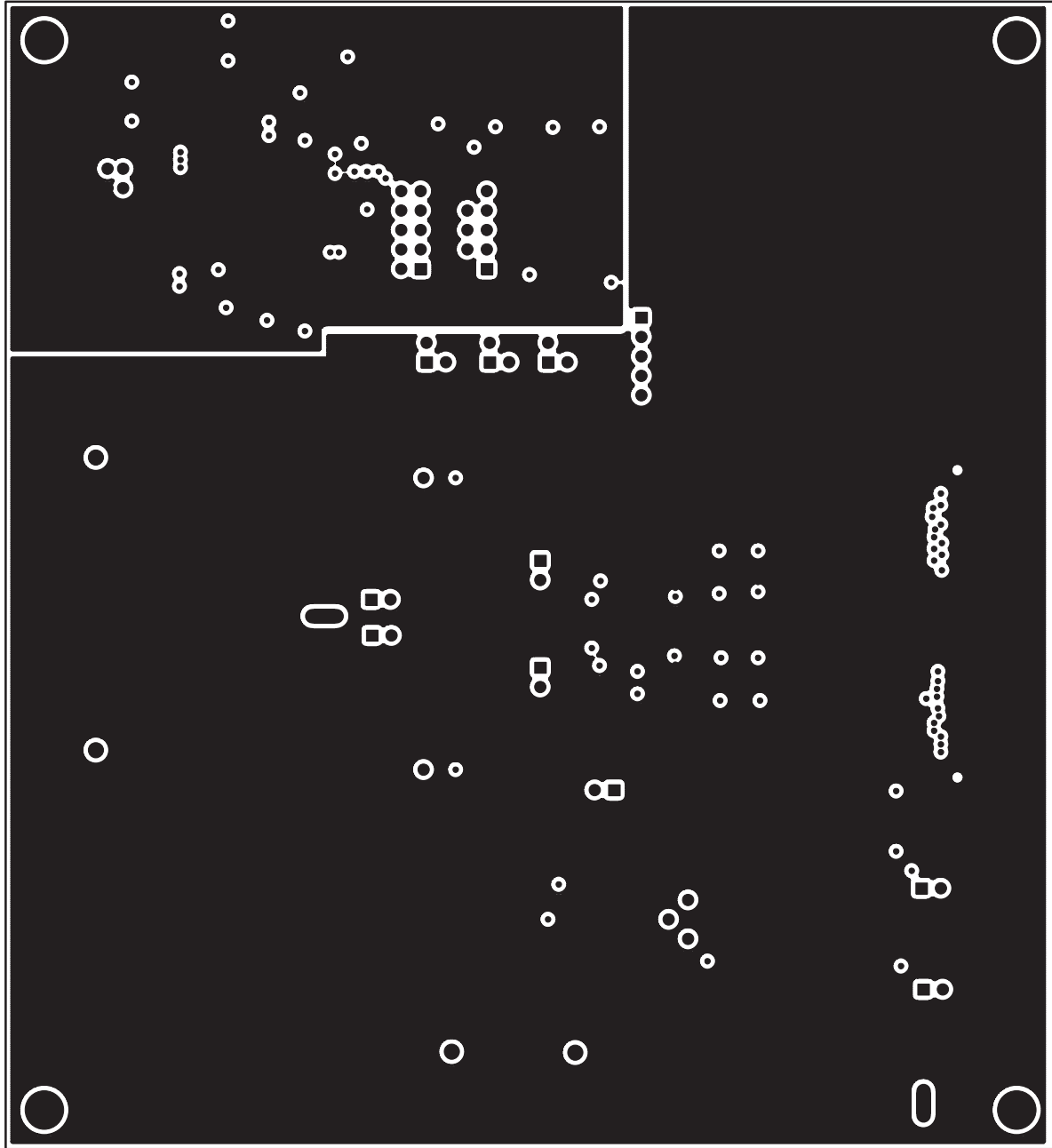
Figure 9. MAX19505–MAX19507/MAX19515–MAX19517 EV Kits PCB Layout (Inner Layer 2)—Ground Planes

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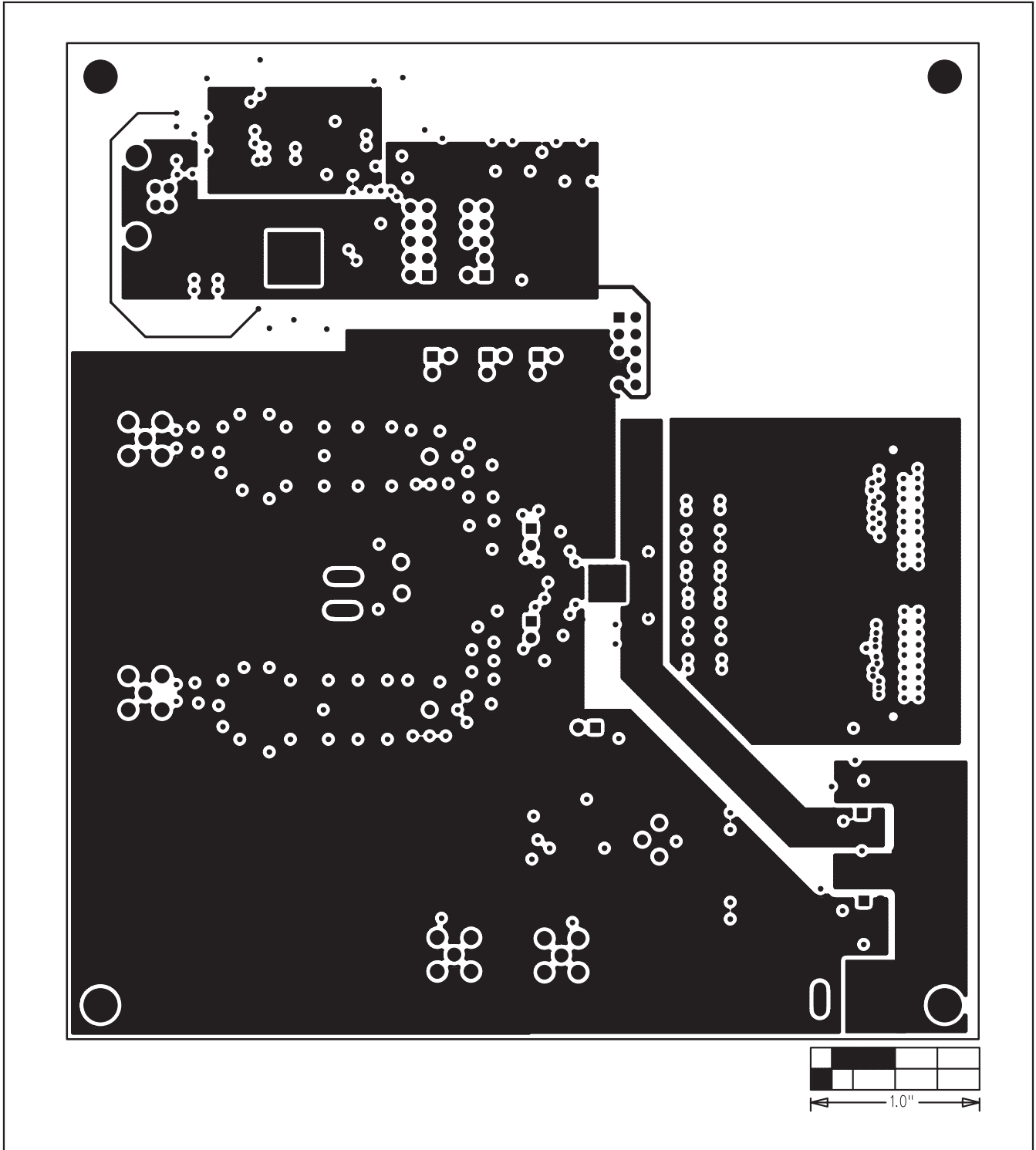
Figure 10. MAX19505–MAX19507/MAX19515–MAX19517 EV Kits PCB Layout (Inner Layer 3)—Power Planes

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1.0"
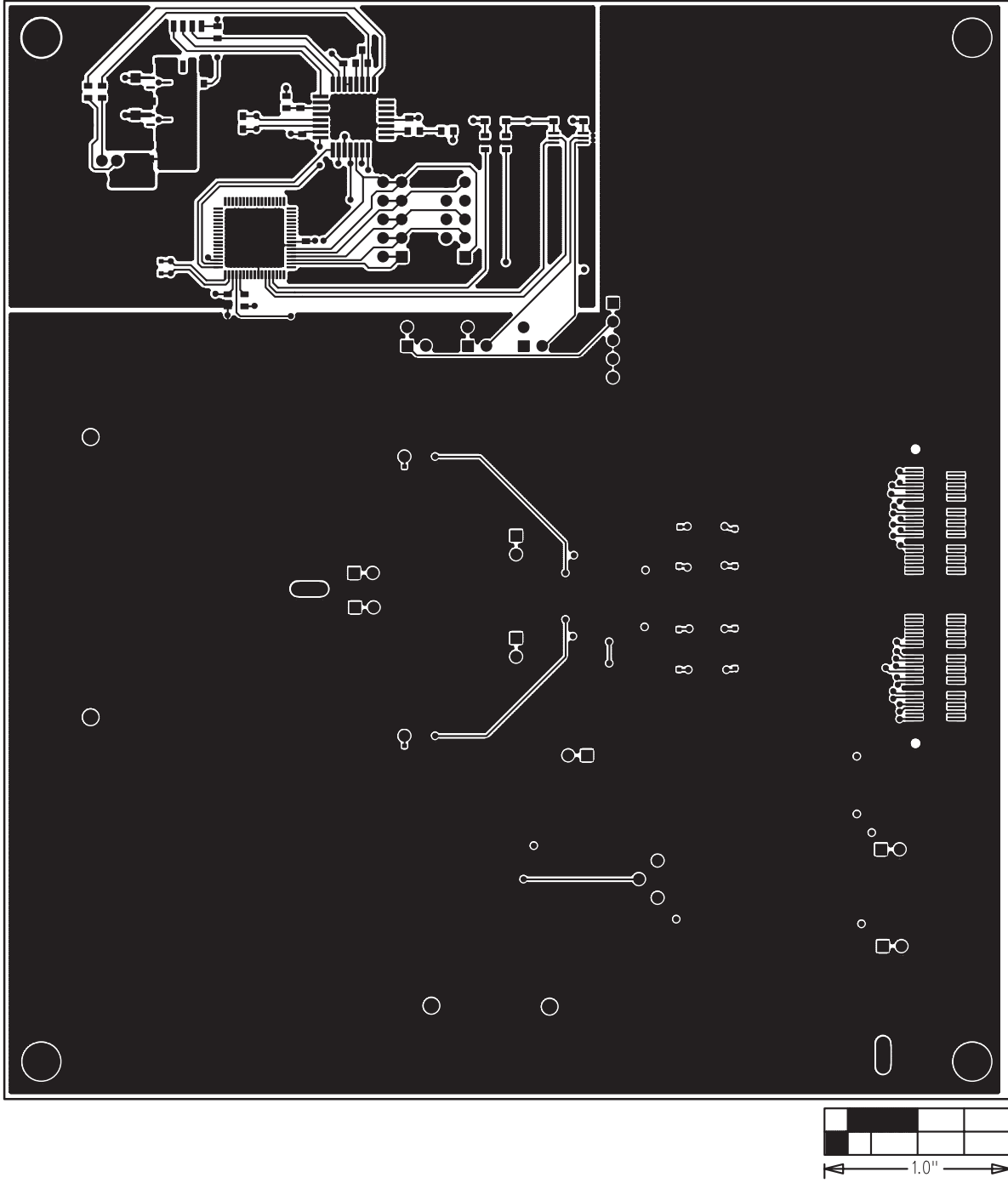
Figure 11. MAX19505–MAX19507/MAX19515–MAX19517 EV Kits PCB Layout—Solder Side

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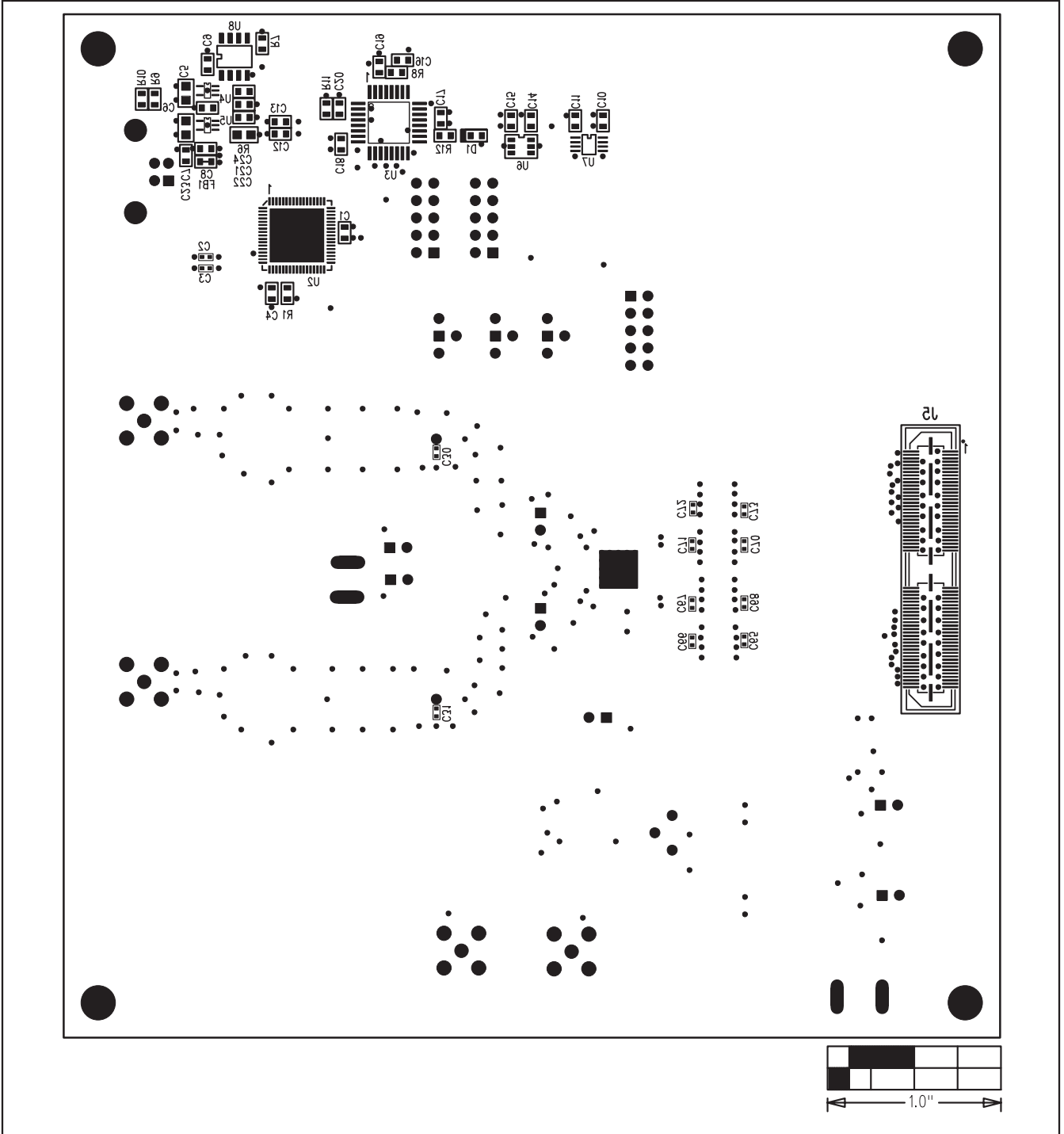
Evaluate: MAX19505–MAX19507/MAX19515–MAX19517

Figure 12. MAX19505–MAX19507/MAX19515–MAX19517 EV Kits PCB Component Placement Guide—Solder Side