Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19-3549; Rev 0; 2/05

EVALUATION KIT AVAILABLE

7.5Msps, Ultra-Low-Power Analog Front-End

MAX19700

General Description

The MAX19700 is an ultra-low-power, mixed-signal analog front-end (AFE) designed for TD-SCDMA handsets and data cards. Optimized for high dynamic performance at ultra-low power, the MAX19700 integrates a dual 10-bit, 7.5Msps receive (Rx) ADC, dual 10-bit, 7.5Msps transmit (Tx) DAC with TD-SCDMA baseband filters, and three fast-settling 12-bit aux-DAC channels for ancillary RF front-end control. The typical operating power in Tx-Rx FAST mode is 36.3mW at a 5.12Msps clock frequency.

The Rx ADCs feature 54.9dB SINAD and 78dBc SFDR at a 1.87MHz input frequency with a 7.5Msps sample frequency. The analog I/Q input amplifiers are fully differential and accept 1.024V_{P-P} full-scale signals. Typical I/Q channel matching is ±0.22° phase and ±0.02dB gain.

The Tx DACs with TD-SCDMA lowpass filters feature -3dB cutoff frequency of 1.27MHz and >55dB stopband rejection at f_{IMAGE} = 4.32MHz. The analog I/Q full-scale output voltage range is selectable at ±410mV or ±500mV. The output common-mode voltage is selectable from 0.9V to 1.4V and the I/Q channel offset is adjustable. The typical I/Q channel matching is ±0.05dB gain and ±0.16° phase.

The Rx ADC and Tx DAC share a single, 10-bit parallel, high-speed digital bus allowing half-duplex operation for time-division duplex (TDD) applications. A 3-wire serial interface controls power-management modes and the aux-DAC channels.

The MAX19700 operates on a single +2.7V to +3.3V analog supply and +1.8V to +3.3V digital I/O supply. The MAX19700 is specified for the extended (-40°C to +85°C) temperature range and is available in a 48-pin, thin QFN package.

Applications

TD-SCDMA Handsets

TD-SCDMA Data Cards

Portable Communication Equipment

Ordering Information

PART*	PIN-PACKAGE	PKG CODE
MAX19700ETM	48 Thin QFN-EP**	T4877-4
MAX19700ETM+	48 Thin QFN-EP**	T4877-4

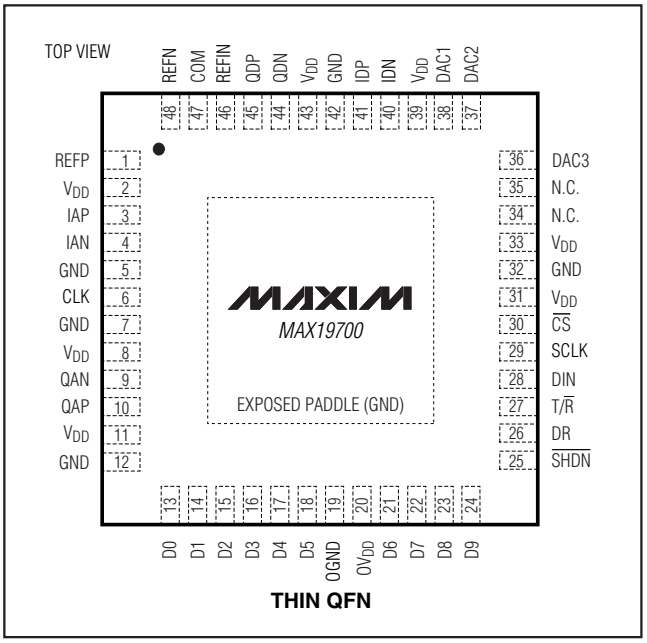
*All devices are specified over the -40°C to +85°C operating range.
**EP = Exposed paddle.
+Denotes lead-free package.

Functional Diagram appears at end of data sheet.

Features

- **Dual 10-Bit Rx ADC and Dual 10-Bit Tx DAC**
- **Ultra-Low Power**
  36.3mW at f_{CLK} = 5.12Msps, Fast Mode
  19.8mW at f_{CLK} = 5.12Msps, Slow Mode
  Low Standby and Shutdown Current
- **Integrated TD-SCDMA Filters with >55dB Stopband Rejection**
- **Excellent Dynamic Performance**
  SINAD = 54.9dB at f_{IN} = 1.87MHz (Rx ADC)
  SFDR = 76.5dBc at f_{OUT} = 620kHz (Tx DAC)
- **Excellent Gain/Phase Match**
  ±0.22° Phase, ±0.02dB Gain (Rx ADC) at f_{IN} = 1.87MHz at -0.5dBFS
- **Three 12-Bit, 1µs Aux-DACs**
- **Single-Supply Operation**
- **Multiplexed Parallel Digital I/O**
- **Serial-Interface Control**
- **Versatile Power-Control Circuits**
  Shutdown, Standby, Idle, Tx-Rx Disable
- **Miniature 48-Pin Thin QFN Package (7mm x 7mm x 0.8mm)**

Pin Configuration



THIN QFN

7.5Msps, Ultra-Low-Power Analog Front-End

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND, OV_{DD} to OGND .....-0.3V to +3.4V
GND to OGND.....-0.3V to +0.3V
IAP, IAN, QAP, QAN, IDP, IDN, QDP, QDN, REFP, REFN, REFIN, COM, DAC1, DAC2, DAC3 to GND .....-0.3V to (V_{DD} + 0.3V)
D0–D9, DR, T/$\overline{R}$, $\overline{SHDN}$, SCLK, DIN, $\overline{CS}$, CLK to OGND .....-0.3V to (OV_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
48-Pin Thin QFN (derate 26.3mW/°C above +70°C) 2.1W
Thermal Resistance θ_{JA} .....38°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		2.7	3.0	3.3	V
Output Supply Voltage	OV_{DD}		1.8		V_{DD}	V
V_{DD} Supply Current		Ext1-Tx, Ext3-Tx, and SPI2-Tx states; transmit DAC operating mode (Tx), f_{CLK} = 5.12MHz, f_{OUT} = 620kHz on both channels; aux-DACs ON and at midscale		10.3		mA
		Ext2-Tx, Ext4-Tx, and SPI4-Tx states; transmit DAC operating mode (Tx), f_{CLK} = 5.12MHz, f_{OUT} = 620kHz on both channels; aux-DACs ON and at midscale		12.4		
		Ext1-Rx, Ext4-Rx, and SPI3-Rx states; receive ADC operating mode (Rx), f_{CLK} = 5.12MHz, f_{IN} = 1.87MHz on both channels; aux-DACs ON and at midscale		12.1		
		Ext2-Rx, Ext3-Rx, and SPI1-Rx modes; receive ADC operating mode (Rx), f_{CLK} = 5.12MHz, f_{IN} = 1.87MHz on both channels; aux-DACs ON and at midscale		6.6		
		Ext2-Tx, Ext4-Tx, and SPI4-Tx modes; transmit DAC operating mode (Tx), f_{CLK} = 7.5MHz, f_{OUT} = 620kHz on both channels; aux-DACs ON and at midscale		13.1	16	
		Ext1-Tx, Ext3-Tx, and SPI2-Tx modes; transmit DAC operating mode (Tx), f_{CLK} = 7.5MHz, f_{OUT} = 620kHz on both channels; aux-DACs ON and at midscale		10.4		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Supply Current		Ext1-Rx, Ext4-Rx, and SPI3-Rx modes; receive ADC operating mode (Rx), f_{CLK} = 7.5MHz, f_{IN} = 1.87MHz on both channels; aux-DACs ON and at midscale		12.8	16	mA
		Ext2-Rx, Ext3-Rx, and SPI1-Rx modes; receive ADC operating mode (Rx), f_{CLK} = 7.5MHz, f_{IN} = 1.87MHz on both channels; aux-DACs ON and at midscale		7		
		Standby mode, CLK = 0 or OV_{DD}; aux-DACs ON and at midscale		2.7	4	
		Idle mode, f_{CLK} = 7.5MHz; aux-DACs ON and at midscale		4.7	6	
		Shutdown mode, CLK = 0 or OV_{DD}		0.7		µA
OV_{DD} Supply Current		Ext1-Rx, Ext2-Rx, Ext3-Rx, Ext4-Rx, SPI1-Rx, SPI3-Rx modes; receive ADC operating mode (Rx), f_{CLK} = 7.5MHz, f_{IN} = 1.87MHz on both channels; aux-DACs ON and at midscale		1.38		mA
		Ext1-Tx, Ext2-Tx, Ext3-Tx, Ext4-Tx, SPI2-Tx, SPI4-Tx modes; transmit DAC operating mode (Tx), f_{CLK} = 7.5MHz, f_{OUT} = 620kHz; aux-DACs ON and at midscale		72.9		µA
		Idle mode, f_{CLK} = 7.5MHz; aux-DACs ON and at midscale		10.9		
		Shutdown mode, CLK = 0 or OV_{DD}		0.01		
		Standby mode, CLK = 0 or OV_{DD}; aux-DACs ON and at midscale		0.03		
Rx ADC DC ACCURACY						
Resolution			10			Bits
Integral Nonlinearity	INL			±0.85		LSB
Differential Nonlinearity	DNL			±0.55		LSB
Offset Error		Residual DC offset error		±0.5	±5	%FS
Gain Error		Include reference error		±1.1	±5	%FS
DC Gain Matching				±0.01	±0.25	dB
Offset Matching				±4.5		LSB
Gain Temperature Coefficient				±15.7		ppm/°C
Power-Supply Rejection	PSRR	Offset error (V_{DD} ±5%)		±0.2		LSB
		Gain error (V_{DD} ±5%)		±0.04		%FS

7.5Msps, Ultra-Low-Power Analog Front-End

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, $C_{REFP} = C_{REFN} = C_{COM}$ = 0.33µF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rx ADC ANALOG INPUT						
Input Differential Range	V_{ID}	Differential or single-ended inputs		±0.512		V
Input Common-Mode Voltage Range	V_{CM}			V_{DD} / 2		V
Input Impedance	R_{IN}	Switched capacitor load		720		kΩ
	C_{IN}			5		pF
Rx ADC CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}	(Note 2)			7.5	MHz
Data Latency (Figure 3)		Channel I		5		Clock Cycles
		Channel Q		5.5		
Rx ADC DYNAMIC CHARACTERISTICS (Note 3)						
Signal-to-Noise Ratio	SNR	f_{IN} = 1.875MHz, f_{CLK} = 7.5MHz	53.7	55		dB
		f_{IN} = 3.5MHz, f_{CLK} = 7.5MHz		54.8		
Signal-to-Noise Plus Distortion	SINAD	f_{IN} = 1.875MHz, f_{CLK} = 7.5MHz	53.6	54.9		dB
		f_{IN} = 3.5MHz, f_{CLK} = 7.5MHz		54.7		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 1.875MHz, f_{CLK} = 7.5MHz	66	78		dBc
		f_{IN} = 3.5MHz, f_{CLK} = 7.5MHz		70.1		
Third-Harmonic Distortion	HD3	f_{IN} = 1.875MHz, f_{CLK} = 7.5MHz		-84		dBc
		f_{IN} = 3.5MHz, f_{CLK} = 7.5MHz		-72.1		
Intermodulation Distortion	IMD	f_1 = 1.8MHz, -7dBFS; f_2 = 1MHz, -7dBFS		-75.6		dBc
Third-Order Intermodulation Distortion	IM3	f_1 = 1.8MHz, -7dBFS; f_2 = 1MHz, -7dBFS		-78		dBc
Total Harmonic Distortion	THD	f_{IN} = 1.875MHz, f_{CLK} = 7.5MHz		-77.9	-64	dBc
		f_{IN} = 3.5MHz, f_{CLK} = 7.5MHz		-71		
Aperture Delay				3.5		ns
Overdrive Recovery Time		1.5x full-scale input		2		ns
Rx ADC INTERCHANNEL CHARACTERISTICS						
Crosstalk Rejection		$f_{INX,Y}$ = 1.875MHz at -0.5dBFS, $f_{INX,Y}$ = 1MHz at -0.5dBFS (Note 4)		-85		dB
Amplitude Matching		f_{IN} = 1.875MHz at -0.5dBFS (Note 5)		±0.02		dB
Phase Matching		f_{IN} = 1.875MHz at -0.5dBFS (Note 5)		±0.22		Degrees

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Tx DAC DC ACCURACY							
Resolution	N			10			Bits
Integral Nonlinearity	INL				±0.45		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 6)			±0.26		LSB
Residual DC Offset	V_{OS}	T_A > +25°C		-4	±1	+4	mV
		T_A < +25°C		-6.5	±1	+6.5	
Full-Scale Gain Error		Include reference error (peak-to-peak error)		-50		+50	mV
TRANSMIT-PATH DYNAMIC PERFORMANCE							
Corner Frequency		3dB corner		1.1	1.27	1.5	MHz
Passband Ripple		DC to 640kHz (Note 6)			0.28	0.5	dB_{P-P}
Group Delay Variation in Passband		DC to 640kHz, guaranteed by design			50	100	ns
Error-Vector Magnitude	EVM	DC to 700kHz			2		%
Stopband Rejection		f_{IMAGE} = 4.32MHz, f_{OUT} = 800kHz, f_{CLK} = 5.12MHz		55			dBc
Baseband Attenuation		Spot relative to 100kHz	2MHz		20		dB
			4MHz		46.5		
			5MHz		54.7		
			10MHz		81		
			20MHz		88		
DAC Conversion Rate	f_{CLK}	(Note 2)				7.5	MHz
In-Band Noise Density	N_D	f_{OUT} = 620kHz, f_{CLK} = 5.12MHz, offset = 500kHz			-121.7		dBc/Hz
Third-Order Intermodulation Distortion	IM3	f_1 = 620kHz, f_2 = 640kHz			76		dBc
Glitch Impulse					10		pV•s
Spurious-Free Dynamic Range to Nyquist	SFDR	f_{CLK} = 7.5MHz, f_{OUT} = 620kHz		60	76.5		dBc
Total Harmonic Distortion to Nyquist	THD	f_{CLK} = 7.5MHz, f_{OUT} = 620kHz			-74.8	-59	dB
Signal-to-Noise Ratio to Nyquist	SNR	f_{CLK} = 7.5MHz, f_{OUT} = 620kHz			57.1		dB

7.5Msps, Ultra-Low-Power Analog Front-End

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TRANSMIT-PATH INTERCHANNEL CHARACTERISTICS						
I-to-Q Output Isolation		$f_{OUTx,Y}$ = 500kHz, $f_{OUTx,Y}$ = 620kHz		85		dB
Gain Mismatch Between DAC Outputs		Measured at DC	-0.3	±0.05	+0.3	dB
Phase Mismatch Between DAC Outputs		f_{OUT} = 620kHz, f_{CLK} = 7.5MHz		±0.16		Degrees
Differential Output Impedance				800		Ω
TRANSMIT-PATH ANALOG OUTPUT						
Full-Scale Output Voltage (Table 6)	V_{FS}	Bit E7 = 0 (default)		±410		mV
		Bit E7 = 1		±500		
Output Common-Mode Voltage (Table 8)		Bits CM1 = 0, CM0 = 0 (default)	1.32	1.4	1.48	V
		Bits CM1 = 0, CM0 = 1		1.25		
		Bits CM1 = 1, CM0 = 0		1.1		
		Bits CM1 = 1, CM0 = 1		0.9		
RECEIVE TRANSMIT-PATH INTERCHANNEL CHARACTERISTICS						
Receive Transmit Isolation		ADC f_{INI} = f_{INQ} = 1.875MHz, DAC f_{OUTI} = f_{OUTQ} = 620kHz, f_{CLK} = 7.5MHz		85		dB
AUXILIARY DACs (DAC1, DAC2, DAC3)						
Resolution		(Note 6)	12			Bits
Integral Nonlinearity	INL			±1.25		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic over codes 100 to 4000 (Note 6)		±0.65		LSB
Gain Error	GE	R_L > 200kΩ		±0.7		%FS
Zero-Code Error				±0.6		%FS
Output-Voltage Low	V_{OL}	R_L > 200kΩ			0.1	V
Output-Voltage High	V_{OH}	R_L > 200kΩ	2.56			V
DC Output Impedance		DC output at midscale		4		Ω
Settling Time		From 1/4 FS to 3/4 FS		1		µs
Glitch Impulse		From 0 to FS transition		24		nV•s
Rx ADC-Tx DAC TIMING CHARACTERISTICS						
CLK Rise to Channel-I Output Data Valid	t_{DOI}	Figure 3 (Note 6)		6.9	10	ns
CLK Fall to Channel-Q Output Data Valid	t_{DOQ}	Figure 3 (Note 6)		9.3	13	ns
CLK Rise/Fall to DR Rise/Fall Time	t_{DR}	Figure 3 (Note 6)		8.5	12	ns
I-DAC DATA to CLK Fall Setup Time	t_{DSI}	Figure 5 (Note 6)	10			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, $C_{REFP} = C_{REFN} = C_{COM}$ = 0.33µF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Q-DAC DATA to CLK Rise Setup Time	t_{DSQ}	Figure 5 (Note 6)	10			ns
CLK Fall to I-DAC Data Hold Time	t_{DHI}	Figure 5 (Note 6)	0			ns
CLK Rise to Q-DAC Data Hold Time	t_{DHQ}	Figure 5 (Note 6)	0			ns
CLK Duty Cycle				50		%
CLK Duty-Cycle Variation				±15		%
Digital Output Rise/Fall Time		20% to 80%		2.3		ns
SERIAL-INTERFACE TIMING CHARACTERISTICS (Figure 6, Note 6)						
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}		10			ns
DIN to SCLK Setup Time	t_{DS}		10			ns
DIN to SCLK Hold Time	t_{DH}		0			ns
SCLK Pulse-Width High	t_{CH}		25			ns
SCLK Pulse-Width Low	t_{CL}		25			ns
SCLK Period	t_{CP}		50			ns
SCLK to $\overline{CS}$ Setup Time	t_{CS}		10			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		80			ns
MODE-RECOVERY TIMING CHARACTERISTICS (Figure 7)						
Shutdown Wake-Up Time	$t_{WAKE,SD}$	From shutdown to Rx mode, ADC settles to within 1dB SINAD		75		µs
		From shutdown to Tx mode, DAC settles to within 10 LSB error		25		
Idle Wake-Up Time (With CLK)	$t_{WAKE,ST0}$	From idle to Rx mode with CLK present during idle, ADC settles to within 1dB SINAD		7.3		µs
		From idle to Tx mode with CLK present during idle, DAC settles to 10 LSB error		5		
Standby Wake-Up Time	$t_{WAKE,ST1}$	From standby to Rx mode, ADC settles to within 1dB SINAD		7.3		µs
		From standby to Tx mode, DAC settles to 10 LSB error		25		
Enable Time from Tx to Rx, (Ext2-Tx to Ext2-Rx, Ext4-Tx to Ext4-Rx, and SPI4-Tx to SPI3-Rx Modes)	$t_{ENABLE, RX}$	ADC settles to within 1dB SINAD		500		ns
Enable Time from Rx to Tx, (Ext1-Rx to Ext1-Tx, Ext4-Rx to Ext4-Tx, and SPI3-Rx to SPI4-Tx Modes)	$t_{ENABLE, TX}$	DAC settles to within 10 LSB error		1		µs

7.5Msps, Ultra-Low-Power Analog Front-End

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Enable Time from Tx to Rx, (Ext1-Tx to Ext1-Rx, Ext3-Tx to Ext3-Rx, and SPI2-Tx to SPI1-Rx Modes)	$t_{ENABLE, RX}$	ADC settles to within 1dB SINAD		7.3		µs
Enable Time from Rx to Tx, (Ext2-Rx to Ext2-Tx, Ext3-Rx to Ext3-Tx, and SPI1-Rx to SPI2-Tx Modes)	$t_{ENABLE,TX}$	DAC settles to within 10 LSB error		5		µs
INTERNAL REFERENCE (REFIN = V_{DD}; V_{REFP}, V_{REFN}, V_{COM} levels are generated internally)						
Positive Reference		V_{REFP} - V_{COM}		0.256		V
Negative Reference		V_{REFN} - V_{COM}		-0.256		V
Common-Mode Output Voltage	V_{COM}		V_{DD} / 2 - 0.15	V_{DD} / 2	V_{DD} / 2 + 0.15	V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
Differential Reference Output	V_{REF}	V_{REFP} - V_{REFN}	+0.490	+0.512	+0.534	V
Differential Reference Temperature Coefficient	REFTC			±10		ppm/°C
BUFFERED EXTERNAL REFERENCE (external REFIN = 1.024V applied; V_{REFP}, V_{REFN}, V_{COM} levels are generated internally)						
Reference Input Voltage	V_{REFIN}			1.024		V
Differential Reference Output	V_{DIFF}	V_{REFP} - V_{REFN}		0.512		V
Common-Mode Output Voltage	V_{COM}			V_{DD} / 2		V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
REFIN Input Current				-0.7		µA
REFIN Input Resistance				500		kΩ
DIGITAL INPUTS (CLK, SCLK, DIN, $\overline{CS}$, D0–D9, T/$\overline{R}$, $\overline{SHDN}$)						
Input High Threshold	V_{INH}	D0–D9, CLK, SCLK, DIN, $\overline{CS}$, T/$\overline{R}$, $\overline{SHDN}$	0.7 x OV_{DD}			V
Input Low Threshold	V_{INL}	D0–D9, CLK, SCLK, DIN, $\overline{CS}$, T/$\overline{R}$, $\overline{SHDN}$			0.3 x OV_{DD}	V
Input Leakage	DI_{IN}	D0–D9, CLK, SCLK, DIN, $\overline{CS}$, T/$\overline{R}$, $\overline{SHDN}$ = OGND or OV_{DD}	-1		+1	µA
Input Capacitance	DC_{IN}			5		pF

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF. Typical values are at T_A = +25°C, unless otherwise noted. C_L < 5pF on all aux-DAC outputs.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL OUTPUTS (D0–D9, DR)						
Output-Voltage Low	V_{OL}	I_{SINK} = 200µA			0.2 x OV_{DD}	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 200µA	0.8 x OV_{DD}			V
Tri-State Leakage Current	I_{LEAK}		-1		+1	µA
Tri-State Output Capacitance	C_{OUT}			5		pF

Note 1: Specifications from T_A = +25°C to +85°C are guaranteed by production tests. Specifications from T_A = +25°C to -40°C are guaranteed by design and characterization.

Note 2: The minimum clock frequency for the MAX19700 is 2MHz.

Note 3: SNR, SINAD, SFDR, HD3, and THD are based on a differential analog input voltage of -0.5dBFS referenced to the amplitude of the digital outputs. SINAD and THD are calculated using HD2 through HD6.

Note 4: Crosstalk rejection is measured by applying a high-frequency test tone to one channel and a low-frequency tone to the second channel. FFTs are performed on each channel. The parameter is specified as the power ratio of the first and second channel FFT test tone.

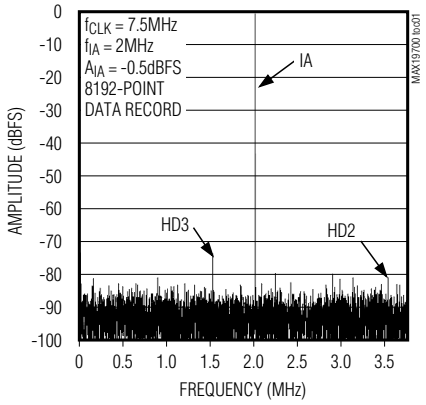
Note 5: Amplitude and phase matching is measured by applying the same signal to each channel, and comparing the two output signals using a sine-wave fit.

Note 6: Guaranteed by design and characterization.

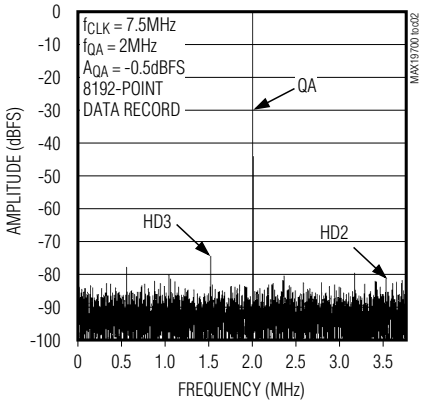
Typical Operating Characteristics

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

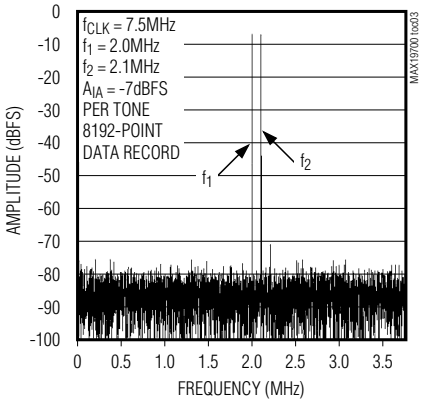
Rx ADC CHANNEL-IA FFT PLOT



Rx ADC CHANNEL-QA FFT PLOT



Rx ADC CHANNEL-IA TWO-TONE FFT PLOT

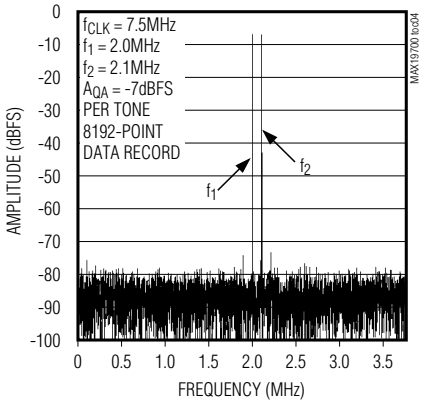


7.5Msps, Ultra-Low-Power Analog Front-End

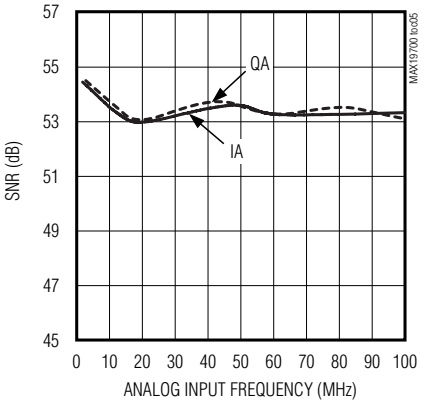
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

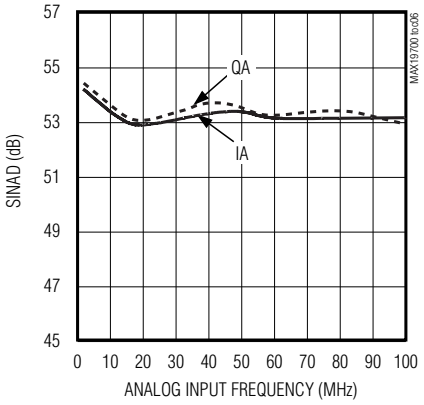
Rx ADC CHANNEL-QA TWO-TONE FFT PLOT



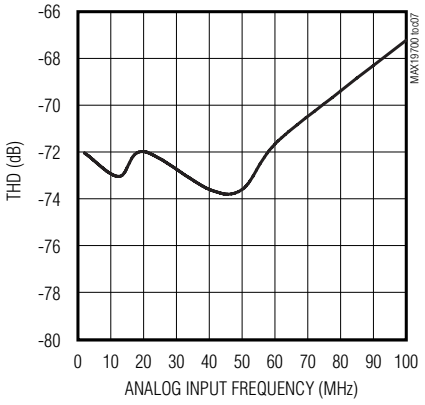
Rx ADC SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY



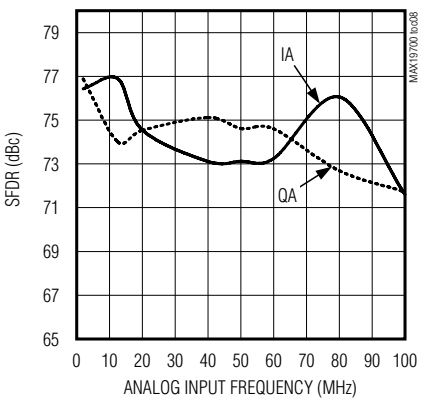
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. ANALOG INPUT FREQUENCY



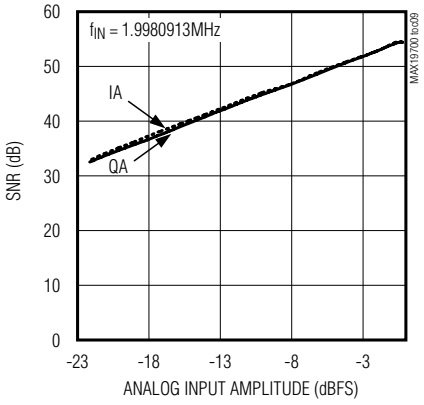
Rx ADC TOTAL HARMONIC DISTORTION vs. ANALOG INPUT FREQUENCY



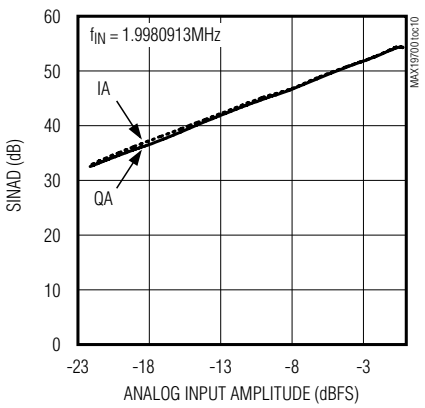
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY



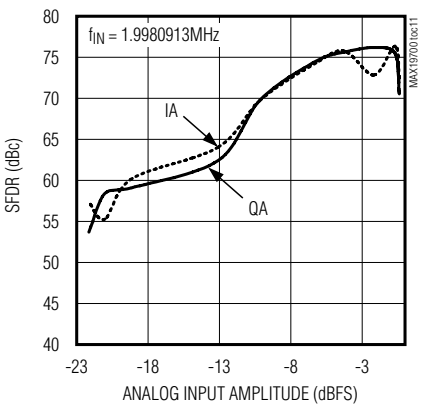
Rx ADC SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT AMPLITUDE



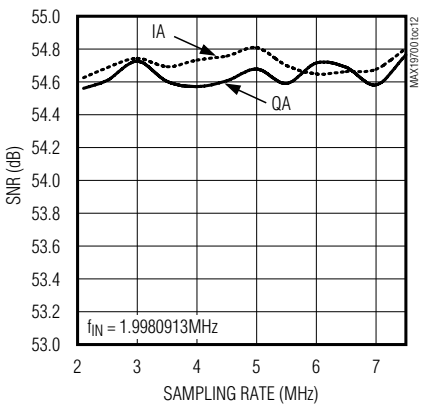
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. ANALOG INPUT AMPLITUDE



Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT AMPLITUDE



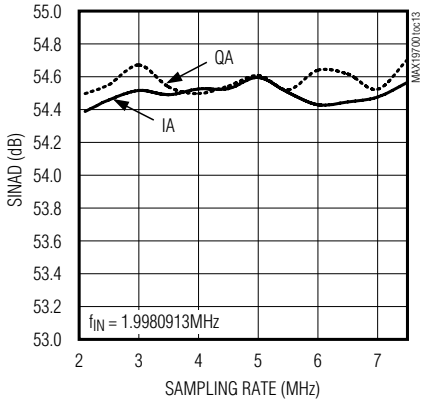
Rx ADC SIGNAL-TO-NOISE RATIO vs. SAMPLING RATE



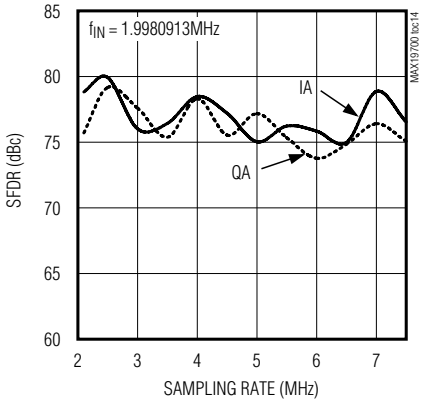
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

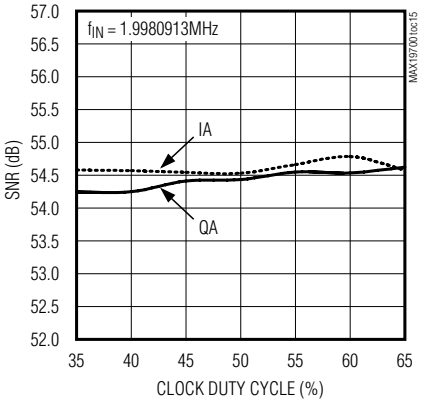
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. SAMPLING RATE



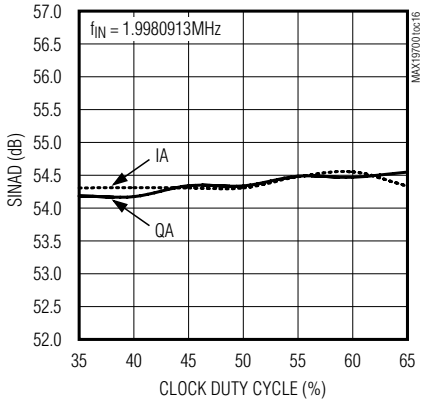
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE



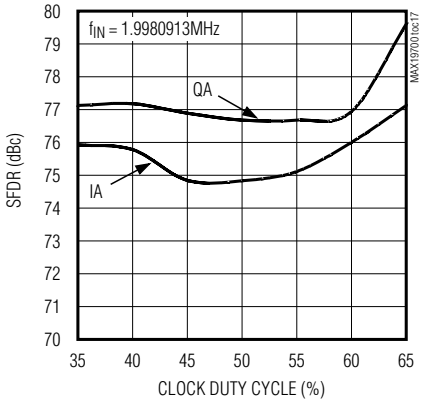
Rx ADC SIGNAL-TO-NOISE RATIO vs. CLOCK DUTY CYCLE



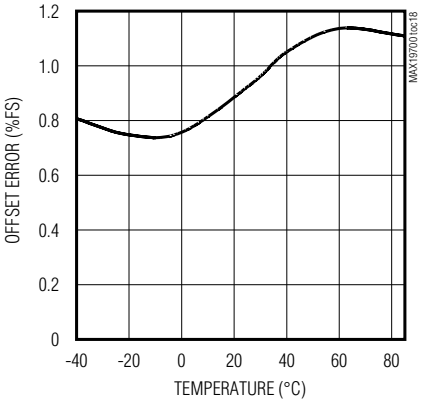
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. CLOCK DUTY CYCLE



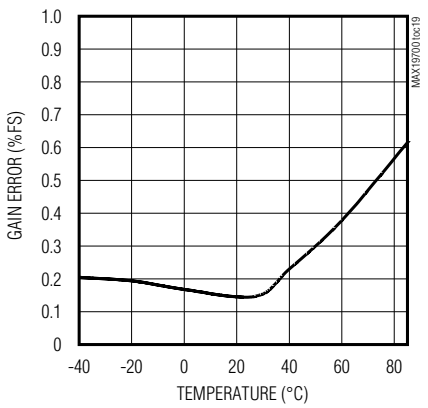
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK DUTY CYCLE



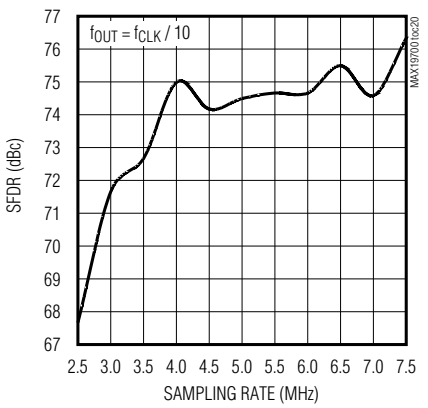
Rx ADC OFFSET ERROR vs. TEMPERATURE



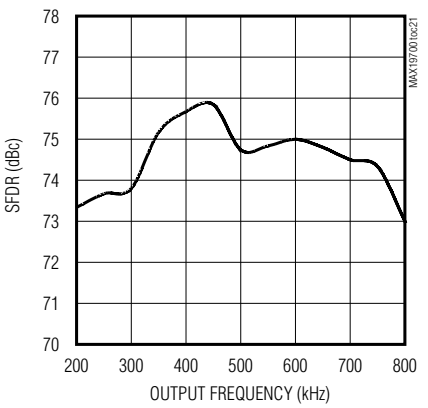
Rx ADC GAIN ERROR vs. TEMPERATURE



Tx PATH SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE



Tx PATH SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY

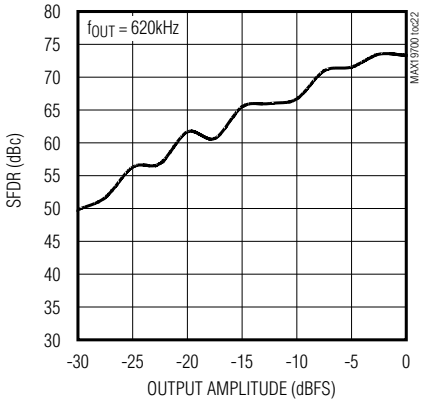


7.5Msps, Ultra-Low-Power Analog Front-End

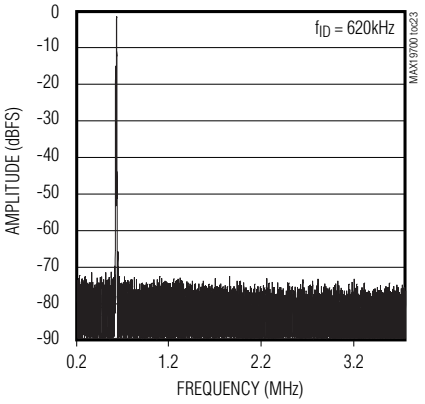
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, $C_{REFP} = C_{REFN} = C_{COM}$ = 0.33µF, T_A = +25°C, unless otherwise noted.)

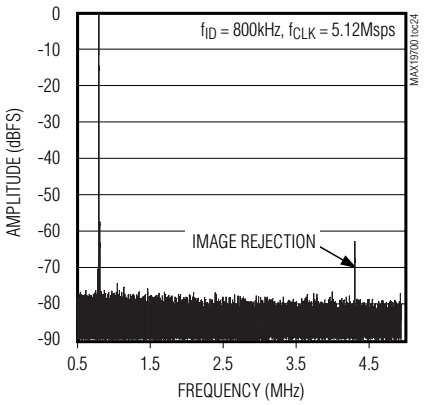
Tx PATH SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT AMPLITUDE



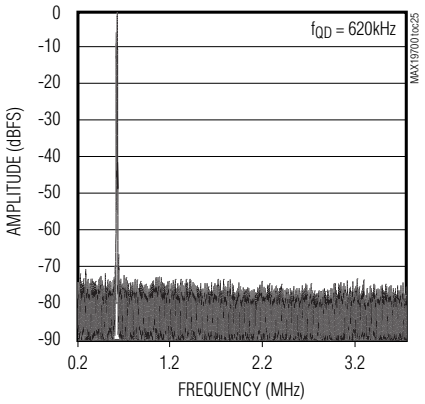
Tx PATH CHANNEL-ID SPECTRAL PLOT



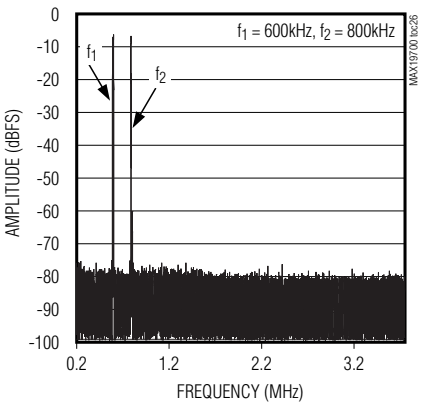
Tx PATH CHANNEL-ID SPECTRAL PLOT WITH IMAGE REJECTION



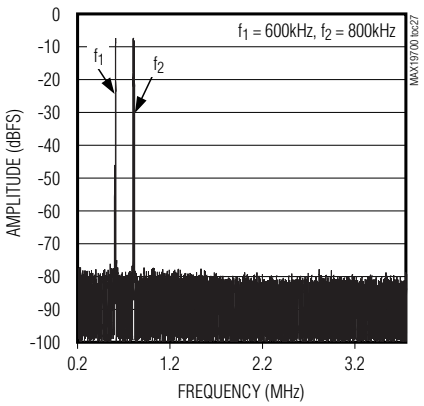
Tx PATH CHANNEL-QD SPECTRAL PLOT



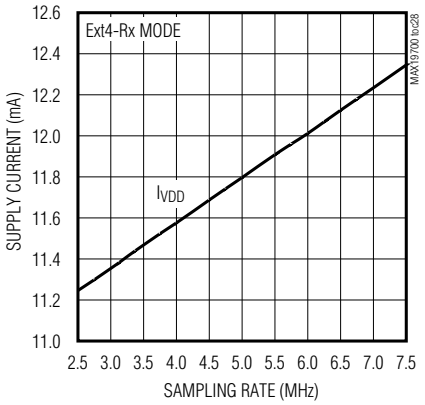
Tx PATH CHANNEL-ID TWO-TONE SPECTRAL PLOT



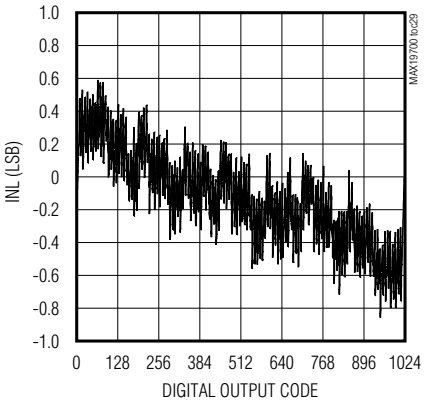
Tx PATH CHANNEL-QD TWO-TONE SPECTRAL PLOT



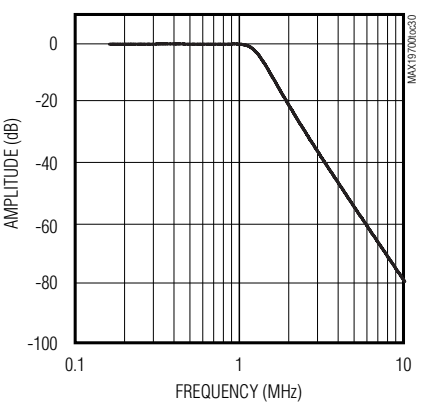
SUPPLY CURRENT vs. SAMPLING RATE



Rx ADC INTEGRAL NONLINEARITY



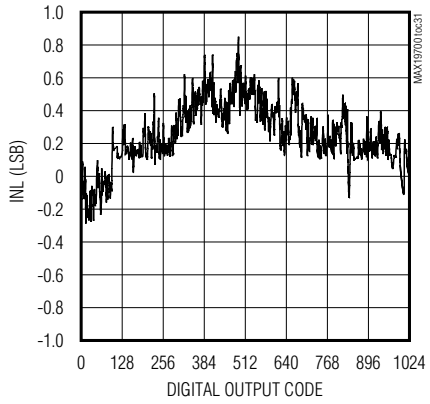
TRANSMIT FILTER FREQUENCY RESPONSE



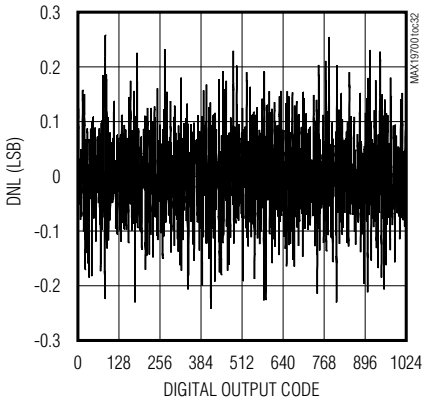
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz 50% duty cycle, ADC input amplitude = -0.5dBFS, DAC output amplitude = 0dBFS, differential ADC input, differential DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

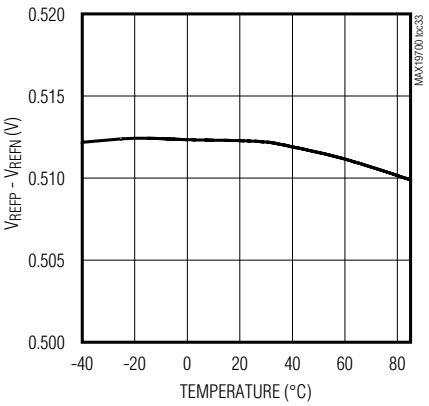
Tx PATH INTEGRAL NONLINEARITY



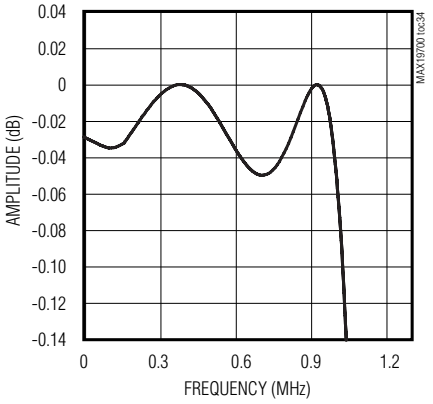
Tx PATH DIFFERENTIAL NONLINEARITY



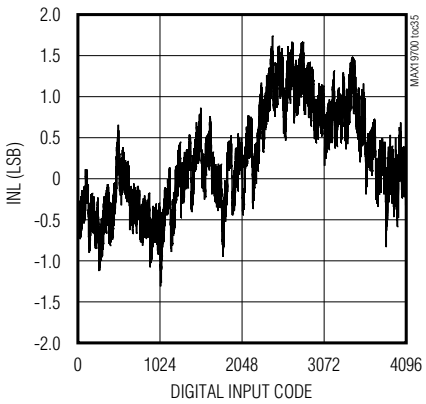
REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



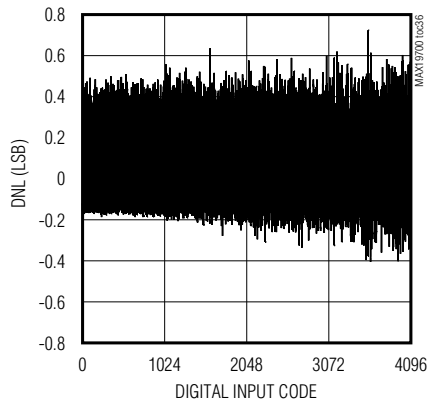
TRANSMIT FILTER PASSBAND RIPPLE



AUX-DAC INTEGRAL NONLINEARITY



AUX-DAC DIFFERENTIAL NONLINEARITY



7.5Msps, Ultra-Low-Power Analog Front-End

Pin Description

PIN	NAME	FUNCTION
1	REFP	Upper Reference Voltage. Bypass with a 0.33µF capacitor to GND as close to REFP as possible.
2, 8, 11, 31, 33, 39 43	V_{DD}	Analog Supply Voltage. Bypass V_{DD} to GND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
3	IAP	Channel IA Positive Analog Input. For single-ended operation, connect signal source to IAP.
4	IAN	Channel IA Negative Analog Input. For single-ended operation, connect IAN to COM.
5, 7, 12, 32, 42	GND	Analog Ground. Connect all GND pins to ground plane.
6	CLK	Conversion Clock Input. Clock signal for both receive ADCs and transmit DACs.
9	QAN	Channel QA Negative Analog Input. For single-ended operation, connect QAN to COM.
10	QAP	Channel QA Positive Analog Input. For single-ended operation, connect signal source to QAP.
13–18, 21–24	D0–D9	Digital I/O. Outputs for receive ADC in Rx mode. Inputs for transmit DAC in Tx mode. D9 is the most significant bit (MSB) and D0 is the least significant bit (LSB).
19	OGND	Output-Driver Ground
20	OV_{DD}	Output-Driver Power Supply. Supply range from +1.8V to V_{DD} to accommodate most logic levels. Bypass OV_{DD} to OGND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
25	$\overline{SHDN}$	Active-Low Shutdown Input. Apply logic-low to place the MAX19700 in shutdown.
26	DR	Data-Ready Indicator. This digital output indicates channel I data (DR = 1) or channel Q data (DR = 0) is present on the output.
27	T/$\overline{R}$	Transmit- or Receive-Mode Select Input. T/$\overline{R}$ logic-low input sets the device in receive mode. A logic-high input sets the device in transmit mode.
28	DIN	3-Wire Serial-Interface Data Input. Data is latched on the rising edge of the SCLK.
29	SCLK	3-Wire Serial-Interface Clock Input
30	$\overline{CS}$	3-Wire Serial-Interface Chip-Select Input. Logic-low enables the serial interface.
34, 35	N.C.	No Connection
36	DAC3	Analog Output for Auxiliary DAC3
37	DAC2	Analog Output for Auxiliary DAC2
38	DAC1	Analog Output for Auxiliary DAC1 (AFC DAC, V_{OUT} = 1.1V During Power-Up)
40, 41	IDN, IDP	DAC Channel-ID Differential Voltage Output
44, 45	QDN, QDP	DAC Channel-QD Differential Voltage Output
46	REFIN	Reference Input. Connect to V_{DD} for internal reference.
47	COM	Common-Mode Voltage I/O. Bypass COM to GND with a 0.33µF capacitor.
48	REFN	Negative Reference I/O. Conversion range is ±(V_{REFP} - V_{REFN}). Bypass REFN to GND with a 0.33µF capacitor.
—	EP	Exposed Paddle. Exposed paddle is internally connected to GND. Connect EP to the GND plane.

Detailed Description

The MAX19700 integrates a dual 10-bit Rx ADC and a dual 10-bit Tx DAC with TD-SCDMA baseband filters while providing ultra-low power and high dynamic performance at a 7.5Msps conversion rate. The Rx ADC analog input amplifiers are fully differential and accept $1V_{P-P}$ full-scale signals. The Tx DAC analog outputs are fully differential with ±410mV full-scale output, selectable common-mode range and offset adjust.

The MAX19700 includes a 3-wire serial interface to control operating modes and power management. The serial interface is SPI™ and MICROWIRE™ compatible. The MAX19700 serial interface selects shutdown, idle, standby, transmit (Tx), and receive (Rx) modes.

SPI is a trademark of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

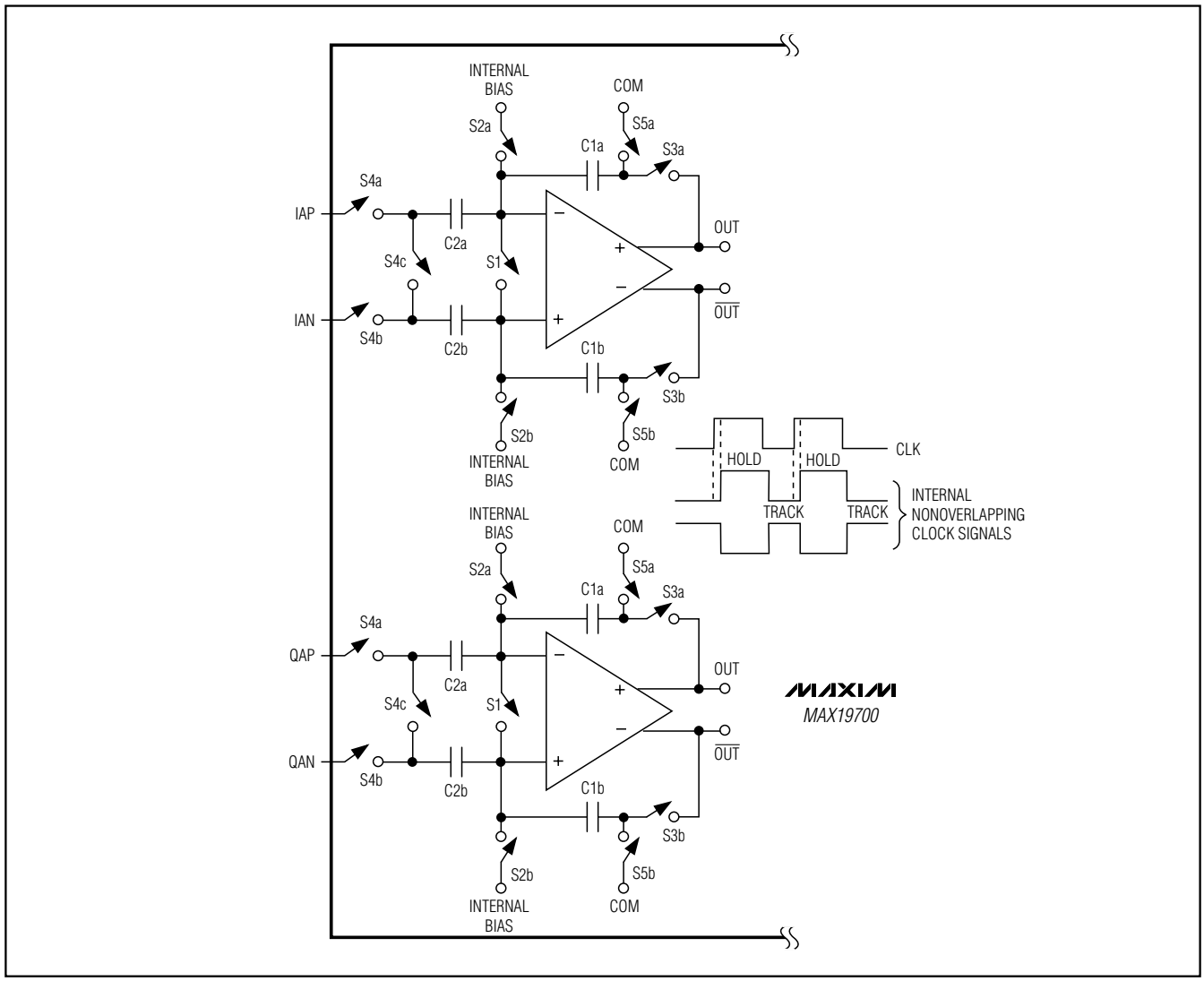


Figure 1. MAX19700 Rx ADC Internal T/H Circuits

To operate the device in TDD applications, configure the MAX19700 for Tx or Rx mode with the 3-wire serial interface. The Rx ADC and Tx DAC share a common digital bus to reduce the digital I/O to a single 10-bit parallel multiplexed bus.

Dual 10-Bit Rx ADC

The ADC uses a seven-stage, fully differential, pipelined architecture that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half clock cycle. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for channel IA and 5.5 clock cycles for channel QA. The ADC full-scale analog input range is $\pm V_{REF}$ with a V_{DD} / 2 ±0.2V common-mode input range. V_{REF} is the difference between V_{REFP} and V_{REFN}. See the *Reference Configurations* section for details.

Input Track-and-Hold (T/H) Circuits

Figure 1 displays a simplified diagram of the Rx ADC input track-and-hold (T/H) circuitry. Both ADC inputs (IAP, QAP, IAN, and QAN) can be driven either differentially or single-ended. Match the impedance of IAP

7.5Msps, Ultra-Low-Power Analog Front-End

Table 1. Output Codes vs. Input Voltage

DIFFERENTIAL INPUT VOLTAGE	DIFFERENTIAL INPUT (LSB)	OFFSET BINARY (D0–D9)	OUTPUT DECIMAL CODE
V_{REF} x 512/512	511 (+Full Scale – 1 LSB)	11 1111 1111	1023
V_{REF} x 511/512	510 (+Full Scale – 2 LSB)	11 1111 1110	1022
V_{REF} x 1/512	+1	10 0000 0001	513
V_{REF} x 0/512	0 (Bipolar Zero)	10 0000 0000	512
-V_{REF} x 1/512	-1	01 1111 1111	511
-V_{REF} x 511/512	-511 (-Full Scale +1 LSB)	00 0000 0001	1
-V_{REF} x 512/512	-512 (-Full Scale)	00 0000 0000	0

and IAN, as well as QAP and QAN, and set the input signal common-mode voltage within the ADC range of $V_{DD}/2$ (±200mV) for optimum performance.

ADC System Timing Requirements

Figure 3 shows the relationship between the clock, analog inputs, DR indicator, and the resulting output data. Channel I (CHI) and channel Q (CHQ) are sampled on the rising edge of the clock signal (CLK) and the resulting data is multiplexed at the D0–D9 outputs. CHI data is updated on the rising edge and CHQ data is updated on the falling edge of the CLK. The DR indicator follows CLK with a typical delay time of 8.5ns and remains high when CHI data is updated and low when CHQ data is updated. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for CHI and 5.5 clock cycles for CHQ.

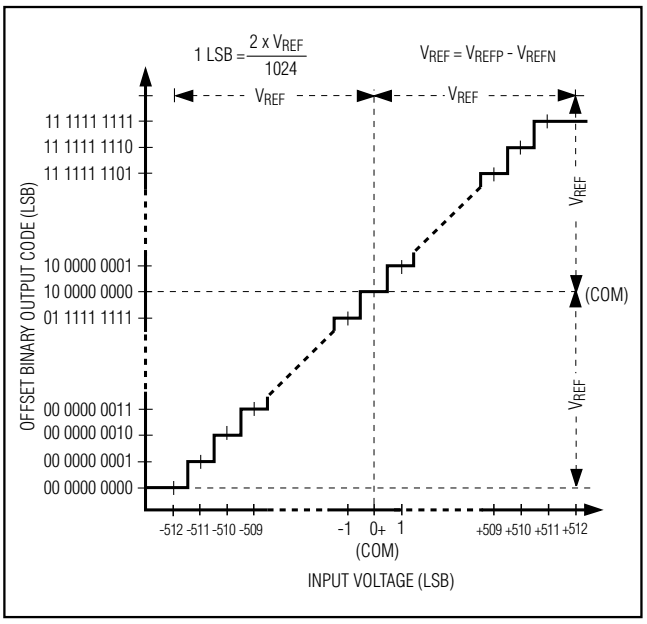


Figure 2. ADC Transfer Function

Digital Input/Output Data (D0–D9)

D0–D9 are the Rx ADC digital logic outputs when the MAX19700 is in receive mode. This bus is shared with the Tx DAC digital logic inputs and operates in half-duplex mode. D0–D9 are the Tx DAC digital logic inputs when the MAX19700 is in transmit mode. The logic level is set by OV_{DD} from 1.8V to V_{DD}. The digital output coding is offset binary (Table 1). Keep the capacitive load on the digital outputs D0–D9 as low as possible (<15pF) to avoid large digital currents feeding back into the analog portion of the MAX19700 and degrading its dynamic performance. Buffers on the digital outputs isolate the outputs from heavy capacitive loads. Adding 100Ω resistors in series with the digital outputs close to the MAX19700 will help improve ADC performance. See the MAX19700EVKIT schematic for an example of the digital outputs driving a digital buffer through 100Ω series resistors.

During SHDN, IDLE, and STBY states, the pins D0–D9 are internally pulled up to prevent floating digital inputs. To ensure no current flows through D0–D9 I/O, the external bus needs to be either tri-stated or pulled up to OV_{DD} and should not be pulled to ground.

Dual 10-Bit Tx DAC and Transmit Path

The dual 10-bit digital-to-analog converters (Tx DAC) operate with clock speeds up to 7.5MHz. The Tx DAC digital inputs, D0–D9, are multiplexed on a single 10-bit bus. The voltage reference determines the Tx path full-scale output voltage. See the *Reference Configurations* section for details on setting the reference voltage. Each Tx path channel integrates a lowpass filter tuned to meet the TD-SCDMA spectral mask requirements. The TD-SCDMA filters are tuned for 1.27MHz cutoff frequency and >55dB image rejection at f_{IMAGE} = 4.32MHz, f_{OUT} = 800kHz, and f_{CLK} = 5.12MHz. See Figure 4 for an illustration of the filter frequency response.

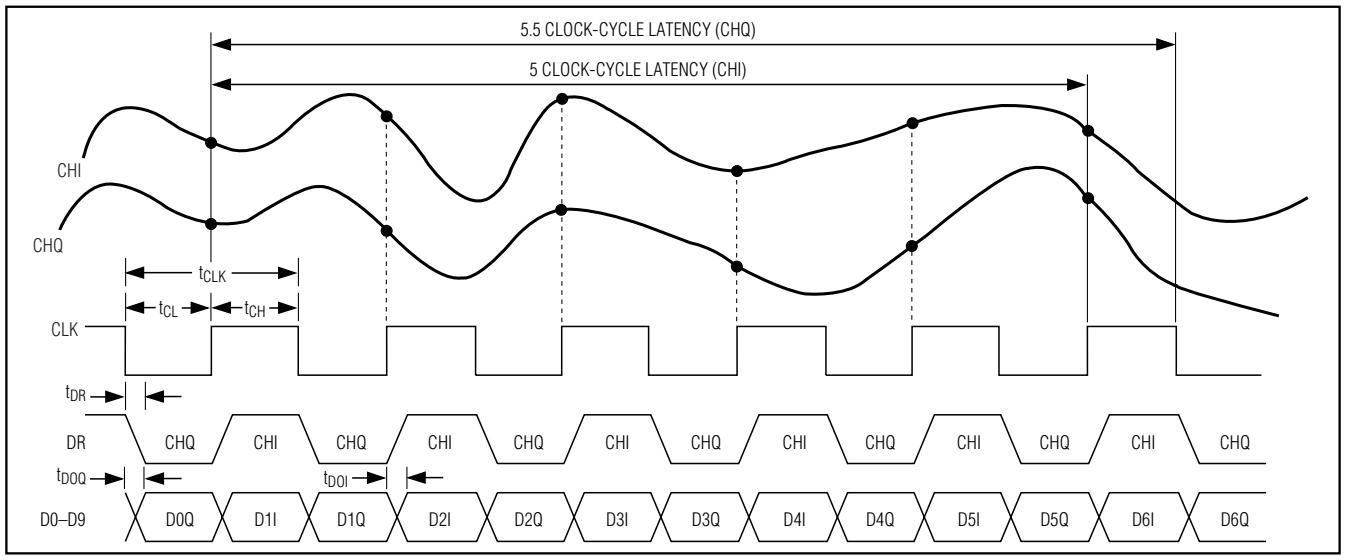


Figure 3. Rx ADC System Timing Diagram

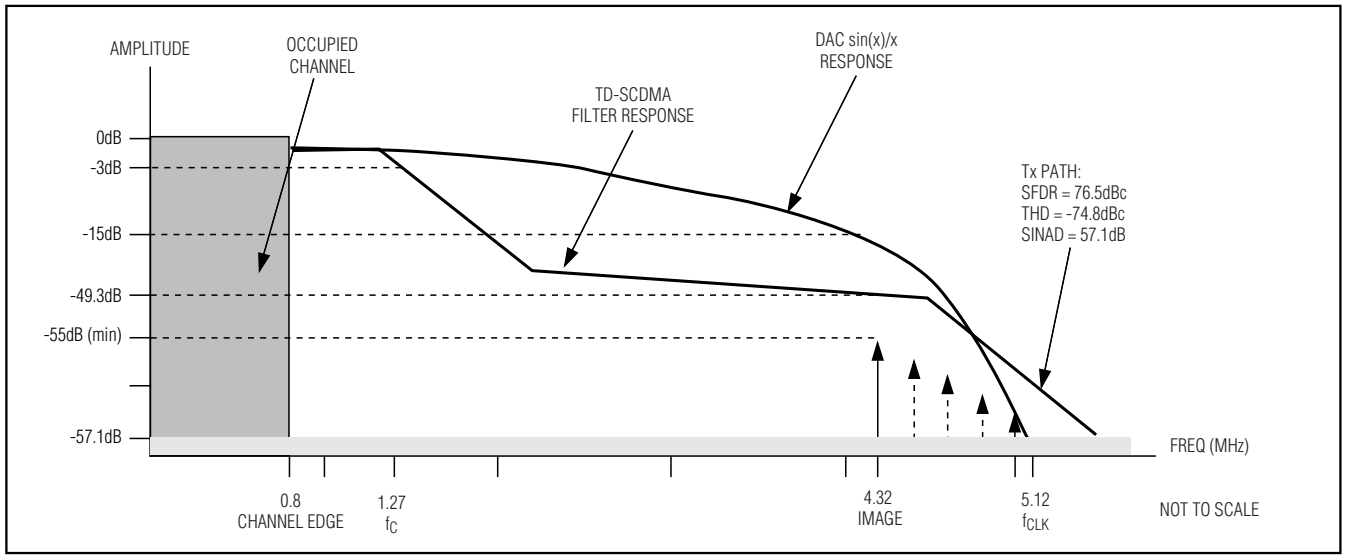


Figure 4. TD-SCDMA Filter Frequency Response

Buffer amplifiers follow the TD-SCDMA filters. The amplifier outputs are biased at an adjustable common-mode DC level and designed to drive a differential input stage with input impedance ≥70kΩ. This simplifies the analog interface between RF quadrature upconverters and the MAX19700. Many RF upconverters require a 0.9V to 1.5V common-mode bias. The SPI-controlled DC common-mode bias eliminates discrete level-setting resistors and code-generated level shifting while preserving the full dynamic range of each Tx DAC. Table 2 shows the Tx path output voltage vs. input codes. Table 10 shows the selection of DC common-mode levels.

The buffer amplifiers also feature a programmable full-scale output level of ±410mV or ±500mV and independent DC offset correction of each I/Q channel. Both features are configured through the SPI interface. The DC offset correction is used to optimize sideband and carrier suppression in the Tx signal path (see Tables 8 and 9).

Table 2. Tx Path Output Voltage vs. Input Codes

(Internal Reference Mode V_{REFDAC} = 1.024V, External Reference Mode V_{REFDAC} = V_{REFIN}; V_{FS} = 410mV for 820mV_{P-P} Full Scale and V_{FS} = 500mV for 1V_{P-P} Full Scale)

DIFFERENTIAL OUTPUT VOLTAGE (V)	OFFSET BINARY (D0–D9)	INPUT DECIMAL CODE
$(V_{FS})\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	11 1111 1111	1023
$(V_{FS})\frac{V_{REFDAC}}{1024} \times \frac{1021}{1023}$	11 1111 1110	1022
$(V_{FS})\frac{V_{REFDAC}}{1024} \times \frac{3}{1023}$	10 0000 0001	513
$(V_{FS})\frac{V_{REFDAC}}{1024} \times \frac{1}{1023}$	10 0000 0000	512
$(V_{FS})\frac{-V_{REFDAC}}{1024} \times \frac{1}{1023}$	01 1111 1111	511
$(V_{FS})\frac{-V_{REFDAC}}{1024} \times \frac{1021}{1023}$	00 0000 0001	1
$(V_{FS})\frac{-V_{REFDAC}}{1024} \times \frac{1023}{1023}$	00 0000 0000	0

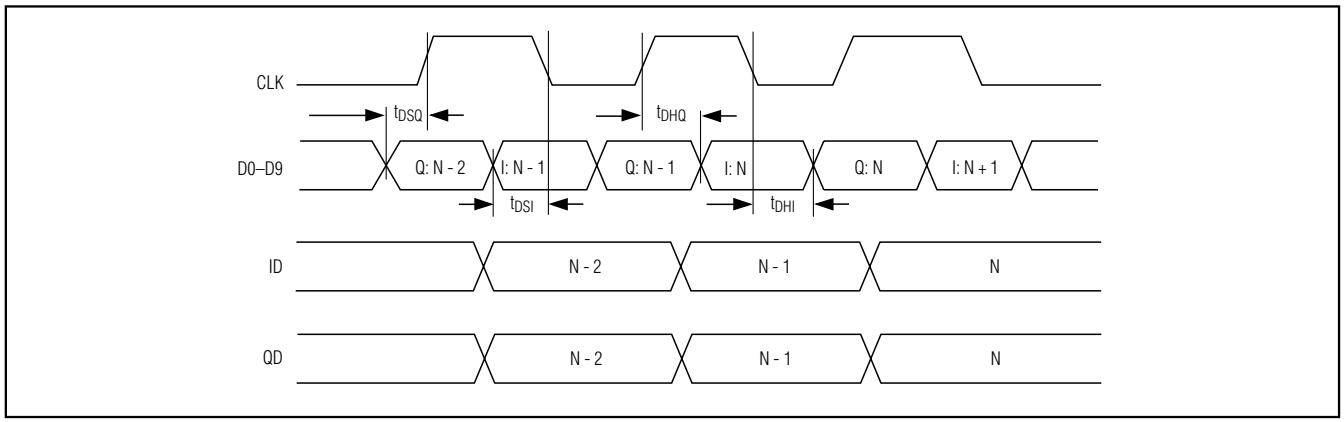


Figure 5. Tx DAC System Timing Diagram

Tx DAC Timing

Figure 5 shows the relationship between the clock, input data, and analog outputs. Data for the I-channel (ID) is latched on the falling edge of the clock signal, and Q-channel (QD) data is latched on the rising edge of the clock signal. Both I and Q outputs are simultaneously updated on the next rising edge of the clock signal.

3-Wire Serial Interface and Operation Modes

The 3-wire serial interface controls the MAX19700 operation modes as well as the three 12-bit aux-DACs. Upon power-up, program the MAX19700 to operate in the desired mode. Use the 3-wire serial interface to program the device for shutdown, idle, standby, Rx, Tx, or aux-DAC modes. A 16-bit data register sets the mode control. The 16-bit word is comprised of A3–A0 control bits and D11–D0 data bits. Tables 4, 5, and 6 show the MAX19700 operating modes and SPI commands. The serial interface remains active in all modes.

SPI Register Description

The operating modes can be selected by programming the control bits, A3–A0, in the register as shown in Table 3. Modifying A3–A0 bits will select from ENABLE-16, Aux-DAC1, Aux-DAC2, Aux-DAC3, IOFFSET, QOFFSET, and COMSEL modes. ENABLE-16 is the default operating mode. This mode allows for shutdown, idle, and standby states as well as switching between FAST, SLOW, Rx, and Tx modes. Table 4 shows the MAX19700 power-management modes. Table 5 shows the T/$\overline{R}$ pin-controlled external Tx-Rx switching modes. Table 6 shows the SPI-controlled Tx-Rx switching modes.

In ENABLE-16 mode, the aux-DACs have independent control bits E6, E5, and E4, and the Tx-path full-scale output can be set with bit E7. Table 7 shows the auxiliary DAC enable codes and Table 8 shows the full-scale output selection. Bits E11 and E10 are reserved and need to be programmed to logic-low. Bits E9 and E8 are not used.

Modes Aux-DAC1, Aux-DAC2, and Aux-DAC3 select the aux-DAC channels named DAC1, DAC2, and DAC3 and hold the data inputs for each DAC. Bits _D11–_D0 are the data inputs for each aux-DAC and can be programmed through SPI. The MAX19700 also includes two 6-bit registers that can be programmed to correct the offsets for the Tx-path I and Q channels independently (see Table 9). Use the COMSEL mode to select the output common-mode voltage with bits CM1 and CM0 (see Table 10).

Shutdown mode offers the most dramatic power savings by shutting down all the analog sections of the MAX19700 and placing the Rx ADC digital outputs in tri-state mode. When the Rx ADC outputs transition from tri-state to active, the last converted word is placed on the digital outputs. The Tx DAC previously stored data is lost when coming out of shutdown mode. The wake-up time from shutdown mode is dominated by the time required to charge the capacitors at REFP, REFN, and COM. In internal reference mode and buffered external reference mode, the wake-up time is typically 75µs to enter Rx mode and 25µs to enter Tx mode.

In idle mode, the reference and clock distribution circuits are powered, but all other functions are off. The Rx ADC outputs are forced to tri-state. The wake-up time is 7.3µs to enter Rx mode and 5µs to enter Tx mode. When the Rx ADC outputs transition from tri-state to active, the last converted word is placed on the digital outputs.

In standby mode, the reference is powered, but the rest of the device functions are off. The wake-up time from standby mode is 7.3µs to enter Rx mode and 25µs to enter Tx mode. When the Rx ADC outputs transition from tri-state to active, the last converted word is placed on the digital outputs.

FAST and SLOW Rx and Tx Modes

In addition to the external Tx-Rx control, the MAX19700 also features SLOW and FAST modes for switching between Rx and Tx operation. In FAST Tx mode, the Rx ADC core is powered on but the ADC core digital outputs are tri-stated on the D0–D9 bus; likewise, in FAST Rx mode the transmit path (DAC core and Tx filter) is powered on but the DAC core digital inputs are tri-stated on the D0–D9 bus. The switching time between Tx to Rx or Rx to Tx is FAST because the converters are on and do not have to recover from a power-down state. In FAST mode, the switching time between Rx to Tx and Tx to Rx is 1µs. However, power consumption is higher in this mode because both the Tx and Rx cores are always on. To prevent bus contention in these states, the Rx ADC output buffers are tri-stated during Tx and the Tx DAC input bus is tri-stated during Rx.

In SLOW mode, the Rx ADC core is off during Tx; likewise the Tx DAC and filters are turned off during Rx to yield lower power consumption in these modes. For example, the power in SLOW Tx mode is 31.2mW. The power consumption during Rx is 21mW compared to power consumption in FAST mode of 38.4mW. However, the recovery time between states is increased. The switching time in SLOW mode between Rx to Tx is 5µs and Tx to Rx is 7.3µs.

External T/$\overline{R}$ Switching Control vs. Serial-Interface Control

Bit E3 in the ENABLE-16 register determines whether the device Tx-Rx mode is controlled externally through the T/$\overline{R}$ input (E3 = low) or through the SPI command (E3 = high). By default, the MAX19700 is in the external Tx-Rx control mode. In the external control mode, use the T/$\overline{R}$ input (pin 27) to switch between Rx and Tx modes. Using the T/$\overline{R}$ pin provides faster switching between Rx and Tx modes. To override the external Tx-Rx control, program the MAX19700 through the serial interface. During SHDN, IDLE, or STBY modes, the T/$\overline{R}$ input is overridden. To restore external Tx-Rx control, program bit E3 low and exit the SHDN, IDLE, or STBY modes through the serial interface.

7.5Msps, Ultra-Low-Power Analog Front-End

SPI Timing

The serial digital interface is a standard 3-wire connection compatible with SPI/QSPI™/MICROWIRE/DSP interfaces. Set $\overline{CS}$ low to enable the serial data loading at DIN. Following a $\overline{CS}$ high-to-low transition, data is shifted synchronously, most significant bit first, on the rising edge of the serial clock (SCLK). After 16 bits are loaded into the serial input register, data is transferred to the latch when $\overline{CS}$ transitions high. $\overline{CS}$ must transition high for a minimum of 80ns before the next write sequence. The SCLK can idle either high or low between transitions. Figure 6 shows the detailed timing diagram of the 3-wire serial interface.

QSPI is a trademark of Motorola, Inc.

Mode-Recovery Timing

Figure 7 shows the mode-recovery timing diagram. t_{WAKE} is the wakeup time when exiting shutdown, idle, or standby mode and entering Rx or Tx mode. t_{ENABLE} is the recovery time when switching between either Rx or Tx mode. t_{WAKE} or t_{ENABLE} is the time for the Rx ADC to settle within 1dB of specified SINAD performance and Tx DAC settling to 10 LSB error. t_{WAKE} and t_{ENABLE} times are measured after either the 16-bit serial command is latched into the MAX19700 by a $\overline{CS}$ transition high (SPI controlled) or a T/$\overline{R}$ logic transition (external Tx-Rx control). In FAST mode, the recovery time is 1µs to switch between Tx or Rx modes.

Table 3. MAX19700 Mode Control

REGISTER NAME	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0
	(MSB)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
ENABLE-16	E11 = 0 Reserved	E10 = 0 Reserved	—	—	E7	E6	E5	E4	E3	E2	E1	E0	0	0	0	0
Aux-DAC1	1D11	1D10	1D9	1D8	1D7	1D6	1D5	1D4	1D3	1D2	1D1	1D0	0	0	0	1
Aux-DAC2	2D11	2D10	2D9	2D8	2D7	2D6	2D5	2D4	2D3	2D2	2D1	2D0	0	0	1	0
Aux-DAC3	3D11	3D10	3D9	3D8	3D7	3D6	3D5	3D4	3D3	3D2	3D1	3D0	0	0	1	1
IOFFSET	—	—	—	—	—	—	IO5	IO4	IO3	IO2	IO1	IO0	0	1	0	0
QOFFSET	—	—	—	—	—	—	QO5	QO4	QO3	QO2	QO1	QO0	0	1	0	1
COMSEL	—	—	—	—	—	—	—	—	—	—	CM1	CM0	0	1	1	0

Table 4. Power-Management Modes

ADDRESS				DATA BITS				T/$\overline{R}$	MODE	FUNCTION (POWER MANAGEMENT)	DESCRIPTION	COMMENT
A3	A2	A1	A0	E3	E2	E1	E0	PIN 27				
0000				X000				X	SHDN	SHUTDOWN	Rx ADC = OFF Tx DAC = OFF Aux-DAC = OFF REF = OFF	Device is in complete shutdown Overrides T/$\overline{R}$ pin
				X001				X	IDLE	IDLE	Rx ADC = OFF Tx DAC = OFF Aux-DAC = Last State CLK = ON REF = ON	Fast turn-on time Moderate idle power Overrides T/$\overline{R}$ pin
				X010				X	STBY	STANDBY	Rx ADC = OFF Tx DAC = OFF Aux-DAC = Last State CLK = OFF REF = ON	Slow turn-on time Low standby power Overrides T/$\overline{R}$ pin

X = Don't care.

Table 5. External Tx-Rx Control Using T/$\overline{R}$ Pin (T/$\overline{R}$ = 0 = Rx Mode, T/$\overline{R}$ = 1 = Tx Mode)

ADDRESS				DATA BITS				T/$\overline{R}$	STATE	FUNCTION Rx TO Tx-Tx TO Rx SWITCHING SPEED	DESCRIPTION	COMMENT
A3	A2	A1	A0	E3	E2	E1	E0	PIN 27				
0000				0011				0	Ext1-Rx	FAST-SLOW	Rx Mode Rx ADC = ON Tx DAC = ON Rx Bus = Enable	Moderate Power Fast Rx to Tx when T/$\overline{R}$ transitions 0 to 1
								1	Ext1-Tx		Tx Mode Rx ADC = OFF Tx DAC = ON Tx Bus = Enable	Low Power Slow Tx to Rx when T/$\overline{R}$ transitions 1 to 0
				0100				0	Ext2-Rx (Default)	SLOW-FAST	Rx Mode Rx ADC = ON Tx DAC = OFF Rx Bus = Enable	Low Power Slow Rx to Tx when T/$\overline{R}$ transitions 0 to 1
								1	Ext2-Tx		Tx Mode Rx ADC = ON Tx DAC = ON Tx Bus = Enable	Moderate Power Fast Tx to Rx when T/$\overline{R}$ transitions 1 to 0
				0101				0	Ext3-Rx	SLOW-SLOW	Rx Mode Rx ADC = ON Tx DAC = OFF Rx Bus = Enable	Low Power Slow Rx to Tx when T/$\overline{R}$ transitions 0 to 1
								1	Ext3-Tx		Tx Mode Rx ADC = OFF Tx DAC = ON Tx Bus = Enable	Low Power Slow Tx to Rx when T/$\overline{R}$ transitions 1 to 0
				0110				0	Ext4-Rx	FAST-FAST	Rx Mode Rx ADC = ON Tx DAC = ON Rx Bus = Enable	Moderate Power Fast Rx to Tx when T/$\overline{R}$ transitions 0 to 1
								1	Ext4-Tx		Tx Mode Rx ADC = ON Tx DAC = ON Tx Bus = Enable	Moderate Power Fast Tx to Rx when T/$\overline{R}$ transitions 1 to 0

System Clock Input (CLK)

Both the Rx ADC and Tx DAC share the CLK input. The CLK input accepts a CMOS-compatible signal level set by OV_{DD} from 1.8V to V_{DD}. Since the interstage conversion of the device depends on the repeatability of the rising and falling edges of the external clock, use a clock with low jitter and fast rise and fall times (<2ns). Specifically, sampling occurs on the rising edge of the clock signal, requiring this edge to provide the lowest

7.5Msps, Ultra-Low-Power Analog Front-End

Table 6. Tx-Rx Control Using SPI Commands

ADDRESS				DATA BITS				T/$\overline{R}$	MODE	FUNCTION (Tx-Rx SWITCHING SPEED)	DESCRIPTION	COMMENTS
A3	A2	A1	A0	E3	E2	E1	E0	PIN 27				
0000				1011				X	SPI1-Rx	SLOW	Rx Mode Rx ADC = ON Tx DAC = OFF Rx Bus = Enable	Low Power Slow Rx to Tx through SPI command
				1100				X	SPI2-Tx	SLOW	Tx Mode Rx ADC = OFF Tx DAC = ON Tx Bus = Enable	Low Power Slow Tx to Rx through SPI command
				1101				X	SPI3-Rx	FAST	Rx Mode Rx ADC = ON Tx DAC = ON Rx Bus = Enabled	Moderate Power Fast Rx to Tx through SPI command
				1110				X	SPI4-Tx	FAST	Tx Mode Rx ADC = ON Tx DAC = ON Tx Bus = Enabled	Moderate Power Fast Tx to Rx through SPI command

X = Don't care.

Table 7. Aux-DAC Enable Table (ENABLE-16 Mode)

E6	E5	E4	Aux-DAC3	Aux-DAC2	Aux-DAC1
0	0	0	ON	ON	ON
0	0	1	ON	ON	OFF
0	1	0	ON	OFF	ON
0	1	1	ON	OFF	OFF
1	0	0	OFF	ON	ON
1	0	1	OFF	ON	OFF
1	1	0	OFF	OFF	ON
1	1	1	OFF	OFF	OFF

Table 8. Tx-Path Full-Scale Select (ENABLE-16 Mode)

E7	Tx-PATH OUTPUT FULL SCALE
0 (Default)	820mV$_{P-P}$
1	1V$_{P-P}$

possible jitter. Any significant clock jitter limits the SNR performance of the on-chip Rx ADC as follows:

$$SNR = 20 \times \log\left(\frac{1}{2 \times \pi \times f_{IN} \times t_{AJ}}\right)$$

where f_{IN} represents the analog input frequency and t_{AJ} is the time of the clock jitter.

Clock jitter is especially critical for undersampling applications. Consider the clock input as an analog input and route away from any analog input or other digital signal lines. The MAX19700 clock input operates with a OV_{DD} / 2 voltage threshold and accepts a 50% ±15% duty cycle.

12-Bit, Auxiliary Control DACs

The MAX19700 includes three 12-bit aux-DACs (DAC1, DAC2, DAC3) with 1µs settling time for controlling variable-gain amplifier (VGA), automatic gain-control (AGC), and automatic frequency-control (AFC) functions. The aux-DAC output range is 0.1V to 2.56V. During power-up, the VGA and AGC outputs (DAC2 and DAC3) are at zero. The AFC DAC (DAC1) is at 1.1V during power-up. The aux-DACs can be independently

Table 9. Offset Control Bits for I and Q Channels (IOFFSET or QOFFSET Mode)

BITS IO5–IO0 WHEN IN IOFFSET MODE, BITS QO5–QO0 WHEN IN QOFFSET MODE						OFFSET 1 LSB = (VFS_{P-P}/1023)
IO5/QO5	IO4/QO4	IO3/QO3	IO2/QO2	IO1/QO1	IO0/QO0	
1	1	1	1	1	1	-31 LSB
1	1	1	1	1	0	-30 LSB
1	1	1	1	0	1	-29 LSB
• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	0	0	0	1	0	-2 LSB
1	0	0	0	0	1	-1 LSB
1	0	0	0	0	0	0mV
0	0	0	0	0	0	0mV (Default)
0	0	0	0	0	1	1 LSB
0	0	0	0	1	0	2 LSB
• • •	• • •	• • •	• • •	• • •	• • •	• • •
0	1	1	1	0	1	29 LSB
0	1	1	1	1	0	30 LSB
0	1	1	1	1	1	31 LSB

Note: *For transmit full-scale select of 820mVP-P: 1 LSB = (820mVP-P/1023) = 0.8016mV. For transmit full-scale select of 1VP-P: 1 LSB = (1VP-P/1023) = 0.9775mV.*

Table 10. Common-Mode Select (COM-SEL Mode)

CM1	CM0	Tx-PATH OUTPUT COMMON MODE (V)
0	0	1.4 (Default)
0	1	1.25
1	0	1.1
1	1	0.9

controlled through the SPI bus, except during SHDN mode where the aux-DACs are turned off completely and the output voltage is set to zero. In STBY and IDLE modes the aux-DACs maintain the last value. On wakeup from SHDN, the aux-DACs resume the last values.

Loading on the aux-DAC outputs should be carefully observed to achieve specified settling time and stability. The capacitive load must be kept to a maximum of 5pF including package and trace capacitance. The resistive load must be greater than 200kΩ. If capacitive loading exceeds 5pF, then add a 10kΩ resistor in series with the output. Adding the series resistor helps drive larger load capacitance (<15pF) at the expense of slower settling time.

Reference Configurations

The MAX19700 features an internal precision 1.024V bandgap reference that is stable over the entire power-supply and temperature ranges. The REFIN input provides two modes of reference operation. The voltage at REFIN (V_{REFIN}) sets the reference operation mode (Table 11).

In internal reference mode, connect REFIN to V_{DD}. V_{REF} is an internally generated 0.512V ±4%. COM, REFP, and REFN are low-impedance outputs with $V_{COM} = V_{DD} / 2$, $V_{REFP} = V_{DD} / 2 + V_{REF} / 2$, and $V_{REFN} = V_{DD} / 2 - V_{REF} / 2$. Bypass REFP, REFN, and COM each with a 0.33µF capacitor. Bypass REFIN to GND with a 0.1µF capacitor.

In buffered external reference mode, apply 1.024V ±10% at REFIN. In this mode, COM, REFP, and REFN are low-impedance outputs with $V_{COM} = V_{DD} / 2$, $V_{REFP} = V_{DD} / 2 + V_{REFIN} / 4$, and $V_{REFN} = V_{DD} / 2 - V_{REFIN} / 4$. Bypass REFP, REFN, and COM each with a 0.33µF capacitor. Bypass REFIN to GND with a 0.1µF

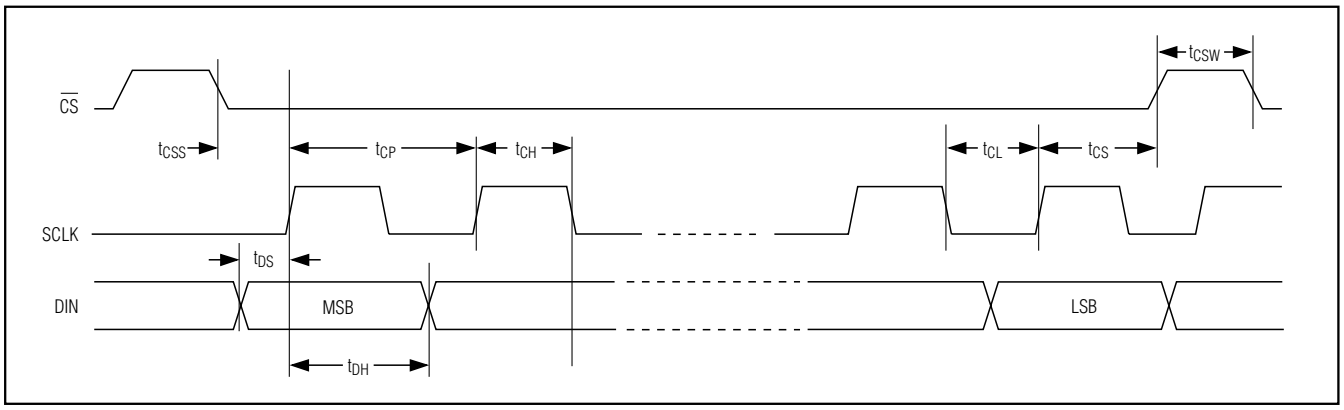


Figure 6. 3-Wire Serial-Interface Timing Diagram

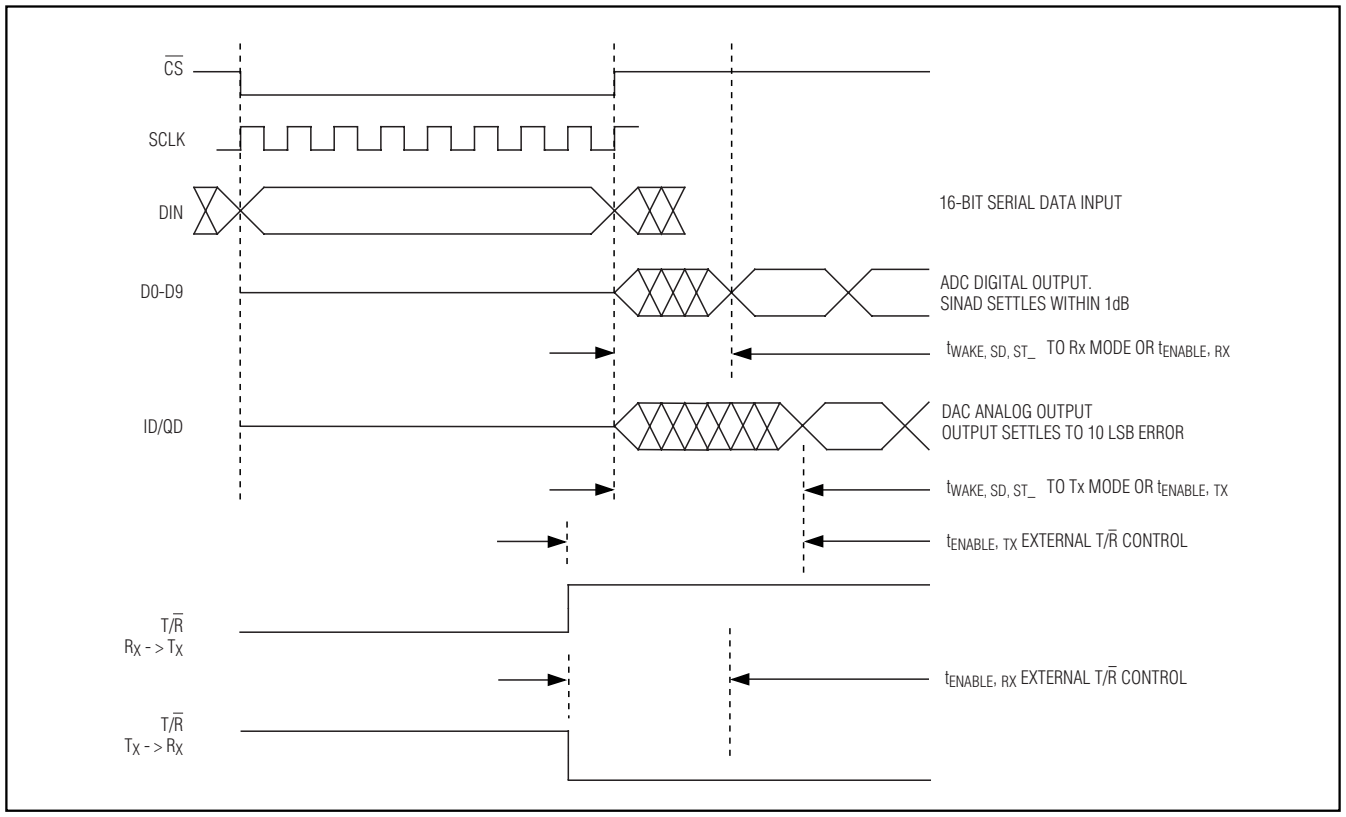


Figure 7. MAX19700 Mode-Recovery Timing Diagram

capacitor. In this mode, the Tx-path full-scale output is proportional to the external reference. For example, if the V_{REFIN} is increased by 10% (max), the Tx-path full-scale output is also increased by 10% or ±451mV.

Power-On Reset

The MAX19700 features a power-on-reset (POR) function that sets the device in a known state upon power-up. The default state is Ext2-Rx. The POR circuit is designed to accommodate power supplies that ramp

Table 11. Reference Modes

V_{REFIN}	REFERENCE MODE
>0.8V x V_{DD}	Internal Reference Mode. V_{REF} is internally generated to be 0.512V. Bypass REFP, REFN, and COM each with a 0.33µF capacitor.
1.024V ±10%	Buffered External Reference Mode. An external 1.024V ±10% reference voltage is applied to REFIN. V_{REF} is internally generated to be V_{REFIN} / 2. Bypass REFP, REFN, and COM each with a 0.33µF capacitor. Bypass REFIN to GND with a 0.1µF capacitor.

from 0V to V_{DD} in less than or equal to 1ms. For power supplies that ramp from 0V to V_{DD} in greater than 1ms, program the MAX19700 to enter the desired state using the SPI interface.

Applications Information

Using Balun Transformer AC-Coupling

An RF transformer (Figure 8) provides an excellent solution to convert a single-ended signal source to a fully differential signal for optimum ADC performance. Connecting the center tap of the transformer to COM provides a V_{DD} / 2 DC level shift to the input. A 1:1 transformer can be used, or a step-up transformer can be selected to reduce the drive requirements. In general, the MAX19700 provides better SFDR and THD with fully differential input signals than single-ended signals, especially for high input frequencies. In differential mode, even-order harmonics are lower as both inputs (IAP, IAN, QAP, QAN) are balanced, and each of the Rx ADC inputs only requires half the signal swing compared to single-ended mode. Figure 9 shows an RF transformer converting the MAX19700 Tx DAC differential analog outputs to single-ended.

Using Op-Amp Coupling

Drive the MAX19700 Rx ADC with op amps when a balun transformer is not available. Figures 10 and 11 show the Rx ADC being driven by op amps for AC-coupled single-ended and DC-coupled differential applications. Amplifiers such as the MAX4454 and MAX4354 provide high speed, high bandwidth, low noise, and low distortion to maintain the input signal integrity. The op-amp circuit shown in Figure 11 can also be used to interface with the Tx DAC differential analog outputs to provide gain or buffering. The Tx DAC differential analog outputs cannot be used in single-ended mode because of the internally generated common-mode level. Also, the Tx DAC analog outputs are designed to drive a differential input stage with input impedance ≥70kΩ. If single-ended outputs are desired, use an amplifier to provide differential-to-single-ended conversion and select an amplifier with proper input common-mode voltage range.

TDD Mode

The MAX19700 is optimized to operate in TD-SCDMA applications. When FAST mode is selected, the MAX19700 can switch between Tx and Rx modes through the T/$\overline{R}$ pin in typically 1µs. The Rx ADC and Tx DAC operate independently. The Rx ADC and Tx DAC digital bus are shared forming a single 10-bit parallel bus. Using the 3-wire serial interface or external T/$\overline{R}$ pin, select between Rx mode to enable the Rx ADC or Tx mode to enable the Tx DAC. When operating in Rx mode, the Tx DAC bus is not enabled and in Tx mode the Rx ADC bus is tri-stated eliminating any unwanted

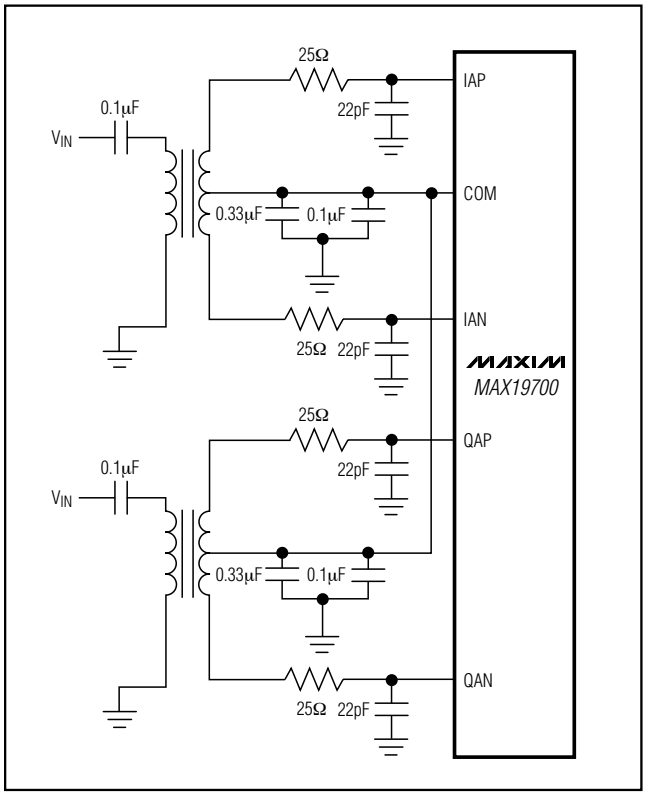


Figure 8. Balun Transformer-Coupled Single-Ended-to-Differential Input Drive for Rx ADC