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19-3826; Rev 1; 6/07

EVALUATION KIT AVAILABLE

10-Bit, 45Msps, Ultra-Low-Power Analog Front-End

MAX19707

General Description

The MAX19707 is an ultra-low-power, mixed-signal analog front-end (AFE) designed for power-sensitive communication equipment. Optimized for high dynamic performance at ultra-low power, the device integrates a dual, 10-bit, 45Msps receive (Rx) ADC; dual, 10-bit, 45Msps transmit (Tx) DAC; three fast-settling 12-bit aux-DAC channels for ancillary RF front-end control; and a 10-bit, 333ksps housekeeping aux-ADC. The typical operating power in Tx-Rx FAST mode is 84.6mW at a 45MHz clock frequency.

The Rx ADCs feature 54.2dB SNR and 71.2dBc SFDR at f_{IN} = 5.5MHz and f_{CLK} = 45MHz. The analog I/Q input amplifiers are fully differential and accept $1.024V_{P-P}$ full-scale signals. Typical I/Q channel matching is ±0.03° phase and ±0.01dB gain.

The Tx DACs feature 73.2dBc SFDR at f_{OUT} = 2.2MHz and f_{CLK} = 45MHz. The analog I/Q full-scale output voltage is ±400mV differential. The Tx DAC common-mode DC level is programmable from 0.71V to 1.05V. The I/Q channel offset is programmable to optimize radio lineup sideband/carrier suppresion. The typical I/Q channel matching is ±0.01dB gain and ±0.07° phase.

The Rx ADC and Tx DAC share a single, 10-bit parallel, high-speed digital bus allowing half-duplex operation for time-division duplex (TDD) applications. A 3-wire serial interface controls power-management modes, the aux-DAC channels, and the aux-ADC channels.

The MAX19707 operates on a single 2.7V to 3.3V analog supply and 1.8V to 3.3V digital I/O supply. The MAX19707 is specified for the extended (-40°C to +85°C) temperature range and is available in a 48-pin, thin QFN package. The *Selector Guide* at the end of the data sheet lists other pin-compatible versions in this AFE family.

Applications

WiMAX CPEs	VoIP Terminals
802.11a/b/g WLAN	Portable Communication Equipment

Ordering Information

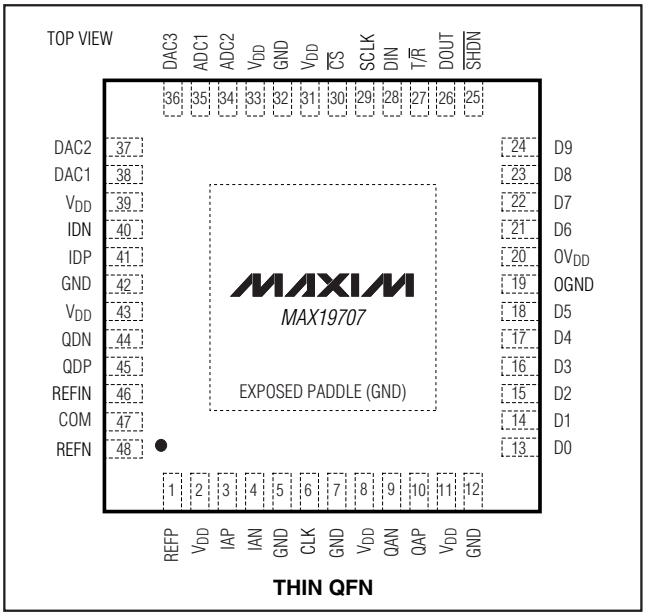
PART*	PIN-PACKAGE	PKG CODE
MAX19707ETM	48 Thin QFN-EP**	T4877-4
MAX19707ETM+	48 Thin QFN-EP**	T4877-4

**All devices are specified over the -40°C to +85°C operating range.*
***EP = Exposed paddle.*
+Denotes lead-free package.

Features

- **Dual, 10-Bit, 45Msps Rx ADC and Dual, 10-Bit, 45Msps Tx DAC**
- **Ultra-Low Power**
  84.6mW at f_{CLK} = 45MHz, Fast Mode
  77.1mW at f_{CLK} = 45MHz, Slow Mode
  Low-Current Standby and Shutdown Modes
- **Programmable Tx DAC Common-Mode DC Level and I/Q Offset Trim**
- **Excellent Dynamic Performance**
  SNR = 54.2dB at f_{IN} = 5.5MHz (Rx ADC)
  SFDR = 73.2dBc at f_{OUT} = 2.2MHz (Tx DAC)
- **Three 12-Bit, 1µs Aux-DACs**
- **10-Bit, 333ksps Aux-ADC with 4:1 Input Mux and Data Averaging**
- **Excellent Gain/Phase Match**
  ±0.03° Phase, ±0.01dB Gain (Rx ADC) at f_{IN} = 5.5MHz
- **Multiplexed Parallel Digital I/O**
- **Serial-Interface Control**
- **Versatile Power-Control Circuits**
  Shutdown, Standby, Idle, Tx/Rx Disable
- **Miniature 48-Pin Thin QFN Package (7mm x 7mm x 0.8mm)**

Pin Configuration



Functional Diagram and Selector Guide appear at end of data sheet.

10-Bit, 45Msps, Ultra-Low-Power Analog Front-End

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND, OV_{DD} to OGND .....-0.3V to +3.6V
GND to OGND.....-0.3V to +0.3V
IAP, IAN, QAP, QAN, IDP, IDN, QDP,
QDN, DAC1, DAC2, DAC3 to GND.....-0.3V to V_{DD}
ADC1, ADC2 to GND.....-0.3V to (V_{DD} + 0.3V)
REFP, REFN, REFIN, COM to GND-0.3V to (V_{DD} + 0.3V)D0–D9, DOUT, T/$\overline{R}$, $\overline{SHDN}$, SCLK, DIN, $\overline{CS}$,
CLK to OGND .....-0.3V to (OV_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
48-Pin Thin QFN (derate 27.8mW/°C above +70°C) 2.22W
Thermal Resistance θ_{JA} .....36°C/W
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 45MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, unless otherwise noted. C_L < 5pF on all aux-DAC outputs. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		2.7	3.0	3.3	V
Output Supply Voltage	OV_{DD}		1.8		V_{DD}	V
V_{DD} Supply Current		Ext1-Tx, Ext3-Tx, and SPI2-Tx states; transmit DAC operating mode (Tx): f_{CLK} = 45MHz, f_{OUT} = 2.2MHz on both channels; aux-DACs ON and at midscale, aux-ADC ON		16.5		mA
		Ext2-Tx, Ext4-Tx, and SPI4-Tx states; transmit DAC operating mode (Tx): f_{CLK} = 45MHz, f_{OUT} = 2.2MHz on both channels; aux-DACs ON and at midscale, aux-ADC ON		29.8	35	
		Ext1-Rx, Ext4-Rx, and SPI3-Rx states; receive ADC operating mode (Rx): f_{CLK} = 45MHz, f_{IN} = 5.5MHz on both channels; aux-DACs ON and at midscale, aux-ADC ON		28.2	34	
		Ext2-Rx, Ext3-Rx, and SPI1-Rx states; receive ADC operating mode (Rx): f_{CLK} = 45MHz, f_{IN} = 5.5MHz on both channels; aux-DACs ON and at midscale, aux-ADC ON		25.7		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 45MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, unless otherwise noted. C_L < 5pF on all aux-DAC outputs. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Supply Current		Standby mode: CLK = 0 or OV_{DD}; aux-DACs ON and at midscale, aux-ADC ON		3.2	5	mA
		Idle mode: f_{CLK} = 45MHz; aux-DACs ON and at midscale, aux-ADC ON		12.1	15	
		Shutdown mode: CLK = 0 or OV_{DD}		1		µA
OV_{DD} Supply Current		Ext1-Rx, Ext2-Rx, Ext3-Rx, Ext4-Rx, SPI1-Rx, SPI3-Rx states; receive ADC operating mode (Rx): f_{CLK} = 45MHz, f_{IN} = 5.5MHz on both channels; aux-DACs ON and at midscale, aux-ADC ON		7.7		mA
		Ext1-Tx, Ext2-Tx, Ext3-Tx, Ext4-Tx, SPI2-Tx, SPI4-Tx states; transmit DAC operating mode (Tx), f_{CLK} = 45MHz, f_{OUT} = 2.2MHz on both channels; aux-DACs ON and at midscale, aux-ADC ON		485		µA
		Standby mode: CLK = 0 or OV_{DD}; aux-DACs ON and at midscale, aux-ADC ON		1		
		Idle mode: f_{CLK} = 45MHz; aux-DACs ON and at midscale, aux-ADC ON		76		
		Shutdown mode: CLK = 0 or OV_{DD}		1		
Rx ADC DC ACCURACY						
Resolution	N			10		Bits
Integral Nonlinearity	INL			±1.6		LSB
Differential Nonlinearity	DNL			±0.7		LSB
Offset Error		Residual DC offset error	-5	±0.5	+5	%FS
Gain Error		Include reference error	-5.5	±1.0	+5.5	%FS
DC Gain Matching			-0.15	±0.01	+0.15	dB
Offset Matching				±13		LSB
Gain Temperature Coefficient				±30		ppm/°C
Power-Supply Rejection	PSRR	Offset error (V_{DD} ±5%)		±0.4		LSB
		Gain error (V_{DD} ±5%)		±0.1		%FS

10-Bit, 45Msps, Ultra-Low-Power Analog Front-End

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 45MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, unless otherwise noted. C_L < 5pF on all aux-DAC outputs. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rx ADC ANALOG INPUT						
Input Differential Range	V_{ID}	Differential or single-ended inputs		±0.512		V
Input Common-Mode Voltage Range	V_{CM}			V_{DD} / 2		V
Input Impedance	R_{IN}	Switched capacitor load		120		kΩ
	C_{IN}			5		pF
Rx ADC CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}	(Note 2)			45	MHz
Data Latency (Figure 3)		Channel I		5		Clock Cycles
		Channel Q		5.5		
Rx ADC DYNAMIC CHARACTERISTICS (Note 3)						
Signal-to-Noise Ratio	SNR	f_{IN} = 5.5MHz, f_{CLK} = 45MHz	52.5	54.2		dB
		f_{IN} = 22MHz, f_{CLK} = 45MHz		54.1		
Signal-to-Noise Plus Distortion	SINAD	f_{IN} = 5.5MHz, f_{CLK} = 45MHz	52.2	54.1		dB
		f_{IN} = 22MHz, f_{CLK} = 45MHz		54		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 5.5MHz, f_{CLK} = 45MHz	62.1	71.2		dBc
		f_{IN} = 22MHz, f_{CLK} = 45MHz		70.4		
Third-Harmonic Distortion	HD3	f_{IN} = 5.5MHz, f_{CLK} = 45MHz		-78.1		dBc
		f_{IN} = 22MHz, f_{CLK} = 45MHz		-73.1		
Intermodulation Distortion	IMD	f_1 = 1.8MHz, -7dBFS; f_2 = 1MHz, -7dBFS		-68.6		dBc
Third-Order Intermodulation Distortion	IM3	f_1 = 1.8MHz, -7dBFS; f_2 = 1MHz, -7dBFS		-79.2		dBc
Total Harmonic Distortion	THD	f_{IN} = 5.5MHz, f_{CLK} = 45MHz		-68.4	-61.5	dBc
		f_{IN} = 22MHz, f_{CLK} = 45MHz		-68.8		
Aperture Delay				3.5		ns
Overdrive Recovery Time		1.5x full-scale input		2		ns
Rx ADC INTERCHANNEL CHARACTERISTICS						
Crosstalk Rejection		$f_{INX,Y}$ = 5.5MHz at -0.5dBFS, $f_{INX,Y}$ = 1.8MHz at -0.5dBFS (Note 4)		-90		dB
Amplitude Matching		f_{IN} = 5.5MHz at -0.5dBFS (Note 5)		±0.01		dB
Phase Matching		f_{IN} = 5.5MHz at -0.5dBFS (Note 5)		±0.03		Degrees

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 45MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, unless otherwise noted. C_L < 5pF on all aux-DAC outputs. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Tx DAC DC ACCURACY							
Resolution	N				10		Bits
Integral Nonlinearity	INL				±0.3		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 6)		-1	±0.2	+1	LSB
Residual DC Offset	V_{OS}	$T_A \geq$ +25°C		-4	±1	+4	mV
		$T_A <$ +25°C		-4.5	±1	+4.5	
Full-Scale Gain Error		Include reference error (peak-to-peak error)	$T_A \geq$ +25°C	-30		+30	mV
			$T_A <$ +25°C	-40		+40	
Tx DAC DYNAMIC PERFORMANCE							
DAC Conversion Rate	f_{CLK}	(Note 2)				45	MHz
In-Band Noise Density	N_D	f_{OUT} = 2.2MHz, f_{CLK} = 45MHz			-130.6		dBc/Hz
Third-Order Intermodulation Distortion	IM3	f_1 = 2MHz, f_2 = 2.2MHz			80		dBc
Glitch Impulse					10		pV•s
Spurious-Free Dynamic Range to Nyquist	SFDR	f_{CLK} = 45MHz, f_{OUT} = 2.2MHz		60	73.2		dBc
Total Harmonic Distortion to Nyquist	THD	f_{CLK} = 45MHz, f_{OUT} = 2.2MHz			-71	-59	dB
Signal-to-Noise Ratio to Nyquist	SNR	f_{CLK} = 45MHz, f_{OUT} = 2.2MHz			57.1		dB
Tx DAC INTERCHANNEL CHARACTERISTICS							
I-to-Q Output Isolation		$f_{OUTX,Y}$ = 2MHz, $f_{OUTX,Y}$ = 2.2MHz			85		dB
Gain Mismatch Between DAC Outputs		Measured at DC	$T_A \geq$ +25°C	-0.3	±0.01	+0.3	dB
			$T_A <$ +25°C	-0.42		+0.42	
Phase Mismatch Between DAC Outputs		f_{OUT} = 2.2MHz, f_{CLK} = 45MHz			±0.07		Degrees
Differential Output Impedance					800		Ω
Tx DAC ANALOG OUTPUT							
Full-Scale Output Voltage	V_{FS}				±400		mV
Output Common-Mode Voltage	V_{COM}	Bits CM1 = 0, CM0 = 0 (default)		1.0	1.05	1.1	V
		Bits CM1 = 0, CM0 = 1			0.95		
		Bits CM1 = 1, CM0 = 0			0.80		
		Bits CM1 = 1, CM0 = 1			0.71		

10-Bit, 45Msps, Ultra-Low-Power Analog Front-End

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 45MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, unless otherwise noted. C_L < 5pF on all aux-DAC outputs. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Rx ADC–Tx DAC INTERCHANNEL CHARACTERISTICS						
Receive Transmit Isolation		ADC f_{INI} = f_{INQ} = 5.5MHz, DAC f_{OUTI} = f_{OUTQ} = 2.2MHz, f_{CLK} = 45MHz		85		dB
AUXILIARY ADC (ADC1, ADC2)						
Resolution	N			10		Bits
Full-Scale Reference	V_{REF}	AD1 = 0 (default)		2.048		V
		AD1 = 1		V_{DD}		
Analog Input Range				0 to V_{REF}		V
Analog Input Impedance		At DC		500		kΩ
Input-Leakage Current		Measured at unselected input from 0 to V_{REF}		±0.1		µA
Gain Error	GE	Includes reference error	-5		+5	%FS
Zero-Code Error	ZE			2		mV
Differential Nonlinearity	DNL			±0.53		LSB
Integral Nonlinearity	INL			±0.45		LSB
Supply Current				210		µA
AUXILIARY DACs (DAC1, DAC2, DAC3)						
Resolution	N	(Note 6)		12		Bits
Integral Nonlinearity	INL			±1.25		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic over codes 100 to 4000 (Note 6)	-1.0	±0.65	+1.1	LSB
Gain Error	GE	R_L > 200kΩ		±0.7		%FS
Zero-Code Error	ZE			±0.6		%FS
Output-Voltage Low	V_{OL}	R_L > 200kΩ			0.1	V
Output-Voltage High	V_{OH}	R_L > 200kΩ	2.56			V
DC Output Impedance		DC output at midscale		4		Ω
Settling Time		From 1/4 FS to 3/4 FS, within ±10 LSB		1		µs
Glitch Impulse		From 0 to FS transition		24		nV•s
Rx ADC–Tx DAC TIMING CHARACTERISTICS						
CLK Rise to Channel-I Output Data Valid	t_{DOI}	Figure 3 (Note 6)	5.4	6.5	8.1	ns
CLK Fall to Channel-Q Output Data Valid	t_{DOQ}	Figure 3 (Note 6)	7.3	8.8	11.1	ns
I-DAC DATA to CLK Fall Setup Time	t_{DSI}	Figure 5 (Note 6)	9			ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 45MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, unless otherwise noted. C_L < 5pF on all aux-DAC outputs. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Q-DAC DATA to CLK Rise Setup Time	t_{DSQ}	Figure 5 (Note 6)	9			ns
CLK Fall to I-DAC Data Hold Time	t_{DHI}	Figure 5 (Note 6)	-4			ns
CLK Rise to Q-DAC Data Hold Time	t_{DHQ}	Figure 5 (Note 6)	-4			ns
CLK Duty Cycle				50		%
CLK Duty-Cycle Variation				±15		%
Digital Output Rise/Fall Time		20% to 80%		2.6		ns
SERIAL-INTERFACE TIMING CHARACTERISTICS (Figure 6, Note 6)						
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time	t_{CSS}		10			ns
DIN to SCLK Setup Time	t_{DS}		10			ns
DIN to SCLK Hold Time	t_{DH}		0			ns
SCLK Pulse-Width High	t_{CH}		25			ns
SCLK Pulse-Width Low	t_{CL}		25			ns
SCLK Period	t_{CP}		50			ns
SCLK to $\overline{CS}$ Setup Time	t_{CS}		10			ns
$\overline{CS}$ High Pulse Width	t_{CSW}		80			ns
$\overline{CS}$ High to DOUT Active High	t_{CSD}	Bit AD0 set		200		ns
$\overline{CS}$ High to DOUT Low (Aux-ADC Conversion Time)	t_{CONV}	Bit AD0 set, no averaging (see Table 14), f_{CLK} = 45MHz, CLK divider = 16 (see Table 15)		4.27		µs
DOUT Low to $\overline{CS}$ Setup Time	t_{DCS}	Bit AD0, AD10 set		200		ns
SCLK Low to DOUT Data Out	t_{CD}	Bit AD0, AD10 set			14.5	ns
$\overline{CS}$ High to DOUT High Impedance	t_{CHZ}	Bit AD0, AD10 set		200		ns
MODE-RECOVERY TIMING CHARACTERISTICS (Figure 7)						
Shutdown Wake-Up Time	$t_{WAKE,SD}$	From shutdown to Rx mode, ADC settles to within 1dB SINAD		85.2		µs
		From shutdown to Tx mode, DAC settles to within 10 LSB error		28.2		
Idle Wake-Up Time (With CLK)	$t_{WAKE,ST0}$	From idle to Rx mode with CLK present during idle, ADC settles to within 1dB SINAD		9.8		µs
		From idle to Tx mode with CLK present during idle, DAC settles to 10 LSB error		6.4		
Standby Wake-Up Time	$t_{WAKE,ST1}$	From standby to Rx mode, ADC settles to within 1dB SINAD		13.7		µs
		From standby to Tx mode, DAC settles to 10 LSB error		24		

10-Bit, 45Msps, Ultra-Low-Power Analog Front-End

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 45MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, unless otherwise noted. C_L < 5pF on all aux-DAC outputs. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Enable Time from Tx to Rx, (Ext2-Tx to Ext2-Rx, Ext4-Tx to Ext4-Rx, and SPI4-Tx to SPI3-Rx States)	$t_{ENABLE, RX}$	ADC settles to within 1dB SINAD		500		ns
Enable Time from Rx to Tx, (Ext1-Rx to Ext1-Tx, Ext4-Rx to Ext4-Tx, and SPI3-Rx to SPI4-Tx States)	$t_{ENABLE, TX}$	DAC settles to within 10 LSB error		500		ns
Enable Time from Tx to Rx, (Ext1-Tx to Ext1-Rx, Ext3-Tx to Ext3-Rx, and SPI1-Tx to SPI2-Rx States)	$t_{ENABLE, RX}$	ADC settles to within 1dB SINAD		4.1		µs
Enable Time from Rx to Tx, (Ext2-Rx to Ext2-Tx, Ext3-Rx to Ext3-Tx, and SPI1-Rx to SPI2-Tx States)	$t_{ENABLE, TX}$	DAC settles to within 10 LSB error		7.0		µs
INTERNAL REFERENCE (V_{REFIN} = V_{DD}; V_{REFP}, V_{REFN}, V_{COM} levels are generated internally)						
Positive Reference		V_{REFP} - V_{COM}		0.256		V
Negative Reference		V_{REFN} - V_{COM}		-0.256		V
Common-Mode Output Voltage	V_{COM}		V_{DD} / 2 - 0.15	V_{DD} / 2	V_{DD} / 2 + 0.15	V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
Differential Reference Output	V_{REF}	V_{REFP} - V_{REFN}	+0.489	+0.512	+0.534	V
Differential Reference Temperature Coefficient	REFTC			±10		ppm/°C
BUFFERED EXTERNAL REFERENCE (external V_{REFIN} = 1.024V applied; V_{REFP}, V_{REFN}, V_{COM} levels are generated internally)						
Reference Input Voltage	V_{REFIN}			1.024		V
Differential Reference Output	V_{DIFF}	V_{REFP} - V_{REFN}		0.512		V
Common-Mode Output Voltage	V_{COM}			V_{DD} / 2		V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
REFIN Input Current				-0.7		µA
REFIN Input Resistance				500		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 45MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, unless otherwise noted. C_L < 5pF on all aux-DAC outputs. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (CLK, SCLK, DIN, $\overline{CS}$, D0–D9, T/$\overline{R}$, $\overline{SHDN}$)						
Input High Threshold	V_{INH}		0.7 x OV_{DD}			V
Input Low Threshold	V_{INL}				0.3 x OV_{DD}	V
Input Leakage	DI_{IN}	D0–D9, CLK, SCLK, DIN, $\overline{CS}$, T/$\overline{R}$, $\overline{SHDN}$ = OGND or OV_{DD}	-1		+1	µA
Input Capacitance	DC_{IN}			5		pF
DIGITAL OUTPUTS (D0–D9, DOUT)						
Output-Voltage Low	V_{OL}	I_{SINK} = 200µA			0.2 x OV_{DD}	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 200µA	0.8 x OV_{DD}			V
Tri-State Leakage Current	I_{LEAK}		-1		+1	µA
Tri-State Output Capacitance	C_{OUT}			5		pF

Note 1: Specifications from T_A = +25°C to +85°C are guaranteed by production tests. Specifications from T_A = +25°C to -40°C are guaranteed by design and characterization.

Note 2: The minimum clock frequency (f_{CLK}) for the MAX19707 is 7.5MHz (typical). The minimum aux-ADC sample rate clock frequency (ACLK) is determined by f_{CLK} and the chosen aux-ADC clock-divider value. The minimum aux-ADC ACLK > 7.5MHz / 128 = 58.6kHz. The aux-ADC conversion time does not include the time to clock the serial data out of the SPI™. The maximum conversion time (for no averaging, NAVG = 1) will be, t_{CONV} (max) = (12 x 1 x 128) / 7.5MHz = 205µs.

Note 3: SNR, SINAD, SFDR, HD3, and THD are based on a differential analog input voltage of -0.5dBFS referenced to the amplitude of the digital outputs. SINAD and THD are calculated using HD2 through HD6.

Note 4: Crosstalk rejection is measured by applying a high-frequency test tone to one channel and a low-frequency tone to the second channel. FFTs are performed on each channel. The parameter is specified as the power ratio of the first and second channel FFT test tone.

Note 5: Amplitude and phase matching is measured by applying the same signal to each channel, and comparing the two output signals using a sine-wave fit.

Note 6: Guaranteed by design and characterization.

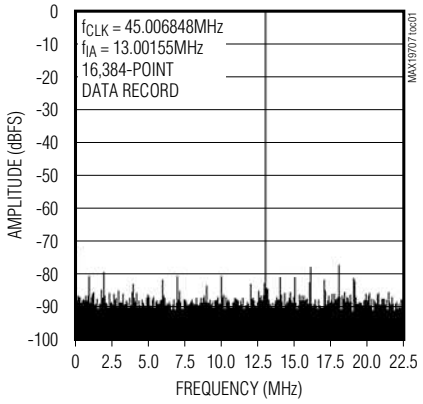
SPI is a trademark of Motorola, Inc.

10-Bit, 45Msps, Ultra-Low-Power Analog Front-End

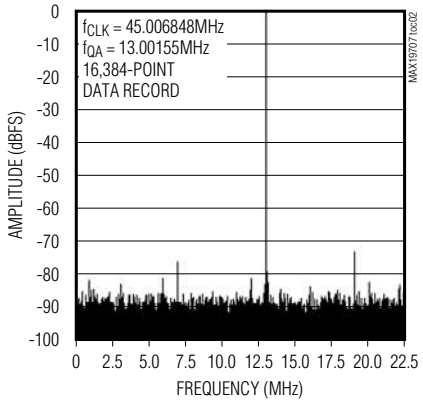
Typical Operating Characteristics

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 45MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, differential Rx ADC input, differential Tx DAC output, $C_{REFP} = C_{REFN} = C_{COM}$ = 0.33µF, T_A = +25°C, unless otherwise noted.)

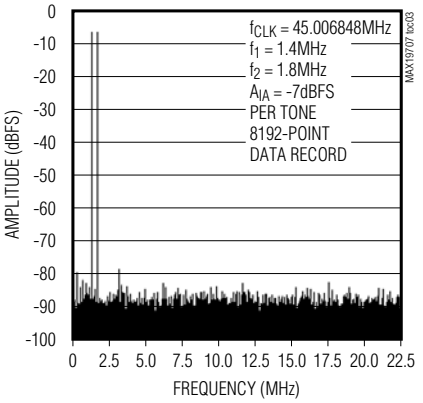
Rx ADC CHANNEL-IA FFT PLOT



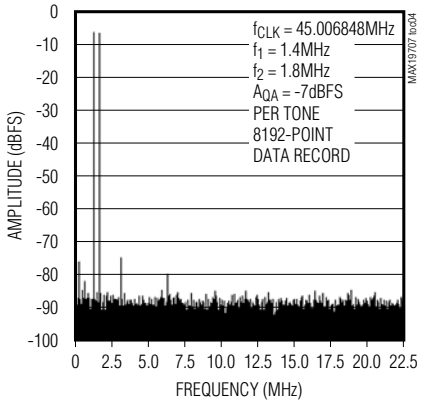
Rx ADC CHANNEL-QA FFT PLOT



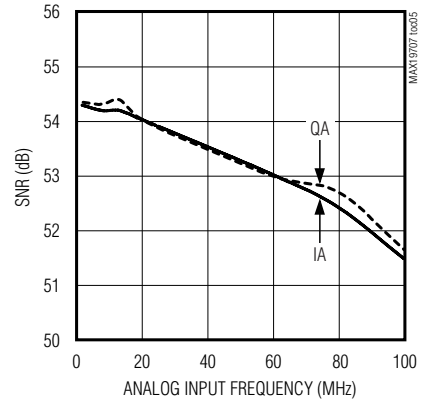
Rx ADC CHANNEL-IA TWO-TONE FFT PLOT



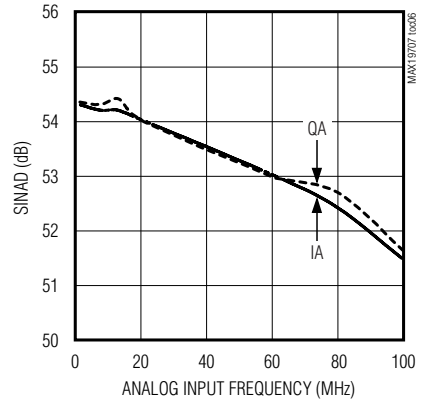
Rx ADC CHANNEL-QA TWO-TONE FFT PLOT



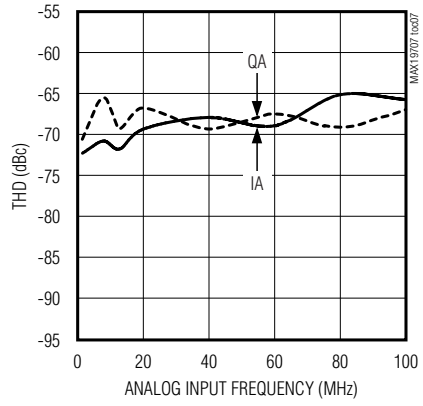
Rx ADC SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY



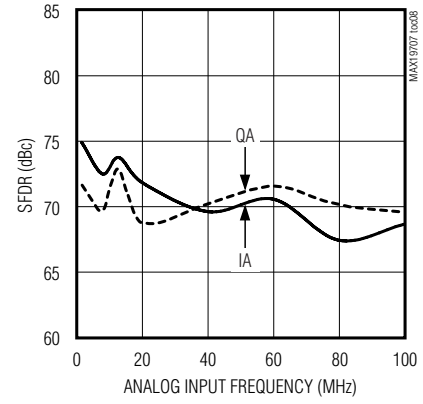
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. ANALOG INPUT FREQUENCY



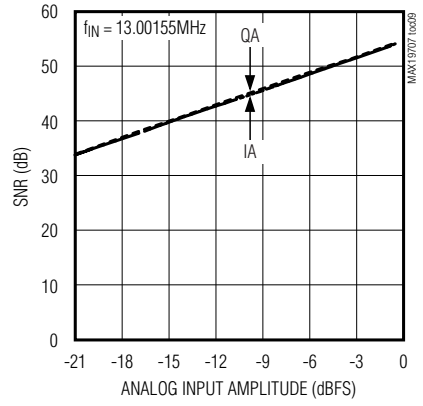
Rx ADC TOTAL HARMONIC DISTORTION vs. ANALOG INPUT FREQUENCY



Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY



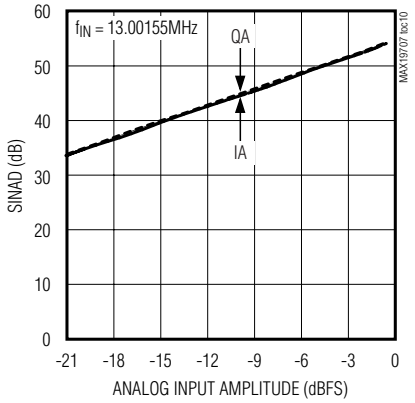
Rx ADC SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT AMPLITUDE



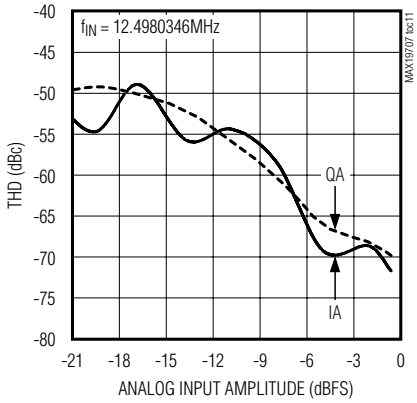
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 45MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

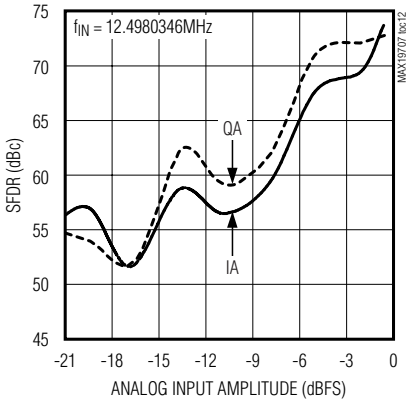
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. ANALOG INPUT AMPLITUDE



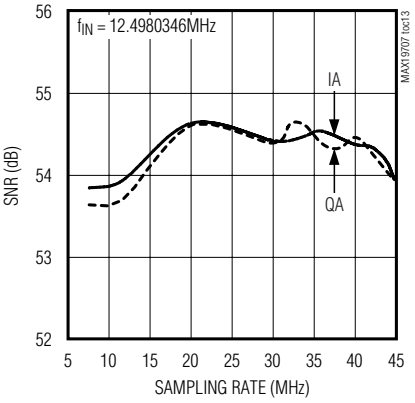
Rx ADC TOTAL HARMONIC DISTORTION vs. ANALOG INPUT AMPLITUDE



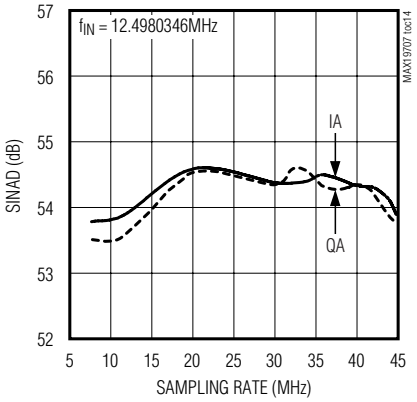
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT AMPLITUDE



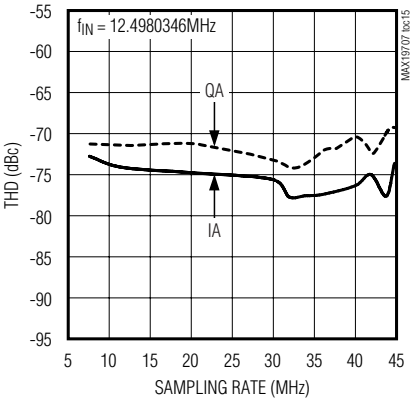
Rx ADC SIGNAL-TO-NOISE RATIO vs. SAMPLING RATE



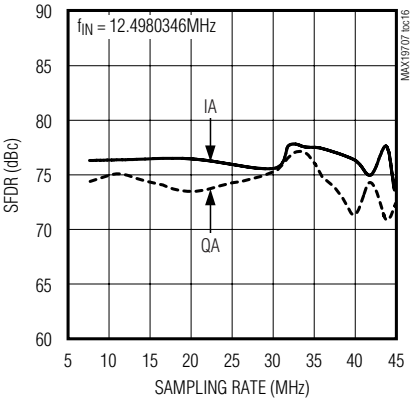
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. SAMPLING RATE



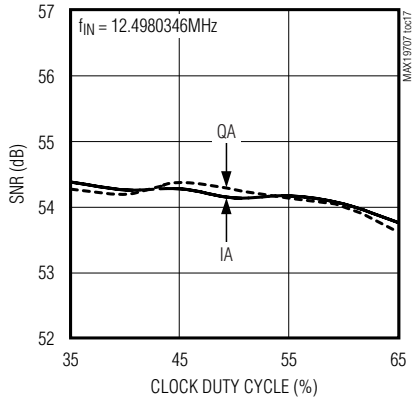
Rx ADC TOTAL HARMONIC DISTORTION vs. SAMPLING RATE



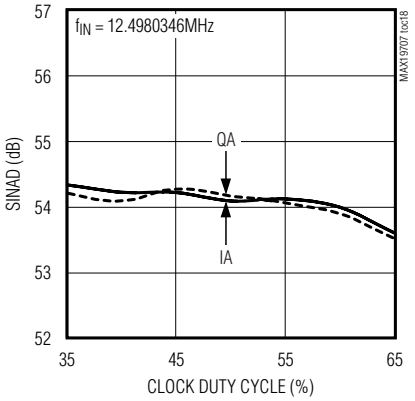
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE



Rx ADC SIGNAL-TO-NOISE RATIO vs. CLOCK DUTY CYCLE



Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. CLOCK DUTY CYCLE



10-Bit, 45Msps, Ultra-Low-Power Analog Front-End

Typical Operating Characteristics (continued)

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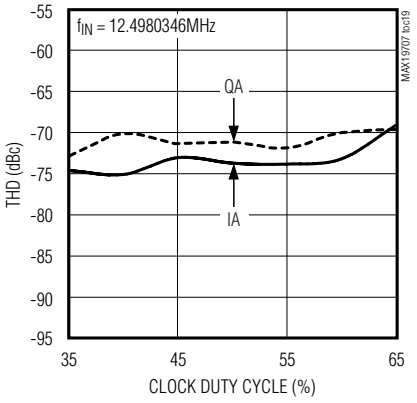
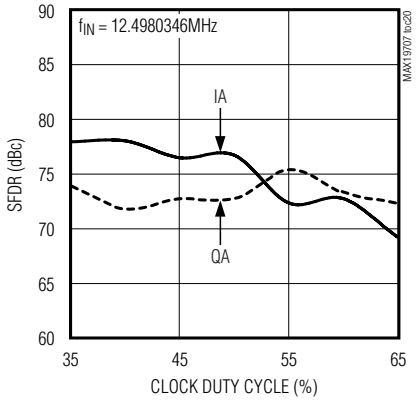
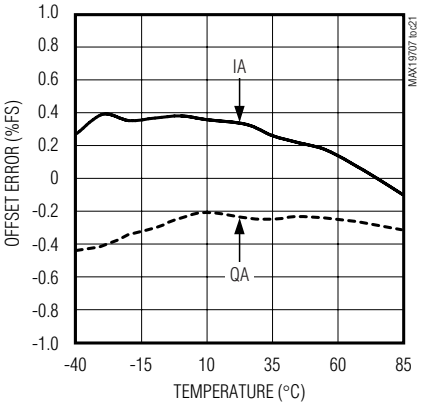
Rx ADC TOTAL HARMONIC DISTORTION vs. CLOCK DUTY CYCLE



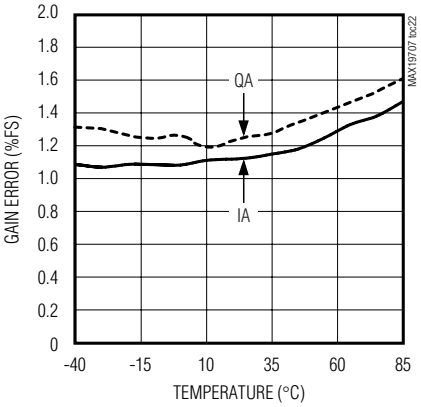
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK DUTY CYCLE



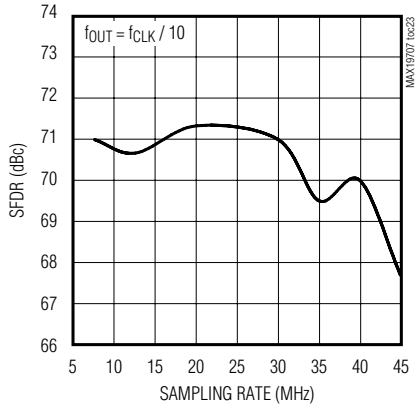
Rx ADC OFFSET ERROR vs. TEMPERATURE



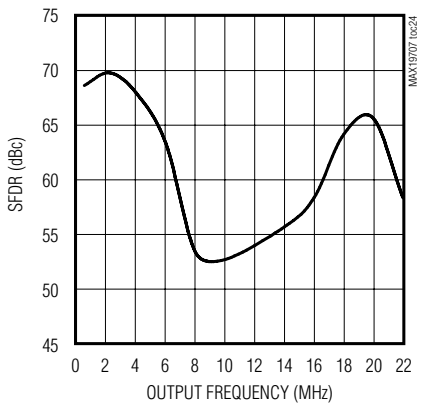
Rx ADC GAIN ERROR vs. TEMPERATURE



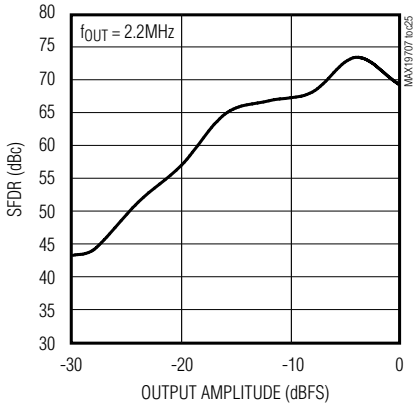
Tx DAC SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING RATE



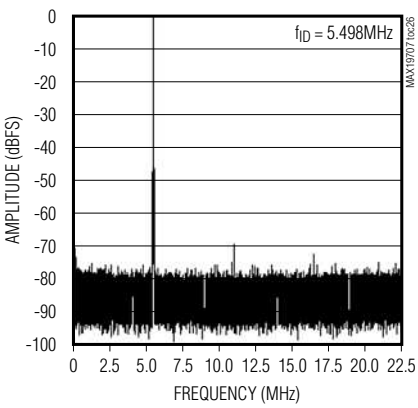
Tx DAC SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY



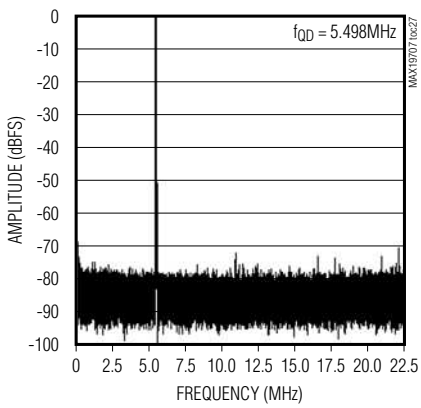
Tx DAC SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT AMPLITUDE



Tx DAC CHANNEL-ID SPECTRAL PLOT



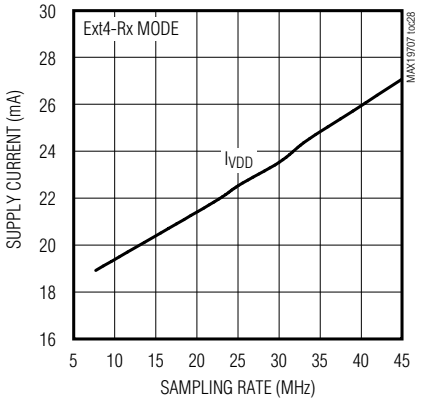
Tx DAC CHANNEL-QD SPECTRAL PLOT



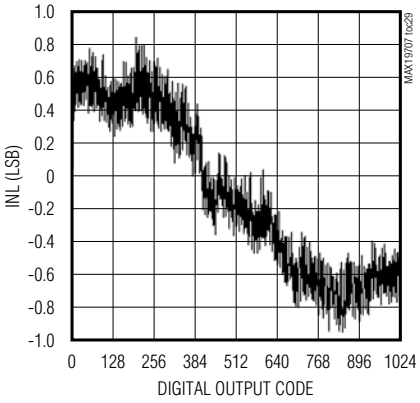
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 45MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

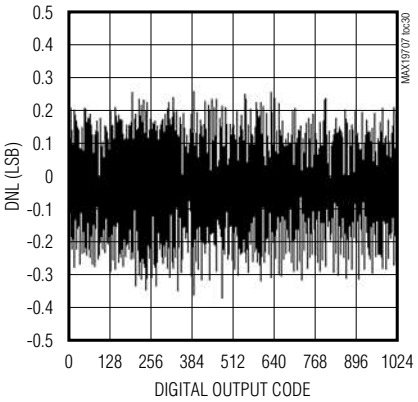
SUPPLY CURRENT vs. SAMPLING RATE



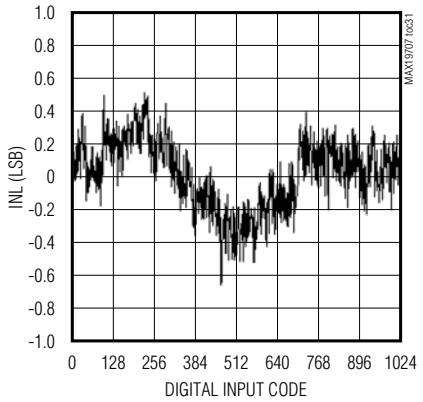
Rx ADC INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



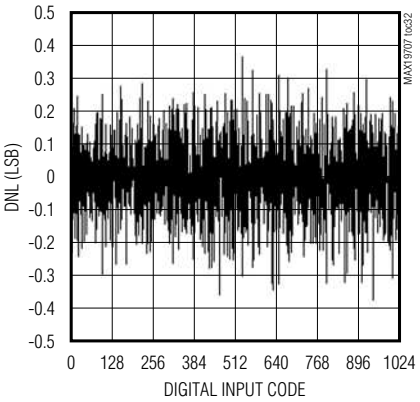
Rx ADC DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



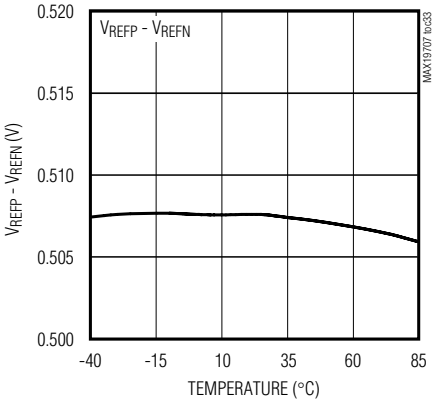
Tx DAC INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



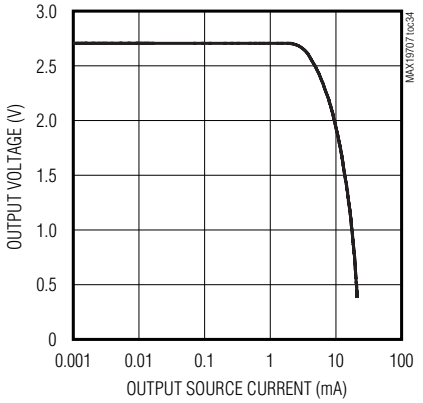
Tx DAC DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



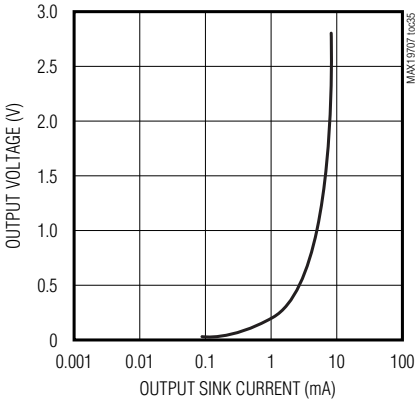
REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



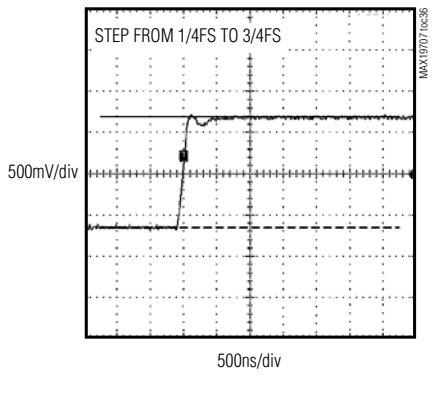
AUX-DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



AUX-DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



AUX-DAC SETTLING TIME



10-Bit, 45Msps, Ultra-Low-Power Analog Front-End

Typical Operating Characteristics (continued)

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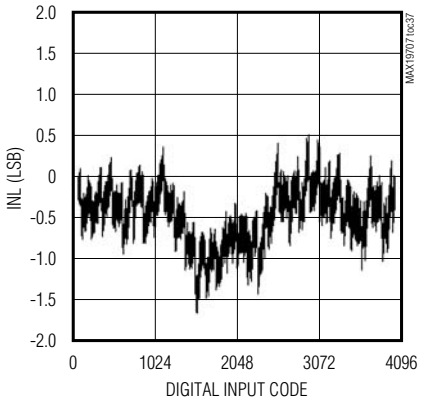
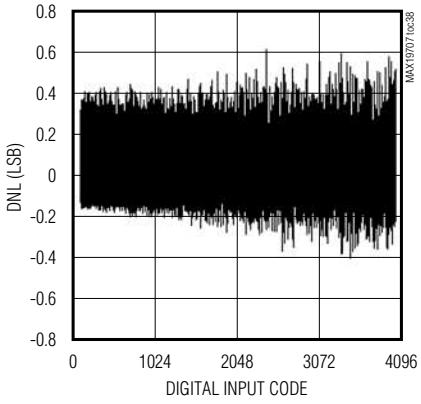
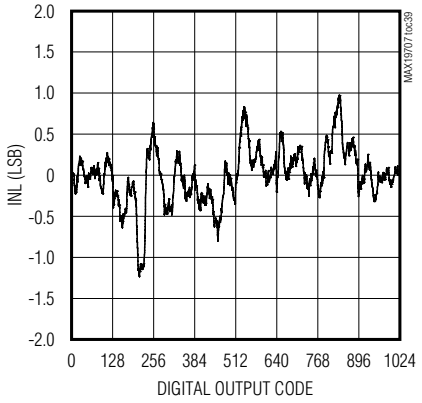
AUX-DAC INTEGRAL NONLINEARITY vs. DIGITAL INPUT CODE



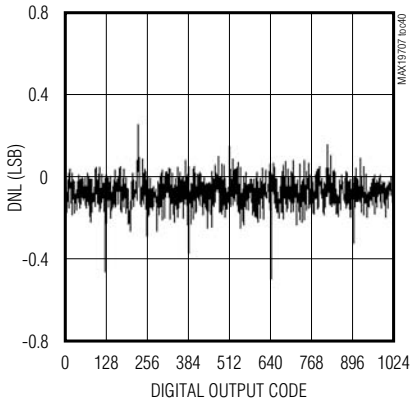
AUX-DAC DIFFERENTIAL NONLINEARITY vs. DIGITAL INPUT CODE



AUX-ADC INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



AUX-ADC DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



Pin Description

PIN	NAME	FUNCTION
1	REFP	Upper Reference Voltage. Bypass with a 0.33µF capacitor to GND as close to REFP as possible.
2, 8, 11, 31, 33, 39, 43	V_{DD}	Analog Supply Voltage. Supply range from 2.7V to 3.3V. Bypass V_{DD} to GND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
3	IAP	Channel-IA Positive Analog Input. For single-ended operation, connect signal source to IAP.
4	IAN	Channel-IA Negative Analog Input. For single-ended operation, connect IAN to COM.
5, 7, 12, 32, 42	GND	Analog Ground. Connect all GND pins to ground plane.
6	CLK	Conversion Clock Input. Clock signal for both receive ADCs and transmit DACs.
9	QAN	Channel-QA Negative Analog Input. For single-ended operation, connect QAN to COM.

Pin Description (continued)

PIN	NAME	FUNCTION
10	QAP	Channel-QA Positive Analog Input. For single-ended operation, connect signal source to QAP.
13–18, 21–24	D0–D9	Digital I/O. Outputs for receive ADC in Rx mode. Inputs for transmit DAC in Tx mode. D9 is the most significant bit (MSB) and D0 is the least significant bit (LSB).
19	OGND	Output-Driver Ground
20	OV_{DD}	Output-Driver Power Supply. Supply range from 1.8V to V_{DD}. Bypass OV_{DD} to OGND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
25	$\overline{SHDN}$	Active-Low Shutdown Input. Apply logic-low to place the MAX19707 in shutdown.
26	DOUT	Aux-ADC Digital Output
27	T/$\overline{R}$	Transmit- or Receive-Mode Select Input. T/$\overline{R}$ logic-low input sets the device in receive mode. A logic-high input sets the device in transmit mode.
28	DIN	3-Wire Serial-Interface Data Input. Data is latched on the rising edge of the SCLK.
29	SCLK	3-Wire Serial-Interface Clock Input
30	$\overline{CS}$	3-Wire Serial-Interface Chip-Select Input. Logic-low enables the serial interface.
34	ADC2	Analog Input for Auxiliary ADC
35	ADC1	Analog Input for Auxiliary ADC
36	DAC3	Analog Output for Auxiliary DAC3
37	DAC2	Analog Output for Auxiliary DAC2
38	DAC1	Analog Output for Auxiliary DAC1 (AFC DAC, V_{OUT} = 1.1V During Power-Up)
40, 41	IDN, IDP	DAC Channel-ID Differential Voltage Output
44, 45	QDN, QDP	DAC Channel-QD Differential Voltage Output
46	REFIN	Reference Input. Connect to V_{DD} for internal reference. Bypass to GND with a 0.1µF capacitor.
47	COM	Common-Mode Voltage I/O. Bypass COM to GND with a 0.33µF capacitor.
48	REFN	Negative Reference I/O. Rx ADC conversion range is ±(V_{REFP} - V_{REFN}). Bypass REFN to GND with a 0.33µF capacitor.
—	EP	Exposed Paddle. Exposed paddle is internally connected to GND. Connect EP to the GND plane.

Detailed Description

The MAX19707 integrates a dual, 10-bit Rx ADC and a dual, 10-bit Tx DAC while providing ultra-low power and high dynamic performance at a 45Msps conversion rate. The Rx ADC analog input amplifiers are fully differential and accept $1.024V_{P-P}$ full-scale signals. The Tx DAC analog outputs are fully differential with ±400mV full-scale output, selectable common-mode DC level, and adjustable I/Q offset trim.

The MAX19707 integrates three 12-bit auxiliary DAC (aux-DAC) channels and a 10-bit, 333ksps auxiliary ADC (aux-ADC) with 4:1 input multiplexer. The aux-DAC channels feature 1µs settling time for fast automatic gain-control (AGC), variable-gain amplifier (VGA), and automatic frequency-control (AFC) level setting. The aux-ADC features data averaging to reduce processor overhead and a selectable clock-divider to program the conversion rate.

The MAX19707 includes a 3-wire serial interface to control operating modes and power management. The serial interface is SPI and MICROWIRE™ compatible. The MAX19707 serial interface selects shutdown, idle, standby, transmit (Tx), and receive (Rx) modes, as well as controls aux-DAC and aux-ADC channels.

The Rx ADC and Tx DAC share a common digital I/O to reduce the digital interface to a single, 10-bit parallel multiplexed bus. The 10-bit digital bus operates on a single 1.8V to 3.3V supply.

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Dual, 10-Bit Rx ADC

The ADC uses a seven-stage, fully differential, pipelined architecture that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half clock cycle. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for channel IA and 5.5 clock cycles for channel QA. The ADC full-scale analog input range is $\pm V_{REF}$ with a V_{DD} / 2 ±0.2V common-mode input range. V_{REF} is the difference between V_{REFP} and V_{REFN}. See the *Reference Configurations* section for details.

Input Track-and-Hold (T/H) Circuits

Figure 1 displays a simplified diagram of the Rx ADC input track-and-hold (T/H) circuitry. Both ADC inputs (IAP, QAP, IAN, and QAN) can be driven either differentially or single-ended. Match the impedance of IAP and IAN, as well as QAP and QAN, and set the input signal common-mode voltage within the Rx ADC range of $V_{DD}/2$ (±200mV) for optimum performance.

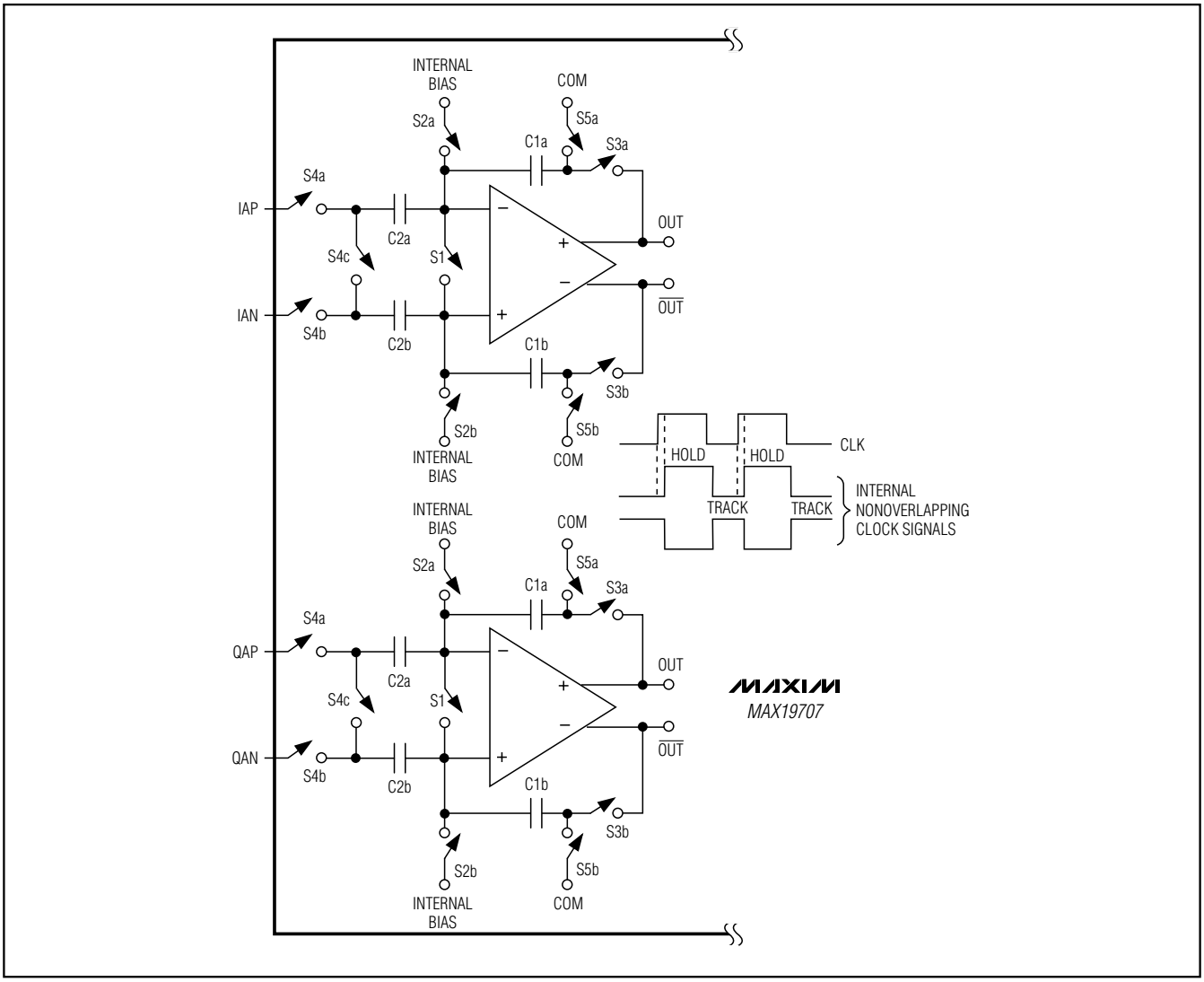

Figure 1. Rx ADC Internal T/H Circuits

Table 1. Rx ADC Output Codes vs. Input Voltage

DIFFERENTIAL INPUT VOLTAGE	DIFFERENTIAL INPUT (LSB)	OFFSET BINARY (D0–D9)	OUTPUT DECIMAL CODE
V_{REF} x 512/512	511 (+Full Scale - 1 LSB)	11 1111 1111	1023
V_{REF} x 511/512	510 (+Full Scale - 2 LSB)	11 1111 1110	1022
V_{REF} x 1/512	+1	10 0000 0001	513
V_{REF} x 0/512	0 (Bipolar Zero)	10 0000 0000	512
-V_{REF} x 1/512	-1	01 1111 1111	511
-V_{REF} x 511/512	-511 (-Full Scale +1 LSB)	00 0000 0001	1
-V_{REF} x 512/512	-512 (-Full Scale)	00 0000 0000	0

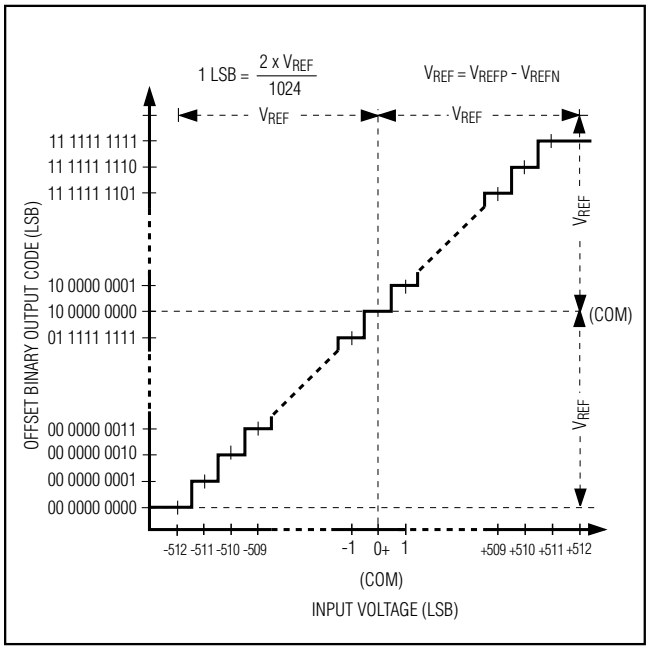

Figure 2. Rx ADC Transfer Function

Rx ADC System Timing Requirements

Figure 3 shows the relationship between the clock, analog inputs, and the resulting output data. Channel I (CHI) and channel Q (CHQ) are sampled on the rising edge of the clock signal (CLK) and the resulting data is multiplexed at the D0–D9 outputs. CHI data is updated on the rising edge and CHQ data is updated on the falling edge of the CLK. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for CHI and 5.5 clock cycles for CHQ.

Digital Input/Output Data (D0–D9)

D0–D9 are the Rx ADC digital logic outputs when the MAX19707 is in receive mode. This bus is shared with the Tx DAC digital logic inputs and operates in half-duplex mode. D0–D9 are the Tx DAC digital logic inputs when the MAX19707 is in transmit mode. The logic level is set by OV_{DD} from 1.8V to V_{DD}. The digital output coding is offset binary (Table 1). Keep the capacitive load on the digital outputs D0–D9 as low as possible (< 15pF) to avoid large digital currents feeding back into the analog portion of the MAX19707 and degrading its dynamic performance. Buffers on the digital outputs isolate the outputs from heavy capacitive loads. Adding 100Ω resistors in series with the digital outputs close to the MAX19707 helps improve Rx ADC and Tx DAC performance. Refer to the MAX19707EVKIT schematic for an example of the digital outputs driving a digital buffer through 100Ω series resistors.

During SHDN, IDLE, and STBY states, D0–D9 are internally pulled up to prevent floating digital inputs. To ensure no current flows through D0–D9 I/O, the external bus needs to be either tri-stated or pulled up to OV_{DD} and should not be pulled to ground.

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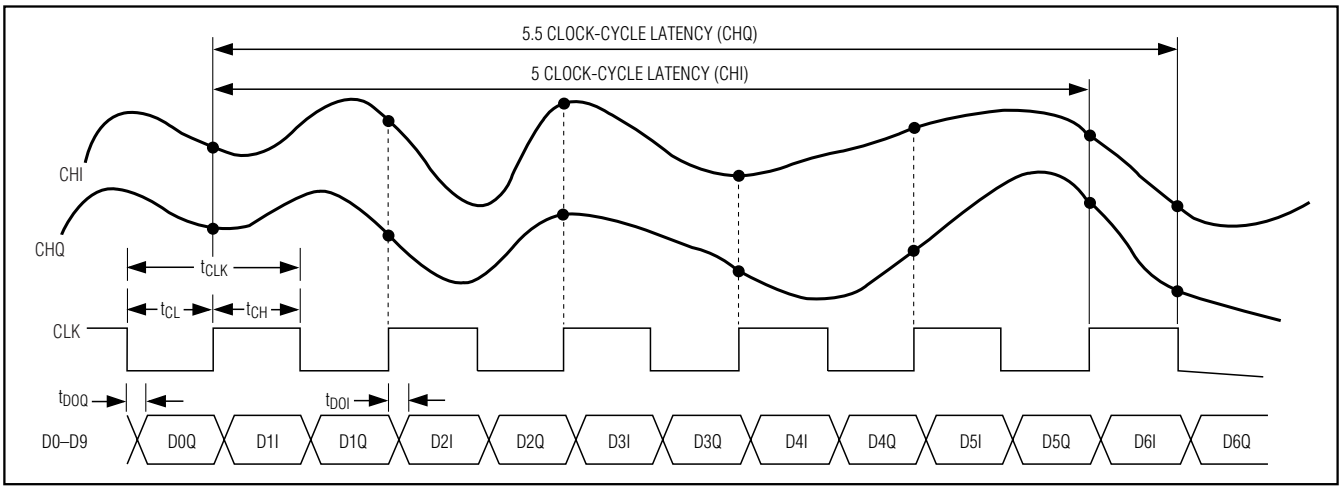

Figure 3. Rx ADC System Timing Diagram

Dual, 10-Bit Tx DAC

The dual, 10-bit digital-to-analog converter (Tx DAC) operates with clock speeds up to 45MHz. The Tx DAC digital inputs, D0–D9, are multiplexed on a single 10-bit bus. The voltage reference determines the Tx DAC full-scale output voltage. See the *Reference Configurations* section for details on setting the reference voltage.

The Tx DAC outputs at IDN, IDP and QDN, QDP are biased at a 0.7V to 1.05V adjustable DC common-mode bias and designed to drive a differential input stage with ≥ 70kΩ input impedance. This simplifies the analog interface between RF quadrature upconverters and the MAX19707. Many RF upconverters require a 0.7V to 1.05V common-mode bias. The Tx DAC DC common-mode bias eliminates discrete level-setting resistors and code-generated level shifting while preserving the full dynamic range of each Tx DAC. The Tx DAC differential analog outputs cannot be used in single-ended mode because of the internally generated common-mode DC level. Table 2 shows the Tx DAC output voltage vs. input codes. Table 10 shows the selection of DC common-mode levels. See Figure 4 for an illustration of the Tx DAC analog output levels.

Table 2. Tx DAC Output Voltage vs. Input Codes

(Internal Reference Mode V_{REFDAC} = 1.024V, External Reference Mode V_{REFDAC} = V_{REFIN}; V_{FS} = ±400 for 800mV_{P-P} Full Scale)

DIFFERENTIAL OUTPUT VOLTAGE (V)	OFFSET BINARY (D0–D9)	INPUT DECIMAL CODE
$(V_{FS})\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	11 1111 1111	1023
$(V_{FS})\frac{V_{REFDAC}}{1024} \times \frac{1021}{1023}$	11 1111 1110	1022
$(V_{FS})\frac{V_{REFDAC}}{1024} \times \frac{3}{1023}$	10 0000 0001	513
$(V_{FS})\frac{V_{REFDAC}}{1024} \times \frac{1}{1023}$	10 0000 0000	512
$(V_{FS})\frac{-V_{REFDAC}}{1024} \times \frac{1}{1023}$	01 1111 1111	511
$(V_{FS})\frac{-V_{REFDAC}}{1024} \times \frac{1021}{1023}$	00 0000 0001	1
$(V_{FS})\frac{-V_{REFDAC}}{1024} \times \frac{1023}{1023}$	00 0000 0000	0

The Tx DAC also features independent DC offset correction of each I/Q channel. This feature is configured through the SPI interface. The DC offset correction is used to optimize sideband and carrier suppression in the Tx signal path (see Table 9).

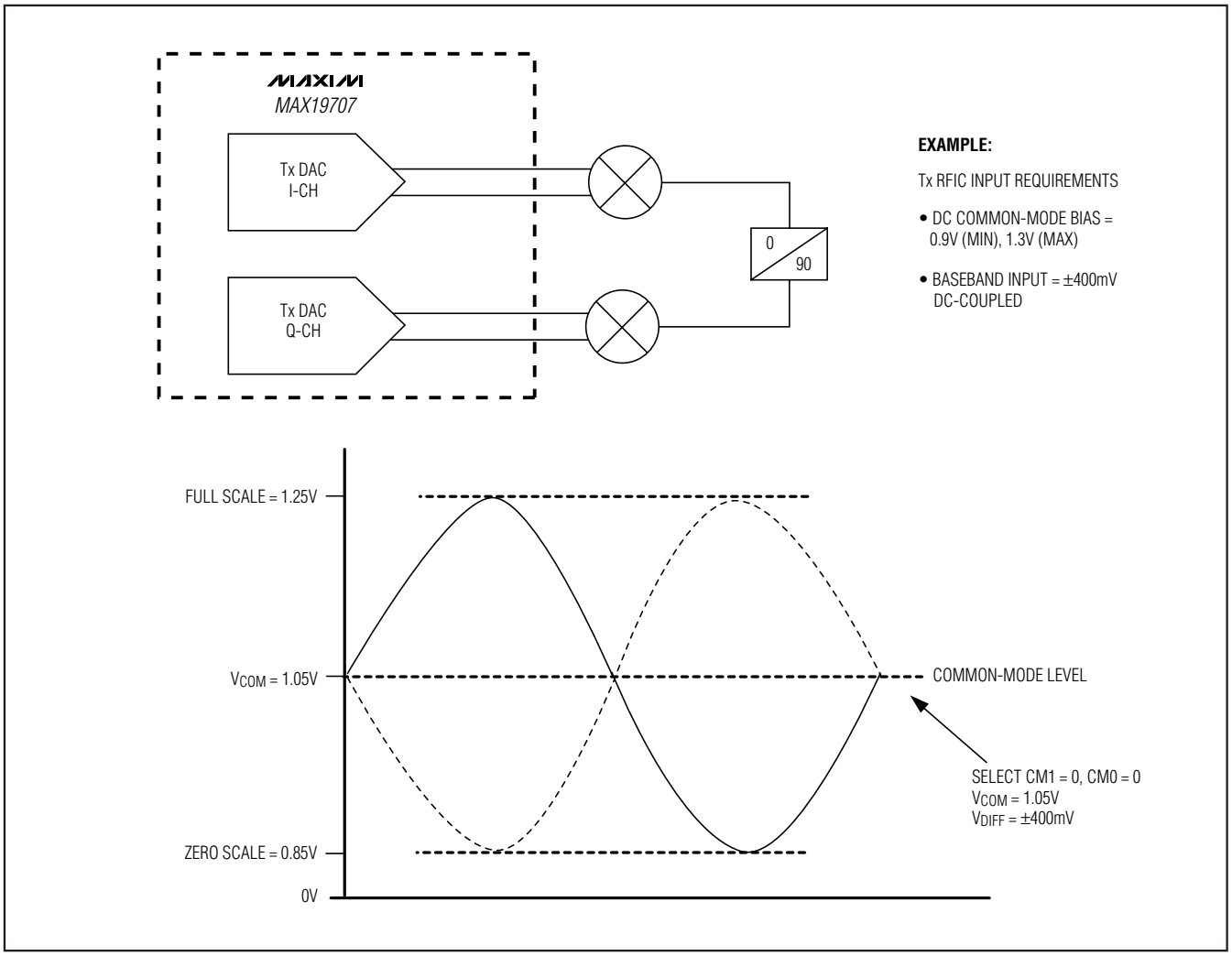

Figure 4. Tx DAC Common-Mode DC Level at IDN, IDP or QDN, QDP Differential Outputs

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Tx DAC Timing

Figure 5 shows the relationship between the clock, input data, and analog outputs. Data for the I channel (ID) is latched on the falling edge of the clock signal, and Q-channel (QD) data is latched on the rising edge of the clock signal. Both I and Q outputs are simultaneously updated on the next rising edge of the clock signal.

3-Wire Serial Interface and Operation Modes

The 3-wire serial interface controls the MAX19707 operation modes as well as the three 12-bit aux-DACs and the 10-bit aux-ADC. Upon power-up, program the MAX19707 to operate in the desired mode. Use the 3-wire serial interface to program the device for shutdown, idle, standby, Rx, Tx, aux-DAC controls, or aux-ADC conversion. A 16-bit data register sets the mode control as shown in Table 3. The 16-bit word is composed of A3–A0 control bits and D11–D0 data bits. Data is shifted in MSB first (D11) and LSB last (A0). Tables 4, 5, and 6 show the MAX19707 operating modes and SPI commands. The serial interface remains active in all modes.

SPI Register Description

Program the control bits, A3–A0, in the register as shown in Table 3 to select the operating mode. Modify A3–A0 bits to select from ENABLE-16, Aux-DAC1, Aux-DAC2, Aux-DAC3, IOFFSET, QOFFSET, Aux-ADC, ENABLE-8, and COMSEL modes. ENABLE-16 is the default operating mode. This mode allows for shutdown, idle, and standby states as well as switching between FAST, SLOW, Rx, and Tx modes. Table 4 shows the MAX19707 power-management modes. Table 5 shows the T/$\overline{R}$ pin-controlled external Tx-Rx switching modes. Table 6 shows the SPI-controlled Tx-Rx switching modes.

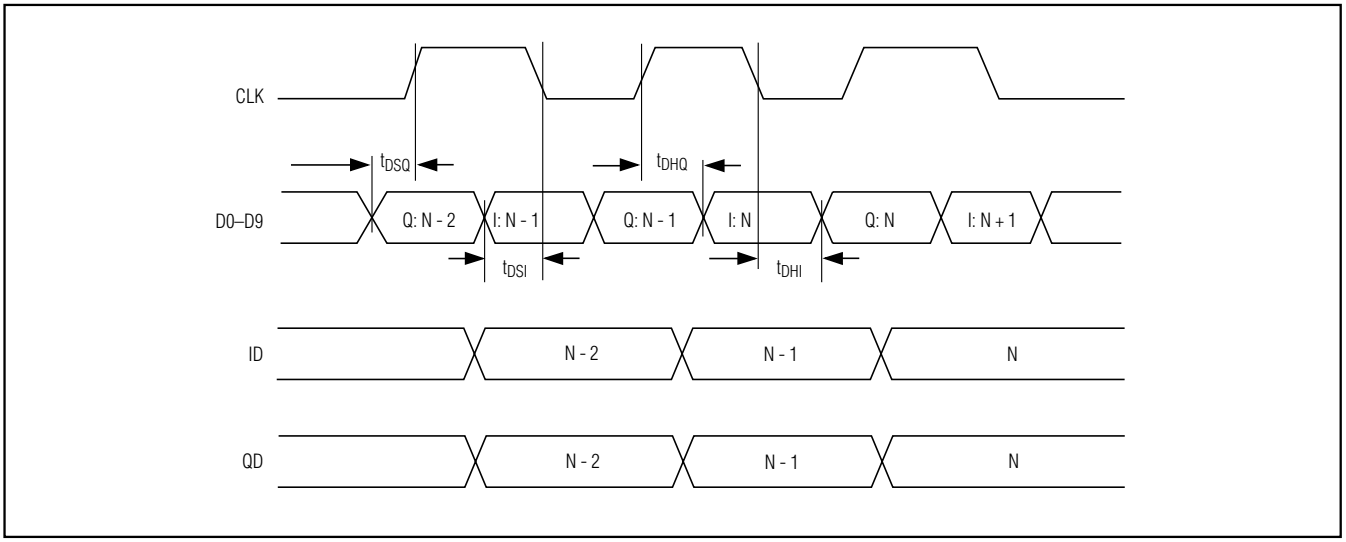

Figure 5. Tx DAC System Timing Diagram

Table 3. MAX19707 Mode Control

REGISTER NAME	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0
	(MSB)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (LSB)
ENABLE-16	E11 = 0 Reserved	E10 = 0 Reserved	E9	—	—	E6	E5	E4	E3	E2	E1	E0	0	0	0	0
Aux-DAC1	1D11	1D10	1D9	1D8	1D7	1D6	1D5	1D4	1D3	1D2	1D1	1D0	0	0	0	1
Aux-DAC2	2D11	2D10	2D9	2D8	2D7	2D6	2D5	2D4	2D3	2D2	2D1	2D0	0	0	1	0
Aux-DAC3	3D11	3D10	3D9	3D8	3D7	3D6	3D5	3D4	3D3	3D2	3D1	3D0	0	0	1	1
IOFFSET	—	—	—	—	—	—	IO5	IO4	IO3	IO2	IO1	IO0	0	1	0	0
QOFFSET	—	—	—	—	—	—	QO5	QO4	QO3	QO2	QO1	QO0	0	1	0	1
COMSEL	—	—	—	—	—	—	—	—	—	—	CM1	CM0	0	1	1	0
Aux-ADC	AD11 = 0 Reserved	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	0	1	1	1
ENABLE-8	—	—	—	—	—	—	—	—	E3	E2	E1	E0	1	0	0	0

— = Not used.

Table 4. Power-Management Modes

ADDRESS				DATA BITS					T/$\overline{R}$	MODE	FUNCTION (POWER MANAGEMENT)	DESCRIPTION	COMMENT
A3	A2	A1	A0	E9*	E3	E2	E1	E0	PIN 27				
0000 (16-Bit Mode) or 1000 (8-Bit Mode)				1X000					X	SHDN	SHUTDOWN	Rx ADC = OFF Tx DAC = OFF Aux-DAC = OFF Aux-ADC = OFF CLK = OFF REF = OFF	Device is in complete shutdown. Overrides T/$\overline{R}$ pin.
				XX001					X	IDLE	IDLE	Rx ADC = OFF Tx DAC = OFF Aux-DAC = Last State CLK = ON REF = ON	Fast turn-on time. Moderate idle power. Overrides T/$\overline{R}$ pin.
				1X010					X	STBY	STANDBY	Rx ADC = OFF Tx DAC = OFF Aux-DAC = Last State Aux-ADC = OFF CLK = OFF REF = ON	Slow turn-on time. Low standby power. Overrides T/$\overline{R}$ pin.

X = Don't care.

**Bit E9 is not available in 8-bit mode.*

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Table 5. External Tx-Rx Control Using T/$\overline{R}$ Pin (T/$\overline{R}$ = 0 = Rx Mode, T/$\overline{R}$ = 1 = Tx Mode)

ADDRESS				DATA BITS				T/$\overline{R}$	STATE	FUNCTION Rx TO Tx-Tx TO Rx SWITCHING SPEED	DESCRIPTION	COMMENT
A3	A2	A1	A0	E3	E2	E1	E0	PIN 27				
0000 (16-Bit Mode) or 1000 (8-Bit Mode)				0011				0	Ext1-Rx	FAST-SLOW	Rx Mode: Rx ADC = ON Tx DAC = ON Rx Bus = Enable	Moderate Power: Fast Rx to Tx when T/$\overline{R}$ transitions 0 to 1.
								1	Ext1-Tx		Tx Mode: Rx ADC = OFF Tx DAC = ON Tx Bus = Enable	Low Power: Slow Tx to Rx when T/$\overline{R}$ transitions 1 to 0.
				0100				0	Ext2-Rx (Default)	SLOW-FAST	Rx Mode: Rx ADC = ON Tx DAC = OFF Rx Bus = Enable	Low Power: Slow Rx to Tx when T/$\overline{R}$ transitions 0 to 1.
								1	Ext2-Tx		Tx Mode: Rx ADC = ON Tx DAC = ON Tx Bus = Enable	Moderate Power: Fast Tx to Rx when T/$\overline{R}$ transitions 1 to 0.
				0101				0	Ext3-Rx	SLOW-SLOW	Rx Mode: Rx ADC = ON Tx DAC = OFF Rx Bus = Enable	Low Power: Slow Rx to Tx when T/$\overline{R}$ transitions 0 to 1.
								1	Ext3-Tx		Tx Mode: Rx ADC = OFF Tx DAC = ON Tx Bus = Enable	Low Power: Slow Tx to Rx when T/$\overline{R}$ transitions 1 to 0.
				0110				0	Ext4-Rx	FAST-FAST	Rx Mode: Rx ADC = ON Tx DAC = ON Rx Bus = Enable	Moderate Power: Fast Rx to Tx when T/$\overline{R}$ transitions 0 to 1.
								1	Ext4-Tx		Tx Mode: Rx ADC = ON Tx DAC = ON Tx Bus = Enable	Moderate Power: Fast Tx to Rx when T/$\overline{R}$ transitions 1 to 0.

Table 6. Tx-Rx Control Using SPI Commands

ADDRESS				DATA BITS				T/$\overline{R}$	MODE	FUNCTION (Tx-Rx SWITCHING SPEED)	DESCRIPTION	COMMENTS
A3	A2	A1	A0	E3	E2	E1	E0	PIN 27				
0000 (16-Bit Mode) or 1000 (8-Bit Mode)				1011				X	SPI1-Rx	SLOW	Rx Mode: Rx ADC = ON Tx DAC = OFF Rx Bus = Enable	Low Power: Slow Rx to Tx through SPI command.
				1100				X	SPI2-Tx	SLOW	Tx Mode: Rx ADC = OFF Tx DAC = ON Tx Bus = Enable	Low Power: Slow Tx to Rx through SPI command.
				1101				X	SPI3-Rx	FAST	Rx Mode: Rx ADC = ON Tx DAC = ON Rx Bus = Enabled	Moderate Power: Fast Rx to Tx through SPI command.
				1110				X	SPI4-Tx	FAST	Tx Mode: Rx ADC = ON Tx DAC = ON Tx Bus = Enabled	Moderate Power: Fast Tx to Rx through SPI command.

X = Don't care.

In ENABLE-16 mode, the aux-DACs have independent control bits E4, E5, and E6, and bit E9 enables the aux-ADC. Table 7 shows the auxiliary DAC enable codes and Table 8 shows the auxiliary ADC enable codes. Bits E11 and E10 are reserved. Program bits E11 and E10 to logic-low.

Modes aux-DAC1, aux-DAC2, and aux-DAC3 select the aux-DAC channels named DAC1, DAC2, and DAC3 and hold the data inputs for each DAC. Bits _D11–_D0 are the data inputs for each aux-DAC and can be programmed through SPI. The MAX19707 also includes two 6-bit registers that can be programmed to adjust the offsets for the Tx DAC I and Q channels independently (see Table 9). Use the COMSEL mode to select the output common-mode voltage with bits CM1 and CM0 (see Table 10). Use Aux-ADC mode to start the auxiliary ADC conversion (see the *10-Bit, 333ksps Auxiliary ADC* section for details). Use ENABLE-8 mode for faster enable and switching between shutdown, idle, and standby states as well as switching between FAST, SLOW, and Rx and Tx modes.

Table 7. Aux-DAC Enable Table (ENABLE-16 Mode)

E6	E5	E4	AUX-DAC3	AUX-DAC2	AUX-DAC1
0	0	0	ON	ON	ON
0	0	1	ON	ON	OFF
0	1	0	ON	OFF	ON
0	1	1	ON	OFF	OFF
1	0	0	OFF	ON	ON
1	0	1	OFF	ON	OFF
1	1	0	OFF	OFF	ON
1	1	1	OFF	OFF	OFF

Table 8. Aux-ADC Enable Table (ENABLE-16 Mode)

E9	SELECTION
0 (Default)	Aux-ADC is Powered ON
1	Aux-ADC is Powered OFF

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Table 9. Offset Control Bits for I and Q Channels (IOFFSET or QOFFSET Mode)

BITS IO5–IO0 WHEN IN IOFFSET MODE, BITS QO5–QO0 WHEN IN QOFFSET MODE						OFFSET 1 LSB = (VFS_{P-P} / 1023)
IO5/QO5	IO4/QO4	IO3/QO3	IO2/QO2	IO1/QO1	IO0/QO0	
1	1	1	1	1	1	-31 LSB
1	1	1	1	1	0	-30 LSB
1	1	1	1	0	1	-29 LSB
• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	0	0	0	1	0	-2 LSB
1	0	0	0	0	1	-1 LSB
1	0	0	0	0	0	0mV
0	0	0	0	0	0	0mV (Default)
0	0	0	0	0	1	1 LSB
0	0	0	0	1	0	2 LSB
• • •	• • •	• • •	• • •	• • •	• • •	• • •
0	1	1	1	0	1	29 LSB
0	1	1	1	1	0	30 LSB
0	1	1	1	1	1	31 LSB

Note: *For transmit full-scale of ±400mV: 1 LSB = ($800mV_{P-P}$ / 1023) = 0.7820mV.*

Table 10. Common-Mode Select (COMSEL Mode)

CM1	CM0	Tx DAC OUTPUT COMMON MODE (V)
0	0	1.05 (Default)
0	1	0.95
1	0	0.80
1	1	0.70

Shutdown mode offers the most dramatic power savings by shutting down all the analog sections of the MAX19707 and placing the Rx ADC digital outputs in tri-state mode. When the Rx ADC outputs transition from tri-state to ON, the last converted word is placed on the digital outputs. The Tx DAC previously stored data is lost when coming out of shutdown mode. The wake-up time from shutdown mode is dominated by the time required to charge the capacitors at REFP, REFN, and COM. In internal reference mode and buffered external reference mode, the wake-up time is typically 85.2µs to enter Rx mode and 28.2µs to enter Tx mode.

In idle mode, the reference and clock distribution circuits are powered, but all other functions are off. The Rx ADC outputs are forced to tri-state. The wake-up time is 9.8µs to enter Rx mode and 6.4µs to enter Tx mode. When the Rx ADC outputs transition from tri-state to ON, the last converted word is placed on the digital outputs.

In standby mode, the reference is powered, but the rest of the device functions are off. The wake-up time from standby mode is 13.7µs to enter Rx mode and 24µs to enter Tx mode. When the Rx ADC outputs transition from tri-state to active, the last converted word is placed on the digital outputs.

FAST and SLOW Rx and Tx Modes

In addition to the external Tx-Rx control, the MAX19707 also features SLOW and FAST modes for switching between Rx and Tx operation. In FAST Tx mode, the Rx ADC core is powered on but the ADC core digital outputs are tri-stated on the D0–D9 bus; likewise, in FAST Rx mode, the transmit DAC core is powered on but the DAC core digital inputs are tri-stated on the D0–D9 bus. The switching time between Tx to Rx or Rx to Tx is FAST because the converters are on and do not have to recover from a power-down state. In FAST mode, the switching time between Rx to Tx and Tx to Rx is 0.5µs.

However, power consumption is higher in this mode because both the Tx and Rx cores are always on. To prevent bus contention in these states, the Rx ADC output buffers are tri-stated during Tx and the Tx DAC input bus is tri-stated during Rx.

In SLOW mode, the Rx ADC core is off during Tx; likewise the Tx DAC and filters are turned off during Rx to yield lower power consumption in these modes. For example, the power in SLOW Tx mode is 49.5mW. The power consumption during Rx is 77.1mW compared to 84.6mW power consumption in FAST mode. However, the recovery time between states is increased. The switching time in SLOW mode between Rx to Tx is 7µs and Tx to Rx is 4.1µs.

External T/$\overline{R}$ Switching Control vs. Serial-Interface Control

Bit E3 in the ENABLE-16 or ENABLE-8 register determines whether the device Tx-Rx mode is controlled externally through the T/$\overline{R}$ input (E3 = low) or through the SPI command (E3 = high). By default, the MAX19707 is in the external Tx-Rx control mode. In the external control mode, use the T/$\overline{R}$ input (pin 27) to switch between Rx and Tx modes. Using the T/$\overline{R}$ pin provides faster switching between Rx and Tx modes. To override the external Tx-Rx control, program the MAX19707 through the serial interface. During SHDN, IDLE, or STBY modes, the T/$\overline{R}$ input is overridden. To restore external Tx-Rx control, program bit E3 low and exit the SHDN, IDLE, or STBY modes through the serial interface.

SPI Timing

The serial digital interface is a standard 3-wire connection compatible with SPI/QSPI™/MICROWIRE/DSP interfaces. Set $\overline{CS}$ low to enable the serial data loading at DIN or output at DOUT. Following a $\overline{CS}$ high-to-low transition, data is shifted synchronously, most significant bit first, on the rising edge of the serial clock (SCLK). After 16 bits are loaded into the serial input register, data is transferred to the latch when $\overline{CS}$ transitions high. $\overline{CS}$ must transition high for a minimum of 80ns before the next write sequence. The SCLK can idle either high or low between transitions. Figure 6 shows the detailed timing diagram of the 3-wire serial interface.

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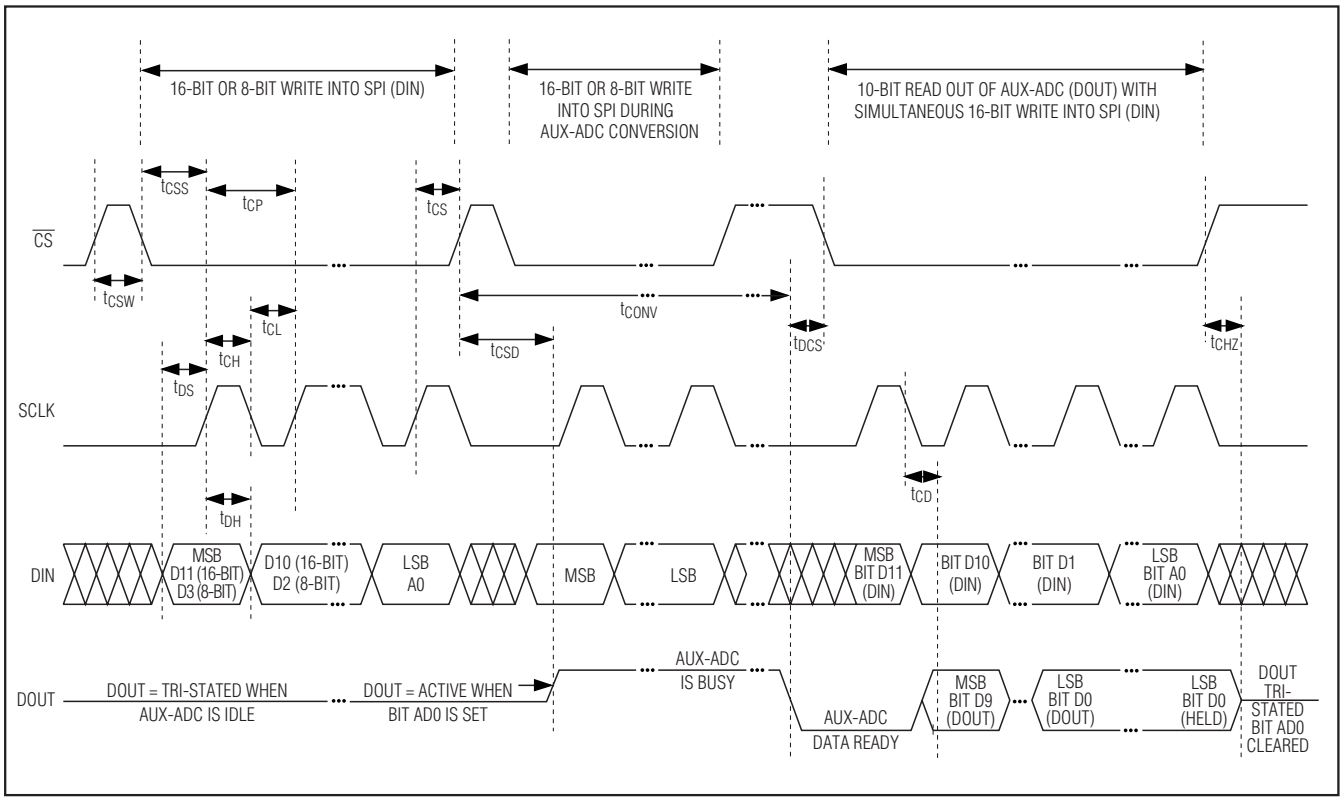

Figure 6. Serial-Interface Timing Diagram