Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

19-0526; Rev 0; 5/06

EVALUATION KIT AVAILABLE

10-Bit, 7.5Msps, Full-Duplex Analog Front-End

MAX19710

General Description

The MAX19710 is an ultra-low-power, highly integrated mixed-signal analog front-end (AFE) ideal for wideband communication applications operating in full-duplex (FD) mode. Optimized for high dynamic performance and ultra-low power, the device integrates a dual 10-bit, 7.5Msps receive (Rx) ADC; dual 10-bit, 7.5Msps transmit (Tx) DAC; three fast-settling 12-bit aux-DAC channels for ancillary RF front-end control; and a 10-bit, 333ksps housekeeping aux-ADC. The typical operating power in FD mode is 30mW at a 7.5MHz clock frequency.

The Rx ADCs feature 54.8dB SINAD and 79.8dBc SFDR at 3.3MHz input frequency with a 7.5MHz clock frequency. The analog I/Q input amplifiers are fully differential and accept 1.024V_{P-P} full-scale signals. Typical I/Q channel matching is ±0.01° phase and ±0.01dB gain.

The Tx DACs feature 73.8dBc SFDR at f_{OUT} = 620kHz and f_{CLK} = 7.5MHz. The analog I-Q full-scale output voltage range is ±400mV differential. The output DC common-mode voltage is from 0.89V to 1.36V. The I/Q channel offset is adjustable to optimize radio lineup sideband/carrier suppression. Typical I-Q channel matching is ±0.01dB gain and ±0.15° phase.

Two independent 10-bit parallel, high-speed digital buses used by the Rx ADC and Tx DAC allow full-duplex operation for frequency-division duplex applications. The Rx ADC and Tx DAC can be disabled independently to optimize power management. A 3-wire serial interface controls power-management modes, the aux-DAC channels, and the aux-ADC channels.

The MAX19710 operates on a single 2.7V to 3.3V analog supply and 1.8V to 3.3V digital I/O supply. The MAX19710 is specified for the extended (-40°C to +85°C) temperature range and is available in a 56-pin, thin QFN package. The *Selector Guide* at the end of the data sheet lists other pin-compatible versions in this AFE family. For time-division duplex (TDD) applications, refer to the MAX19705–MAX19708 AFE family of products.

Applications

Broadband Access Radio

Portable Communication Equipment

Private Mobile Radio

Ordering Information

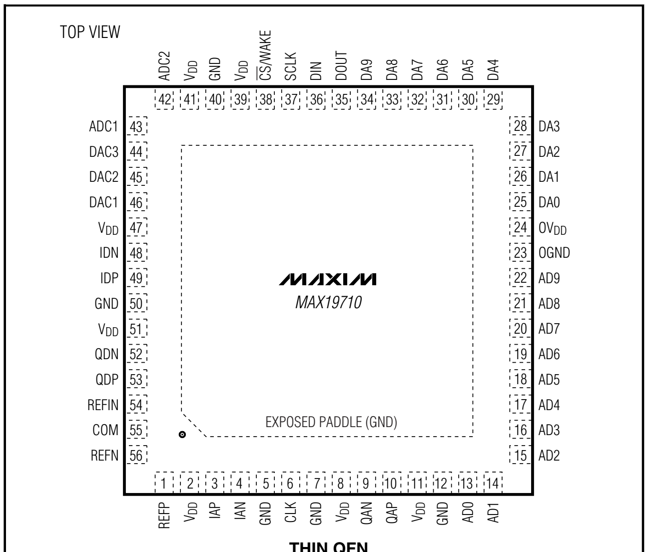
PART*	PIN-PACKAGE	PKG CODE
MAX19710ETN	56 Thin QFN-EP**	T5677-1
MAX19710ETN+	56 Thin QFN-EP**	T5677-1

**All devices are specified over the -40°C to +85°C operating range.*
***EP = Exposed paddle. +Denotes lead-free package.*

Features

- **Dual 10-Bit, 7.5Msps Rx ADC and Dual 10-Bit, 7.5Msps Tx DAC**
- **Ultra-Low Power**
  - **30mW at f_{CLK} = 7.5MHz, FD Mode**
  - **21.3mW at f_{CLK} = 7.5MHz, Slow Rx Mode**
  - **21.9mW at f_{CLK} = 7.5MHz, Slow Tx Mode**
  - **Low-Current Standby and Shutdown Modes**
- **Programmable Tx DAC Common-Mode DC Level and I/Q Offset Trim**
- **Excellent Dynamic Performance**
  - **SNR = 54.9dB at f_{IN} = 3.3MHz (Rx ADC)**
  - **SFDR = 73.8dBc at f_{OUT} = 620kHz (Tx DAC)**
- **Three 12-Bit, 1µs Aux-DACs**
- **10-Bit, 333ksps Aux-ADC with 4:1 Input Mux and Data Averaging**
- **Excellent Gain/Phase Match**
  - **±0.01° Phase, ±0.01dB Gain (Rx ADC) at f_{IN} = 1.8MHz**
- **Multiplexed Parallel Digital I/O**
- **Serial-Interface Control**
- **Versatile Power-Control Circuits**
  - **Shutdown, Standby, Idle, Tx/Rx Disable**
- **Miniature 56-Pin Thin QFN Package (7mm x 7mm x 0.8mm)**

Pin Configuration



NOTE: THE PIN 1 INDICATOR IS "+" FOR LEAD-FREE DEVICES.

Functional Diagram and Selector Guide appear at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND, OV_{DD} to OGND ....-0.3V to +3.6V
GND to OGND...-0.3V to +0.3V
IAP, IAN, QAP, QAN, IDP, IDN, QDP,
QDN, DAC1, DAC2, DAC3 to GND.....................-0.3V to V_{DD}
ADC1, ADC2 to GND.................................-0.3V to (V_{DD} + 0.3V)
REFP, REFN, REFIN, COM to GND...........-0.3V to (V_{DD} + 0.3V)
AD0–AD9, DA0–DA9, SCLK, DIN, $\overline{CS}$/WAKE,
CLK, DOUT to OGND ....-0.3V to (OV_{DD} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
56-Pin Thin QFN-EP (derate 27.8mW/°C above +70°C) 2.22W
Thermal Resistance θ_{JA} ....36°C/W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature...+150°C
Storage Temperature Range ....-60°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, $C_{REFP} = C_{REFN} = C_{COM}$ = 0.33µF, C_L < 5pF on all aux-DAC outputs, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIREMENTS						
Analog Supply Voltage	V_{DD}		2.7	3.0	3.3	V
Output Supply Voltage	OV_{DD}		1.8		V_{DD}	V
V_{DD} Supply Current		FD mode: f_{CLK} = 7.5MHz, f_{OUT} = 620kHz on both DAC channels; f_{IN} = 1.875MHz on both ADC channels; aux-DACs ON and at midscale, aux-ADC ON		10	12	mA
		SPI2-Tx mode: f_{CLK} = 7.5MHz, f_{OUT} = 620kHz on both DAC channels; Rx ADC OFF; aux-DACs ON and at midscale, aux-ADC ON		7.3	9	
		SPI1-Rx mode: f_{CLK} = 7.5MHz, f_{IN} = 1.875MHz on both ADC channels; Tx DAC OFF (Tx DAC outputs at 0V); aux-DACs ON and at midscale, aux-ADC ON		7.1	9	
		SPI4-Tx mode: f_{CLK} = 7.5MHz, f_{OUT} = 620kHz on both DAC channels; Rx ADC ON (output tri-stated); aux-DACs ON and at midscale, aux-ADC ON		9.7	12	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, C_L < 5pF on all aux-DAC outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Supply Current		SPI3-Rx mode: f_{CLK} = 7.5MHz, f_{IN} = 1.875MHz on both channels; Tx DAC ON (Tx DAC outputs at midscale); aux-DACs ON and at midscale, aux-ADC ON		9.5	12	mA
		Standby mode: CLK = 0 or OV_{DD}; aux-DACs ON and at midscale, aux-ADC ON		2.7	3.5	mA
		Idle mode: f_{CLK} = 7.5MHz; aux-DACs ON and at midscale, aux-ADC ON		4.6	6	mA
		Shutdown mode: CLK = 0 or OV_{DD}, or aux-ADC OFF		0.5	5	µA
OV_{DD} Supply Current		FD mode: f_{CLK} = 7.5MHz, f_{OUT} = 620kHz on both DAC channels; f_{IN} = 1.875MHz on both ADC channels; aux-DACs ON and at midscale, aux-ADC ON		0.94		mA
		SPI1-Rx and SPI3-Rx modes: f_{CLK} = 7.5MHz, f_{IN} = 1.875MHz on both ADC channels; DAC input bus tri-stated; aux-DACs ON and at midscale, aux-ADC ON		0.90		mA
		SPI2-Tx and SPI4-Tx modes: f_{CLK} = 7.5MHz, f_{OUT} = 620kHz on both DAC channels; ADC output bus tri-stated; aux-DACs ON and at midscale, aux-ADC ON		52		µA
		Standby mode: CLK = 0 or OV_{DD}; aux-DACs ON and at midscale, aux-ADC ON		0.1		µA
		Idle mode: f_{CLK} = 7.5MHz; aux-DACs ON and at midscale, aux-ADC ON		12.8		µA
		Shutdown mode: CLK = 0 or OV_{DD}, or aux-ADC OFF		0.1		µA
Rx ADC DC ACCURACY						
Resolution	N		10			Bits
Integral Nonlinearity	INL			±0.5		LSB
Differential Nonlinearity	DNL	No missing codes over temperature (Note 2)	-0.8	±0.4	+1.0	LSB
Offset Error		Residual DC offset error	-5	±0.2	+5	%FS
Gain Error		Includes reference error	-5	±0.9	+5	%FS
DC Gain Matching			-0.15	±0.04	+0.15	dB
Offset Matching				±11		LSB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, C_L < 5pF on all aux-DAC outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Gain Temperature Coefficient				±30		ppm/°C
Power-Supply Rejection	PSRR	Offset (V_{DD} ±5%)		±0.2		LSB
		Gain (V_{DD} ±5%)		±0.05		
Rx ADC ANALOG INPUT						
Input Differential Range	V_{ID}	Differential or single-ended inputs		±0.512		V
Input Common-Mode Voltage Range	V_{CM}			V_{DD} / 2		V
Input Impedance	R_{IN}	Switched capacitor load		720		kΩ
	C_{IN}			5		pF
Rx ADC CONVERSION RATE						
Maximum Clock Frequency	f_{CLK}	(Note 3)			7.5	MHz
Data Latency		Channel IA		5		Clock Cycles
		Channel QA		5.5		
Rx ADC DYNAMIC CHARACTERISTICS (Note 4)						
Signal-to-Noise Ratio	SNR	f_{IN} = 1.875MHz	53.2	54.8		dB
		f_{IN} = 3.3MHz		54.9		
Signal-to-Noise and Distortion	SINAD	f_{IN} = 1.875MHz	53.1	54.7		dB
		f_{IN} = 3.3MHz		54.8		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 1.875MHz	64.2	73.9		dBc
		f_{IN} = 3.3MHz		79.8		
Total Harmonic Distortion	THD	f_{IN} = 1.875MHz		-71.7	-62.8	dBc
		f_{IN} = 3.3MHz		-74.3		
Third-Harmonic Distortion	HD3	f_{IN} = 1.875MHz		-76.8		dBc
		f_{IN} = 3.3MHz		-83.8		
Intermodulation Distortion	IMD	f_{IN1} = 1.8MHz, A_{IN1} = -7dBFS; f_{IN2} = 1MHz, A_{IN2} = -7dBFS		-72		dBc
Third-Order Intermodulation Distortion	IM3	f_{IN1} = 1.8MHz, A_{IN1} = -7dBFS; f_{IN2} = 1MHz, A_{IN2} = -7dBFS		-83		dBc
Aperture Delay				3.5		ns
Aperture Jitter				2		ps_{RMS}
Overdrive Recovery Time		1.5x full-scale input		2		ns
Rx ADC INTERCHANNEL CHARACTERISTICS						
Crosstalk Rejection		$f_{INX,Y}$ = 1.8MHz, $A_{INX,Y}$ = -0.5dBFS, $f_{INY,X}$ = 1MHz, $A_{INY,X}$ = -0.5dBFS (Note 5)		-91		dB
Amplitude Matching		f_{IN} = 1.8MHz, A_{IN} = -0.5dBFS (Note 6)		±0.01		dB
Phase Matching		f_{IN} = 1.8MHz, A_{IN} = -0.5dBFS (Note 6)		±0.01		Degrees

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, C_L < 5pF on all aux-DAC outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Tx DAC DC ACCURACY						
Resolution	N		10			Bits
Integral Nonlinearity	INL			±0.3		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic (Note 2)	-0.75	±0.2	+0.75	LSB
Residual DC Offset	V_{OS}		-4	±1.2	+4	mV
Full-Scale Gain Error			-40	±1.6	+40	mV
Tx DAC DYNAMIC PERFORMANCE						
DAC Conversion Rate	f_{CLK}	(Note 3)			7.5	MHz
In-Band Noise Density	N_D	f_{OUT} = 620kHz		-120		dBFS/Hz
Third-Order Intermodulation Distortion	IM3	f_{OUT1} = 620kHz, f_{OUT2} = 640kHz		-79		dBc
Glitch Impulse				10		pV•s
Spurious-Free Dynamic Range to Nyquist	SFDR	f_{OUT} = 620kHz	61	73.8		dBc
Total Harmonic Distortion to Nyquist	THD	f_{OUT} = 620kHz		-72.2	-59.7	dBc
Signal-to-Noise Ratio to Nyquist	SNR	f_{OUT} = 620kHz		55.1		dB
Tx DAC INTERCHANNEL CHARACTERISTICS						
I-to-Q Output Isolation		$f_{OUTX,Y}$ = 2MHz, $f_{OUTY,X}$ = 2.2MHz		92		dB
Gain Mismatch Between I and Q Channels		Measured at DC	-0.4	±0.01	+0.4	dB
Phase Mismatch Between I and Q Channels		f_{OUT} = 620kHz		±0.15		Degrees
Differential Output Impedance				800		Ω
Tx DAC ANALOG OUTPUT						
Full-Scale Output Voltage	V_{FS}			±400		mV
Output Common-Mode Voltage	V_{COMD}	Bits CM1 = 0, CM0 = 0 (default)	1.29	1.36	1.42	V
		Bits CM1 = 0, CM0 = 1	1.14	1.2	1.27	
		Bits CM1 = 1, CM0 = 0	0.96	1.05	1.15	
		Bits CM1 = 1, CM0 = 1	0.78	0.89	1.03	
Rx ADC–Tx DAC INTERCHANNEL CHARACTERISTICS						
Receive Transmit Isolation		ADC f_{INI} = f_{INQ} = 1.8MHz, DAC f_{OUTI} = f_{OUTQ} = 620kHz		92		dB
AUXILIARY ADCs (ADC1, ADC2)						
Resolution	N		10			Bits

10-Bit, 7.5Msps, Full-Duplex Analog Front-End

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, C_L < 5pF on all aux-DAC outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Full-Scale Reference	V_{REF}	AD1 = 0 (default)		2.048		V
		AD1 = 1		V_{DD}		
Analog Input Range				0 to V_{REF}		V
Analog Input Impedance		Measured at DC		500		kΩ
Input-Leakage Current		Measured at unselected input from 0 to V_{REF}		±0.1		µA
Gain Error	GE	Includes reference error, AD1 = 0	-5		+5	%FS
Zero-Code Error	ZE			±2		mV
Differential Nonlinearity	DNL			±0.6		LSB
Integral Nonlinearity	INL			±0.6		LSB
Supply Current				210		µA
AUXILIARY DACs (DAC1, DAC2, DAC3)						
Resolution	N		12			Bits
Integral Nonlinearity	INL	From code 100 to code 4000		±1.25		LSB
Differential Nonlinearity	DNL	Guaranteed monotonic over code 100 to code 4000 (Note 2)	-1.0	±0.65	+1.2	LSB
Output-Voltage Low	V_{OL}	R_L > 200kΩ			0.2	V
Output-Voltage High	V_{OH}	R_L > 200kΩ	2.57			V
DC Output Impedance		DC output at midscale		4		Ω
Settling Time		From code 1024 to code 3072, within ±10 LSB		1		µs
Glitch Impulse		From code 0 to code 4095		24		nV•s
Rx ADC–Tx DAC TIMING CHARACTERISTICS						
CLK Rise to Channel-I Output Data Valid	t_{DOI}	Figure 3 (Note 2)	5.5	8.2	11.5	ns
CLK Fall to Channel-Q Output Data Valid	t_{DOQ}	Figure 3 (Note 2)	6.5	9.3	13.0	ns
I-DAC DATA to CLK Fall Setup Time	t_{DSI}	Figure 5 (Note 2)	10			ns
Q-DAC DATA to CLK Rise Setup Time	t_{DSQ}	Figure 5 (Note 2)	10			ns
CLK Fall to I-DAC Data Hold Time	t_{DHI}	Figure 5 (Note 2)	0			ns
CLK Rise to Q-DAC Data Hold Time	t_{DHQ}	Figure 5 (Note 2)	0			ns
CLK Duty Cycle				50		%
CLK Duty-Cycle Variation				±15		%
Digital Output Rise/Fall Time		20% to 80%		2.4		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, C_L < 5pF on all aux-DAC outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SERIAL-INTERFACE TIMING CHARACTERISTICS (Figures 6 and 8, Note 2)						
Falling Edge of $\overline{CS}$/WAKE to Rising Edge of First SCLK Time	t_{CSS}		10			ns
DIN to SCLK Setup Time	t_{DS}		10			ns
DIN to SCLK Hold Time	t_{DH}		0			ns
SCLK Pulse-Width High	t_{CH}		25			ns
SCLK Pulse-Width Low	t_{CL}		25			ns
SCLK Period	t_{CP}		50			ns
SCLK to $\overline{CS}$/WAKE Setup Time	t_{CS}		10			ns
$\overline{CS}$/WAKE High Pulse Width	t_{CSW}		80			ns
$\overline{CS}$/WAKE High to DOUT Active High	t_{CSD}	Bit AD0 set		200		ns
$\overline{CS}$/WAKE High to DOUT Low (Aux-ADC Conversion Time)	t_{CONV}	Bit AD0 set, no averaging, f_{CLK} = 7.5MHz, CLK divider = 2		4.3		µs
DOUT Low to $\overline{CS}$/WAKE Setup Time	t_{DCS}	Bit AD0, AD10 set		200		ns
SCLK Low to DOUT Data Out	t_{CD}	Bit AD0, AD10 set			14.5	ns
$\overline{CS}$/WAKE High to DOUT High Impedance	t_{CHZ}	Bit AD0, AD10 set		200		ns
MODE-RECOVERY TIMING CHARACTERISTICS (Figure 7)						
Shutdown Wake-Up Time (With CLK)	$t_{WAKE,SD}$	From shutdown to Rx mode, ADC settles to within 1dB SINAD		500		µs
		From shutdown to Tx mode, DAC settles to within 10 LSB error		26.2		
		From aux-ADC enable to aux-ADC start conversion		10		
		From shutdown to aux-DAC output valid		28		
		From shutdown to FD mode, ADC settles to within 1dB SINAD, DAC settles to within 10 LSB error		500		
Idle Wake-Up Time (With CLK)	$t_{WAKE,ST0}$	From idle to Rx mode, ADC settles to within 1dB SINAD		7.3		µs
		From idle to Tx mode, DAC settles to 10 LSB error		5.2		
		From idle to FD mode, ADC settles to within 1dB SINAD, DAC settles to within 10 LSB error		7.3		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, C_L < 5pF on all aux-DAC outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Standby Wake-Up Time (With CLK)	$t_{WAKE,ST1}$	From standby to Rx mode, ADC settles to within 1dB SINAD		7.5		µs
		From standby to Tx mode, DAC settles to 10 LSB error		22.2		
		From standby to FD mode, ADC settles to within 1dB SINAD, DAC settles to within 10 LSB error		22.2		
Enable Time from Tx to Rx, Fast Mode	$t_{ENABLE,RX}$	ADC settles to within 1dB SINAD		0.1		µs
Enable Time from Rx to Tx, Fast Mode	$t_{ENABLE,TX}$	DAC settles to within 10 LSB error		0.1		µs
Enable Time from Tx to Rx, Slow Mode	$t_{ENABLE,RX}$	ADC settles to within 1dB SINAD		7.3		µs
Enable Time from Rx to Tx, Slow Mode	$t_{ENABLE,TX}$	DAC settles to within 10 LSB error		5.2		µs
INTERNAL REFERENCE (V_{REFIN} = V_{DD}; V_{REFP}, V_{REFN}, V_{COM} levels are generated internally)						
Positive Reference		V_{REFP} - V_{COM}		0.256		V
Negative Reference		V_{REFN} - V_{COM}		-0.256		V
Common-Mode Output Voltage	V_{COM}		V_{DD} / 2 - 0.15	V_{DD} / 2	V_{DD} / 2 + 0.15	V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
Differential Reference Output	V_{REF}	V_{REFP} - V_{REFN}	+0.490	+0.512	+0.534	V
Differential Reference Temperature Coefficient	REFTC			±30		ppm/°C
BUFFERED EXTERNAL REFERENCE (external V_{REFIN} = 1.024V applied; V_{REFP}, V_{REFN}, V_{COM} levels are generated internally)						
Reference Input Voltage	V_{REFIN}			1.024		V
Differential Reference Output	V_{DIFF}	V_{REFP} - V_{REFN}		0.512		V
Common-Mode Output Voltage	V_{COM}			V_{DD} / 2		V
Maximum REFP/REFN/COM Source Current	I_{SOURCE}			2		mA
Maximum REFP/REFN/COM Sink Current	I_{SINK}			2		mA
REFIN Input Current				-0.7		µA
REFIN Input Resistance				500		kΩ

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, C_L < 5pF on all aux-DAC outputs, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (CLK, SCLK, DIN, $\overline{CS}$/WAKE, DA9–DA0)						
Input High Threshold	V_{INH}		0.7 x OV_{DD}			V
Input Low Threshold	V_{INL}				0.3 x OV_{DD}	V
Input Leakage	DI_{IN}	CLK, SCLK, DIN, $\overline{CS}$/WAKE = OGND or OV_{DD}	-1		+1	µA
		DA9–DA0 = OV_{DD}	-1		+1	
		DA9–DA0 = OGND	-5		+5	
Input Capacitance	DC_{IN}			5		pF
DIGITAL OUTPUTS (AD9–AD0, DOUT)						
Output-Voltage Low	V_{OL}	I_{SINK} = 200µA			0.2 x OV_{DD}	V
Output-Voltage High	V_{OH}	I_{SOURCE} = 200µA	0.8 x OV_{DD}			V
Tri-State Leakage Current	I_{LEAK}		-1		+1	µA
Tri-State Output Capacitance	C_{OUT}			5		pF

Note 1: Specifications from T_A = +25°C to +85°C guaranteed by production tests. Specifications at T_A < +25°C guaranteed by design and characterization.

Note 2: Guaranteed by design and characterization.

Note 3: The minimum clock frequency (f_{CLK}) for the MAX19710 is 1.5MHz (typ). The minimum aux-ADC sample rate clock frequency (A_{CLK}) is determined by f_{CLK} and the chosen aux-ADC clock-divider value. The minimum aux-ADC A_{CLK} > 1.5MHz / 128 = 11.7kHz. The aux-ADC conversion time does not include the time to clock the serial data out of DOUT. The maximum conversion time (for no averaging, NAVG = 1) will be t_{CONV} (max) = (12 x 1 x 128) / 1.5MHz = 1024µs.

Note 4: SNR, SINAD, SFDR, HD3, and THD are based on a differential analog input voltage of -0.5dBFS referenced to the amplitude of the digital outputs. SINAD and THD are calculated using HD2 through HD6.

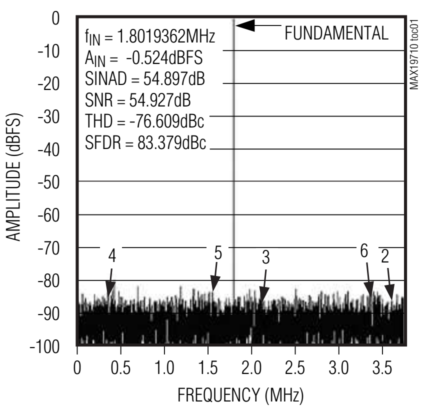
Note 5: Crosstalk rejection is measured by applying a high-frequency test tone to one channel and a low-frequency tone to the second channel. FFTs are performed on each channel. The parameter is specified as the power ratio of the first and second channel FFT test tones.

Note 6: Amplitude and phase matching are measured by applying the same signal to each channel, and comparing the two output signals using a sine-wave fit.

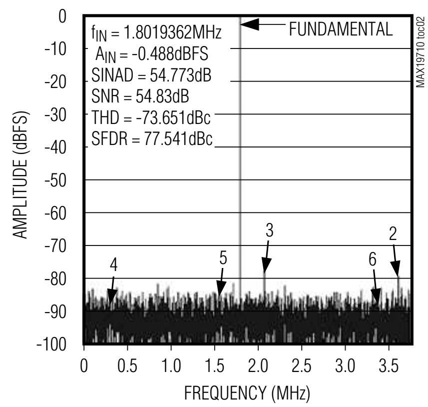
Typical Operating Characteristics

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), C_L ≈ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

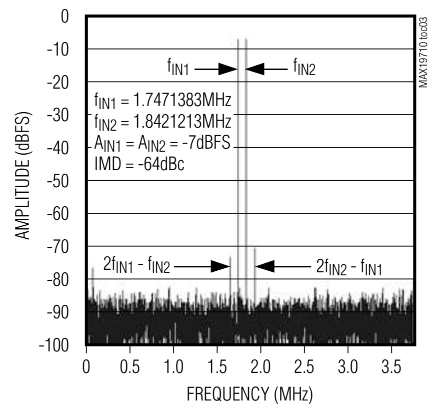
Rx ADC CHANNEL-IA FFT PLOT



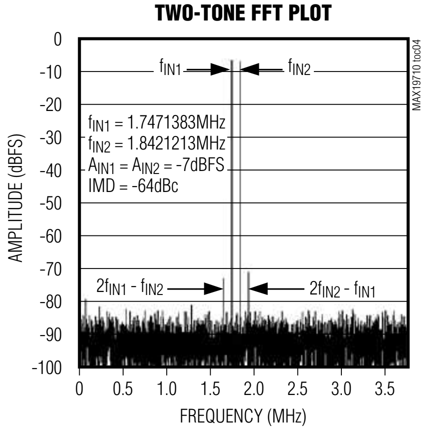
Rx ADC CHANNEL-QA FFT PLOT



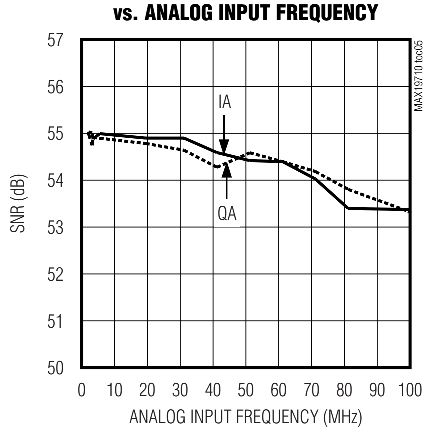
Rx ADC CHANNEL-IA TWO-TONE FFT PLOT



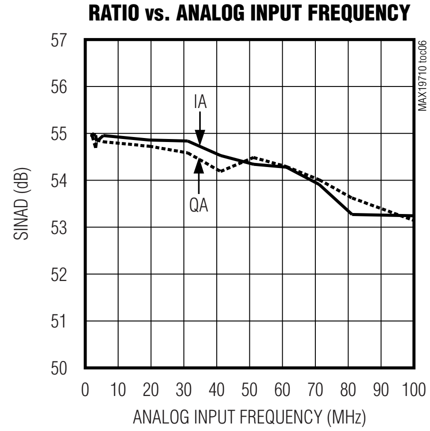
Rx ADC CHANNEL-QA TWO-TONE FFT PLOT



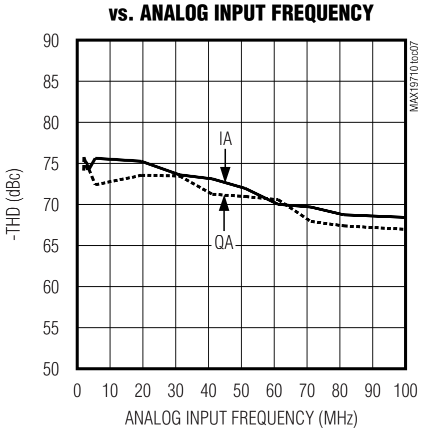
Rx ADC SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT FREQUENCY



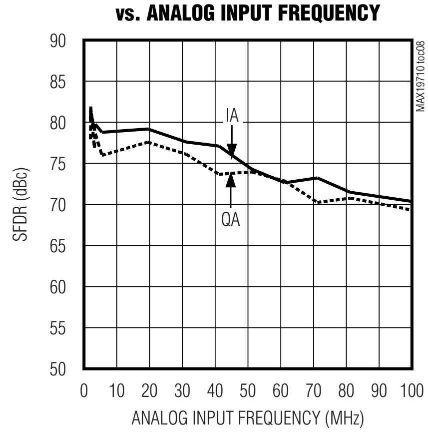
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. ANALOG INPUT FREQUENCY



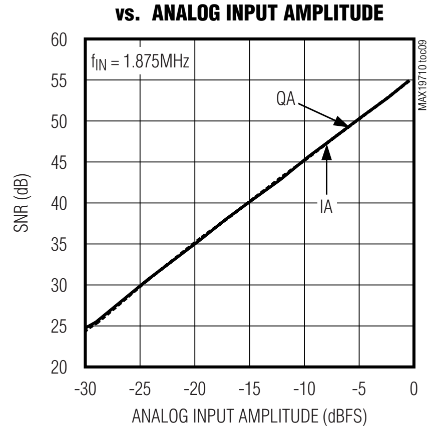
Rx ADC TOTAL HARMONIC DISTORTION vs. ANALOG INPUT FREQUENCY



Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT FREQUENCY



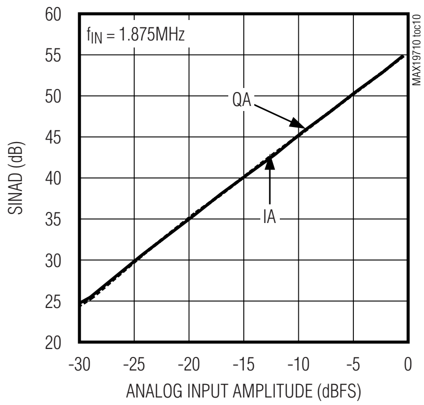
Rx ADC SIGNAL-TO-NOISE RATIO vs. ANALOG INPUT AMPLITUDE



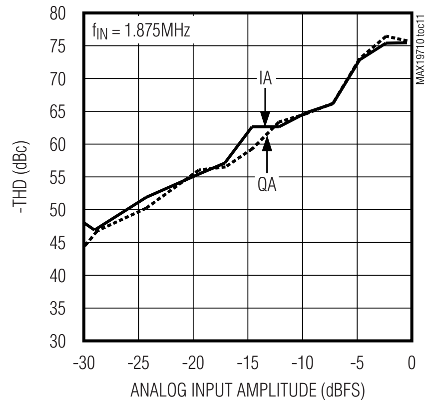
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

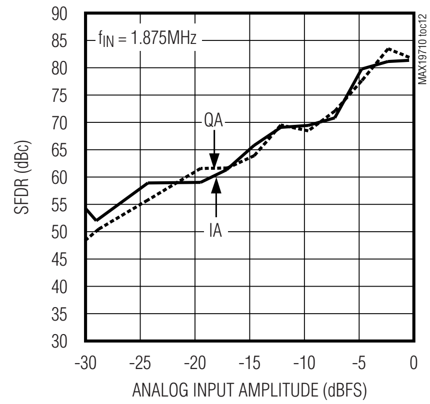
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. ANALOG INPUT AMPLITUDE



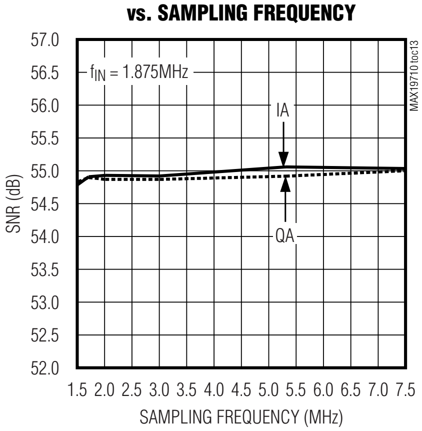
Rx ADC TOTAL HARMONIC DISTORTION vs. ANALOG INPUT AMPLITUDE



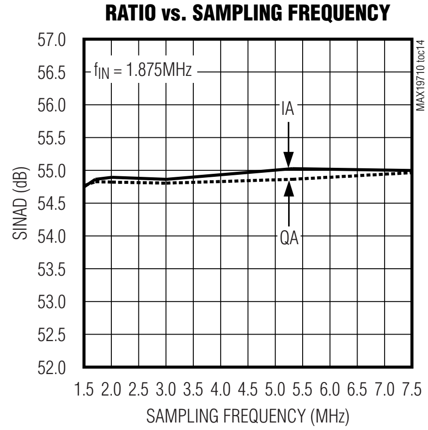
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. ANALOG INPUT AMPLITUDE



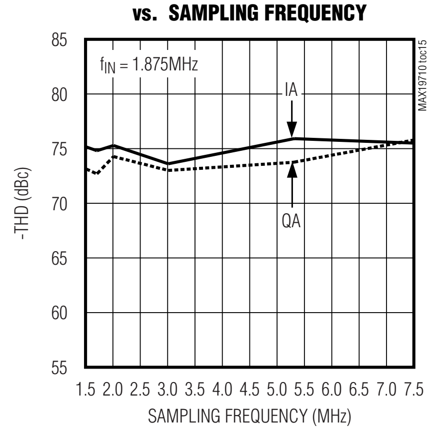
Rx ADC SIGNAL-TO-NOISE RATIO vs. SAMPLING FREQUENCY



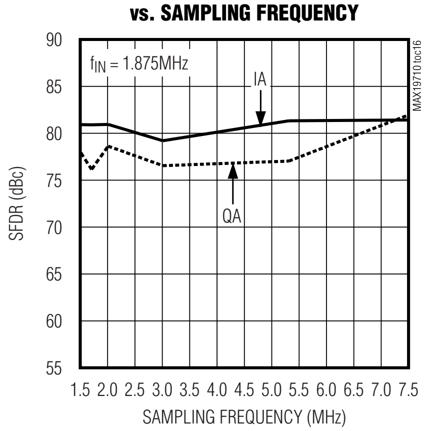
Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. SAMPLING FREQUENCY



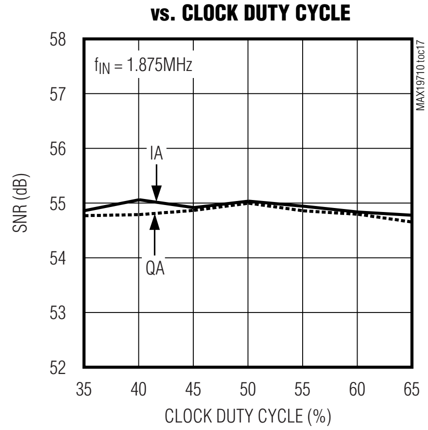
Rx ADC TOTAL HARMONIC DISTORTION vs. SAMPLING FREQUENCY



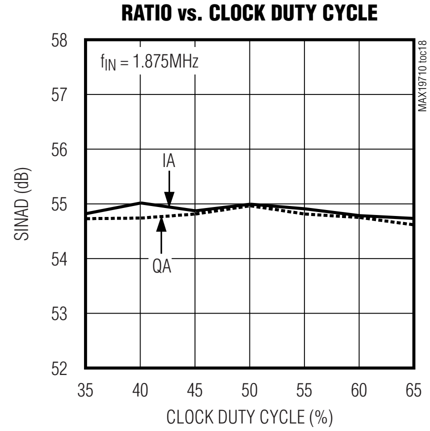
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING FREQUENCY



Rx ADC SIGNAL-TO-NOISE RATIO vs. CLOCK DUTY CYCLE



Rx ADC SIGNAL-TO-NOISE AND DISTORTION RATIO vs. CLOCK DUTY CYCLE

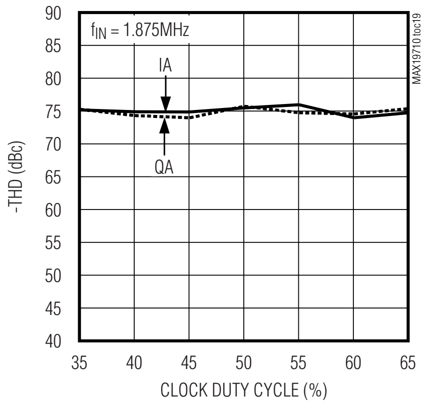


10-Bit, 7.5Msps, Full-Duplex Analog Front-End

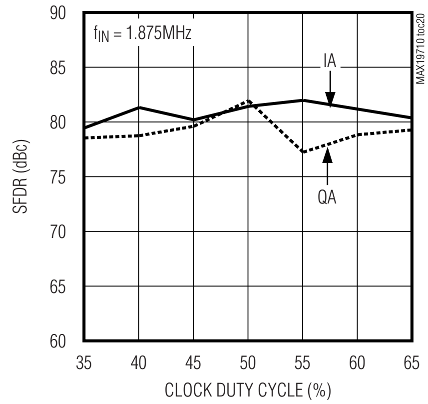
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

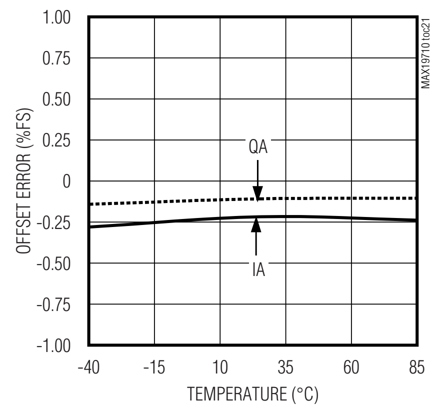
Rx ADC TOTAL HARMONIC DISTORTION vs. CLOCK DUTY CYCLE



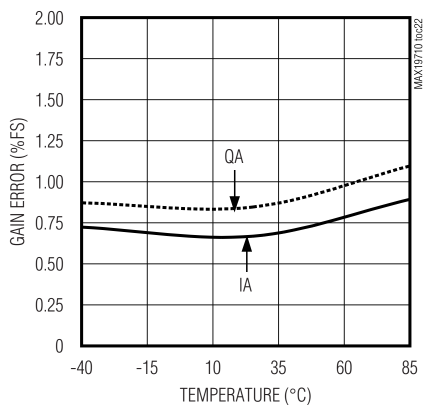
Rx ADC SPURIOUS-FREE DYNAMIC RANGE vs. CLOCK DUTY CYCLE



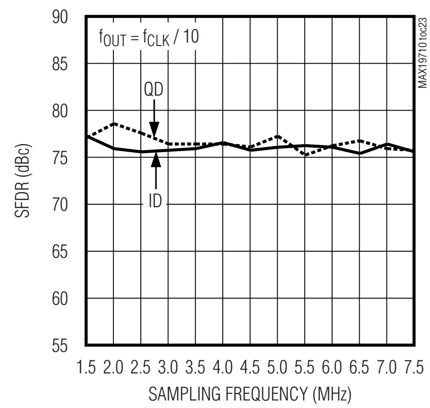
Rx ADC OFFSET ERROR vs. TEMPERATURE



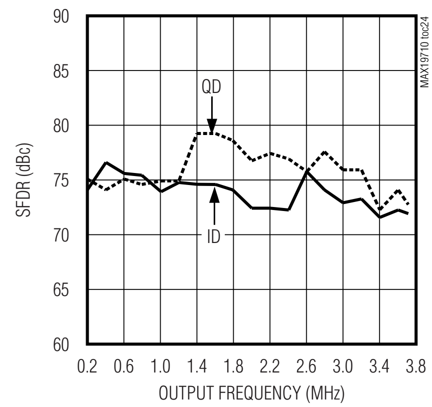
Rx ADC GAIN ERROR vs. TEMPERATURE



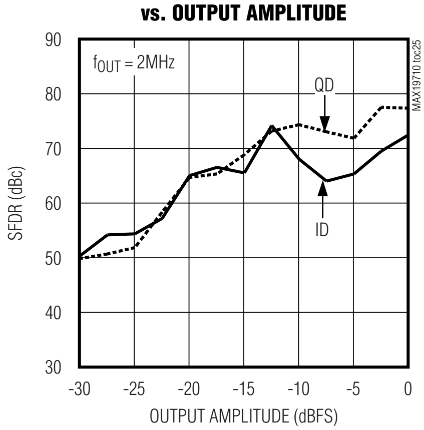
Tx DAC SPURIOUS-FREE DYNAMIC RANGE vs. SAMPLING FREQUENCY



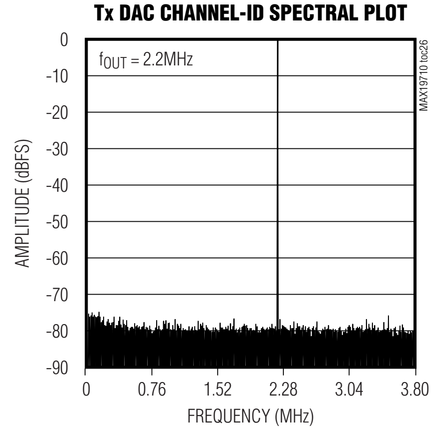
Tx DAC SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT FREQUENCY



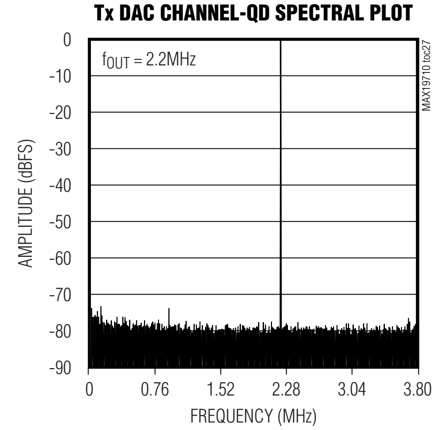
Tx DAC SPURIOUS-FREE DYNAMIC RANGE vs. OUTPUT AMPLITUDE



Tx DAC CHANNEL-ID SPECTRAL PLOT



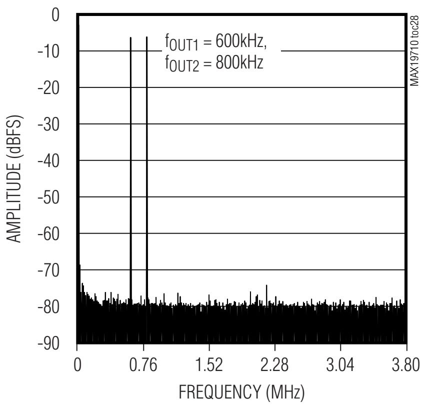
Tx DAC CHANNEL-QD SPECTRAL PLOT



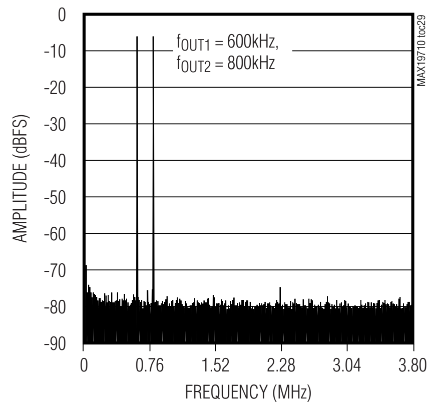
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

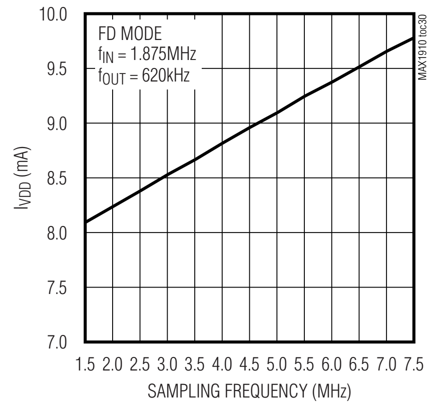
Tx DAC CHANNEL-ID TWO-TONE SPECTRAL PLOT



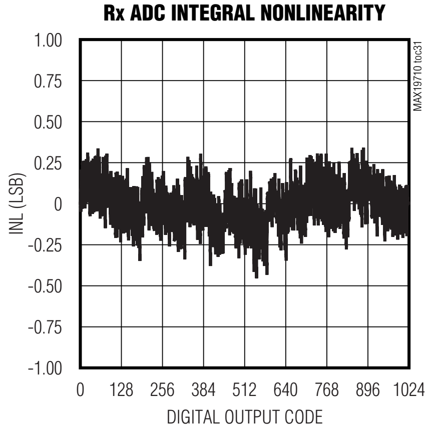
Tx DAC CHANNEL-QD TWO-TONE SPECTRAL PLOT



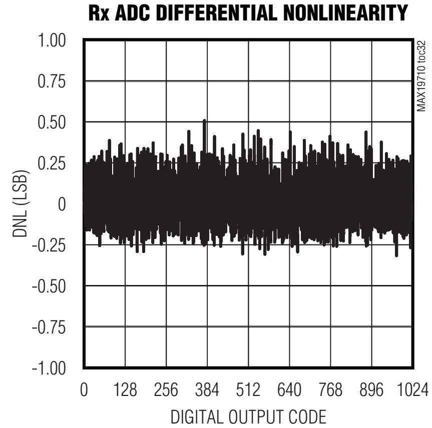
SUPPLY CURRENT vs. SAMPLING FREQUENCY



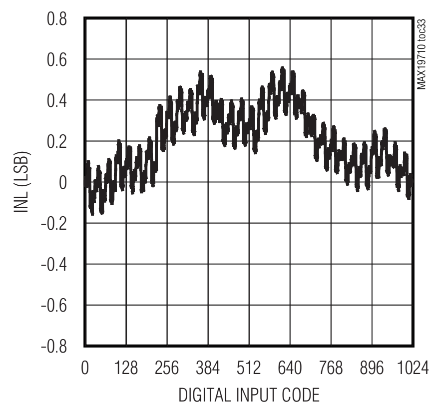
Rx ADC INTEGRAL NONLINEARITY



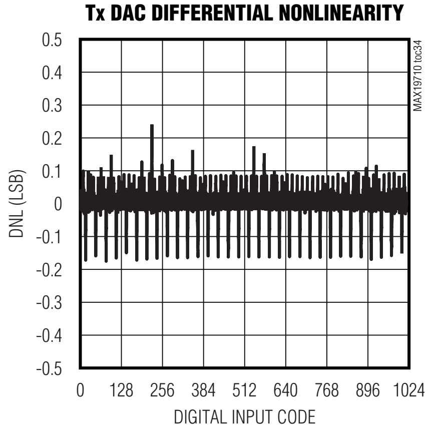
Rx ADC DIFFERENTIAL NONLINEARITY



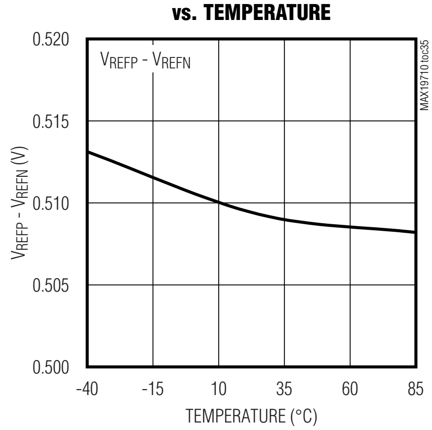
Tx DAC INTEGRAL NONLINEARITY



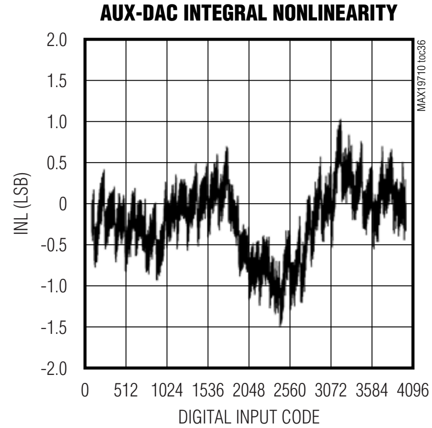
Tx DAC DIFFERENTIAL NONLINEARITY



REFERENCE OUTPUT VOLTAGE vs. TEMPERATURE



AUX-DAC INTEGRAL NONLINEARITY

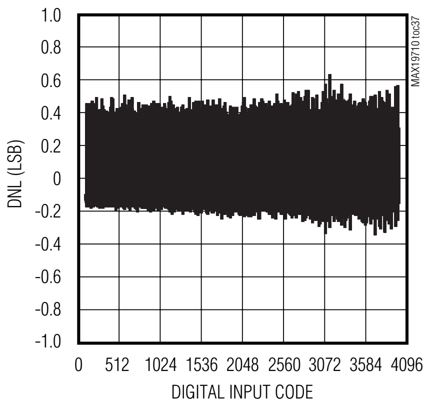


10-Bit, 7.5Msps, Full-Duplex Analog Front-End

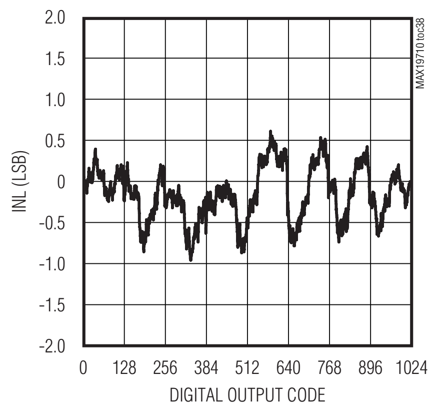
Typical Operating Characteristics (continued)

(V_{DD} = 3V, OV_{DD} = 1.8V, internal reference (1.024V), $C_L \approx$ 10pF on all digital outputs, f_{CLK} = 7.5MHz (50% duty cycle), Rx ADC input amplitude = -0.5dBFS, Tx DAC output amplitude = 0dBFS, CM1 = 0, CM0 = 0, differential Rx ADC input, differential Tx DAC output, C_{REFP} = C_{REFN} = C_{COM} = 0.33µF, T_A = +25°C, unless otherwise noted.)

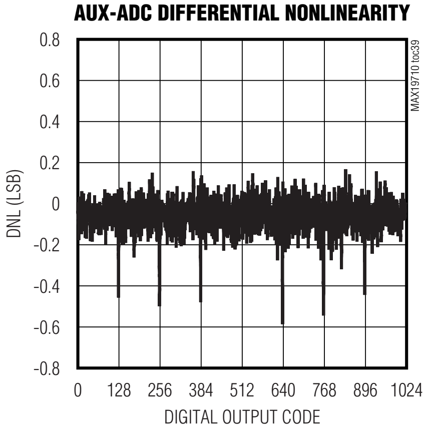
AUX-DAC DIFFERENTIAL NONLINEARITY



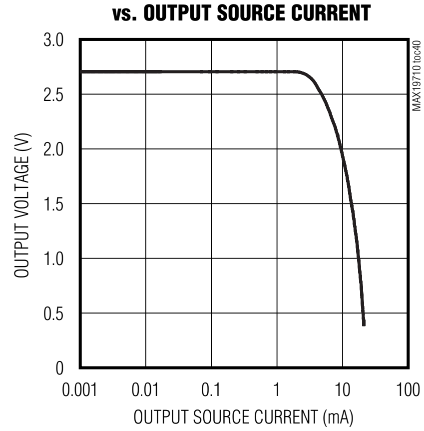
AUX-ADC INTEGRAL NONLINEARITY



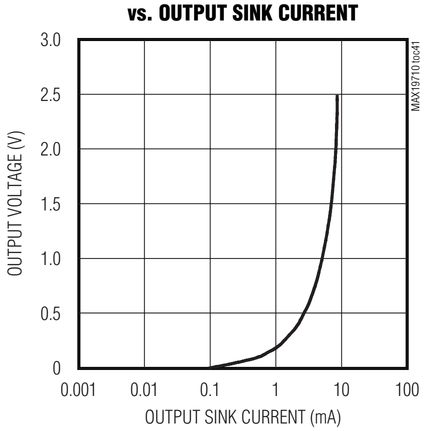
AUX-ADC DIFFERENTIAL NONLINEARITY



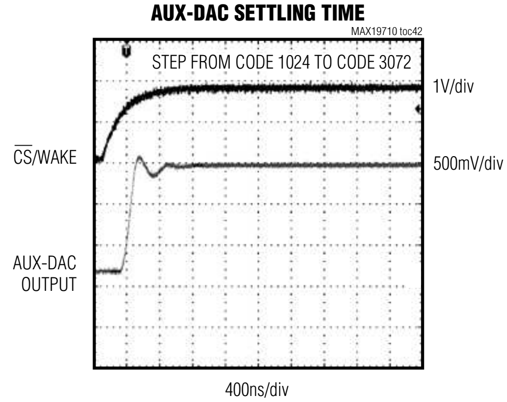
AUX-DAC OUTPUT VOLTAGE vs. OUTPUT SOURCE CURRENT



AUX-DAC OUTPUT VOLTAGE vs. OUTPUT SINK CURRENT



AUX-DAC SETTLING TIME



Pin Description

PIN	NAME	FUNCTION
1	REFP	Positive Reference Voltage Input Terminal. Bypass with a 0.33µF capacitor to GND as close to REFP as possible.
2, 8, 11, 39, 41, 47, 51	V_{DD}	Analog Supply Voltage. Bypass V_{DD} to GND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
3	IAP	Channel-IA Positive Analog Input. For single-ended operation, connect signal source to IAP.
4	IAN	Channel-IA Negative Analog Input. For single-ended operation, connect IAN to COM.
5, 7, 12, 40, 50	GND	Analog Ground. Connect all GND pins to ground plane.
6	CLK	Conversion Clock Input. Clock signal for both receive ADCs and transmit DACs.
9	QAN	Channel-QA Negative Analog Input. For single-ended operation, connect QAN to COM.
10	QAP	Channel-QA Positive Analog Input. For single-ended operation, connect signal source to QAP.
13–22	AD0–AD9	Receive ADC Digital Outputs. AD9 is the most significant bit (MSB) and AD0 is the least significant bit (LSB).
23	OGND	Output-Driver Ground
24	OV_{DD}	Output-Driver Power Supply. Supply range from +1.8V to V_{DD}. Bypass OV_{DD} to OGND with a combination of a 2.2µF capacitor in parallel with a 0.1µF capacitor.
25–34	DA0–DA9	Transmit DAC Digital Inputs. DA9 is the most significant bit (MSB) and DA0 is the least significant bit (LSB). DA0–DA9 are internally pulled up to OV_{DD}.
35	DOUT	Aux-ADC Digital Output
36	DIN	3-Wire Serial-Interface Data Input. Data is latched on the rising edge of SCLK.
37	SCLK	3-Wire Serial-Interface Clock Input
38	$\overline{CS}$/WAKE	3-Wire Serial-Interface Chip-Select/WAKE Input. When the MAX19710 is in shutdown, $\overline{CS}$/WAKE controls the wake-up function. See the *Wake-Up Function* section.
42	ADC2	Selectable Auxiliary ADC Analog Input 2
43	ADC1	Selectable Auxiliary ADC Analog Input 1
44	DAC3	Auxiliary DAC3 Analog Output (V_{OUT} = 0 at Power-Up)
45	DAC2	Auxiliary DAC2 Analog Output (V_{OUT} = 0 at Power-Up)
46	DAC1	Auxiliary DAC1 Analog Output (AFC DAC, V_{OUT} = 1.1V at Power-Up)
48	IDN	Tx Path Channel-ID Differential Negative Output
49	IDP	Tx Path Channel-ID Differential Positive Output
52	QDN	Tx Path Channel-QD Differential Negative Output
53	QDP	Tx Path Channel-QD Differential Positive Output
54	REFIN	Reference Input. Connect to V_{DD} for internal reference.
55	COM	Common-Mode Voltage I/O. Bypass COM to GND with a 0.33µF capacitor.
56	REFN	Negative Reference Voltage Input Terminal. Rx ADC conversion range is ±(V_{REFP} - V_{REFN}). Bypass REFN to GND with a 0.33µF capacitor.
—	EP	Exposed Paddle. Exposed paddle is internally connected to GND. Connect EP to the GND plane.

Detailed Description

The MAX19710 integrates a dual, 10-bit Rx ADC and a dual, 10-bit Tx DAC while providing ultra-low power and high dynamic performance at 7.5Msps conversion rate. The Rx ADC analog input amplifiers are fully differential and accept 1.024V_{P-P} full-scale signals. The Tx DAC analog outputs are fully differential with ±400mV full-scale output, selectable common-mode DC level, and adjustable channel ID–QD offset trim.

10-Bit, 7.5Msps, Full-Duplex Analog Front-End

The MAX19710 integrates three 12-bit auxiliary DACs (aux-DACs) and a 10-bit, 333ksps auxiliary ADC (aux-ADC) with 4:1 input multiplexer. The aux-DAC channels feature 1µs settling time for fast AGC, VGA, and AFC level setting. The aux-ADC features data averaging to reduce processor overhead and a selectable clock-divider to program the conversion rate.

The MAX19710 includes a 3-wire serial interface to control operating modes and power management. The serial interface is SPI™ and MICROWIRE™ compatible. The MAX19710 serial interface selects shutdown, idle, standby, FD, transmit (Tx), and receive (Rx) modes, as well as controls aux-DAC and aux-ADC channels.

The MAX19710 features two independent, high-speed, 10-bit buses for the Rx ADC and Tx DAC, which allow full-duplex (FD) operation for frequency-division duplex applications. Each bus can be disabled to optimize power management through the 3-wire interface. The MAX19710 operates from a single 2.7V to 3.3V analog supply and a 1.8V to 3.3V digital supply.

MICROWIRE is a trademark of National Semiconductor Corp.
SPI is a trademark of Motorola, Inc.

Dual 10-Bit Rx ADC

The ADC uses a seven-stage, fully differential, pipelined architecture that allows for high-speed conversion while minimizing power consumption. Samples taken at the inputs move progressively through the pipeline stages every half clock cycle. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for channel IA and 5.5 clock cycles for channel QA. The ADC full-scale analog input range is $\pm V_{REF}$ with a V_{DD} / 2 (±0.8V) common-mode input range. V_{REF} is the difference between V_{REFP} and V_{REFN}. See the *Reference Configurations* section for details.

Input Track-and-Hold (T/H) Circuits

Figure 1 displays a simplified diagram of the Rx ADC input track-and-hold (T/H) circuitry. Both ADC inputs (IAP, QAP, IAN, and QAN) can be driven either differen-

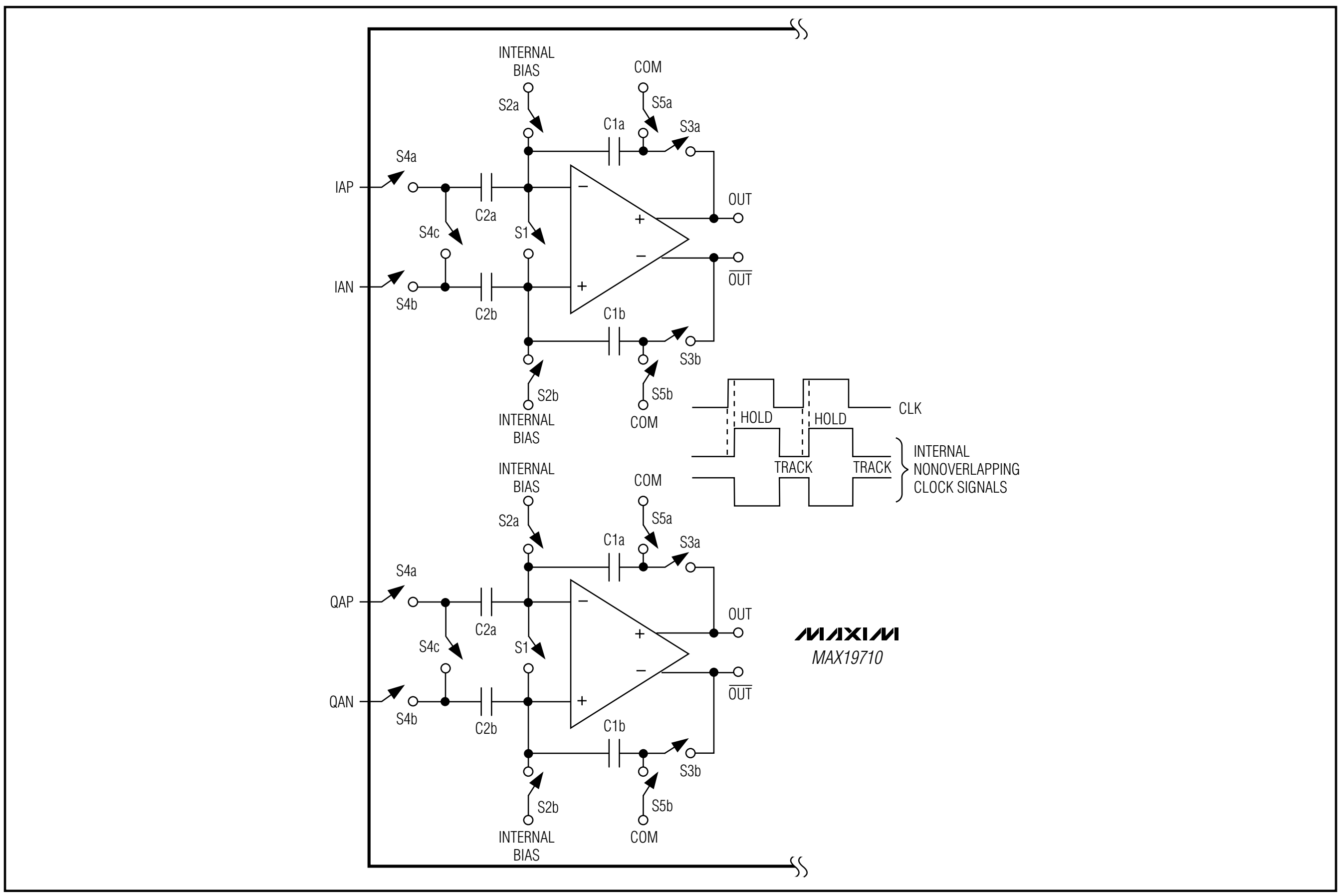


Figure 1. Rx ADC Internal T/H Circuits

Table 1. Rx ADC Output Codes vs. Input Voltage

DIFFERENTIAL INPUT VOLTAGE	DIFFERENTIAL INPUT (LSB)	OFFSET BINARY (AD0–AD9)	OUTPUT DECIMAL CODE
V_{REF} x 512/512	511 (+Full Scale - 1 LSB)	11 1111 1111	1023
V_{REF} x 511/512	510 (+Full Scale - 2 LSB)	11 1111 1110	1022
V_{REF} x 1/512	+1	10 0000 0001	513
V_{REF} x 0/512	0 (Bipolar Zero)	10 0000 0000	512
$-V_{REF}$ x 1/512	-1	01 1111 1111	511
$-V_{REF}$ x 511/512	-511 (-Full Scale + 1 LSB)	00 0000 0001	1
$-V_{REF}$ x 512/512	-512 (-Full Scale)	00 0000 0000	0

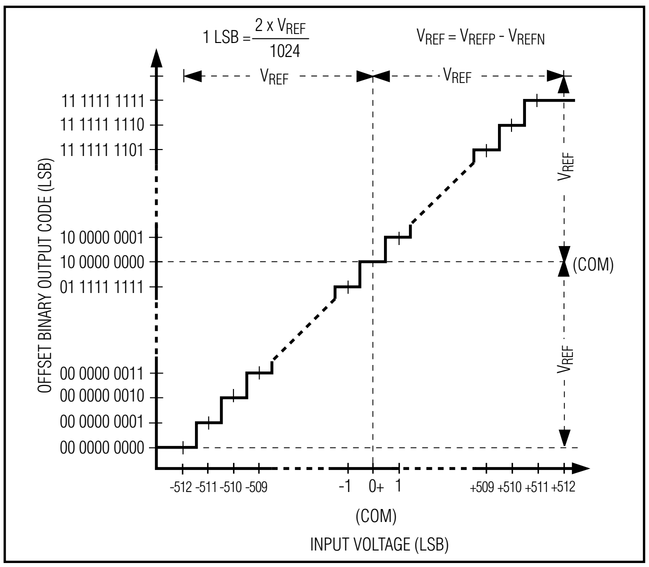


Figure 2. Rx ADC Transfer Function

tially or single-ended. Match the impedance of IAP and IAN, as well as QAP and QAN, and set the input signal common-mode voltage within the V_{DD} / 2 (±0.8V) Rx ADC range for optimum performance.

Rx ADC System Timing Requirements

Figure 3 shows the relationship between the clock, analog inputs, and the resulting output data. Channels IA and QA are sampled on the rising edge of the clock signal (CLK) and the resulting data is multiplexed at the AD0–AD9 outputs. Channel IA data is updated on the rising edge and channel QA data is updated on the falling edge of CLK. Including the delay through the output latch, the total clock-cycle latency is 5 clock cycles for channel IA and 5.5 clock cycles for channel QA.

Digital Output Data (AD0–AD9)

AD0–AD9 are the Rx ADC digital logic outputs of the MAX19710. The logic level is set by OV_{DD} from 1.8V to V_{DD}. The digital output coding is offset binary (Table 1). Keep the capacitive load on the digital outputs AD0–AD9 as low as possible (< 15pF) to avoid large digital currents feeding back into the analog portion of the MAX19710 and degrading its dynamic performance. Buffers on the digital outputs isolate the outputs from heavy capacitive loads. Adding 100Ω resistors in series with the digital outputs close to the MAX19710 will help improve ADC performance. Refer to the MAX19710EVKIT schematic for an example of the digital outputs driving a digital buffer through 100Ω series resistors.

During SHDN, IDLE, STBY, SPI2, and SPI4 states, digital outputs AD0–AD9 are tri-stated.

Dual 10-Bit Tx DACs

The dual 10-bit digital-to-analog converters (Tx DACs) operate with clock speeds up to 7.5MHz. The Tx DAC digital inputs, DA0–DA9, are multiplexed on a single 10-bit transmit bus. The voltage reference determines the Tx DAC full-scale voltage at IDP, IDN and QDP, QDN analog outputs. See the *Reference Configurations* section for setting the reference voltage.

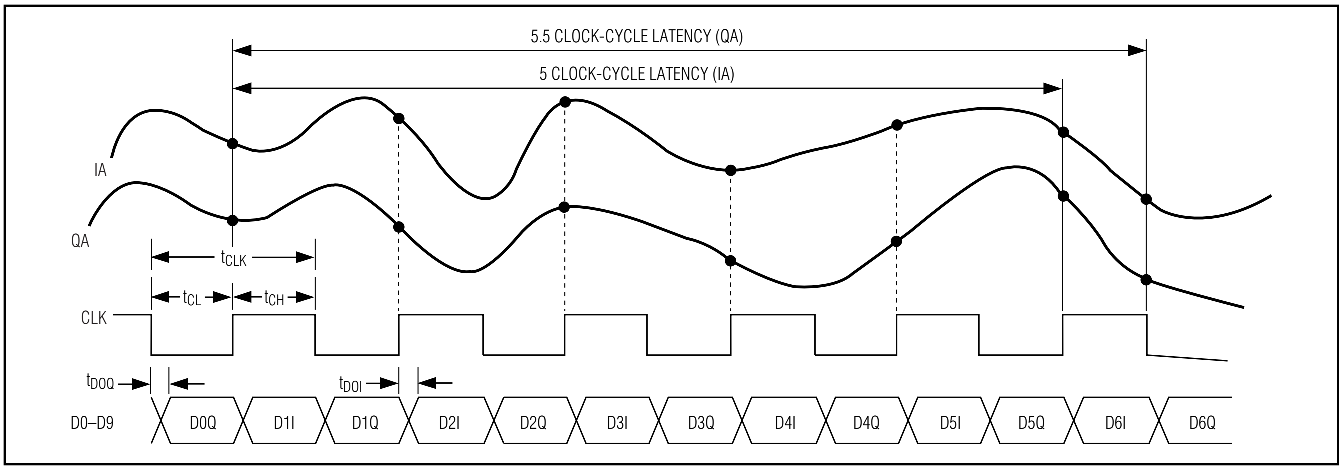


Figure 3. Rx ADC System Timing Diagram

Table 2. Tx DAC Output Voltage vs. Input Codes

(Internal Reference Mode V_{REFDAC} = 1.024V, External Reference Mode $V_{REFDAC} = V_{REFIN}$, V_{FS} = 400 for 800mV_{P-P} Full Scale)

DIFFERENTIAL OUTPUT VOLTAGE (V)	OFFSET BINARY (DA0–DA9)	INPUT DECIMAL CODE
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	11 1111 1111	1023
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	11 1111 1110	1022
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	10 0000 0001	513
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	10 0000 0000	512
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	01 1111 1111	511
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	00 0000 0001	1
$\left(V_{FS}\right)\frac{V_{REFDAC}}{1024} \times \frac{1023}{1023}$	00 0000 0000	0

The Tx DAC outputs (IDN, IDP, QDN, QDP) are biased at an adjustable common-mode DC level and designed to drive a differential input stage with ≥ 70kΩ input impedance. This simplifies the analog interface between RF quadrature upconverters and the MAX19710. Many RF upconverters require a 0.89V to 1.36V common-mode bias. The MAX19710 common-mode DC bias eliminates discrete level-setting resistors and code-generated level shifting while preserving the full dynamic range of each Tx DAC. **The Tx DAC differential analog outputs cannot be used in single-ended mode because of the internally generated common-mode DC level.** Table 2 shows the Tx DAC output voltage vs. input codes. Table 10 shows the selection of DC common-mode levels. See Figure 4 for an illustration of the Tx DAC analog output levels.

The Tx DAC also features independent DC offset trim on each ID–QD channel. This feature is configured through the SPI interface. The DC offset correction is used to optimize sideband and carrier suppression in the Tx signal path (see Table 9).

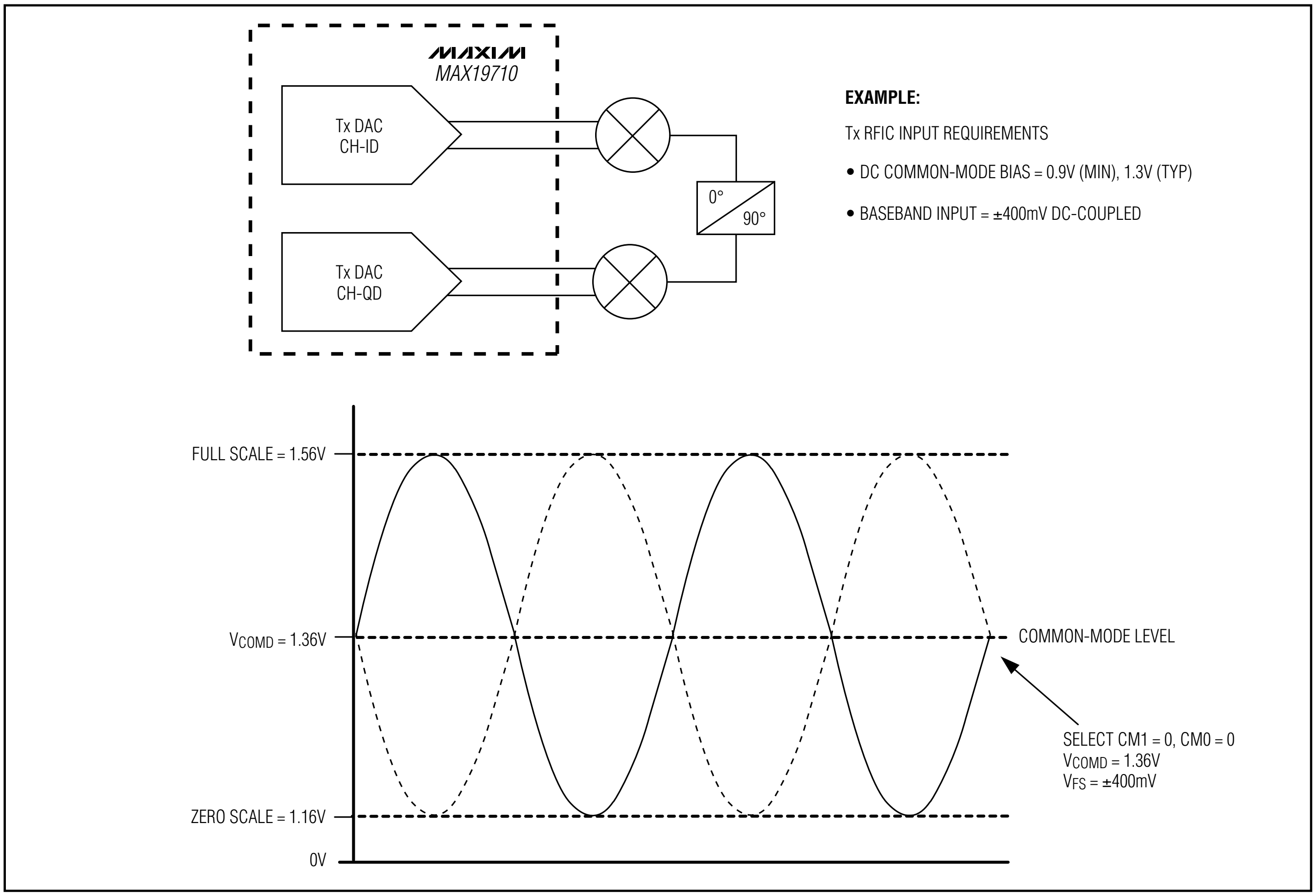


Figure 4. Tx DAC Common-Mode DC Level at IDN, IDP or QDN, QDP Differential Outputs

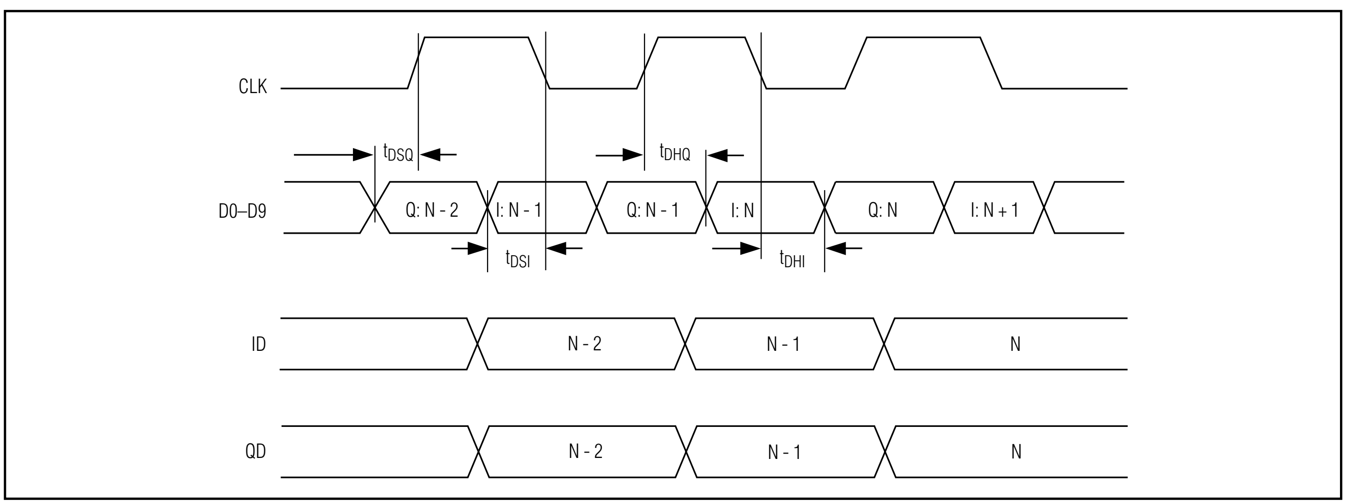


Figure 5. Tx DAC System Timing Diagram

Tx DAC Timing

Figure 5 shows the relationship among the clock, input data, and analog outputs. Channel ID data is latched on the falling edge of the clock signal, and channel QD data is latched on the rising edge of the clock signal, at which point both ID and QD outputs are simultaneously updated.

3-Wire Serial Interface and Operation Modes

The 3-wire serial interface controls the MAX19710 operation modes as well as the three 12-bit aux-DACs and the 10-bit aux-ADC. Upon power-up, program the MAX19710 to operate in the desired mode. Use the 3-wire serial interface to program the device for shutdown, idle, standby, FD, Rx, Tx, aux-DAC controls, or aux-ADC conversion. A 16-bit data register sets the mode control as shown in Table 3. The 16-bit word is composed of four control bits (A3–A0) and 12 data bits (D11–D0). Data is shifted in MSB first (D11) and LSB last (A0) format. Table 4 shows the MAX19710 power-management modes. Table 5 shows the SPI-controlled Tx, Rx, and FD modes. The serial interface remains active in all modes.

SPI Register Description

Program the control bits, A3–A0, in the register as shown in Table 3 to select the operating mode. Modify A3–A0 bits to select from ENABLE-16, Aux-DAC1, Aux-DAC2, Aux-DAC3, IOFFSET, QOFFSET, COMSEL, Aux-ADC, ENABLE-8, and WAKEUP-SEL modes. ENABLE-16 is the default operating mode (see Table 6). This mode allows for shutdown, idle, and standby states as well as switching between FAST, SLOW, Rx and Tx modes. Tables 4 and 5 show the required SPI settings for each mode.

In ENABLE-16 mode, the aux-DACs have independent control bits E4, E5, and E6, and bit E9 enables the aux-ADC. Table 7 shows the auxiliary DAC enable codes. Table 8 shows the auxiliary ADC enable code. Bits E11 and E10 are reserved. Program bits E11 and E10 to logic-low. Bits E3, E7, and E8 are not used.

Modes aux-DAC1, aux-DAC2, and aux-DAC3 select the aux-DAC channels named DAC1, DAC2, and DAC3 and hold the data inputs for each DAC. Bits _D11–_D0 are the data inputs for each aux-DAC and can be programmed through SPI. The MAX19710 also includes two 6-bit registers that can be programmed to adjust the offsets for the Tx DAC ID and QD channels independently (see Table 9). Use the COMSEL mode to select the output common-mode voltage with bits CM1 and CM0 (see Table 10). Use the aux-ADC mode to start the auxiliary ADC conversion (see the *10-Bit, 333ksps Auxiliary ADC* section for details). Use ENABLE-8 mode for faster enable and switching between shutdown, idle, and standby states as well as switching between FAST, SLOW, Rx and Tx modes and the FD mode.

The WAKEUP-SEL register selects the operating mode that the MAX19710 is to enter immediately after coming out of shutdown (Table 11). See the *Wake-Up Function* section for more information.

Shutdown mode offers the most dramatic power savings by shutting down all the analog sections (including the reference) of the MAX19710. In shutdown mode, the Rx ADC digital outputs are in tri-state mode, the Tx DAC digital inputs are internally pulled to OV_{DD}, and the Tx DAC outputs are at 0V. When the Rx ADC outputs transition from tri-state to active mode, the last converted word is placed on the digital output bus. The Tx DAC previously stored data is lost when coming out of shutdown mode. The wake-up time from shutdown mode is dominated by the time required to charge the capacitors at REFP, REFN, and COM. In internal reference mode and buffered external reference mode, the wake-up time is typically 500µs to enter Rx mode, 26.2µs to enter Tx mode, and 500µs to enter FD mode.

In all operating modes the Tx DAC inputs DA0–DA9 are internally pulled to OV_{DD}. To reduce the supply current of the MAX19710 in shutdown mode do not pull DA0–DA9 low. This consideration is especially important in shutdown mode to achieve the lowest quiescent current.

In idle mode, the reference and clock distribution circuits are powered, but all other functions are off. The Rx ADC outputs AD0–AD9 are forced to tri-state. The Tx DAC DA0–DA9 inputs are internally pulled to OV_{DD}, while the Tx DAC outputs are at 0V. The wake-up time is 7.3µs to enter Rx mode, 5.2µs to enter Tx mode, and 7.3µs to enter FD mode. When the Rx ADC outputs transition from tri-state to active, the last converted word is placed on the digital output bus.

In standby mode, the reference is powered but all other device functions are off. The wake-up time from standby mode is 7.5µs to enter Rx mode, 22.2µs to enter Tx mode, and 22.2µs to enter FD mode. When the Rx ADC outputs transition from tri-state to active, the last converted word is placed on the digital output bus.

FAST and SLOW Rx and Tx Modes

The MAX19710 features FAST and SLOW modes for switching between Rx and Tx operation. In FAST Tx mode, the Rx ADC core is powered on but the ADC digital outputs AD0–AD9 are tri-stated. The Tx DAC digital bus is active and the DAC core is fully operational.

Table 3. MAX19710 Mode Control

REGISTER NAME	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	A3	A2	A1	A0
	(MSB)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1 (LSB)
ENABLE-16	E11 = 0 Reserved	E10 = 0 Reserved	E9	—	—	E6	E5	E4	—	E2	E1	E0	0	0	0	0
Aux-DAC1	1D11	1D10	1D9	1D8	1D7	1D6	1D5	1D4	1D3	1D2	1D1	1D0	0	0	0	1
Aux-DAC2	2D11	2D10	2D9	2D8	2D7	2D6	2D5	2D4	2D3	2D2	2D1	2D0	0	0	1	0
Aux-DAC3	3D11	3D10	3D9	3D8	3D7	3D6	3D5	3D4	3D3	3D2	3D1	3D0	0	0	1	1
IOFFSET	—	—	—	—	—	—	IO5	IO4	IO3	IO2	IO1	IO0	0	1	0	0
QOFFSET	—	—	—	—	—	—	QO5	QO4	QO3	QO2	QO1	QO0	0	1	0	1
COMSEL	—	—	—	—	—	—	—	—	—	—	CM1	CM0	0	1	1	0
Aux-ADC	AD11 = 0 Reserved	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	0	1	1	1
ENABLE-8	—	—	—	—	—	—	—	—	—	E2	E1	E0	1	0	0	0
WAKEUP-SEL	—	—	—	—	—	—	—	—	—	W2	W1	W0	1	0	0	1

— = Not used.

Table 4. Power-Management Modes

ADDRESS				DATA BITS				MODE	FUNCTION (POWER MANAGEMENT)	DESCRIPTION	COMMENT
A3	A2	A1	A0	E9*	E2	E1	E0				
0000 (16-Bit Mode) or 1000 (8-Bit Mode)				1	0	0	0	SHDN	SHUTDOWN	Rx ADC = OFF Tx DAC = OFF (TX DAC outputs at 0V) Aux-DAC = OFF Aux-ADC = OFF CLK = OFF REF = OFF	Device is in complete shutdown.
				X**	0	0	1	IDLE	IDLE	Rx ADC = OFF Tx DAC = OFF (TX DAC outputs at 0V) Aux-DAC = Last State CLK = ON REF = ON	Fast turn-on time. Moderate idle power.
				X**	0	1	0	STBY	STANDBY	Rx ADC = OFF Tx DAC = OFF (TX DAC outputs at 0V) Aux-DAC = Last State CLK = OFF REF = ON	Slow turn-on time. Low standby power.

X = Don't care.
**Bit E9 is not available in 8-bit mode.*
***In IDLE and STBY modes, the aux-ADC can be turned on or off.*

Table 5. MAX19710 Tx, Rx, and FD Control Using SPI Commands

ADDRESS				DATA BITS			MODE	FUNCTION (Tx-Rx SWITCHING SPEED)	DESCRIPTION	COMMENT
A3	A2	A1	A0	E2	E1	E0				
0000 (16-Bit Mode) and 1000 (8-Bit Mode)				0	1	1	SPI1-Rx	SLOW	**Rx Mode:** Rx ADC = ON Rx Bus = Enabled Tx DAC = OFF (Tx DAC outputs at 0V) Tx Bus = OFF (all inputs are pulled high)	Slow transition to Tx mode from this mode. Low power.
				1	0	0	SPI2-Tx	SLOW	**Tx Mode:** Rx ADC = OFF Rx Bus = Tri-state Tx DAC = ON Tx Bus = ON	Slow transition to Rx mode from this mode. Low power.
				1	0	1	SPI3-Rx	FAST	**Rx Mode:** Rx ADC = ON Rx Bus = Enabled Tx DAC = ON (Tx DAC outputs at midscale) Tx Bus = OFF (all inputs are pulled high)	Fast transition to Tx mode from this mode. Moderate power.
				1	1	0	SPI4-Tx	FAST	**Tx Mode:** Rx ADC = ON Rx Bus = Tri-state Tx DAC = ON Tx Bus = ON	Fast transition to Rx mode from this mode. Moderate power.
				1	**1**	**1**	**FD**	**FAST**	**FD Mode:** Rx ADC = ON Rx Bus = ON Tx DAC = ON Tx Bus = ON	**Default Mode** Fast transition to any mode. Moderate power.

In FAST Rx mode, the Tx DAC core is powered on. The Tx DAC outputs are set to midscale. In this mode, the Tx DAC input bus is disconnected from the DAC core and DA0–DA9 are internally pulled to OV_{DD}. The Rx ADC digital bus is active and the ADC core is fully operational.

In FAST mode, the switching time from Tx to Rx, or Rx to Tx is minimized because the converters are on and do not have to recover from a power-down state. In FAST mode, the switching time from Rx to Tx and Tx to Rx is 0.1µs. Power consumption is higher in FAST mode because both Tx and Rx cores are always on.

In SLOW Tx mode, the Rx ADC core is powered off and the ADC digital outputs AD0–AD9 are tri-stated. The Tx DAC digital bus is active and the DAC core is fully operational. In SLOW Rx mode, the Tx DAC core is powered off. The Tx DAC outputs are set to 0. In SLOW Rx mode, the Tx DAC input bus is disconnected from the DAC core and DA0–DA9 are internally pulled to OV_{DD}. The Rx ADC digital bus is active and the ADC core is fully operational. The switching times for SLOW modes are 5.2µs for Rx to Tx and 7.3µs for Tx to Rx.

Table 6. MAX19710 Default (Power-On) Register Settings

REGISTER NAME	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	16 (MSB)	15	14	13	12	11	10	9	8	7	6	5
ENABLE-16	0	0	0	—	—	0	0	0	—	1	1	1
			Aux-ADC = ON			Aux-DAC1 to Aux-DAC3 = ON				FD mode		
Aux-DAC1	0	1	1	0	1	0	0	0	1	1	0	0
	DAC1 output set to 1.1V											
Aux-DAC2	0	0	0	0	0	0	0	0	0	0	0	0
	DAC2 output set to 0V											
Aux-DAC3	0	0	0	0	0	0	0	0	0	0	0	0
	DAC3 output set to 0V											
IOFFSET	—	—	—	—	—	—	0	0	0	0	0	0
							No offset on channel ID					
QOFFSET	—	—	—	—	—	—	0	0	0	0	0	0
							No offset on channel QD					
COMSEL	—	—	—	—	—	—	—	—	—	—	0	0
											V_{COMD} = 1.36V	
Aux-ADC	0	0	0	0	0	0	0	0	0	0	0	0
		Aux-ADC = ON, Conversion = IDLE, Aux-ADC REF = 2.048V, MUX = ADC1, Averaging = 1, Clock Divider = 1, DOUT = Disabled										
ENABLE-8	—	—	—	—	—	—	—	—	—	1	1	1
										FD mode		
WAKEUP-SEL	—	—	—	—	—	—	—	—	—	1	1	1
										Wake-up state = FD mode		

Table 7. Aux-DAC Enable Table (ENABLE-16 Mode)

E6	E5	E4	Aux-DAC3	Aux-DAC2	Aux-DAC1
0	0	0	ON	ON	ON
0	0	1	ON	ON	OFF
0	1	0	ON	OFF	ON
0	1	1	ON	OFF	OFF
1	0	0	OFF	ON	ON
1	0	1	OFF	ON	OFF
1	1	0	OFF	OFF	ON
1	1	1	OFF	OFF	OFF
0	**0**	**0**	**Default mode**		

Table 8. Aux-ADC Enable Table (ENABLE-16 Mode)

E9	SELECTION
0 (Default)	Aux-ADC is Powered ON
1	Aux-ADC is Powered OFF

Power consumption in SLOW Tx mode is 21.9mW, and 21.3mW in SLOW Rx mode. Power consumption in FAST Tx mode is 29.1mW, and 28.5mW in FAST Rx mode.

FD Mode

The MAX19710 features an FD mode, which is ideal for applications supporting frequency-division duplex. In FD mode, both Rx ADC and Tx DAC, as well as their

10-Bit, 7.5Msps, Full-Duplex Analog Front-End

Table 9. Offset Control Bits for ID and QD Channels (IOFFSET or QOFFSET Mode)

BITS IO5–IO0 WHEN IN IOFFSET MODE, BITS QO5–QO0 WHEN IN QOFFSET MODE						OFFSET 1 LSB = (VFS_{P-P} / 1023)
IO5/QO5	IO4/QO4	IO3/QO3	IO2/QO2	IO1/QO1	IO0/QO0	
1	1	1	1	1	1	-31 LSB
1	1	1	1	1	0	-30 LSB
1	1	1	1	0	1	-29 LSB
• • •	• • •	• • •	• • •	• • •	• • •	• • •
1	0	0	0	1	0	-2 LSB
1	0	0	0	0	1	-1 LSB
1	0	0	0	0	0	0mV
0	0	0	0	0	0	0mV (Default)
0	0	0	0	0	1	1 LSB
0	0	0	0	1	0	2 LSB
• • •	• • •	• • •	• • •	• • •	• • •	• • •
0	1	1	1	0	1	29 LSB
0	1	1	1	1	0	30 LSB
0	1	1	1	1	1	31 LSB

Note: *1 LSB = (800mV$_{P-P}$ / 1023) = 0.782mV.*

Table 10. Common-Mode Select (COMSEL Mode)

CM1	CM0	Tx PATH OUTPUT COMMON MODE (V)
0	0	1.36 (Default)
0	1	1.20
1	0	1.05
1	1	0.89

Table 11. WAKEUP-SEL Register

W2	W1	W0	POWER MODE AFTER WAKE-UP (WAKE-UP STATE)
0	0	0	**Invalid Value**. This value is ignored when inadvertently written to the WAKEUP-SEL register.
0	0	1	IDLE
0	1	0	STBY
0	1	1	SPI1-SLOW Rx
1	0	0	SPI2-SLOW Tx
1	0	1	SPI3-FAST Rx
1	1	0	SPI4-FAST Tx
1	1	1	FD **(Default)**

respective digital buses, are active and the device can receive and transmit simultaneously. Switching from FD mode to other Rx or Tx modes is fast (0.1µs) since the on-board converters are already powered. Consequently, power consumption in this mode is the maximum of all operating modes. In FD mode the MAX19710 consumes 30mW.

Wake-Up Function

The MAX19710 uses the SPI interface to control the operating modes of the device including the shutdown and wake-up functions. Once the device has been placed in shutdown through the appropriate SPI command, the first pulse on $\overline{CS}$/WAKE performs a wake-up function. At the first rising edge of $\overline{CS}$/WAKE, the MAX19710 is forced to a preset operating mode determined by the WAKEUP-SEL register. This mode is termed the wake-up state. If the WAKEUP-SEL register has not been programmed, the wake-up state for the MAX19710 is FD mode by default (Tables 6, 11). The WAKEUP-SEL register cannot be programmed with W2

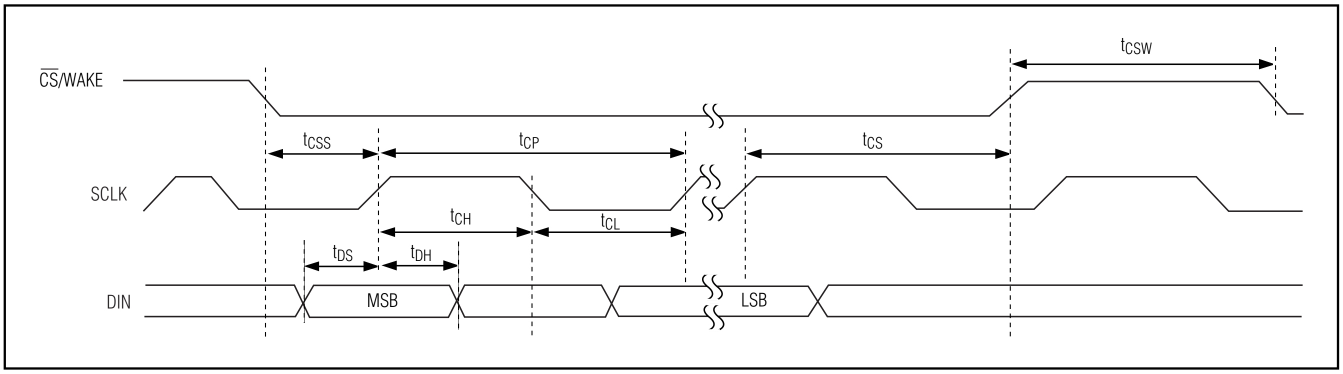


Figure 6. Serial-Interface Timing Diagram

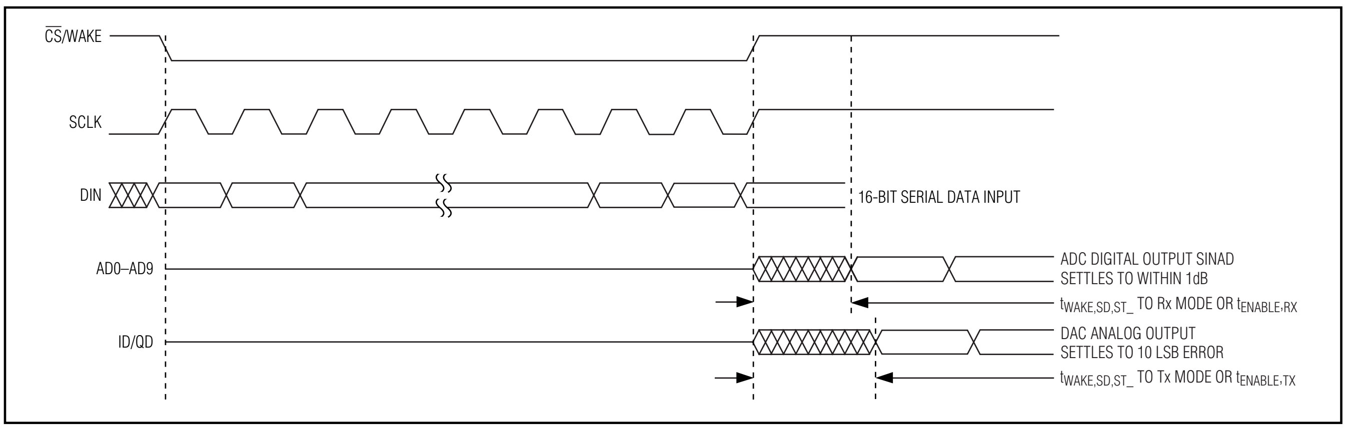


Figure 7. Mode-Recovery Timing Diagram

= 0, W1 = 0, and W0 = 0. If this value is inadvertently written to the device, it is ignored and the register continues to store its previous value. Upon wake-up, the MAX19710 enters the power mode determined by the WAKEUP-SEL register, however, all other settings (Tx DAC offset, Tx DAC common-mode voltage, aux-DAC settings, aux-ADC state) are restored to their values prior to shutdown.

The only SPI line that is monitored by the MAX19710 during shutdown is $\overline{CS}$/WAKE. Any information transmitted to the MAX19710 concurrent with the $\overline{CS}$/WAKE wake-up pulse is ignored.

SPI Timing

The serial digital interface is a standard 3-wire connection $\overline{CS}$/WAKE, SCLK, DIN) compatible with SPI/QSPI™/MICROWIRE/DSP interfaces. Set $\overline{CS}$/WAKE low to enable the serial data loading at DIN or output at DOUT. Following a $\overline{CS}$/WAKE high-to-low transition, data is shifted synchronously, most significant bit first, on the rising edge of the serial clock (SCLK). After 16 bits are loaded into the serial input register, data is transferred to the latch when $\overline{CS}$/WAKE transitions high. $\overline{CS}$/WAKE must transition high for a minimum of 80ns before the next write sequence. SCLK can idle either high or low between transitions. Figure 6 shows the detailed timing diagram of the 3-wire serial interface.

Mode-Recovery Timing

Figure 7 shows the mode-recovery timing diagram. t_{WAKE} is the wake-up time when exiting shutdown, idle, or standby mode and entering Rx, Tx, or FD mode. t_{ENABLE} is the recovery time when switching between either Rx or Tx mode. t_{WAKE} or t_{ENABLE} is the time for the Rx ADC to settle within 1dB of specified SINAD performance and Tx DAC settling to 10 LSB error. t_{WAKE} and t_{ENABLE} times are measured after the 16-bit serial command is latched into the MAX19710 by a $\overline{CS}$/WAKE transition high. In FAST mode, the recovery time is 0.1µs to switch between Tx or Rx modes.

QSPI is a trademark of Motorola, Inc.