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MAX20050–MAX20053

2A Synchronous-Buck LED Drivers with Integrated MOSFETs

General Description

The MAX20050–MAX20053 are high-brightness LED (HB LED) drivers for automotive exterior lighting applications. Consisting of a fully synchronous step-down converter with integrated MOSFETs, the devices are capable of driving a series string of LEDs at up to 2A, with a minimum number of external components. The MAX20050/MAX20052 utilize internal loop compensation to minimize component count, while the MAX20051/MAX20053 use external compensation for full flexibility.

The wide 4.5V to 65V input supply range supports extreme automotive cold crank and load-dump conditions. A low- and high-switching frequency option (400kHz or 2.1MHz) provides the designer with the flexibility to optimize for solution size or efficiency, while avoiding interference within the AM band. Spread spectrum provides further options for the designer to reduce EMI at the system level. The MAX20050/MAX20051 have an internal switching frequency of 400kHz, while the MAX20052/MAX20053 have an internal switching frequency of 2.1MHz.

High-side current regulation means only a single connection to the LED string is required; grounding of the string can be done locally. In addition to PWM dimming, the ICs provide analog dimming using the REFI pin. Full-scale current regulation accuracy is $\pm 2.5\%$, while the accuracy is $\pm 8\%$ at 10% of full-scale over the full temperature range of -40°C to $+125^{\circ}\text{C}$. A 5V, 10mA LDO output is available for biasing other circuits.

Fault-protection mechanisms include output overload, short-circuit, and device overtemperature protection. The devices are specified for operation over the full -40°C to $+125^{\circ}\text{C}$ temperature range and are available in thermally enhanced 12-pin (3mm x 3mm) TDFN and 14-pin (5mm x 4.4mm) TSSOP packages with an exposed pad.

Applications

- Daytime Running Lamps (DRLs)
- Fog Lamps
- Clearance Lamps (CLLs)
- Corner Lamps (CLs)
- Rear Lamps
- Head Lamps
- Commercial, Industrial, and Architectural Lighting

Benefits and Features

- Fully Synchronous 2A Step-Down Converter with Integrated 0.14 Ω (typ) MOSFETs
- Wide 4.5V to 65V Input Supply Range
- Two Switching Frequency Options: 400kHz and 2.1MHz
- Internal Loop Compensation (MAX20050/MAX20052) and External Loop Compensation (MAX20051/MAX20053) Options
- Switching Frequency Synchronized to PWM Dimming Signal
- Active-Low Fault (FLT) Indicator
- Output Short-Circuit Protection
- High-Side Current Regulation Eliminates One Connection to LED String
- Spread-Spectrum Mode Alleviates EMI Problems
- Low 200mV Full-Scale High-Side Current-Sense Voltage
- REFI Pin Adjusts LED Current Down to Zero
- PWM Dimming Disconnects Both High- and Low-Side MOSFET Drivers
- 5V, 10mA LDO Output Provides Bias to Other Circuits
- Ultra-Low Shutdown Current (5 μA typ)
- Output Overload, Short-Circuit, and Overtemperature Protections
- 12-Pin (3mm x 3mm) TDFN and 14-Pin (5mm x 4.4mm) TSSOP Package Options

Ordering Information appears at end of data sheet.

Absolute Maximum Ratings

IN to AGND.....	-0.3V to +70V	Short-Circuit Duration on V _{CC}	Continuous
PGND to AGND.....	-0.3V to +0.3V	Continuous Power Dissipation (T _A = +70°C) (Note 1)	
CS+, CS-, LX to AGND.....	-0.3V to (IN + 0.3V)	12-Pin TDFN-EP (derate 24.4 mW/°C	
BST to AGND.....	-0.3V to +75V	above +70°C).....	1951.2mW
BST to LX.....	-0.3V to +6V	14-Pin TSSOP-EP (derate 25.6 mW/°C	
PWM, FLT to AGND.....	-0.3V to +6V	above +70°C).....	2051.3mW
V _{CC} to AGND.....	-0.3V to MIN (+6V, IN + 0.3V)	Operating Temperature Range.....	-40°C to +125°C
COMP, REFI to AGND.....	-0.3V to V _{CC} + 0.3V	Junction Temperature.....	+150°C
CS+ to CS-.....	-0.3V to + 0.3V	Storage Temperature Range.....	-65°C to +150°C
Continuous Current on LX.....	2.1A	Lead Temperature (soldering, 10s).....	+300°C
Continuous Current on IN for TDFN.....	1.6A	Soldering Temperature (reflow).....	+260°C
Continuous Current on IN for TSSOP.....	2.1A		

Package Thermal Characteristics (Note 1)

TDFN	Junction-to-Ambient Thermal Resistance (θ _{JA}).....	41°C/W	TSSOP	Junction-to-Ambient Thermal Resistance (θ _{JA}).....	39°C/W
	Junction-to-Case Thermal Resistance (θ _{JC}).....	8.5°C/W		Junction-to-Case Thermal Resistance (θ _{JC}).....	3°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(V_{IN} = 12V, V_{REFI} = 1.2V, V_{PWM} = V_{CC}, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Supply Voltage	V _{IN}		4.5		65	V
IN Undervoltage Lockout	V _{INUVLO}	V _{IN} rising inferred by V _{CCUVLOR}			4.45	V
IN Undervoltage Hysteresis	V _{INHSTL}			225		mV
Supply Current	I _{INQ}	PWM = 0 (no switching)	V _{IN} = 12V	5	8	μA
			V _{IN} = 65V	8	20	
		PWM = 100% (and during regulation switching)	V _{IN} = 12V (MAX20050/51)	5	10	mA
			V _{IN} = 65V (MAX20050/51)	20	10	
V_{CC} REGULATOR (V_{CC})						
V _{CC} Output Voltage	V _{CC}	I _{VCC} = 1mA, 5.5V < V _{IN} < 65V	4.875	5	5.125	V
		I _{VCC} = 10mA, 6V < V _{IN} < 25V				
V _{CC} Dropout Voltage		I _{VCC} = 5mA, V _{IN} = 4.5V		50	100	mV
V _{CC} Short-Circuit Current	V _{CCIMAX}	V _{CC} = 0V	50	80	110	mA
V _{CC} Undervoltage Lockout	V _{CCUVLOR}	Rising	4	4.2	4.35	V
	V _{CCUVLHYS}	Hysteresis	150	200	250	mV
REFI Input Voltage Range	REFIRNG		0.2		1.20	V
REFI Zero-Current Threshold	REFIZC_VTH	CS _{DIFF} < 5mV	0.165	0.18	0.195	V

Electrical Characteristics (continued)

(V_{IN} = 12V, V_{REFI} = 1.2V, V_{PWM} = V_{CC}, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFI Clamp Voltage	REFI _{CLMP}	I _{REFI} sink = 1μA	1.274	1.3	1.326	V
Input Bias Current	REFI _{IIN}	V _{REFI} = 0 to V _{CC}	0	20	200	nA
Common-Mode Input Range	CSCM _{IIN}		-0.2		+65	V
Differential Signal Range	CS _{DIFF}		0		200	mV
CS+ Input Bias Current	IB _{CS+}	V _{CS+} = 60V	V _{CS+} - V _{CS-} = 200mV	40	70	μA
			V _{CS+} - V _{CS-} = 0V	8	15	
CS- Input Bias Current	IB _{CS-}	V _{CS-} = 60V	V _{CS+} - V _{CS-} = 200mV	100	150	μA
			V _{CS+} - V _{CS-} = 0V	66	110	
Current-Sense Input Offset	CS _{OS}	T _J = 25°C, CSCM _{IIN} 3V to 60V	-0.1			mV
		3V < CSCM _{IIN} < 60V	-1.8		+1.8	
Current-Sense Voltage Gain	CS _{GAIN}	(CS+ - CS-) = 200mV, 3V < CSCM _{IIN} < 60V	4.95	5	5.05	V/V
Regulation Voltage Accuracy	CS _{ACC}	REFI = 1.4V, 3V < CSCM _{IIN} < 60V	215	220	225	mV
		REFI = 1.2V, 3V < CSCM _{IIN} < 60V	196	200	204	
		REFI = 0.7V, 3V < CSCM _{IIN} < 60V	100			
		REFI = 0.4V, 3V < CSCM _{IIN} < 60V	37.8	40	42.2	
Regulation Voltage Accuracy Low Range	CS _{ACC}	V _{REFI} = 1.2V 0V < CSCM _{IIN} < 3V	192	200	208	mV
		V _{REFI} = 0.4V 0V < CSCM _{IIN} < 3V	35	40	45	
CS Common-Mode Range Input Selector	RNG _{SEL}	V _{CS+} rising	2.75	2.85	2.95	V
		V _{CS+} falling	2.5	2.6	2.7	
Cycle-by-Cycle Current Limit	CS _{LIM}	V _{CS-} > OUT _{VTH_LOW}	285	300	315	mV
		V _{CS-} < OUT _{VTH_LOW}	CS _{ACC} - 5	CS _{ACC}	CS _{ACC} + 5	
Transconductance	g _M	V _{CS+} - V _{CS-} = 200mV	480	600	720	μS
Open-Loop DC Gain			75			dB
COMP Bias Current	COMP _{IBIAS}	PWM = 0	-200		+200	nA
COMP Sink Current	COMP _{ISINK}	V _{COMP} = 5V	85	100	115	μA
COMP Source Current	COMP _{ISRC}	V _{COMP} = 0V	85	100	115	μA
High-Side DMOS RDS _{ON}	R _{ON,HS}	I _{LX} = 200mA, V _{CS+} = 3V		170	340	mΩ
Low-Side DMOS RDS _{ON}	R _{ON,LS}	V _{CC} = 5V, I _{LX} = 200mA		140	300	mΩ
LX Rise Time	t _{RISE,LS}		10			ns
Switching Frequency	f _{SW}	MAX20050/MAX20051, frequency dither disabled	360	400	440	kHz
		MAX20052/MAX20053, frequency dither disabled	1890	2100	2310	

Electrical Characteristics (continued)

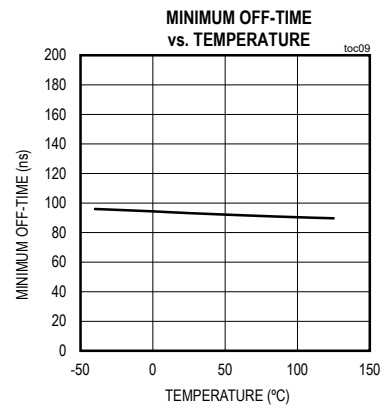
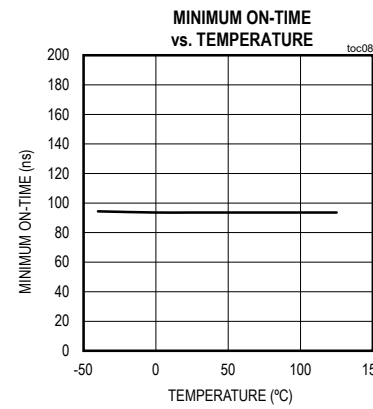
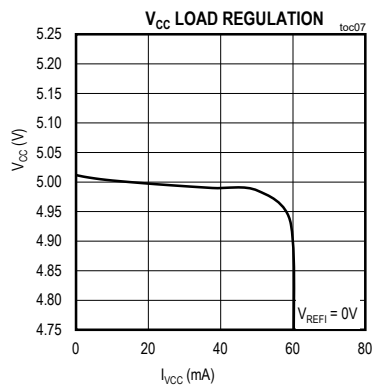
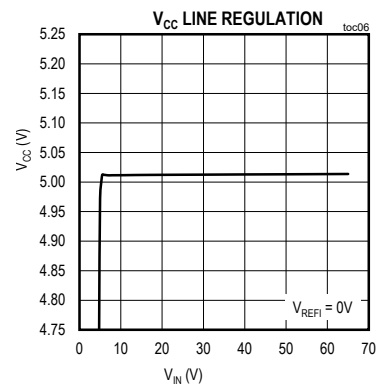
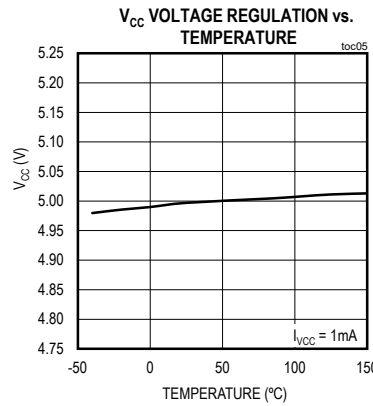
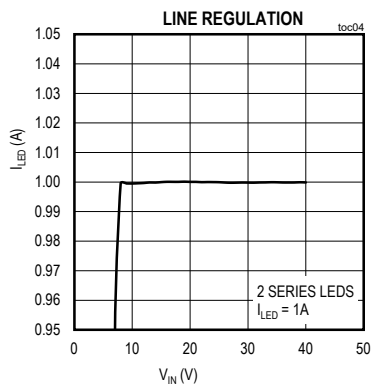
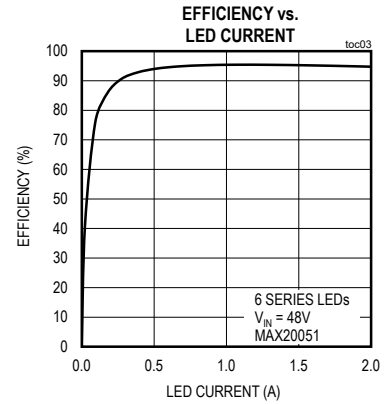
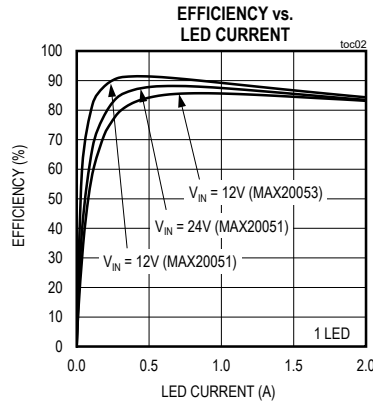
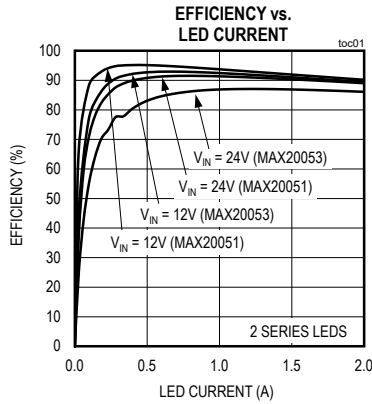
(V_{IN} = 12V, V_{REFI} = 1.2V, V_{PWM} = V_{CC}, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum On-Time	t _{ON_MIN}		50	80	120	ns
Minimum Off-Time	t _{OFF_MIN}		50	80	120	ns
Spread Spectrum Range	SS			±3		%
PWM Input Frequency	PWM _{FR}		100		2000	Hz
PWM-to-LX Delay	PWM _{DLY}	Rising (during regulation)		2	5	μs
		Falling (during regulation)		2	5	
PWM Threshold	PWM _{VTHR}	Rising			2	V
	PWM _{VTHF}	Falling	800			mV
PWM Pullup Current	PWM _{RIN}	V _{IN} = 12V	1	2	3	μA
PWM Shutdown Timer	PWM _{SHDW}	PWM low time to enter shutdown mode	140	210	300	ms
Startup Time	t _{STUP}	IN, PWM rising to LX delay	180	250	350	μs
Thermal Shutdown		Rising		165		°C
		Hysteresis		10		°C
LED Open-Fault REFI Range	LOF _{REFI_RNG}	V _{REFI} rising	300	325	350	mV
LED Open-Fault Enable Rising Threshold	LOF _{IN_RNG}	V _{IN} rising	8	9	10	V
LED Open-Fault Enable Falling Threshold	LOF _{IN_FLNG}	V _{IN} falling	7.3	8.3	9.3	V
LED Open-Fault Threshold	LOF _{VTH}	CS _{DIFF} falling, duty = max	10	25	40	%
LED Open-Fault Hysteresis	LOF _{VTH_HYS}		3	6	9	%
Output-Voltage Low Threshold	OUTV _{TH_LOW}	V _{CS-} falling	1.35	1.5	1.65	V
FAULT Output Voltage	FAULT _{VOL}	I _{SINK} = 1mA, V _{CS+} = 1V, after FAULT _{DEG} elapsed		0.05	0.3	V
FAULT Deglitch Timer	FAULT _{DEG}	(Note 3)	70	105	150	μs
FAULT Mask Timer	FAULT _{MASK}	(Note 4)	140	210	300	μs
FAULT Leakage Current	FAULT _{LK}	V _{FAULT} = 5.5V			1	μs

Note 2: 100% tested at T_A = +25°C. All limits over temperature are guaranteed by design, not production tested.**Note 3:** The time duration for which the fault condition has to remain active before asserting $\overline{\text{FLT}}$ pin.**Note 4:** The mask timer occurs each time PWM goes from low to high. Open LED condition cannot be detected during the mask time period.

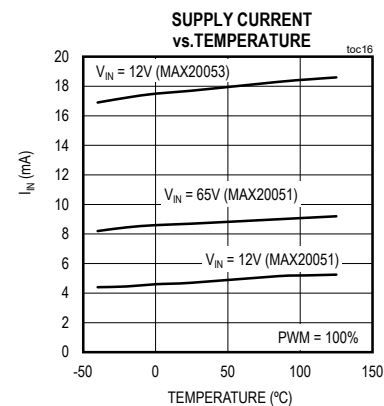
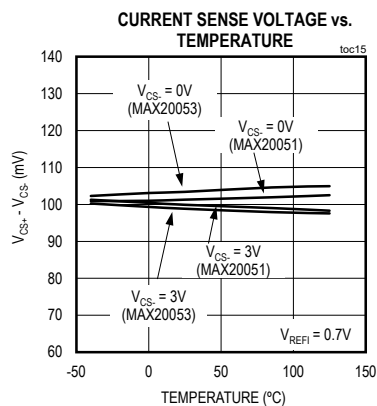
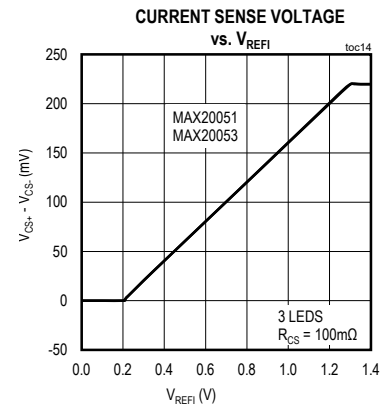
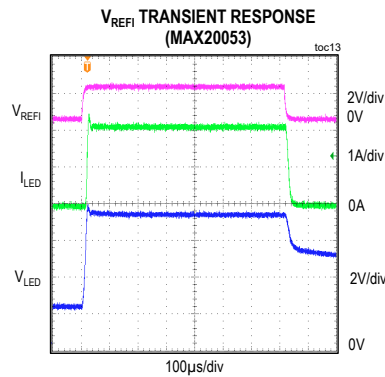
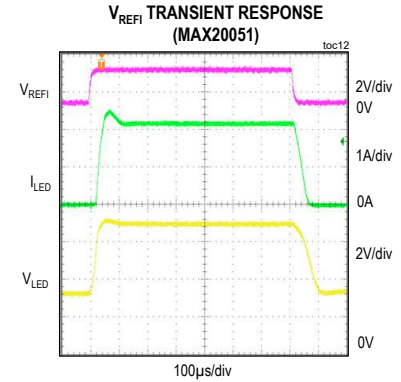
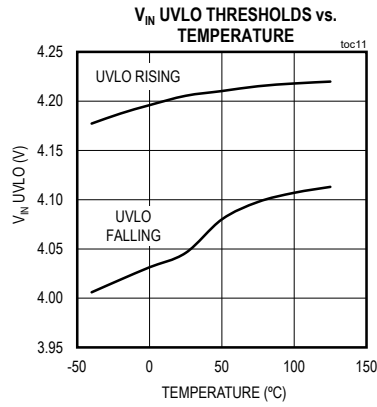
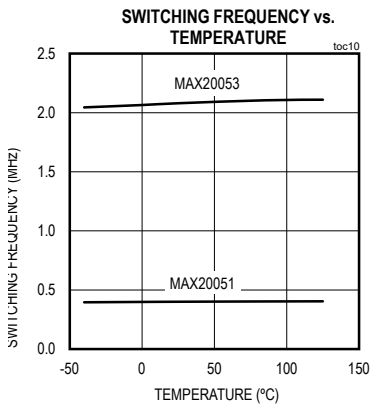
Typical Operating Characteristics

($V_{IN} = 12V$, $V_{REF1} = 1.2V$, $V_{PWM} = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)

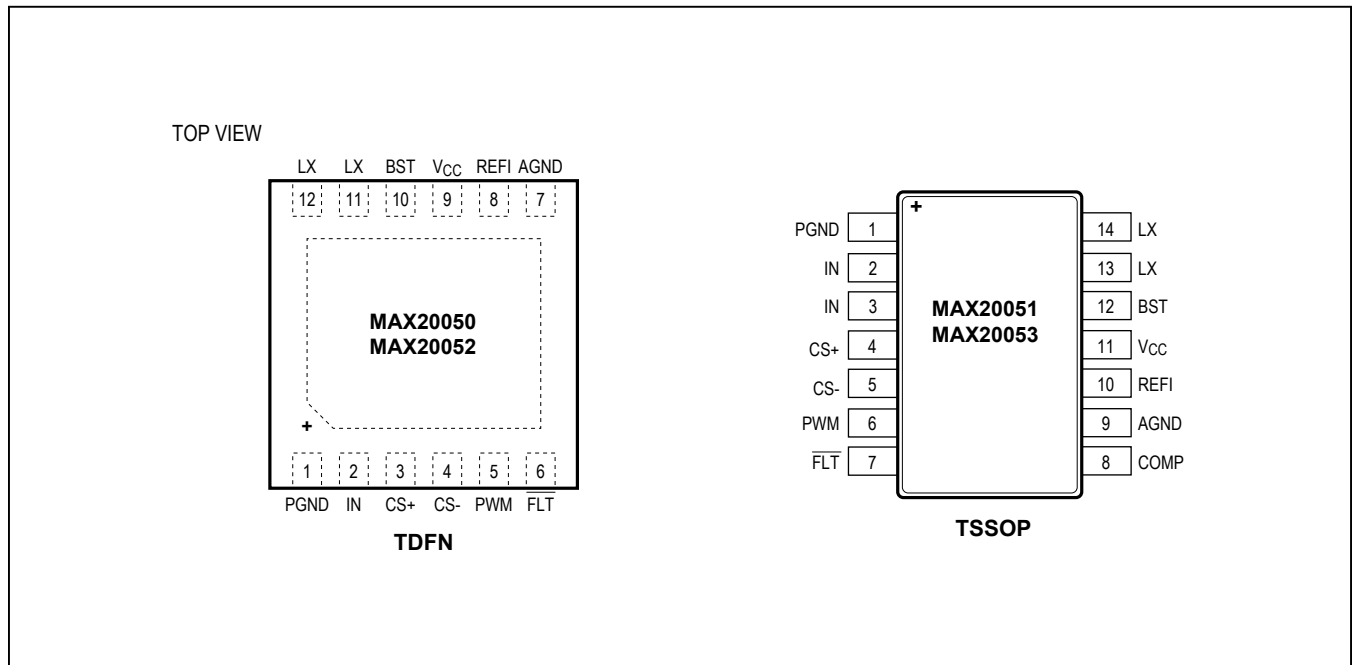


Typical Operating Characteristics (continued)

($V_{IN} = 12V$, $V_{REF1} = 1.2V$, $V_{PWM} = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted.)



Pin Configurations



Pin Descriptions

TDFN	TSSOP	NAME	FUNCTION
MAX20050 MAX20052	MAX20051 MAX20053		
1	1	PGND	Power Ground
2	2, 3	IN	Power-Supply Input. Bypass to PGND with a minimum of 1µF ceramic capacitor.
3	4	CS+	Current-Sense Positive Pin. This is the positive input of the high-side average current-mode control amplifier. See the <i>Programming the LED Current</i> section for information on setting the resistor value. The output inductor and current-sense resistor are connected at this node.
4	5	CS-	Current-Sense Negative Pin. This is the negative input of the high-side average current-mode control amplifier. See the <i>Programming the LED Current</i> section for information on setting the resistor value. This node goes to the anode of the LED string. One end of the current-sense resistor connects to this pin.
5	6	PWM	Logic-Level Dimming Input. Drive PWM low to turn off the current regulator. Drive PWM high to enable the current regulator. If PWM is driven low for greater than 210ms, the device turns off.

Pin Descriptions (continued)

TDFN	TSSOP	NAME	FUNCTION
MAX20050 MAX20052	MAX20051 MAX20053		
6	7	$\overline{\text{FLT}}$	Open-Drain Fault Output. Refer to the Fault Pin Behavior section for information on Fault.
—	8	COMP	Compensation Output (MAX20051/MAX20053). Connect an external RC network for loop compensation. The MAX20050/MAX20052 are internally compensated.
7	9	AGND	Analog Ground
8	10	REFI	Analog Dimming-Control Input. Connect an analog voltage from 0 to 1.2V for analog dimming of LED current.
9	11	V _{CC}	5V Regulator Output. Connect a 1 μ F ceramic capacitor to AGND from this pin for stable operation.
10	12	BST	High-Side Power Supply for Gate Drive. Connect a 0.1 μ F ceramic capacitor from BST to LX.
11, 12	13, 14	LX	Switching Node. Connect to one end of output inductor.
—	—	EP	Exposed Pad. Connect EP to a large-area ground plane for effective power dissipation. Connect EP to AGND. Do not use as the only ground connection,

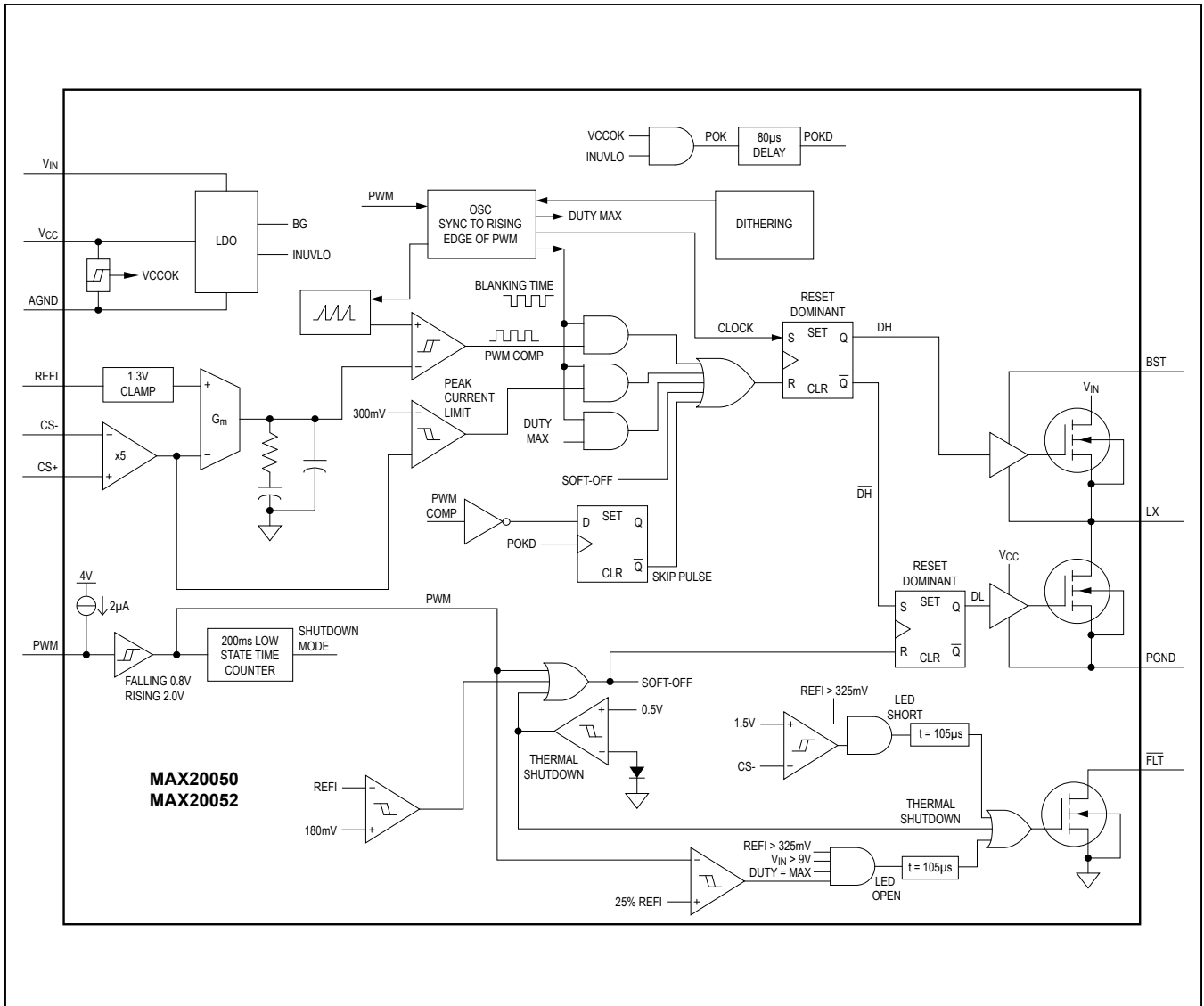


Figure 1. Block Diagram of the MAX20050/MAX20052

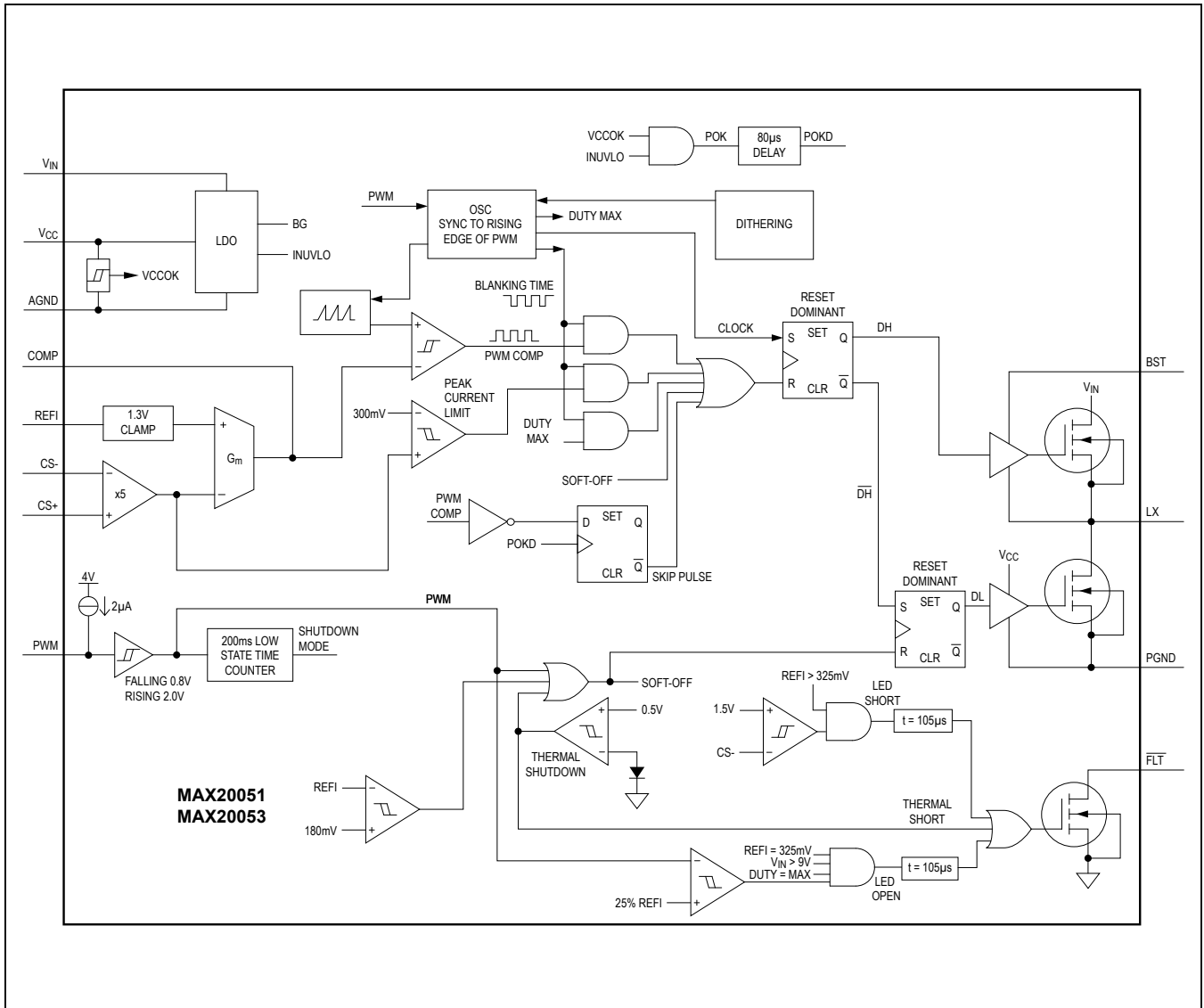


Figure 2. Block Diagram of the MAX20051/MAX20053

Detailed Description

The MAX20050–MAX20053 are HB LED drivers for automotive exterior lighting applications. Consisting of a fully synchronous step-down converter with integrated MOSFETs, the devices are capable of driving a series string of LEDs at up to 2A, with a minimum number of external components. The MAX20050/MAX20052 utilize internal loop compensation to minimize component count, while the MAX20051/MAX20053 use external compensation for full flexibility.

The wide 4.5V to 65V input supply range supports extreme automotive cold-crank and load-dump conditions. A low- and high-switching frequency option (400kHz or 2.1MHz) provides the designer with the flexibility to optimize for solution size or efficiency, while avoiding interference within the AM band. Spread spectrum provides further options for the designer to reduce EMI at the system level. The MAX20050/MAX20051 have an internal switching frequency of 400kHz, while the MAX20052/MAX20053 have an internal switching frequency of 2.1MHz.

High-side current regulation means only a single connection to the LED string is required; grounding of the string can be done locally. In addition to PWM dimming, the ICs provide analog dimming using the REF1 pin. Full-scale current regulation accuracy is $\pm 2.5\%$, while the accuracy is $\pm 8\%$ at 10% of full scale, over the full temperature range of -40°C to $+125^{\circ}\text{C}$. A 5V, 10mA LDO output is available for biasing other circuits.

Fault-protection mechanisms include output overload, short-circuit, and device overtemperature protections.

Functional Operation of MAX20050–MAX20053

The MAX20050–MAX20051 are monolithic, constant frequency average current mode step-down DC-DC LED drivers. A fixed frequency internal oscillator sets the switching frequency of the devices. For the MAX20050/MAX20051, the switching frequency is set at 400kHz, and for the MAX20052/MAX20053, the switching frequency is set at 2.1MHz. Spread spectrum is added to the internal oscillator to improve the EMI performance of the LED driver at higher frequencies. The oscillator turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the internal PWM comparator trips and turns off the

top power switch. The duty cycle at which the top switch turns off is controlled by an internal PWM comparator that has the output of an error amplifier going to the negative input of the comparator and a saw tooth ramp going to the positive input of the comparator. The error amplifier is a transconductance amplifier that compares the analog control voltage REF1 with an amplified current sense signal. The output of the error amplifier is then fed to a PWM comparator. The other input of the PWM comparator is a saw tooth ramp with a peak to peak voltage of 2.25V. The REF1 voltage programs the LED current. When the top power switch turns off, the synchronous power switch at the bottom turns on until the next clock cycle begins. The current sense signal is derived by a current sense resistor in series with the output inductor. This current sense signal is amplified by a factor of 5 and is then fed to the input of the error amplifier. This amplified signal is also fed to a comparator input which compares the amplified current sense signal with a 300mV reference. If the amplified current sense signal exceeds 300mV, then the top switch is immediately turned off independent of the PWM comparator and the bottom synchronous switch is turned on until the start of the next oscillator cycle. In the MAX20050/MAX20052, the output of the error amplifier is not available and the loop compensation is fixed inside the device. In the MAX20051/MAX20053, the output of the error amplifier appears on a pin and the loop can be compensated externally.

The device also includes a PWM dimming input that is used for PWM dimming of the LED current. When this signal is low both, the top and bottom switches are turned off and when the PWM signal goes high the inductor current is controlled by the device. The rising edge of the PWM signal also restarts the internal oscillator allowing the top switch to be turned on at the same instant as the rising edge of the PWM signal. This provides consistent dimming performance at low dimming duty cycles. The PWM signal can also be used as an enable input where if the PWM signal stays low for a period exceeding 200ms the device goes into a shutdown mode. In shutdown mode, the quiescent current drawn by the device goes to $5\mu\text{A}$ at an input of 12V.

The devices also feature a fault flag that indicates open or shorts on the output. Thermal shutdown shuts down the devices to protect them from damage at high temperatures.

Analog Dimming

The devices have an analog dimming-control input (REFI). The voltage at REFI sets the LED current level when $V_{REFI} \leq 1.2V$. For $V_{REFI} > 1.2V$, REFI is clamped to 220mV (typ). The maximum withstand voltage of this input is 5.5V. The LED current is guaranteed to be at zero when the REFI voltage is at or below 0.18V. The LED current can be linearly adjusted from zero to full scale for the REFI voltage in the range of 0.2V to 1.2V.

High-Side Current Sense (CS+, CS-)

A resistor is connected between the inductor and the anode of the LED string to program the maximum LED current. The full-scale signal is 200mV. The CS+ pin should be connected to the positive terminal of the current-sense resistor (inductor side) and the CS- pin should be connected to the negative terminal of the current-sense resistor (LED string anode side).

PWM Dimming Control (PWM)

A low signal on this pin turns off both the high- and low-side MOSFETs. For the MAX20051/MAX20053, a logic-low on this pin also disconnects the external compensation components on the COMP pin from the internal loads. If this pin is not used, connect it to V_{CC} . The device goes into shutdown mode if there is no positive-going dimming pulse for 210ms. In shutdown mode, the input current is less than 5 μ A (typ).

5V Regulator (V_{CC})

A regulated 5V output is provided for biasing other circuitries up to 10mA load. Bypass V_{CC} to AGND with a minimum of 1 μ F ceramic capacitor as close as possible to the device.

Input Voltage (IN)

The input supply pin (IN) must be locally bypassed with a minimum of 1 μ F capacitance close to the pin. All the input current that is drawn by the LED driver goes through this pin. The positive terminal of the bypass capacitor must be placed as close as possible to this pin and the negative terminal of the bypass capacitor must be placed as close as possible to the PGND pin.

Switching Node (LX)

The source of the internal high-side switching MOSFET and the drain of the low-side synchronous switching MOSFET is connected to these pins. Connect these pins together externally and connect them to the inductor and the boost capacitor. The $R_{DS(ON)}$ of both the high- and low-side switching MOSFETs is 0.3 Ω maximum at a junction temperature of +125°C.

Boost Capacitor Node (BST)

The BST pin is used to provide a drive voltage to the high-side switching MOSFET that is higher than the input voltage. An internal diode is connected from BST to V_{CC} . Connect a 0.1 μ F ceramic capacitor from this pin to the LX pins. Place the capacitor as close as possible to this pin.

Power Ground (PGND)

The source of the internal low-side power MOSFET is connected to this pin. Place the negative terminal of the input bypass capacitor as close as possible to the PGND pin.

Analog Ground (AGND)

This is the analog ground pin for all the control circuitry of the LED driver. Connect the PGND and the AGND together at the negative terminal of the input bypass capacitor.

**Compensation (COMP)
(MAX20051/MAX20053)**

The COMP pin is present in the MAX20051/MAX20053. Connect the external compensation network to this pin for stable loop compensation.

Fault Pin Behavior

The \overline{FLT} pin is an open-drain output. See the [LED Open](#) and [LED Short](#) sections.

LED Open

The LED open is detected when the following conditions are true at the same time for a period longer than 105 μ s:

- Input voltage > 9V
- REFI > 325mV
- Current sense < 25% expected REFI value
- Max duty cycle

If a LED open is detected and the input voltage goes below 9V or REF1 goes below 325mV, the $\overline{\text{FLT}}$ flag remains asserted until the input voltage goes above 9V and REF1 goes above 325mV. If PWM is high and a LED open occurs, the $\overline{\text{FLT}}$ pin asserts after a deglitch period of 105 μs . When the PWM goes low, the $\overline{\text{FLT}}$ status is latched. LED open condition cannot be detected if PWM pulse width is shorter than the maximum mask timer period of 300 μs .

The LED open condition cannot be detected if the PWM pulse width is shorter than the mask timer period. The mask timer counter uses an internal clock (15 μs typical period) to perform the mask timing measurement. If the PWM dimming pulse is in the range of 140 μs to 300 μs , there is a timing window of 1-clock cycle width (210 μs -225 μs typical), where the $\overline{\text{FLT}}$ pin can toggle between high and low state from one PWM dimming pulse to another in case of an LED open fault. If the PWM pulse width is longer than the mask timer period and an LED open fault is detected, the $\overline{\text{FLT}}$ flag goes low. Once the open LED fault condition disappears, the $\overline{\text{FLT}}$ flag goes high.

LED Short

The LED short is detected when the following two conditions are true at the same time for a period longer than 105 μs :

- REF1 > 325mV
- Output voltage < 1.5V

After LED short is recovered, the fault flag is deasserted, irrelevant to the input voltage.

Thermal Shutdown

The $\overline{\text{FLT}}$ pin goes low when thermal shutdown is activated.

Exposed Pad

The device package features an exposed thermal pad on its underside that should be used as a heat sink. This pad lowers the package's thermal resistance by providing a direct heat-conduction path from the die to the PCB. Connect the exposed pad and AGND together using a large pad or ground plane, or multiple vias to the AGND plane layer.

Inductor Peak Current-Limit Comparator

The peak current comparator provides a path for fast cycle-by-cycle current limit during extreme fault conditions. The average current-limit threshold, set by the REF1 voltage, limits the output current during short circuit.

Spread-Spectrum Modulation

The devices include a unique spread-spectrum mode that reduces emission (EMI) at the switching frequency and its harmonics.

The spread spectrum uses a pseudorandom dithering technique, where the switching frequency is varied in the range of 400kHz \pm 3% for the MAX20050/MAX20051 and 2.1MHz \pm 3% for the MAX20052/MAX20053.

Instead of a large amount of spectral energy present at multiples of the switching frequency, the total energy at the fundamental and each harmonic is spread over a wider bandwidth, reducing the energy peak.

Thermal Protection

The devices feature thermal protection. When the junction temperature exceeds +165°C, the LX pin starts operating at the minimum pulse width to reduce the power dissipation in the internal power MOSFETs. The part returns to regulation mode once the junction temperature goes below +155°C. This results in a cycled output during continuous thermal-overload conditions.

High-Side Current-Sense Amplifier

The devices feature a high-bandwidth, high-side current-sense amplifier that is used to sense the inductor current. The gain of this current-sense amplifier is 5. The differential voltage between CS+ and CS- is fed to the internal high-side current-sense amplifier. This amplified signal is then transferred to the low side and is then connected to the negative input of an internal transconductance amplifier. The 3dB bandwidth of the high-side current-sense amplifier is 1.5MHz.

Internal Transconductance Amplifier

The devices have a built-in transconductance amplifier used to amplify the error signal inside the feedback loop. The output of the high-side current-sense amplifier, plus an offset voltage of 0.2V, is fed to the negative input of this internal transconductance amplifier. The positive input is the voltage on the REF1 pin. In the case of the MAX20050/MAX20052, the loop of this amplifier is internally compensated and is not available as an output pin. In the case of the MAX20051/MAX20053, the output of this amplifier is available on the COMP pin and can be compensated with an external compensation network. The transconductance of this amplifier is 600 μS .

Applications Information

Programming the LED Current

Normal sensing of the LED current should be done on the high side where the LED current-sense resistor is connected to the inductor. The other side of the LED current-sense resistor goes to the anode of the external LED string. The LED current is programmed using R_{CS} (see Figure 3). When REF1 is left open, the voltage at REF1 is clamped to 1.3V. When REF1 is open, the internal reference regulates the voltage across R_{CS} to 220mV. The current is given by:

$$I_{LED} = \frac{0.220}{R_{CS}}$$

The LED current can also be programmed using the voltage on REF1 when $V_{REF1} \leq 1.2V$ (analog dimming). The current is given by:

$$I_{LED} = \frac{(V_{REF1} - 0.2)}{(5 \times R_{CS})}$$

Inductor Selection

The peak inductor current, selected switching frequency, and the allowable inductor current ripple determine the value and size of the output inductor. The MAX20050/MAX20051 have an internal switching frequency of

400kHz, whereas the MAX20052/MAX20053 have a switching frequency of 2.1MHz. Selecting a higher switching frequency reduces the inductance requirements, but at the cost of efficiency. The charge/discharge cycle of the gate capacitance of the internal switching MOSFET's gate and drain capacitance create switching losses, which worsen at higher input voltages since the switching losses are proportional to the square of the input voltage. Choose inductors from the standard high-current, surface-mount inductor series available from various manufacturers. High inductor ripple current causes large peak-to-peak flux excursion, increasing the core losses at higher frequencies.

For the typical operating circuit of Figure 4 ($V_{IN} = 12V$), the inductor value has to be in the range of 22µH to 33µH for the MAX20050 and in the range of 10µH to 68µH for the MAX20052. For the typical application circuit of Figure 5 ($V_{IN} = 24V$), the inductor value has to be in the range of 33µH to 82µH for the MAX20050. For the typical application circuit of Figure 6 ($V_{IN} = 40V$ to 60V), the inductor value has to be in the range of 47µH to 150µH for the MAX20050. For the MAX20051/MAX20053, the inductor value can be optimized further and can be higher or lower than the values suggested for the MAX20050/MAX20052. The MAX20051/MAX20053 have an external compensation pin for loop stability and this gives more flexibility for output inductor values.

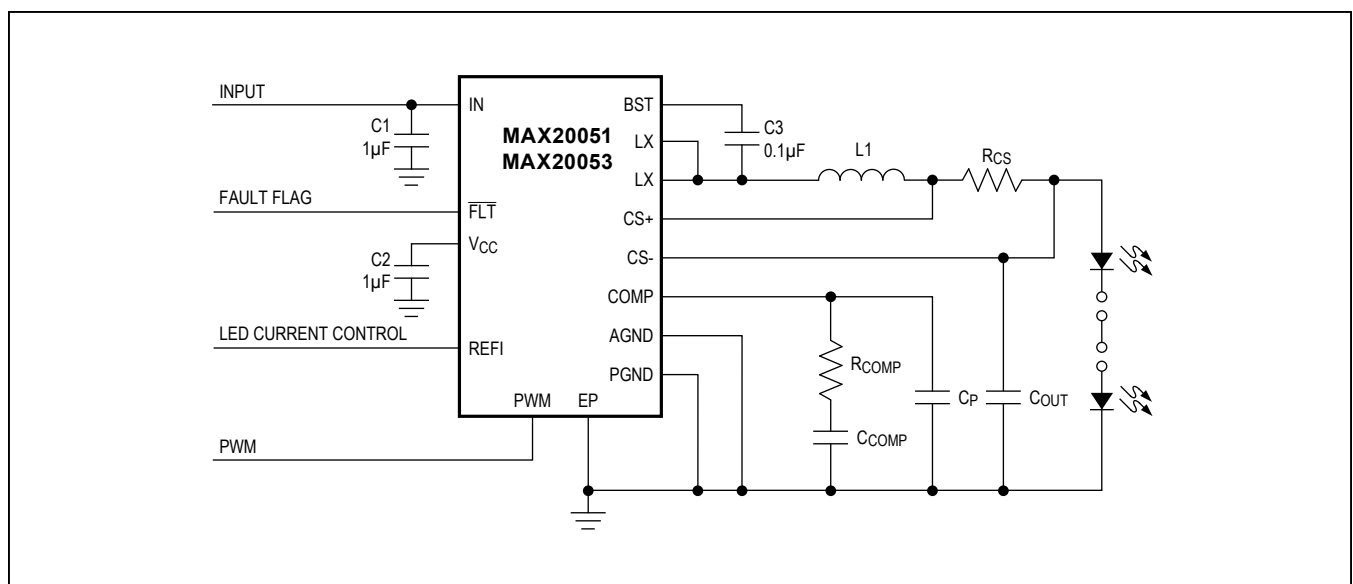


Figure 3. Typical Application Circuit Using the MAX20051

Input Capacitor

The discontinuous input-current waveform of the buck converter causes large ripple currents in the input capacitor. The switching frequency, peak inductor current, and the allowable peak-to-peak voltage ripple reflected back to the source dictate the capacitance requirement. The input ripple is comprised of ΔV_Q (caused by the capacitor discharge) and ΔV_{ESR} (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. A 1 μ F ceramic capacitor is recommended for most applications.

Output Capacitor

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and the bulk capacitance of the output capacitor contribute to the output ripple. In most applications, using low-ESR ceramic capacitors can dramatically reduce the output ESR and

ESL effects. To reduce the ESL effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance.

The output capacitance C_{OUT} is calculated using the following equation:

$$C_{OUT} = \frac{((V_{IN_MIN} - V_{LED}) \times V_{LED})}{(\Delta V_R \times 2 \times L \times V_{IN_MAX} \times f_{SW}^2)}$$

where ΔV_R is the maximum allowable voltage ripple.

The output capacitance for MAX20050 in [Figure 4](#) has to be in the range of 0.22 μ F to 4.7 μ F for a stable operation. The output capacitance for MAX20052 has to be in the range of 0.1 μ F to 4.7 μ F. For the application circuit of [Figure 5](#), the output capacitance has to be in the range of 0.47 μ F to 4.7 μ F for the MAX20050. For the application circuit of [Figure 6](#), the output capacitance has to be in the range of 0.1 μ F to 2.2 μ F for the MAX20050.

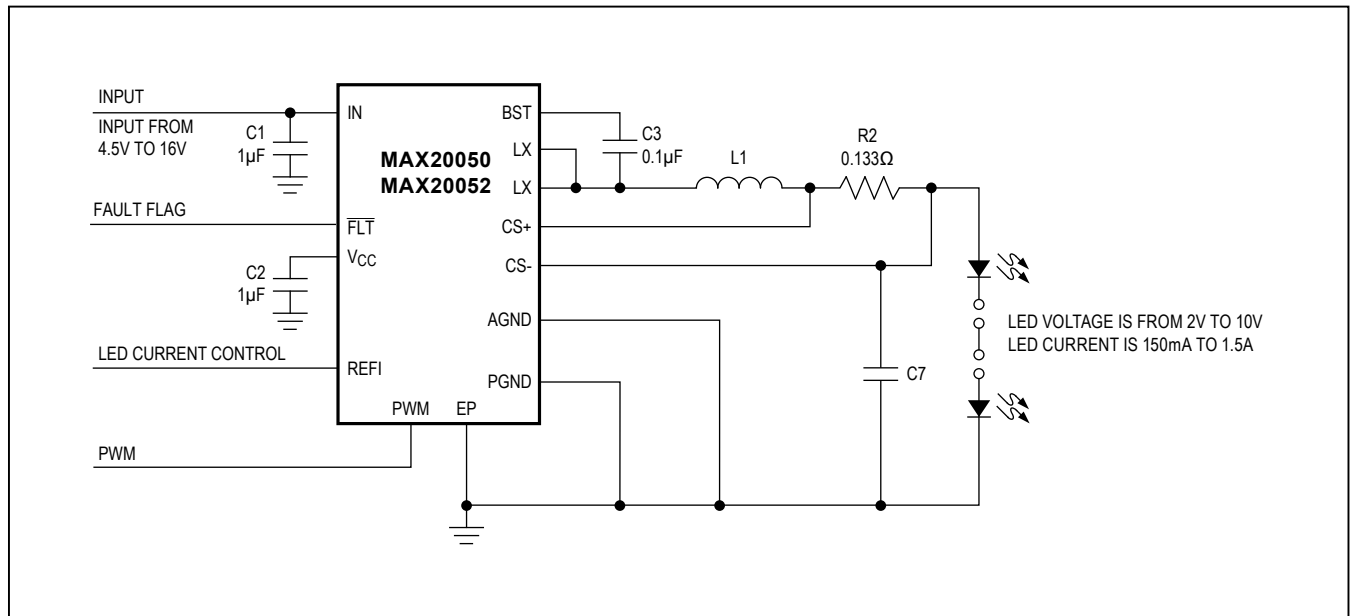


Figure 4. Typical Input Voltage (12V)

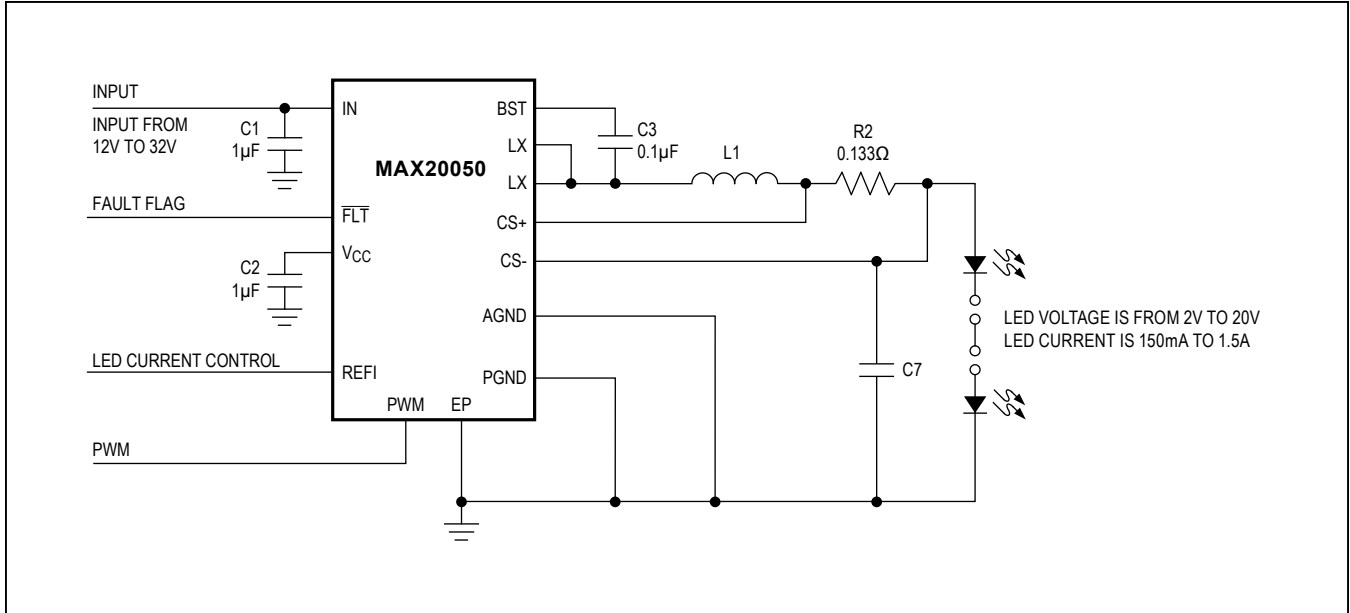


Figure 5. Typical Input Voltage (24V)

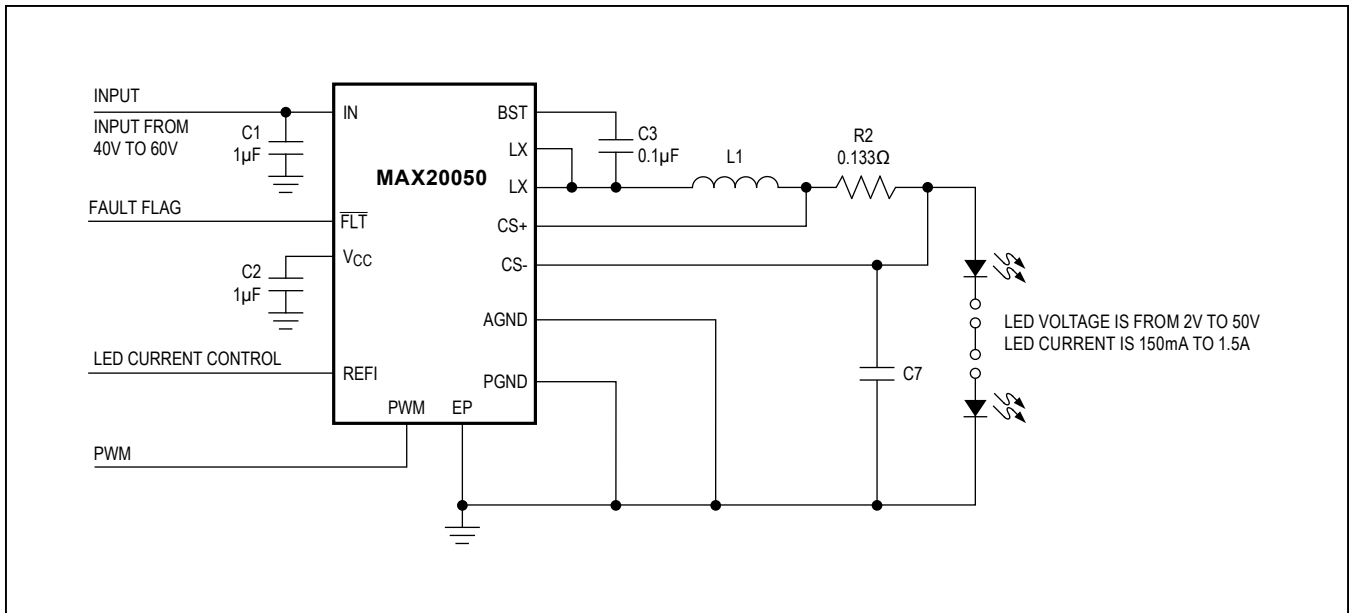


Figure 6. Typical Input Voltage (50V)

Table 1. Suggest L–C Network for Internally Compensated Parts

L AND C COMPONENT VALUES (MAX20050, f _{SW} = 400kHz)					
Output Capacitor Range (C7)		V _{IN} = 12V (typ), Figure 4	0.22	4.7	μF
		V _{IN} = 24V (typ), Figure 5	0.47	4.7	
		V _{IN} = 55V (typ), Figure 6	0.1	2.2	
Inductor Range (L1)		V _{IN} = 12V (typ), Figure 4	22	33	μH
		V _{IN} = 24V (typ), Figure 5	33	82	
		V _{IN} = 55V (typ), Figure 6	47	150	
L AND C COMPONENT VALUES (MAX20050, f _{SW} = 2.1MHz)					
Output Capacitor Range (C7)		V _{IN} = 12V (typ), Figure 4	0.1	4.7	μF
Inductor Range (L1)		V _{IN} = 12V (typ), Figure 4	10	68	μH

Compensation

The MAX20050/MAX20052 have internal loop compensation and there is no user-available adjustability of the loop compensation components. In the case of the MAX20051/MAX20053, an external COMP pin is present and an external compensation network is required for stable operation. See Figure 3 for the typical application circuit using the MAX20051.

The compensator should be designed as follows. The high-side current sense amplifier introduces a high-frequency pole to around 420kHz. This is close to the switching frequency. The current loop gain is:

$$T_i(s) = \frac{F_m V_{IN}}{R} \times \frac{(1 + sR_{COUT})}{\left(1 + s\frac{L}{R} + s^2 LC_{OUT}\right)} \times \frac{G_m (sC_{COMP} R_{COMP} + 1) 5R_{CS}}{s_{COMP} \left(1 + \frac{s}{w_p}\right)}$$

where G_m is the transconductance of the error amplifier inside the MAX20051/MAX20053, R_{CS} is the current sense resistor, R is the total dynamic resistance of the LED string, L is the inductance, R_{COMP} is the compensation resistor, C_{OUT} is the output capacitance, w_p is the pole from the high side current sense amplifier at 2πfp and F_m is the modulator gain that is given by:

$$F_m = \frac{1}{(s_e + s_n)T_s}$$

where T_s is 1/fs where fs is the switching frequency, s_e is the dv/dt of the ramp in the PWM comparator which is 2.25fs and s_n is the dv/dt of the voltage from the output of the G_m amplifier.

In the MAX20051 the compensation zero formed by R_{COMP}C_{COMP} should be set at 20kHz and for the MAX20053 at 100kHz. Initially, the value of the capacitor C_{COMP} can be calculated by the formula:

$$C_{COMP} = \frac{G_m}{\left(0.5 + \frac{1}{\pi}\right) F_m V_{IN} R_{CS} w_z}$$

where w_z is the zero at R_{COMP}C_{COMP} and f_s is the switching frequency. Initially, F_m is assumed as 0.555 and the initial values of C_{COMP} is calculated and then R_{COMP} is calculated based on the zero location at 20kHz for the MAX20051 and 100kHz for the MAX20053. The values of R_{COMP}, C_{COMP}, and C_P may need to be optimized further when testing, so as to get the optimum loop response.

LED Current Derating Using REFI

The MAX20050–MAX20053 are designed specifically for driving high current LEDs. High current LEDs require derating the maximum current based on operating temperature to prevent damage of the LEDs. Some LEDs come with an accompanying thermistor in the same package. The thermistor may be an NTC. Under normal operating conditions the voltage on the REFI pin is above the clamp voltage of the MAX20050–MAX20053. See Figure 7. As the temperature of the LEDs increase, the

resistance R1 decreases until the voltage on the REF1 pin reaches 1.3V. The resistors R2 and R1 should be selected so that the voltage on REF1 is 1.3V at the desired temperature T1. It may also be necessary that at a certain temperature T2, the current in the LEDs are close to zero. At this temperature, the voltage on REF1 pin is:

$$1.3 = \frac{V_{CC} \times R1(T1)}{(R1(T1) + R2)}$$

where V_{CC} is 5V and R1(T1) is the resistance of the resistor from REF1 to ground at temperature T1 and R2 is the resistance from V_{CC} to REF1.

$$0.2 = \frac{V_{CC} \times R1(T2)}{(R1(T2) + R2)}$$

where R1(T2) is the resistance of the resistor of the resistor from REF1 to ground at temperature T2. In some cases, the NTC in the LED can be used as is and in others, an additional resistor in series or in parallel or some other combination may need to be added to provide the desired resistance.

PCB Layout

For proper operation and minimum EMI, PCB layout should follow the guidelines below (also see [Figure 8](#)):

- 1) Large switched currents flow in the IN and PGND pins and the input capacitor C1 of [Figure 3](#). The loop formed by the input capacitor should be as small as possible by placing this capacitor as close as possible to the IN and PGND pins. The input capacitor, device, output inductor, and output capacitor should be placed on the same side of the PCB and the connections should be made on the same layer.
- 2) Place an unbroken ground plane on the layer closest to the surface layer with the inductor, device, and the input and output capacitors.
- 3) The surface area of the LX and BST nodes should be as small as possible to minimize emissions.
- 4) The exposed pad on the bottom of the package must be soldered to ground so that the pad is connected to ground electrically and also acts as a heat sink thermally. To keep thermal resistance low, extend the ground plane as much as possible, and add thermal vias under and near the device to additional ground planes within the circuit board.

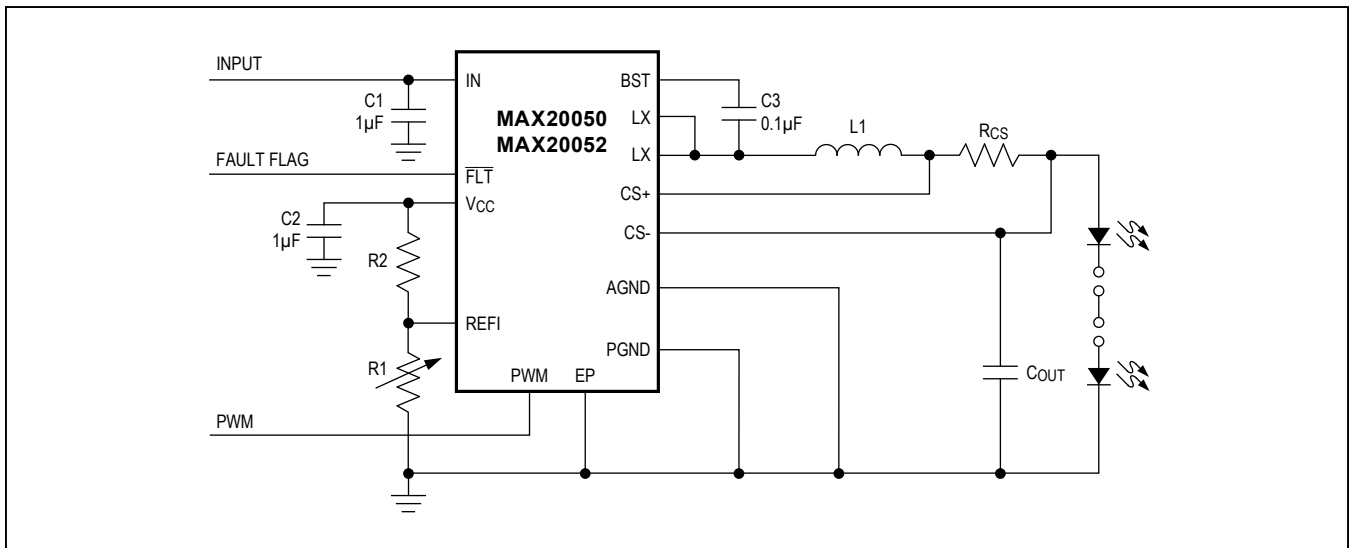


Figure 7. Application Circuit for LED Current Derating with Temperature

- 5) Run the current-sense lines (CS+ and CS-) very close to each other to minimize the loop area. Do not cross these critical signal lines with power circuitry. Sense the current right at the pads of the current-sense resistors. The current-sense signal has a full-scale amplitude of 200mV. To prevent contamination of this signal from high dv/dt and high di/dt components and traces, use a ground plane layer to separate the power traces from this signal trace.
- 6) Use separate ground planes on different layers of the PCB for AGND and PGND. Connect both of these planes together at a single point close to the input bypass capacitor.
- 7) Use 2oz or thicker copper to keep trace inductances and resistances to a minimum. Thicker copper conducts heat more effectively, thereby reducing thermal impedance. Thin copper PCBs compromise efficiency in applications involving high currents.
- 8) Place capacitor C3 as close as possible to the BST and LX pins.

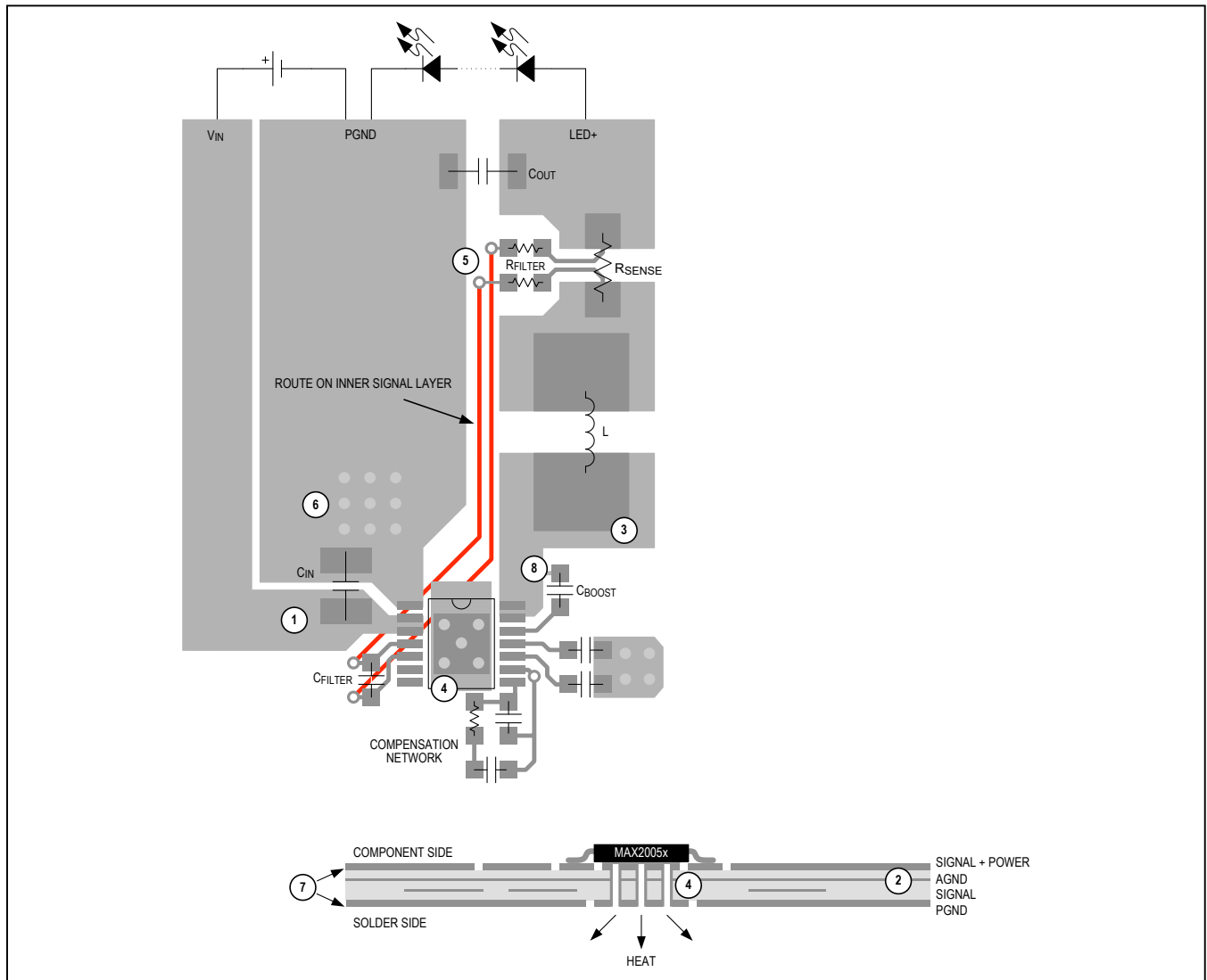


Figure 8. Section from MAX20051 EV Kit PCB Layout

Ordering Information

PART	TEMP RANGE	SWITCHING FREQUENCY	COMPENSATION	PIN-PACKAGE	BOND WIRE
MAX20050 ATC/V+	-40°C to +125°C	400kHz	Internal	12 TDFN-EP*	Copper
MAX20050ATC+	-40°C to +125°C	400kHz	Internal	12 TDFN-EP*	Copper
MAX20051 AAUD/V+	-40°C to +125°C	400kHz	External	14 TSSOP-EP*	Copper
MAX20051AUD/V+	-40°C to +125°C	400kHz	External	14 TSSOP-EP*	Gold
MAX20051AUD+	-40°C to +125°C	400kHz	External	14 TSSOP-EP*	Gold
MAX20052 ATC/V+	-40°C to +125°C	2.1MHz	Internal	12 TDFN-EP*	Copper
MAX20053 AAUD/V+	-40°C to +125°C	2.1MHz	External	14 TSSOP-EP*	Copper
MAX20053AUD/V+	-40°C to +125°C	2.1MHz	External	14 TSSOP-EP*	Gold

/V denotes an automotive qualified part.

+Denotes a lead(Pb)-free/RoHS-compliant package.

*EP = Exposed pad.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
12 TDFN-EP	TD1233+1C	21-0664	90-0397
14 TSSOP-EP	U14E+4	21-0108	90-0463

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/14	Initial release	—
1	11/14	Updated the LED Open-Fault Enable Threshold min/typ values in <i>Electrical Characteristics</i> table	4
2	12/15	Updated Current-Sense Input Offset, DMOS RDS _{ON} , and changed LED Open-Fault Enable Threshold, LED Open-Fault Enable Hysteresis in <i>Electrical Characteristics</i> table; changed LED Open and Logic V _{IN} from 10.5V to 9V in Figures 1 and 2 and in the <i>LED Open</i> section; added new Figure 8 in <i>PCB Layout</i> section	3, 4, 9, 10, 12, 13, 19
3	2/16	Updated V _{CC} Output Voltage in <i>Electrical Characteristics</i> table; removed future product designations in <i>Ordering Information</i> table	2, 20
4	5/16	Updated Figure 8	19
5	6/16	Added MAX20050ATC+ and MAX20051AUD+ to <i>Ordering Information</i> table	20
6	6/16	Added MAX20050ATC+T and MAX20051AUD+T to <i>Ordering Information</i> table	20
7	6/16	Changed land pattern number for TSSOP package in <i>Package Information</i> table	20
8	7/16	Updated PWM pin in Figures 1 and 2	9, 10
9	5/18	Added MAX20051AAUD/V+ and MAX20053AAUD/V+ to <i>Ordering Information</i> table, as well as a new column for Bond Wire	20

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

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