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# MAX20310

# Ultra-Low Quiescent Current PMIC with SIMO Buck-Boost for Wearable Applications

## General Description

The MAX20310 is a compact power management integrated circuit (PMIC) for space-constrained, battery-powered applications where size and efficiency are critical. The device combines two single inductor, multiple output (SIMO) buck-boosted outputs with two LDOs and other system power management features like a push-button monitor and sequencing controller.

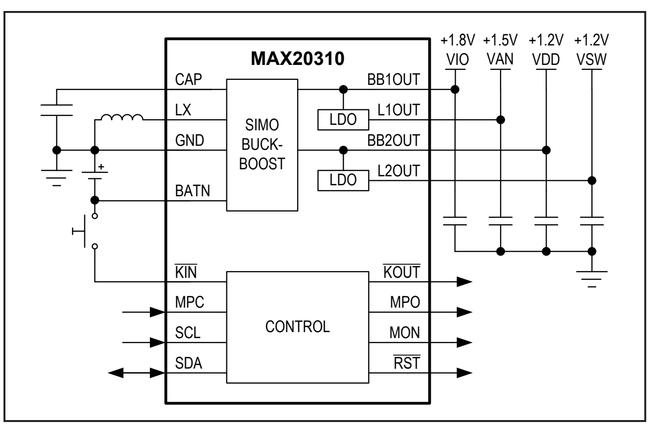
The device includes a SIMO buck-boost switching regulator that provides two programmable voltage rails using a single inductor, minimizing solution footprint. The MAX20310 operates with battery voltages down to 0.7V for use with Zinc Air, Silver Oxide, or Alkaline batteries. The architecture allows for output voltages above or below the battery voltage.

Additionally, the MAX20310 has two programmable low-dropout (LDO) linear regulators. The linear regulators can also operate as power switches that can disconnect the quiescent load of system peripherals.

The MAX20310 includes a programmable power controller that allows the device to be configured for use in applications that require a true off state or for always-on applications. This controller provides a delayed reset signal, voltage sequencing, and customized button timing for on/off control and recovery hard reset.

The device also features a multiplexer for monitoring the power inputs and outputs of each function. The MAX20310 is available in a 16-bump 0.4mm pitch 1.63mm x 1.63mm wafer-level package (WLP) and operates over the -40°C to +85°C extended temperature range.

## Typical Operating Circuit




## Benefits and Features

- Extend System Battery Use Time
  - Single Inductor, Multiple Output (SIMO) Ultra-Low $I_Q$ Buck-Boost Regulator
    - Battery Input Voltage from 0.7V to 2.0V
    - Output Voltage Programmable From 0.9V to 4.05V
    - 250mW Maximum Total Input Power
    - Incremental CAP Quiescent Current 1μA per channel
    - 84% Efficiency for 1.8V, 10mA Output
    - Input Current Limited
  - Dual Ultra-Low $I_Q$ 50mA LDO
    - Inputs Supplied by Dual Buck-Boost Outputs
    - Output Programmable from 0.5V to 3.65V
    - Quiescent Current 1.1μA per LDO / 600nA per Load Switch
    - Configurable as Load Switch
- Extend Product Shelf-Life
  - Battery Seal Mode
    - 10nA Battery Current (typ)
- Minimize Board Area
  - 1.63mm x 1.63mm WLP
- Easy-to-Implement System Control
  - Voltage Monitor Multiplexer
    - 1% Accurate Battery Inverter (±10mV at 1.0V)
  - Power Button Monitor
    - Buffered Output
  - Power Sequencing
  - Reset Output
  - $I^2C$ Control Interface

## Applications

- Wearable Medical Devices
- Wearable Fitness Devices
- Portable Medical Devices

***Ordering Information* appears at end of data sheet.**

*19-8611; Rev 2; 3/18*

## Absolute Maximum Ratings

(Voltages reference to GND unless otherwise noted)
CAP, BB1OUT, BB2OUT, L1OUT, L2OUT
MPC, SDA, SCL, $\overline{RST}$, $\overline{KOUT}$ to GND, BATN ....-0.3V to +6V
$\overline{KIN}$........................................... (BATN – 0.3V) to (GND + 0.3V)
LX to BATN.............................................................-0.3V to +6V
MPO, MON to BATIN ............................................-0.3V to +6V
GND to BATN .....................................................-0.3V to +2.2V
Continuous Current into LX, BATN ...................................+0.5A
Continuous Current into any other terminal ..................±100mA
Continuous Power Dissipation ($T_A$ = +70°C):
16-bump WLP 1.65mm x 1.65mm 0.4mm Pitch
(derate 17.4mW/°C above +70°C) .............................957mW
Operating Temperature Range.......................... -40°C to +85°C
Junction Temperature ...................................................+150°C
Storage Temperature Range ........................... -65°C to +150°C
Soldering Temperature (reflow) .....................................+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

| **PACKAGE TYPE: 16 WLP** | |
|---|---|
| Package Code | W161F1+1 |
| Outline Number | **21-0491** |
| Land Pattern Number | Refer to **Application Note 1891** |
| **THERMAL RESISTANCE, FOUR-LAYER BOARD** | |
| Junction to Ambient ($\theta_{JA}$) | 58°C/W |

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

## Electrical Characteristics

($V_{BAT}$ = +1.2V, $V_{BB1OUT}$ = +1.8V, $V_{BB2OUT}$ = +1.2V, $V_{L1OUT}$ = +1.5V, $V_{L2OUT}$ = +1.0V, $I_{BB1OUT}$ = $I_{BB2OUT}$ = $I_{L1OUT}$ = $I_{L2OUT}$ = 0A, $T_A$ = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at $T_A$ = +25°C) (Note 1) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| Seal Input Current | $I_{SEAL}$ | Seal mode, all functions disabled, $T_A$ = +25°C | | 0.01 | 0.2 | µA |
| $\overline{KIN}$ Pullup Resistor to GND | $\overline{KIN}_{PULLUP}$ | | | 465 | | kΩ |
| CAP Quiescent Current | $I_{Q\_CAP}$ | Buck-boost 1 enabled | | 4 | | µA |
| | | Buck-boost 1 and 2 enabled | | 5 | | µA |
| | | Buck-boost 1 and 2 and LDO 1 enabled | | 5.25 | | µA |
| | | Buck-boost 1 and 2 and LDO 1 and 2 enabled | | 5.5 | | µA |
| **POWER SEQUENCE** | | | | | | |
| Reset Time Accuracy | $t_{RST}$ | | -10 | | +10 | % |
| **BUCK-BOOST REGULATOR** | | | | | | |
| Input Voltage | $V_{BAT}$ | Operating | 0.7 | | 2 | V |
| | | Startup | 0.8 | | 2 | |
| Output Voltage Range | $V_{OUT}$ | 50mV steps, (Note 3) | 0.9 | | 4.05 | V |
| Quiescent Supply Current From CAP | $I_{Q\_BB}$ | Burst mode, no switching, $V_{BB\_OUT}$ = +1.8V | | 1 | | µA |
| Output Accuracy | $V_{OUT\_ACC\_BB\_OUT}$ | $T_A$ = +25°C | -1 | | 1 | % |
| | | $T_A$ = 0°C to +85°C | -1.8 | | +1.8 | |
| | | $T_A$ = -40°C to +85°C | -3 | | +3 | |
| Power Supply Rejection Ratio | PSRR | $C_{BB\_OUT}$ = 10µF | | 40 | | dB |
| Maximum Input Power | $P_{IN}$ | (Note 5) | 250 | | | mW |
| Maximum Input Current | $I_{IN}$ | $V_{BB\_OUT}$ = +1.8V | | 200 | | mA |
| | | $V_{BB\_OUT}$ = +3.3V | | 244 | | |
| Short-Circuit Current Limit | $I_{LIM}$ | Maximum programmable current setting | | 0.6 | | A |
| Passive Discharge Resistance | $R_{PAS\_BB\_OUT}$ | | | 10 | | kΩ |
| **LDO** | | | | | | |
| Quiescent Supply Current | $I_{Q\_LDO}$ | LDO UVLO enabled | | 1.1 | 2 | µA |
| | | Switch mode, $V_{BB\_OUT}$ = +1.8V | | 0.4 | | |
| Quiescent supply Current in Dropout | $I_{Q\_LDO\_D}$ | $V_{BB\_OUT}$ = $V_{LDO\_SET}$ – 0.1V | | 1.7 | 3.5 | µA |
| Maximum Output Current | $I_{MAX\_LDO}$ | (Note 4) | 50 | | | mA |
| Output Voltage | $V_{OUT\_LDO}$ | 50mV steps | 0.5 | | 3.65 | V |

## Electrical Characteristics (continued)

($V_{BAT}$ = +1.2V, $V_{BB1OUT}$ = +1.8V, $V_{BB2OUT}$ = +1.2V, $V_{L1OUT}$ = +1.5V, $V_{L2OUT}$ = +1.0V, $I_{BB1OUT}$ = $I_{BB2OUT}$ = $I_{L1OUT}$ = $I_{L2OUT}$ = 0A, $T_A$ = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at $T_A$ = +25°C) (Note 1) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Output Accuracy | $V_{OUT\_ACC\_LDO}$ | $V_{BB\_OUT}$ = ($V_{LDO\_SET}$ + 0.5V) or higher, $I_{LOAD}$ = 1mA | $T_A$ = 0°C to +85°C | -3 | | 3 | % |
| | | | $T_A$ = -40°C to +85°C | -3.5 | | +3.5 | |
| Dropout Voltage | $V_{DROP\_LDO}$ | $V_{BB\_OUT}$ = $V_{LDO\_SET}$ = +1.8V, $I_{LOAD}$ = 50mA | | | | 100 | mV |
| Line Regulation | $LINEREG_{LDO}$ | $V_{BB\_OUT}$ = ($V_{LDO\_SET}$ + 0.5V) to +4.05V | | -1 | | 1 | %/V |
| Load Regulation | $LOADREG_{LDO}$ | $I_{LOAD}$ = 50µA to 50mA | | | 0.003 | | %/mA |
| Passive Discharge Resistance | $R_{PAS\_LDO}$ | | | | 10 | | kΩ |
| Power Switch Mode Resistance | $R_{ON\_LS}$ | $V_{BB\_OUT}$ = +1.2V | | | | 1 | Ω |
| Turn-On Time | $t_{ON\_SLOPE}$ | $I_{LDO\_OUT}$ = 0mA | | | 0.7 | | V/µs |
| | | $I_{LDO\_OUT}$ = 0mA. Switch mode. | | | 2.8 | | |
| Thermal Shutdown Threshold | $T_{SD}$ | $T_J$ rising | | | 150 | | °C |
| Thermal Shutdown Hysteresis | $T_{HYS}$ | | | | 21 | | °C |
| **MONITOR MULTIPLEXER** | | | | | | | |
| MON Impedance | $R_{MON}$ | Sense pin voltage > +0.5V | | | | 500 | Ω |
| Battery Voltage Buffer Precision | $V_{BAT\_OFF}$ | | | -10 | | 10 | mV |
| **DIGITAL SIGNALS** | | | | | | | |
| SDA, SCL, MPC Input Logic-High | $V_{IH}$ | | | 1.4 | | | V |
| SDA, SCL, MPC Input Logic-Low | $V_{IL}$ | | | | | 0.5 | V |
| SDA, $\overline{RST}$, $\overline{KOUT}$ Output Logic-Low | $V_{OL}$ | $I_{OL}$ = 4mA | | | | 0.4 | V |
| MPO Output Logic-Low | $V_{OL\_MPO}$ | $I_{OL}$ = 4mA to GND | | | | 0.4 | V |
| | | $I_{OL}$ = 4mA to BATN | | | | 0.4 | |
| SCL Clock Frequency | $f_{SCL}$ | (Note 5) | | 0 | | 400 | kHz |
| Bus Free Time Between a STOP and START Condition | $t_{BUF}$ | | | 1.3 | | | µs |

## Electrical Characteristics (continued)

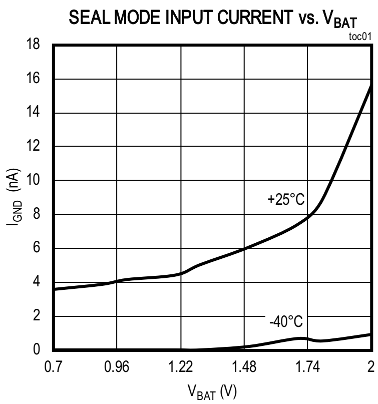
($V_{BAT}$ = +1.2V, $V_{BB1OUT}$ = +1.8V, $V_{BB2OUT}$ = +1.2V, $V_{L1OUT}$ = +1.5V, $V_{L2OUT}$ = +1.0V, $I_{BB1OUT}$ = $I_{BB2OUT}$ = $I_{L1OUT}$ = $I_{L2OUT}$ = 0A, $T_A$ = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at $T_A$ = +25°C) (Note 1) (Note 2)

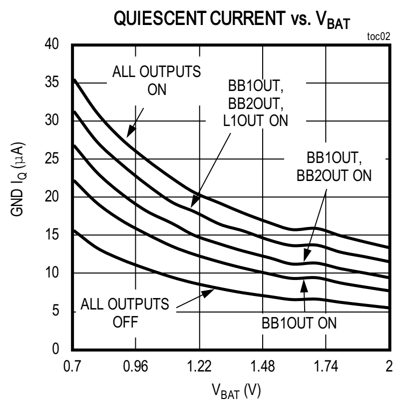
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| START Condition (Repeated) Hold Time | $t_{HD:STA}$ | (Note 6) | 0.6 | | | µs |
| Low Period of SCL Clock | $t_{LOW}$ | | 1.3 | | | µs |
| High Period of SCL Clock | $t_{HIGH}$ | | 0.6 | | | µs |
| Setup Time for a Repeated START Condition | $t_{SU:STA}$ | | 0.6 | | | µs<br>µs |
| Data Hold Time | $t_{HD:DAT}$ | (Notes 7, 8) | 0 | | | µs |
| Data Setup Time | $t_{SU:DAT}$ | (Note 7) | 100 | | | ns |
| Setup Time for STOP Condition | $t_{SU:STO}$ | | 0.6 | | | µs |

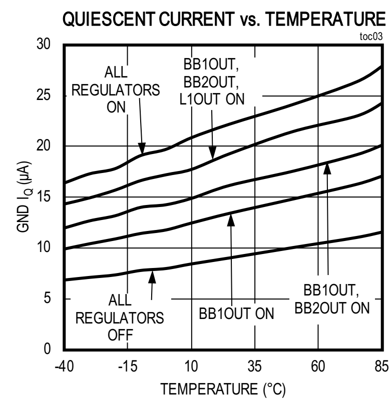
**Note 1:** All devices are 100% production tested at $T_A$ = +25°C. Limits over the operating temperature range are guaranteed by design.
**Note 2:** $V_{BAT}$ refers to the voltage across the battery terminals; $V_{BAT}$ = $V_{GND}$ – $V_{BATN}$.
**Note 3:** Output voltage must not exceed $V_{BB\_OUT}$ - $V_{BATN}$ = 5.0V.
**Note 4:** Actual value may be limited by the lower of the capability of the source (battery) or the maximum input power of the MAX20310.
**Note 5:** Timing must be fast enough to prevent the device from entering sleep mode due to bus low for period > $t_{SLEEP}$.
**Note 6:** $f_{SCL}$ must meet the minimum clock low time plus the rise/fall times.
**Note 7:** The maximum $t_{HD:DAT}$ has to be met only if the device does not stretch the low period ($t_{LOW}$) of the SCL signal.
**Note 8:** The device internally provides a hold time of at least 100ns for the SDA signal (referred to the $V_{IH\_MIN}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

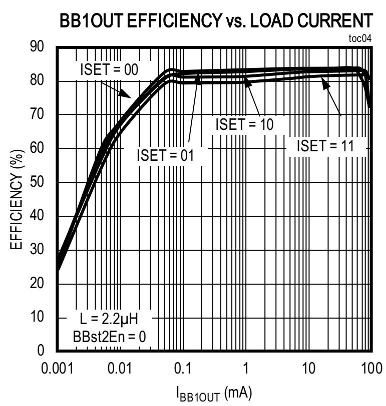
## Typical Operating Characteristics

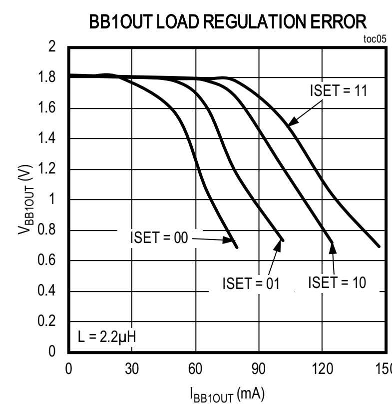
($V_{BAT}$ = 1.2V, $V_{BB1OUT}$ = 1.8V, $V_{BB2OUT}$ = 1.2V, $V_{L1OUT}$ = 1.5V, $V_{L2OUT}$ = 1.0V, L = 1.5µH, $C_{BB\_OUT}$ = 10µF (effective), $C_{CAP}$ = 1µF (effective), $C_{LDO}$ = 2.2µF (effective) no load on any rail, $T_A$ = +25°C, unless otherwise noted.)

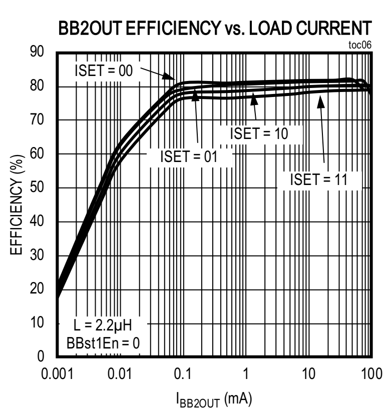


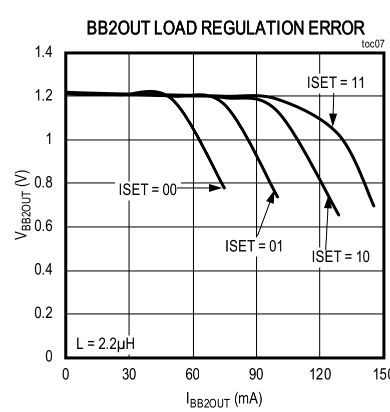



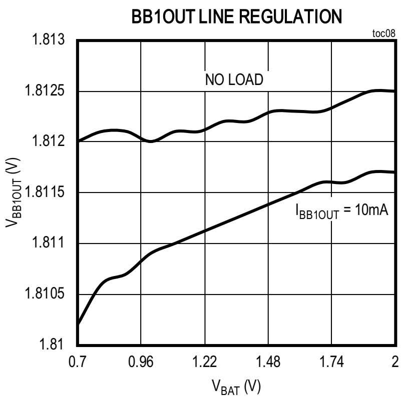



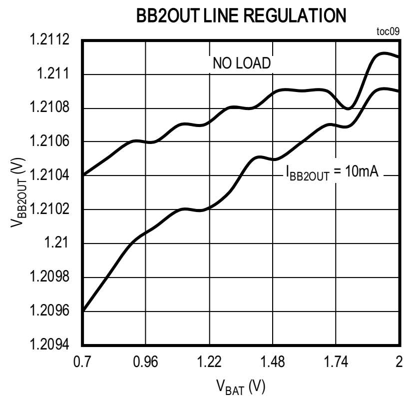



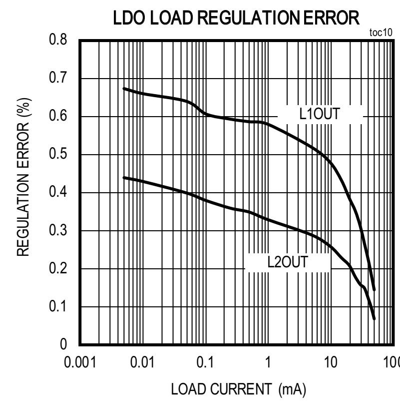



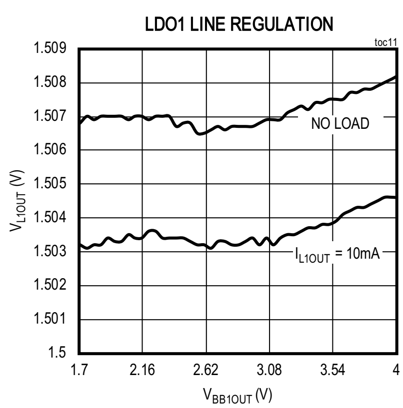
## Typical Operating Characteristics (continued)

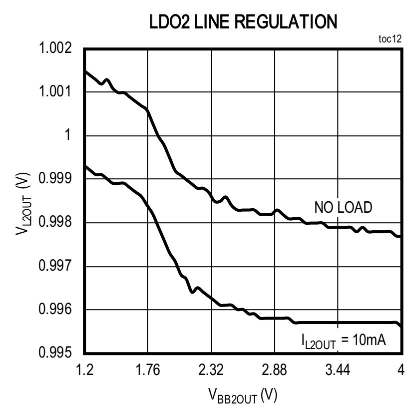
($V_{BAT}$ = 1.2V, $V_{BB1OUT}$ = 1.8V, $V_{BB2OUT}$ = 1.2V, $V_{L1OUT}$ = 1.5V, $V_{L2OUT}$ = 1.0V, L = 1.5μH, $C_{BB\_OUT}$ = 10μF (effective), $C_{CAP}$ = 1μF (effective), $C_{LDO}$ = 2.2μF (effective) no load on any rail, $T_A$ = +25°C, unless otherwise noted.)

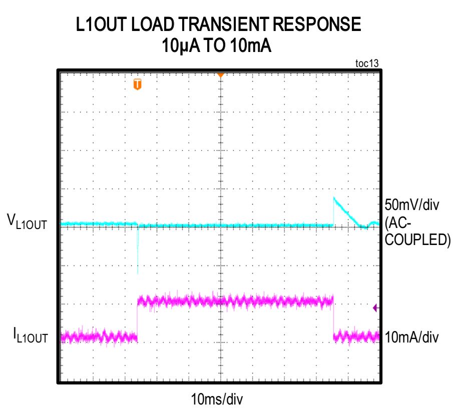


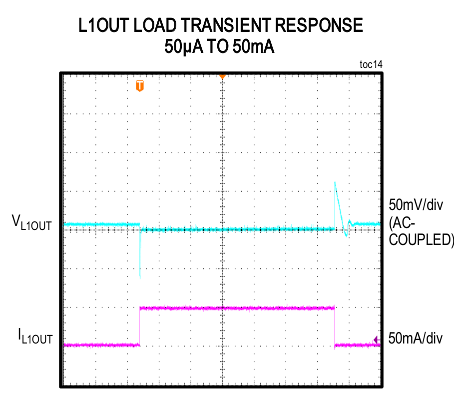



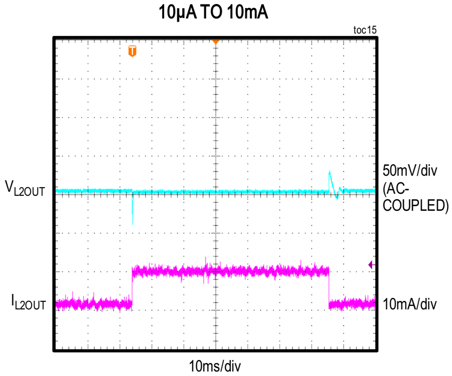



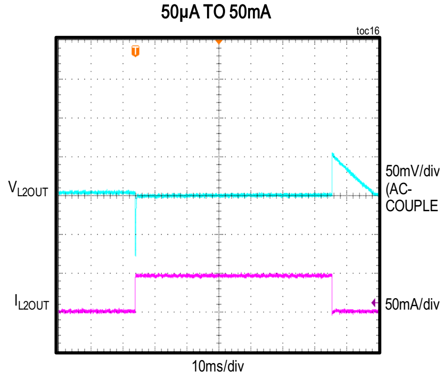
## Typical Operating Characteristics (continued)

($V_{BAT}$ = 1.2V, $V_{BB1OUT}$ = 1.8V, $V_{BB2OUT}$ = 1.2V, $V_{L1OUT}$ = 1.5V, $V_{L2OUT}$ = 1.0V, L = 1.5µH, $C_{BB\_OUT}$ = 10µF (effective), $C_{CAP}$ = 1µF (effective), $C_{LDO}$ = 2.2µF (effective) no load on any rail, $T_A$ = +25°C, unless otherwise noted.)

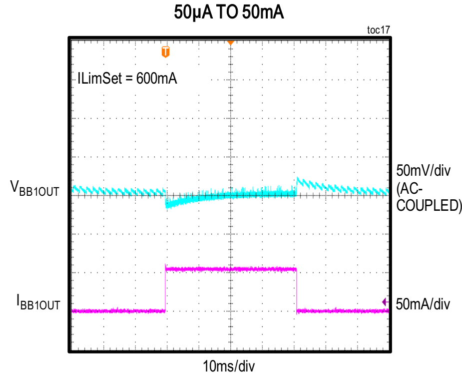
L2OUT LOAD TRANSIENT RESPONSE 10µA TO 10mA



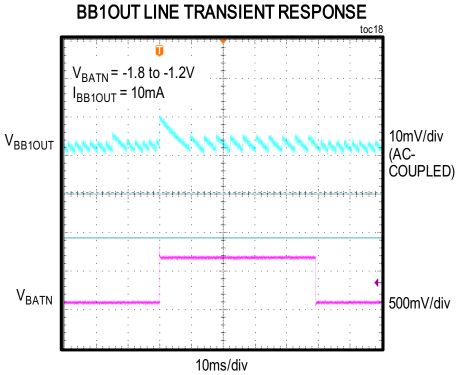

L2OUT LOAD TRANSIENT RESPONSE 50µA TO 50mA



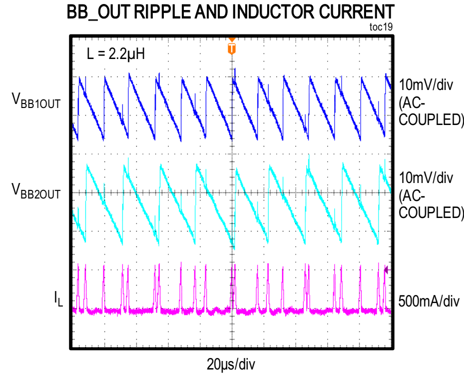

BB1OUT LOAD TRANSIENT RESPONSE 50µA TO 50mA



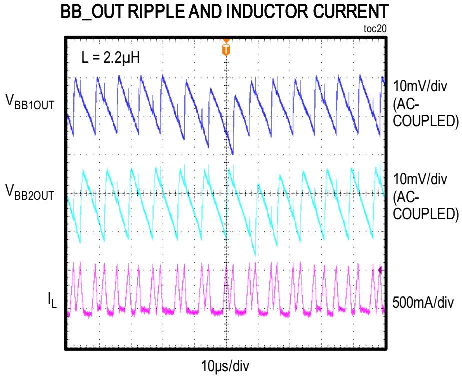

BB1OUT LINE TRANSIENT RESPONSE



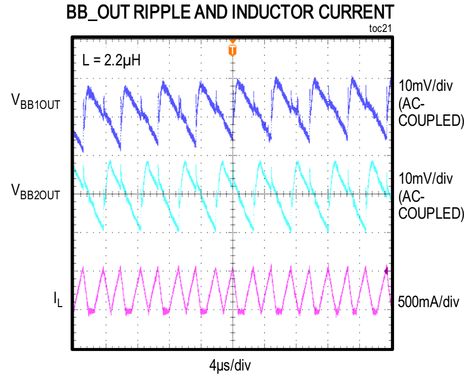

BB_OUT RIPPLE AND INDUCTOR CURRENT



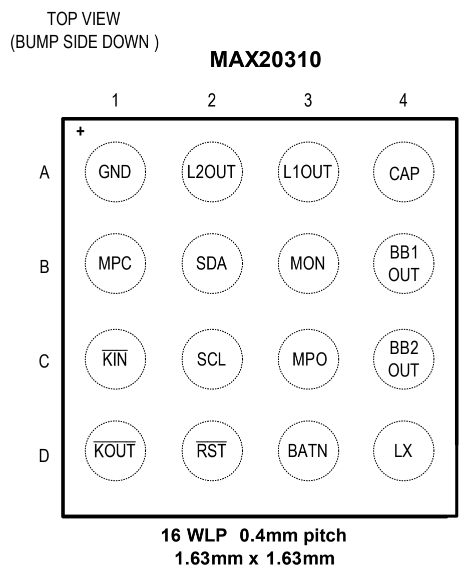

BB_OUT RIPPLE AND INDUCTOR CURRENT




BB_OUT RIPPLE AND INDUCTOR CURRENT



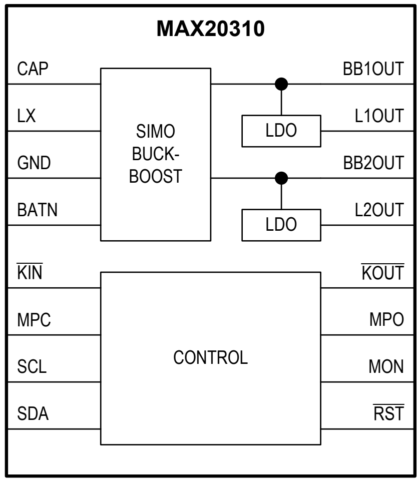
## Bump Configuration




## Bump Description

| BUMP | NAME | FUNCTION |
|---|---|---|
| A1 | GND | Ground/Battery Positive Terminal |
| A2 | L2OUT | LDO/Switch 2 Output |
| A3 | L1OUT | LDO/Switch 1 Output |
| A4 | CAP | Internal Supply Decoupling. Connect a minimum 1μF of capacitance to GND. |
| B1 | MPC | Multipurpose Control Input |
| B2 | SDA | $I^2C$ Serial Data |
| B3 | MON | Monitor Multiplexer Output |
| B4 | BB1OUT | Buck-Boost 1 Output |
| C1 | $\overline{\text{KIN}}$ | Key Input, Internally Pulled to GND. To signal active, short $\overline{\text{KIN}}$ to BATN. |
| C2 | SCL | $I^2C$ Serial Clock |
| C3 | MPO | Multipurpose Output. Level shifted digital output for controlling devices referenced to the negative battery terminal. |
| C4 | BB2OUT | Buck-Boost 2 Output |
| D1 | $\overline{\text{KOUT}}$ | Key Output. Active-low, level-shifted button status output. |
| D2 | $\overline{\text{RST}}$ | Reset Output. Active-low, open-drain output indicates completion of sequencer. |
| D3 | BATN | Battery Negative Terminal |
| D4 | LX | Inductor Switch Connection |

## Functional Block Diagram




## Detailed Description

### Power Regulation

The MAX20310 features an ultra-low $I_Q$ SIMO buck-boost switching regulator that provides two programmable voltage rails and two low-$I_Q$ LDOs. The regulators minimize quiescent current and operate on low input voltages. This makes the MAX20310 ideal for applications powered by singe-cell Alkaline, Zinc Air, or Silver Oxide batteries. All regulator outputs are capable of being discharged through a resistive load (passive discharge) when turned off. The discharge mode is set by the PDsc bits in each regulator's configuration register.

### Switching Regulator

In order to maximize efficiency, the switching regulator is implemented with an inverting buck-boost topology. Referencing the battery's positive terminal to ground configures the battery as a negative supply and the switching regulator output is positive. The switching regulator operates at supplies from -2.0V down to -0.7V, but requires -0.8V to start up. The outputs are independently configurable in 50mV increments.

### LDO

For applications that require lower noise supplies, or simply need additional regulated voltages, the MAX20310 includes two LDO regulators. In normal operation, each LDO can source up to 50mA. The LDO inputs are supplied by the buck-boost outputs. As such, an LDO cannot be enabled unless its corresponding switching regulator output is active. The LDOs can be used as switches to disconnect the quiescent loads of peripheral systems, increasing battery life. The LDO outputs are configurable from 0.5 to 3.65V in 50mV increments.

### Voltage Monitor Multiplexer

In addition to the four regulator outputs, the MAX20310 includes a voltage monitor multiplexer. The $I^2C$ controlled multiplexer connects the MON pin to any one of the regulator outputs or to BATN. This provides access to the different voltage rails in the device for ADC measurements. An inverting amplifier buffers the BATN channel in order to allow a positive, single-ended ADC to measure the voltage.

### Multipurpose Control Input

The MAX20310 includes a multipurpose control (MPC) pin that can control various functions inside the part based on the buck-boost and LDO configuration and sequence register settings. For devices with at least one BBst_Seq[2:0] or LDO_Seq[2:0] field set by the factory to 101 (enabled by MPC, active-low) or 110 (enabled by MPC, active-high) according to Table 19, the MPC pin can be configured to control the multipurpose output (MPO) pin for level-shifting to the battery voltage. See the *Multipurpose Output* section below for details. If the MPC pin is unused, it must be tied to GND.

### Multipurpose Output

In addition to the MPC pin, the MAX20310 also features a multipurpose output (MPO). The MPO pin can be configured to pull down to BATN, to pull up to GND, to pullup/down (push/pull), or be disabled (no pull). On devices with at least one BBst_Seq[2:0] or LDO_Seq[2:0] field set by the factory to 101 (enabled by MPC, active-low) or 110 (enabled by MPC, active-high), as detailed in table 19, the MPOCfg register allows the state of the MPO pin to be controlled either by I2C command or by the MPC pin, regardless of polarity. Table 1 below shows the truth table associated with such devices. Devices with none of the one BBst_Seq[2:0] or LDO_Seq[2:0] fields set by the factory to 101 (enabled by MPC, active-low) or 110 (enabled by MPC, active-high) allow the MPO output to be controlled by I2C command only. Table 2 below shows the truth table associated with such devices. An example implementation is included in Figure 1 to show how to use this pin to control an external regulator powered directly from the battery.

### Table 1. MPO Truth Table for Devices with One or More BBst_Seq[2:0]/LDO_Seq[2:0] Field Set to 101 or 110 by the Factory

| MPOPull[1:0] | | MPOEn[1:0] | | MPC | OUTPUT STATE |
|---|---|---|---|---|---|
| 0 | 0 | X | X | X | High-Impedance |
| 0 | 1 | 0 | 0 | X | High-Impedance |
| 0 | 1 | 0 | 1 | X | Pulled to BATN |
| 0 | 1 | 1 | 0 | 0 | Pulled to BATN |
| 0 | 1 | 1 | 0 | 1 | High-Impedance |
| 0 | 1 | 1 | 1 | 0 | High-Impedance |
| 0 | 1 | 1 | 1 | 1 | Pulled to BATN |
| 1 | 0 | 0 | 0 | X | Pulled to GND |
| 1 | 0 | 0 | 1 | X | High-Impedance |
| 1 | 0 | 1 | 0 | 0 | High-Impedance |
| 1 | 0 | 1 | 0 | 1 | Pulled to GND |
| 1 | 0 | 1 | 1 | 0 | Pulled to GND |
| 1 | 0 | 1 | 1 | 1 | High-Impedance |
| 1 | 1 | 0 | 0 | X | Pulled to GND |
| 1 | 1 | 0 | 1 | X | Pulled to BATN |
| 1 | 1 | 1 | 0 | 0 | Pulled to BATN |
| 1 | 1 | 1 | 0 | 1 | Pulled to GND |
| 1 | 1 | 1 | 1 | 0 | Pulled to GND |
| 1 | 1 | 1 | 1 | 1 | Pulled to BATN |

### Table 2. MPO Truth Table for Devices with None of the BBst_Seq[2:0]/LDO_Seq[2:0] Fields Set to 101 or 110 by the Factory

| MPOPull[1:0] | | MPOEn[1:0] | | MPC | OUTPUT STATE |
|---|---|---|---|---|---|
| 0 | 0 | X | X | X | High-Impedance |
| 0 | 1 | 0 | 0 | X | High-Impedance |
| 0 | 1 | 0 | 1 | X | Pulled to BATN |
| 1 | 0 | 0 | 0 | X | Pulled to GND |
| 1 | 0 | 0 | 1 | X | High-Impedance |
| 1 | 1 | 0 | 0 | X | Pulled to GND |
| 1 | 1 | 0 | 1 | X | Pulled to BATN |

## Power On/Off and Reset Control

The MAX20310 is intended for use in small battery-powered applications. It includes an off mode to minimize drain on the battery. In the off mode, all outputs are disabled and the part waits until the $\overline{KIN}$ input goes active to wake the device. The $\overline{KIN}$ input is internally pulled to GND and needs to be shorted to BATN to wake the device. An open-drain buffered copy of the state of $\overline{KIN}$ is available at $\overline{KOUT}$ allowing the system to monitor the status of the button. When the device is powered on, each function can be automatically enabled by a sequencing controller or remain off until an $I^2C$ command enables it. This behavior is determined by the factory settings. A button monitor is present on the MAX20310 and can produce different actions for long or short button presses. The list of settings and corresponding actions is shown in Table 18. A button press always wakes up the device, and the factory configuration determines other behavior.

## Reverse Battery Protection

Some applications use batteries like AAA's that do not have mechanical reverse installation protection. In such applications, an optional external nMOSFET and resistor connected as shown in Figure 2 provide reverse battery protection for the system. In normal operation, the 100Ω resistor slows the charging of $C_{IN}$ at startup until $V_{CAP}$-$V_{BATN}$ exceeds the threshold of the external MOSFET. Thereafter, the circuit functions nominally. In the case of battery reversal, the 100Ω resistor limits the current from the battery and protects the downstream system.

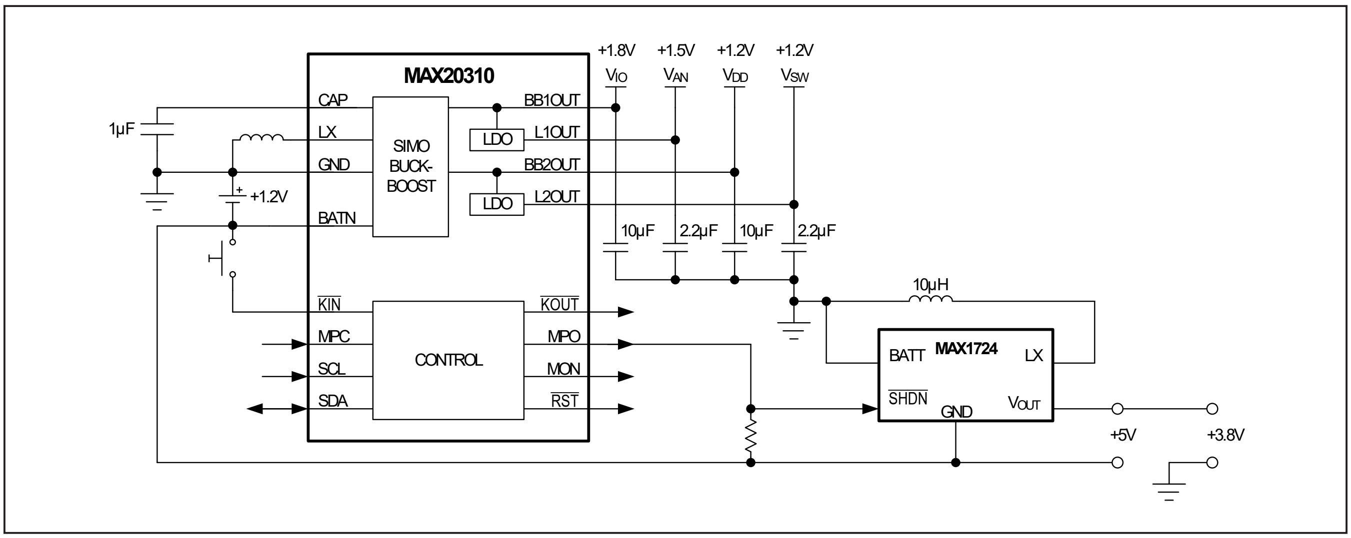



*Figure 1. Controlling an External Regulator with MPO*

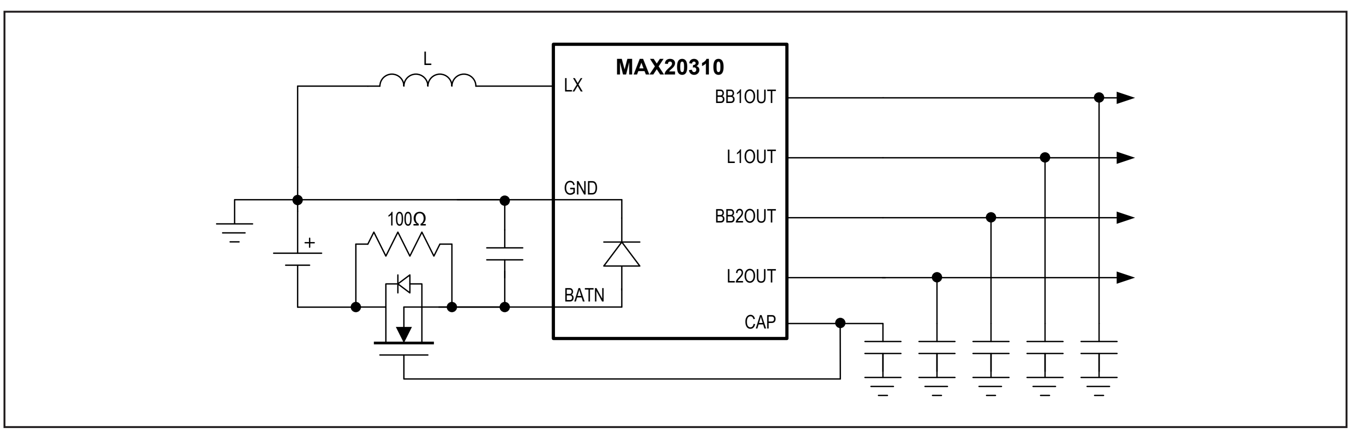



*Figure 2. Reverse Battery Protection Using an External MOSFET*

### Power Sequencing

The sequencing of the voltage regulators during power-on is configurable. Regulators can be configured to turn on at one of four points during the power on process. The four points are: 100ms after the power-on event, after the $\overline{RST}$ signal is released, or at two points in between. The two points are fixed proportionally to the duration of the Power-On Reset (POR) process, but the overall time of the reset delay is configurable (refer to PwrCfg register). The timing relationship is presented graphically in Figure 3. Additionally, the regulators are controllable by the sequencer, an input pin, or $I^2C$ command after reset is released. Note that the LDOs will not turn on until the associated switching output is also enabled.

### $I^2C$ Interface

The MAX20310 uses the two-wire $I^2C$ interface to communicate with a host microcontroller. The configuration settings and status information provided through this interface are detailed in the register descriptions. The slave address is 0x50 for writes and 0x51 for reads.

## Applications Information

### Always-On Devices

Due to its low power consumption, the MAX20310 is ideal for always-on applications. Products targeting these always-on, buttonless applications should select a version of the MAX20310 with PwrCfgMd[1:0] = 00 and connect the $\overline{KIN}$ input to BATN as shown in Figure 4. This PwrCfgMd setting configures a $\overline{KIN}$ press to only turn on the device. When a fresh battery is inserted, or when a battery tab used during product shelf life is removed, $\overline{KIN}$ is pulled to BATN and the device turns on.

### Additional Voltage Regulators

In applications with additional voltage regulators operating directly from the battery, careful consideration must be given to battery and system power domains. Due to the negative battery implementation of the MAX20310, the common node for the system power domain (GND) is connected to the positive terminal of the battery.

Regulators using the battery as a positive supply should connect BATN as the local ground and GND as the input supply. However, the output must always be referenced to the positive terminal of the battery (GND). This causes the output voltage of the regulator, referenced to GND, to equal $V_{OUT} – V_{BAT}$. As the battery discharges, this voltage might change over time.

For example, in Figure 1, the external MAX1724 step-up converter produces 5V with respect to the regulator ground (BATN). Because the battery voltage is 1.2V, the output voltage in the system power domain is 3.8V. Due to the relative flatness of the discharge curves for Silver-Oxide, Zinc-Air, and other common coin cell batteries, the challenges associated with a changing reference node are reduced. However, designs should account for some variation of the BATN node.

### $I^2C$ Interface

The MAX20310 contains an $I^2C$-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

#### Start, Stop, and Repeated Start Conditions

When writing to the MAX20310 using $I^2C$, the master sends a START condition (S) followed by the MAX20310

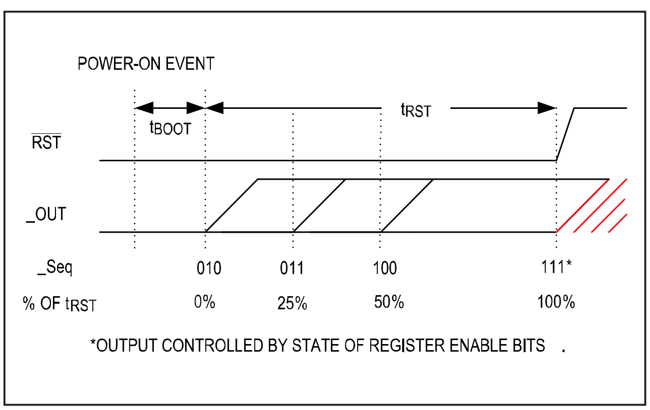



*Figure 3. Reset Sequence Programming*

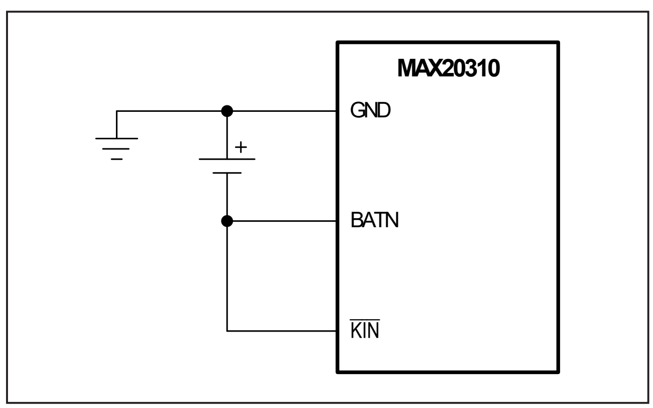



*Figure 4. $\overline{KIN}$ Connected to BATN for Always-On Applications*

I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See Figure 5.

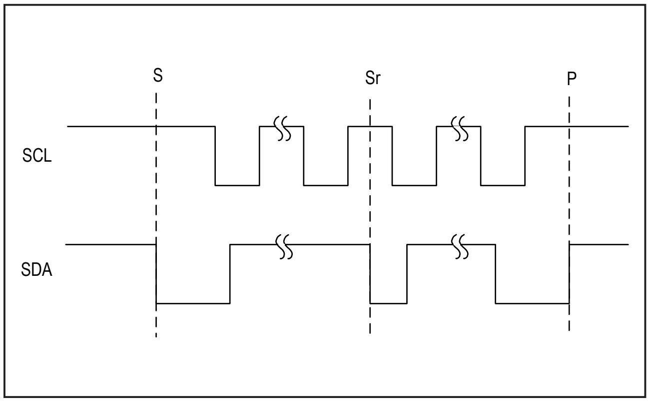



*Figure 5. I²C START, STOP and REPEATED START Conditions*

### Slave Address

Set the Read/$\overline{\text{Write}}$ bit high to configure the MAX20310 to read mode. Set the Read/$\overline{\text{Write}}$ bit low to configure the MAX20310 to write mode. The address is the first byte of information sent to the MAX20310 after the START condition.

### Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the START, STOP and REPEATED START Conditions section). Both SDA and SCL remain high when the bus is not active.

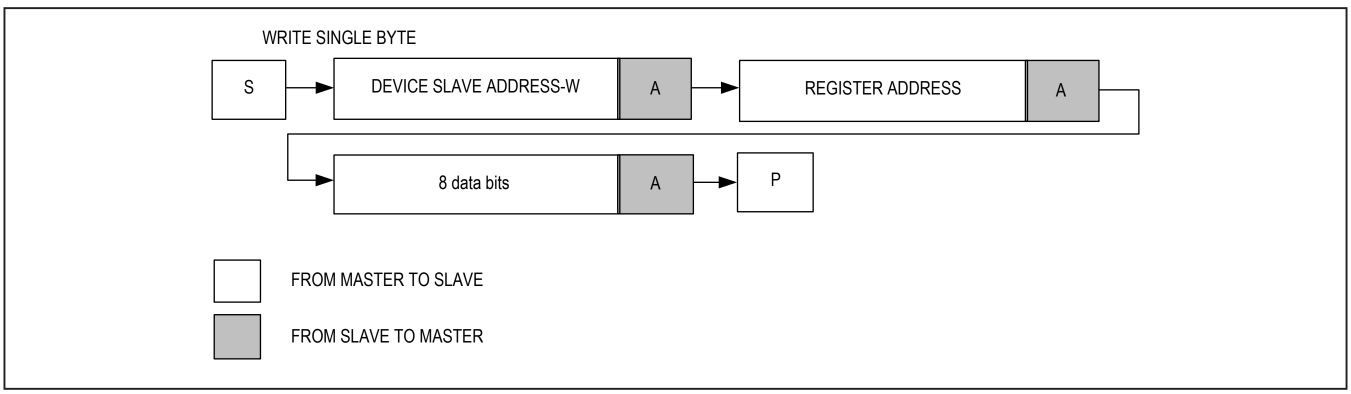



*Figure 6. Write Byte Sequence*

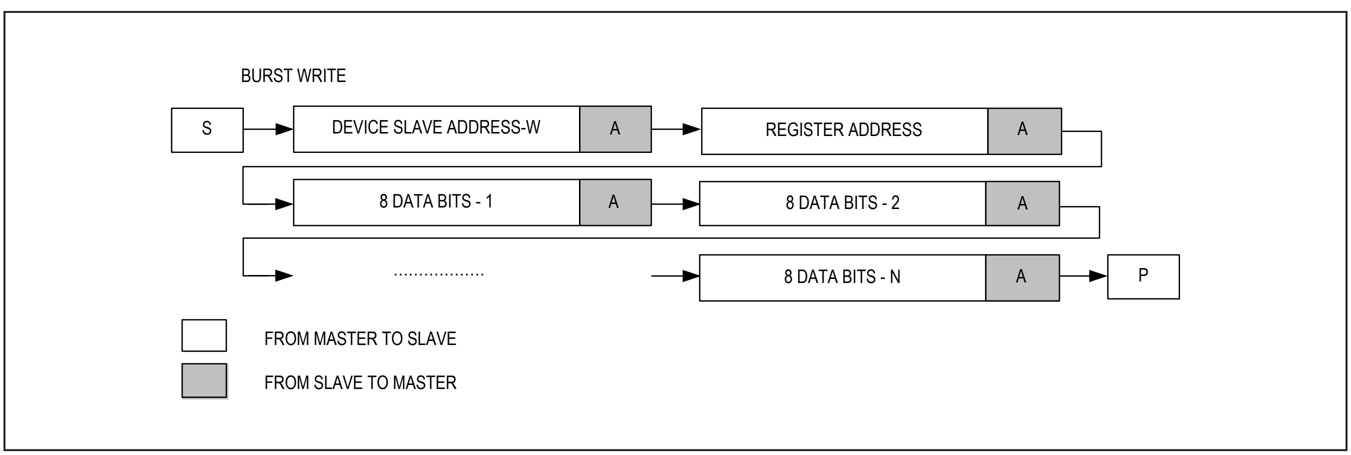



*Figure 7. Burst Write Sequence*

### Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 6). The following procedure describes the single byte write operation:

The master sends a START condition

The master sends the 7-bit slave address plus a write bit (low)

The addressed slave asserts an ACK on the data line

The master sends the 8-bit register address

The slave asserts an ACK on the data line only if the address is valid (NAK if not)

The master sends 8 data bits

The slave asserts an ACK on the data line

The master generates a STOP condition

### Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 7). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

The master sends a START condition

The master sends the 7-bit slave address plus a write bit (low)

The addressed slave asserts an ACK on the data line

The master sends the 8-bit register address

The slave asserts an ACK on the data line only if the address is valid (NAK if not)

The master sends 8 data bits

The slave asserts an ACK on the data line

Repeat 6 and 7 N-1 times

The master generates a STOP condition

### Single-Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 8). The following procedure describes the single byte read operation:

The master sends a START condition

The master sends the 7-bit slave address plus a write bit (low)

The addressed slave asserts an ACK on the data line

The master sends the 8-bit register address

The slave asserts an ACK on the data line only if the address is valid (NAK if not)

The master sends a REPEATED START condition

The master sends the 7-bit slave address plus a read bit (high)

The addressed slave asserts an ACK on the data line

The slave sends 8 data bits

The master asserts a NACK on the data line

The master generates a STOP condition

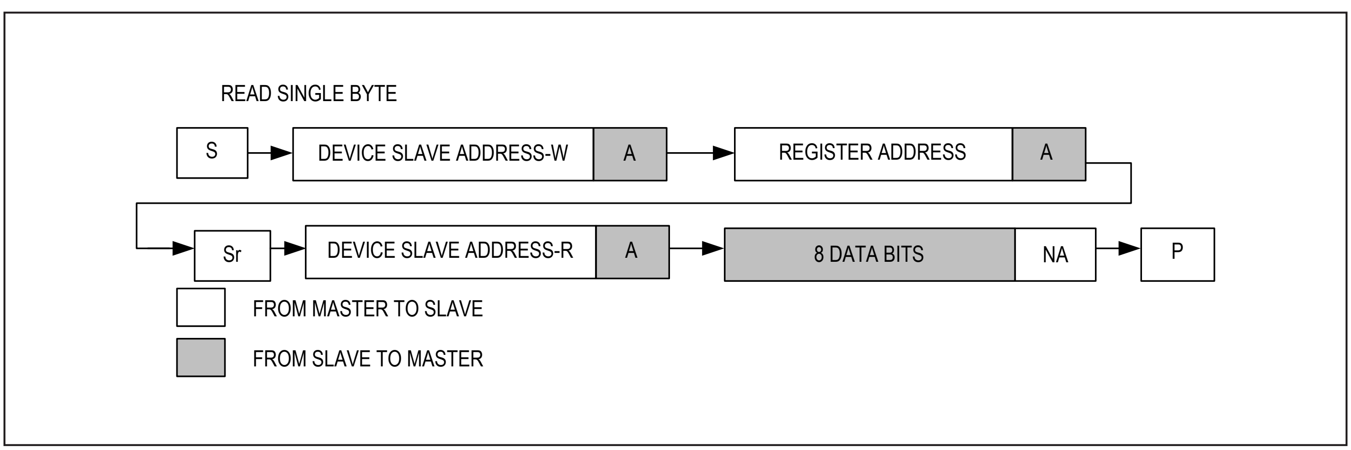



*Figure 8. Read Byte Sequence*

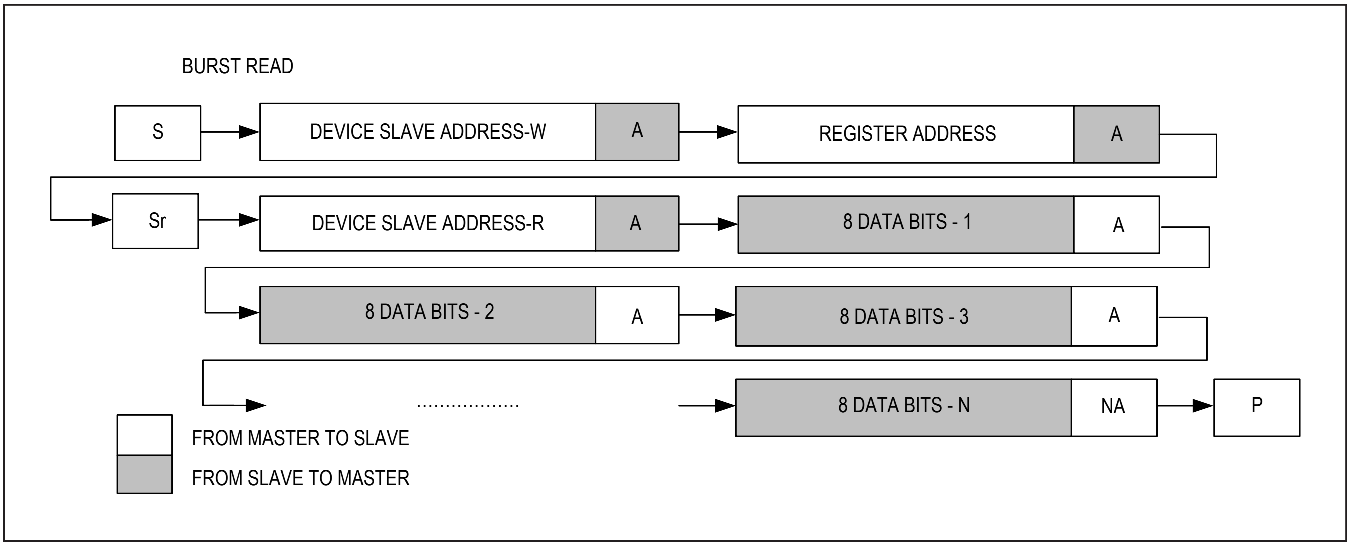



*Figure 9. Burst Read Sequence*

### Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 9). The following procedure describes the burst byte read operation:

The master sends a START condition

The master sends the 7-bit slave address plus a write bit (low)

The addressed slave asserts an ACK on the data line

The master sends the 8-bit register address

The slave asserts an ACK on the data line only if the address is valid (NAK if not)

The master sends a REPEATED START condition

The master sends the 7-bit slave address plus a read bit (high)

The slave asserts an ACK on the data line

The slave sends 8 data bits

The master asserts an ACK on the data line

Repeat 9 and 10 N-2 times

The slave sends the last 8 data bits

The master asserts a NACK on the data line

The master generates a STOP condition

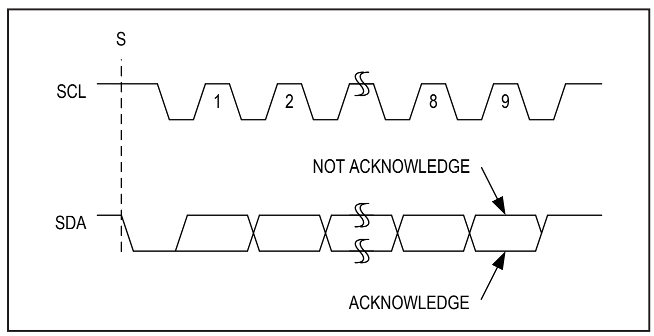



*Figure 10. Acknowledge*

### Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX20310 generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see Figure 10). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

## I²C Register Map

| REGISTER ADDRESS | REGISTER NAME | R/W | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x00 | ChipId | R | ChipId[7] | ChipId[6] | ChipId[5] | ChipId[4] | ChipId[3] | ChipId[2] | ChipId[1] | ChipId[0] |
| 0x01 | ChipRev | R | ChipRev[7] | ChipRev[6] | ChipRev[5] | ChipRev[4] | ChipRev[3] | ChipRev[2] | ChipRev[1] | ChipRev[0] |
| 0x02 | BBstCfg | R/W | BBstDmpEn | — | — | — | ILimSet[1] | ILimSet[0] | FetScale[1] | FetScale[0] |
| 0x03 | Reserved | — | — | — | — | — | — | — | — | — |
| 0x04 | BBst1VSet | R/W | — | — | BBst1VSet[5] | BBst1VSet[4] | BBst1VSet[3] | BBst1VSet[2] | BBst1VSet[1] | BBst1VSet[0] |
| 0x05 | BBst1VCfg | R/W | BBst1En[1] | BBst1En[0] | BBst1PDsc | BBst1ADsc | BBst1RmpDis | — | — | — |
| 0x06 | BBst2VSet | R/W | — | — | BBst2VSet[5] | BBst2VSet[4] | BBst2VSet[3] | BBst2VSet[2] | BBst2VSet[1] | BBst2VSet[0] |
| 0x07 | BBst2VCfg | R/W | BBst2En[1] | BBst2En[0] | BBst2PDsc | BBst2ADsc | BBst2RmpDis | — | — | — |
| 0x08 | LDO1Vset | R/W | — | — | LDO1VSet[5] | LDO1VSet[4] | LDO1VSet[3] | LDO1VSet[2] | LDO1VSet[1] | LDO1VSet[0] |
| 0x09 | LDO1Cfg | R/W | LDO1En[1] | LDO1En[0] | LDO1PDsc | LDO1ADsc | — | — | — | LDO1Mode |
| 0x0A | LDO2Vset | R/W | — | — | LDO2VSet[5] | LDO2VSet[4] | LDO2VSet[3] | LDO2VSet[2] | LDO2VSet[1] | LDO2VSet[0] |
| 0x0B | LDO2Cfg | R/W | LDO2En[1] | LDO2En[0] | LDO2PDsc | LDO2ADsc | — | — | — | LDO2Mode |
| 0x0C | MonCfg | R/W | — | — | — | — | MonHiZ | MonSel[2] | MonSel[1] | MonSel[0] |
| 0x0D | MPOCfg | R/W | MPOEn[1] | MPOEn[0] | — | — | — | — | MPOPull[1] | MPOPull[0] |
| 0x0E | PwrCmd | R/W | PwrCmd[7] | PwrCmd[6] | PwrCmd[5] | PwrCmd[4] | PwrCmd[3] | PwrCmd[2] | PwrCmd[1] | PwrCmd[0] |
| 0x0F | Status | R | LDO2UVLO | LDO1UVLO | LDO2Thm | LDO1Thm | LDO2CrMd | LDO1CrMd | KINSts | MPCSts |
| 0x10 | PwrCfg | R | PwrCfgMd[1] | PwrCfgMd[0] | GPasDsc | — | — | — | BootDly[1] | BootDly[0] |
| 0x11 | BBstSeq | R | — | BBst2Seq[2] | BBst2Seq[1] | BBst2Seq[0] | — | BBst1Seq[2] | BBst1Seq[1] | BBst1Seq[0] |
| 0x12 | LDOSeq | R | — | LDO2Seq[2] | LDO2Seq[1] | LDO2Seq[0] | — | LDO1Seq[2] | LDO1Seq[1] | LDO1Seq[0] |

## I²C Register Descriptions

### Table 3. ChipId Register (0x00)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ADDRESS | 0x00 (Read-Only) | | | | | | | |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | ChipId[7:0] | | | | | | | |
| ChipId[7:0] | ChipId[7:0] bits show information about the version of the MAX20310 | | | | | | | |

### Table 4. ChipRev Register (0x01)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ADDRESS | 0x01 (Read-Only) | | | | | | | |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | ChipRev[7:0] | | | | | | | |
| ChipRev[7:0] | ChipRev shows information about the revision of the MAX20310 silicon | | | | | | | |

### Table 5. BBstCfg Register (0x02)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ADDRESS | 0x02 (Read, Write) | | | | | | | |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | BBstDmpEn | - | - | - | ILimSet[1:0] | | FetScale[1:0] | |
| BBstDmpEn | Buck-Boost Dump Enable<br>This enables a dump switch to reduce LX oscillations<br>0: Switch disabled<br>1: Switch enabled | | | | | | | |
| ILimSet[1:0] | Buck-Boost Peak Current Limit Setting<br>Sets the peak current supplied by the buck-boost regulator<br>00: 300mA<br>01: 400mA<br>10: 500mA<br>11: 600mA | | | | | | | |
| FetScale[1:0] | FetScale<br>Scales the switching FETs to optimize efficiency at a given load<br>00: 28%<br>01: 60%<br>10: 80%<br>11: 100% | | | | | | | |

## Table 6. BBst1VSet Register (0x04)

| ADDRESS | 0x04 (Read, Write) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | - | - | BBst1VSet[5:0] | | | | | |
| BBst1VSet[5:0] | Buck-Boost 1 Output Voltage Setting<br>0.90V to 4.05V, linear scale, 50mV increments<br>000000 = 0.90V<br>000001 = 0.95V<br>…<br>111110 = 4.00V<br>111111 = 4.05V | | | | | | | |

## Table 7. BBst1Cfg Register (0x05)

| ADDRESS | 0x05 (Read, Write) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | BBst1En[1:0] | | BBst1PDsc | — | BBst1RmpDis | — | — | — |
| BBst1En[1:0] | Buck-Boost 1 Enable<br>00: Disabled<br>01: Enabled<br>10: Controlled by MPC (active low)<br>11: Controlled by MPC (active high) | | | | | | | |
| BBst1PDsc | Buck-Boost 1 Passive Discharge<br>0: Disabled<br>1: Enabled when output is off | | | | | | | |
| BBst1RmpDis | Disable the ramped output of Buck-Boost output 1. If disabled, the BBst1VSet value is immediately applied to the output.<br>1: Immediate transition to set value<br>0: Ramp to set value mode | | | | | | | |

## Table 8. BBst2VSet Register (0x06)

| ADDRESS | 0x06 (Read, Write) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | - | - | BBst2VSet[5:0] | | | | | |
| BBst2VSet[5:0] | Buck-Boost 2 Output Voltage Setting<br>0.90V to 4.05V, linear scale, 50mV increments<br>000000 = 0.90V<br>000001 = 0.95V<br>…<br>111110 = 4.00V<br>111111 = 4.05V | | | | | | | |

## Table 9. BBst2Cfg Register (0x07)

| ADDRESS | 0x07 (Read, Write) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | BBst2En[1:0] | | BBst2PDsc | - | BBst2RmpDis | - | - | - |
| BBst2En[1:0] | Buck-Boost 2 Output Enable<br>00: Disabled<br>01: Enabled<br>10: Controlled by MPC (active-low)<br>11: Controlled by MPC (active-high) | | | | | | | |
| BBst2PDsc | Buck-Boost 2 Passive Discharge<br>0: Disabled<br>1: Enabled when output is off | | | | | | | |
| BBst2RmpDis | Disable the ramped output of Buck-Boost output 2. If disabled, the BBst2VSet value is immediately applied to the output.<br>1: Immediate transition to set value<br>0: Ramp to set value mode | | | | | | | |

## Table 10. LDO1VSet Register (0x08)

| ADDRESS | 0x08 (Read, Write) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | — | — | LDO1VSet[5:0] | | | | | |
| LDO1VSet[5:0] | LDO 1 Output Voltage Setting<br>0.50V to 3.65V, 50mV increments<br>000000 = 0.50V<br>000001 = 0.55V<br>…<br>111110 = 3.60V<br>111111 = 3.65V | | | | | | | |

## Table 11. LDO1Cfg Register (0x09)

| ADDRESS | 0x09 (Read, Write) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | LDO1En[1:0] | | LDO1PDsc | LDO1ADsc | — | — | — | LDO1Mode |
| LDO1En[1:0] | LDO 1 Output Enable<br>00: Disabled<br>01: Enabled<br>10: Controlled by MPC (active-low)<br>11: Controlled by MPC (active-high) | | | | | | | |
| LDO1PDsc | LDO 1 Passive Discharge<br>0: Disabled<br>1: Enabled when output is off | | | | | | | |
| LDO1Mode | LDO 1 Mode<br>Configure LDO1 as an LDO or a load switch<br>0: LDO<br>1: Load Switch | | | | | | | |

## Table 12. LDO2VSet Register (0x0A)

| ADDRESS | 0x0A (Read, Write) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | — | — | LDO2VSet[5:0] | | | | | |
| LDO2VSet[5:0] | LDO 2 Output Voltage Setting<br>0.50V to 3.65V, 50mV increments<br>000000 = 0.50V<br>000001 = 0.55V<br>…<br>111110 = 3.60V<br>111111 = 3.65V | | | | | | | |

## Table 13. LDO2Cfg Register (0x0B)

| ADDRESS | 0x0B (Read, Write) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | LDO2En[1:0] | | LDO2PDsc | — | — | — | — | LDO2Mode |
| LDO2En[1:0] | LDO 2 Output Enable<br>00: Disabled<br>01: Enabled<br>10: Controlled by MPC (active-low)<br>11: Controlled by MPC (active-high) | | | | | | | |
| LDO2PDsc | LDO 2 Passive Discharge<br>0: Disabled<br>1: Enabled when output is off | | | | | | | |
| LDO2Mode | LDO 2 Mode<br>Configure LDO2 as an LDO or a load switch<br>0: LDO<br>1: Load Switch | | | | | | | |

## Table 14. MonCfg Register (0x0C)

| ADDRESS | 0x0C (Read, Write) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | — | — | — | — | MonHiZ | MonSel[2:0] | | |
| MonHiZ | Monitor Off Mode Condition<br>0: 100kΩ pulldown when disabled<br>1: High impedance when disabled | | | | | | | |
| MonSel[2:0] | Monitor Pin Source Selection<br>000: Disabled<br>001: BB1OUT selected<br>010: BB2OUT selected<br>011: L1OUT selected<br>100: L2OUT selected<br>101: BATIN selected<br>110: CAP selected<br>111: Reserved | | | | | | | |

## Table 15. MPOCfg Register (0x0D)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ADDRESS | 0x0D (Read, Write) | | | | | | | |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | MPOEn[1:0] | | — | — | — | — | MPOPull[1:0] | |
| MPOEn[1:0] | Multipurpose Output Enable<br>00: Pull up (to GND)<br>01: Pull down (to BATN)<br>10: Pull up when MPC high, pull down when MPC low<br>11: Pull up when MPC low, pull down when MPC high | | | | | | | |
| MPOPull[1:0] | Multipurpose Output Pull Mode<br>00: Disabled<br>01: Pull down (to BATN)<br>10: Pull up (to GND)<br>11: Pull up/down (Push/Pull) | | | | | | | |

## Table 16. PwrCmd Register (0x0E)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| ADDRESS | 0x0E (Read, Write) | | | | | | | |
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | PwrCmd[7:0] | | | | | | | |
| PwrCmd[7:0] | Power Command Register<br>10110010: Power Off - Turn off and stay off<br>11000011: Hard Reset - Turn off and return back on<br>11010100: Soft Reset - Pulse $\overline{\text{RST}}$ low | | | | | | | |

## Table 17. Status Register (0x0F)

| ADDRESS | 0x0F (Read-Only) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | LDO2UVLO | LDO1UVLO | LDO2Thm | LDO1Thm | LDO2CrMd | LDO1CrMd | KINSts | MPCSts |
| LDO2UVLO | LDO 2 Undervoltage Lockout Status<br>0: Normal<br>1: Undervoltage | | | | | | | |
| LDO1UVLO | LDO 1 Undervoltage Lockout Status<br>0: Normal<br>1: Undervoltage | | | | | | | |
| LDO2Thm | LDO 2 Thermal Limit Status<br>0: Normal<br>1: Thermal shutdown | | | | | | | |
| LDO1Thm | LDO 1 Thermal Limit Status<br>0: Normal<br>1: Thermal shutdown | | | | | | | |
| LDO2CrMd | LDO 2 Current Mode<br>0: LDO<br>1: Switch | | | | | | | |
| LDO1CrMd | LDO 1 Current Mode<br>0: LDO<br>1: Switch | | | | | | | |
| KINSts | $\overline{\text{KIN}}$ Status<br>0: Low<br>1: High | | | | | | | |
| MPCSts | Multi-Purpose Control Status<br>0: Low<br>1: High | | | | | | | |

## Table 18. PwrCfg Register (0x10)

| ADDRESS | 0x10 (Read-Only) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | PwrCfgMd[1:0] | | GPasDsc | — | — | — | BootDly[1:0] | |
| PwrCfgMd[1:0] | Power Configuration Mode<br>A short button press will always wake the device from the off state.<br>00: Button only wakes device (can be turned off by $I^2C$ command)<br>01: Long button press generates reset pulse<br>10: Long button press power cycles and reboots device<br>11: Long button press turns device off | | | | | | | |
| GPasDsc | Global Passive Discharge<br>0: Passive discharge disabled in off state<br>1: Passive discharged enabled in off state | | | | | | | |
| BootDly[1:0] | Boot Sequence Delay ($t_{RST}$)<br>00: 80ms<br>01: 120ms<br>10: 160ms<br>11: 200ms | | | | | | | |

## Table 19. BBstSeq Register (0x11)

| ADDRESS | 0x11 (Read-Only) | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| BIT | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| NAME | — | BBst2Seq[2:0] | | | — | BBst1Seq[2:0] | | |
| BBst2Seq[2:0] | Buck-Boost 2 Sequencing Configuration<br>000: Disabled<br>001: Reserved<br>010: Enabled at 0% of power on delay<br>011: Enabled at 25% of power on delay<br>100: Enabled at 50% of power on delay<br>101: Enabled by MPC (active low)<br>110: Enabled by MPC (active high)<br>111: Controlled by BBst2En[1:0] after 100% of power on delay | | | | | | | |
| BBst1Seq[2:0] | Buck-Boost 2 Sequencing Configuration<br>000: Disabled<br>001: Reserved<br>010: Enabled at 0% of power on delay<br>011: Enabled at 25% of power on delay<br>100: Enabled at 50% of power on delay<br>101: Enabled by MPC (active low)<br>110: Enabled by MPC (active high)<br>111: Controlled by BBst1En[1:0] after 100% of power on delay | | | | | | | |