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MAX20328/MAX20328A

MUX Switch for USB Type-C Audio Adapter Accessories

General Description

The MAX20328/MAX20328A are USB Type-C audio interface ICs for use in portable devices. As USB Type-C and USB power delivery (PD) make a high-voltage charging solution readily available, the data and SBU lines are at risk of shorting to a high bus voltage, risking permanent damage to the portable device. USB 2.0 data lines also need protection when multiplexed with analog audio signals that vary from positive to negative voltages. The devices can detect a CC pin connection event to disable the microphone bias and eliminate pop up noise when an audio accessory is attached.

The MAX20328/MAX20328A come in a 5 x 5 array, 25-bump, 0.4mm pitch, 2.34mm x 2.34mm wafer-level package (WLP).

Applications

- Smart Phones
- Phablets
- Tablet PCs

Benefits and Features

- Versatile and Flexible Switch Configurations
  - High-Speed USB Data or Audio Switch Paths
  - Automatic Impedance Detection in Audio Configurations
  - Full Manual Switch Control
  - Beyond-the-Rails™ Signal Capability
- Overvoltage Protected Data and Audio Channels
  - Two Separate OVLO Blocks
  - OVLO Threshold Programmable to 3.37V, 4.00V, 4.70V, or 5.00V
- Negative Voltage Capable Audio Channel
  - ±5V Audio Signals (Limited by Positive OVLO Threshold)
  - -100dB THD+N
  - -100dB PSRR at 217Hz
- High ESD and Surge-Protected USB Type-C Contacts
  - ±12kV HBM
  - ±25V Surge Capable on USB Type-C Pins
- Minimal Solution size
  - 5 x 5 Array, 0.4mm Pitch 2.34mm x 2.34mm WLP

***Ordering Information* appears at end of data sheet.**

Beyond-the-Rails is a trademark of Maxim Integrated Products, Inc.

19-100294; Rev 0; 3/18

maxim integrated™

Absolute Maximum Ratings (Note 2)

All voltages are referenced to AGND unless otherwise noted
V_{CC}, MIC, SDA, SCL ..... -0.3 to +6V
DGND ..... -0.3 to +0.3V
CC ..... -0.3 to +26V
SBU1_MG, SBU2_GM, MG_SR,
GM_SR (Note 1) ..... -0.3 to +12V
MG_SL, GM_SL (MAX20328 Only) (Note 1) ..... -0.3 to +12V
DP_T, DM_T, DP_B, DM_B (Note 1) ..... -6 to min [(LA + 12V, RA + 12V), +12V]
DP_AP1, DM_AP1, DP_AP2, DM_AP2 ..... -0.3 to +6V
LA, RA ..... -6 to +6V
GSNS_L (MAX20328 only) ..... -0.3 to min [+6V, (MG_SL + 0.3V, GM_SL + 0.3V)].
GSNS_R (MAX20328 only) ..... -0.3 to min [+6V, (MG_SR + 0.3V, GM_SR + 0.3V)]
GSNS_ (MAX20328A only) ..... -0.3 to min [+6V, (MG_SR + 0.3V, GM_SR + 0.3V)]
TX, RX, $\overline{INT}$ (MAX20328A only) ..... -0.3 to +6V
Continuous Current Into Any Pin ..... ±200mA
Continuous Power Dissipation (Multilayer Board)
(Derate 19.07mW/°C above +70°C) 1525.6mW
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (Reflow) ..... +260°C

Note 1: Surge capable up to ±25V (IEC61000-4-5 Connector Class 0)

Package Thermal Characteristics (Note 2)

WLP
Junction-to-Ambient Thermal Resistance,
Four-Layer Board (θ_{JA}) ..... 52.43°C/W

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at V_{CC} = +3.7V, T_A = +25°C) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
VCC						
Supply Voltage Range	V_{CC}		2.7		5.5	V
Input Supply Current	I_{CC}	V_{CC} = 3.7V		256	400	µA
OVLO Shutdown Current	I_{CC_O}	$V_{DP\_/DM\_}$ = 6V, $V_{LA/RA}$ = $V_{DP\_/DM\_AP\_}$ = 0V		256	400	µA
Shutdown Current	I_{CC_SHDN}	V_{CC} = 3.7V, EN = 0		3.9	7	µA
Undervoltage Lockout (POR) Rising Threshold	V_{UVLOR}			2.395		V
Undervoltage Lockout (POR) Falling Threshold	V_{UVLOF}			2.365		V
Undervoltage Lockout (POR) Threshold Hysteresis	V_{UVLOH}			30		mV
Start-up Delay	t_{START}	From (V_{CC} rising crosses V_{UVLOR} OR EN from 0 to 1) to EOB rising from 0 to 1		0.85	2	ms

Electrical Characteristics (continued)

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at V_{CC} = +3.7V, T_A = +25°C) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
OVERVOLTAGE PROTECTION DP/M_, SBU_, MG_S, GM_S							
Overvoltage Trip Level	V_{OVLO}	V_{IN} Rising (Note 4)	SET_OVTH[1:0] = 00	3.220	3.37	3.520	V
			SET_OVTH[1:0] = 01	3.845	4.0	4.155	
			SET_OVTH[1:0] = 10	4.535	4.7	4.865	
			SET_OVTH[1:0] = 11	4.830	5.0	5.170	
Overvoltage Trip Level Hysteresis	V_{OVLOH}				60		mV
Overvoltage Fault Protection Response Time	t_{FP}	V_{IN} = 1V to 10V step, V_{CC} = 3.7V, R_L = 50Ω			100		ns
DP/DM Overvoltage Fault Protection Recovery Time	t_{FPR}	V_{IN} = 10V to 1V step, V_{CC} = 3.7V, R_L = 50Ω			10		ms
DP_, DM_ (DATA AND AUDIO SWITCHES)							
Analog Signal Range Audio	$V_{DP\_/DM\_}$			-5		V_{OVLO}	V
Analog Signal Range Data	$V_{DP\_/DM\_}$			0		V_{OVLO}	V
Single Channel On Resistance	$R_{ON-DP\_/DM\_}$	V_{CC} = 3.7V, T_A = +25°C			2.24	4	Ω
On Resistance Match Between Channels	$\Delta R_{ON-DP\_/DM\_}$	V_{CC} = 3.7V, $V_{DP/M\_}$ = 0V, $ID\_$ = 10mA (Note 5)			0.02	0.21	Ω
On Resistance Flatness	$R_{FLAT-DP\_/DM\_}$	V_{CC} = 3.7V, $I_{DP\_/DM\_}$ = 10mA, $V_{DP\_/DM\_}$ = -1.0V to +1.0V (Note 6)			0.00005	0.02	Ω
Off Leakage Current	$I_{DP\_/DM\_OFF}$	V_{CC} = 3.7V, EN = 0, $V_{DP\_/DM\_}$ = 2.5V, $V_{LA/RA}$ = $V_{DP\_AP\_/DM\_AP\_}$ = 0V		-0.5	+0.5	+1.5	µA
On Leakage Current	$I_{DP\_/DM\_ON}$	Data Channel Closed V_{CC} = 3.7V, EN = 1, $V_{DP\_/DM\_}$ = 2.5V, $V_{DP\_AP\_/DM\_AP\_}$ = Floating $V_{LA/RA}$ = 0V		-0.7	+0.4	+1.5	µA
	I_{LA/RA_ON}	Audio Channel Closed V_{CC} = 3.7V, EN = 1, $V_{LA/RA}$ = 2.5V, $V_{DP\_/DM\_}$ = Floating $V_{DP\_AP\_/DM\_AP\_}$ = 0V		-0.5	+0.8	+2.1	

Electrical Characteristics (continued)

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at V_{CC} = +3.7V, T_A = +25°C) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Turn-On Time	$t_{ON-DP\_/DM\_}$	$V_{DP\_/DM\_}$ = 1.5V, R_L = 50Ω, I^2C control , time from last data bit processed to 90% of final value		50		µs
Turn-Off Time	$t_{OFF-DP\_/DM\_}$	$V_{DP\_/DM\_}$ = 1.5V, R_L = 50Ω, I^2C control, time from last data bit processed to 10% of initial value		5		µs
Output Skew Same Switch	t_{SKSS}	(Note 7)		40		ps
Output Skew Between Switches	t_{SKBS}	(Note 7)		40		ps
Break-Before-Make Time Delay	t_{BBM}	R_L = 50Ω, Time delay between one side of the mux switch opening and the other side closing.		10		µs
Bandwidth	$BW_{DP\_/DM\_}$	$BW_{DP\_/DM\_}$ = 0dBm, R_S = R_L = 50Ω		800		MHz
Off Isolation	$V_{ISO-DP\_/DM\_}$	f = 20Hz to 20kHz, $V_{D\_}$ = $400V_{Pk-Pk}$, R_L = 50Ω		-90		dB
Crosstalk (Note 8)	$V_{CT-DP\_/DM\_}$	f = 20Hz to 20kHz, $V_{D\_}$ = $400V_{Pk-Pk}$, R_L = 50Ω		-80		dB
THD+N	$THD_{DP\_/DM\_}$	f = 20Hz to 20kHz, $V_{D\_}$ = $1V_{Pk-Pk}$, DC bias = 0V, R_L = 32, 600Ω		-100		dB
PSRR	$PSRR_{DP\_/DM\_}$	V_{CC} = 3.7V, V = $400mV_{Pk-Pk}$, f = 217Hz, R_S = R_L = 50Ω		-110		dB
L_{AUDIO} Current Source	I_{LA_SRC}	MANUAL_IDET = 1, SET_IDET = 01	95	100	105	µA
		MANUAL_IDET = 1, SET_IDET = 10	1.05	1.1	1.15	mA
		MANUAL_IDET = 1, SET_IDET = 11	5.25	5.5	5.75	
L_{AUDIO} Current Source Ramp Up/Down Time	t_{RAMP}		43.75	50	56.25	ms
MIC Bias Detection Threshold	MIC_{THR}	V_{CC} = 3.7V, V_{MIC} rising	450	788	1150	mV
	MIC_{THF}	V_{CC} = 3.7V, V_{MIC} falling	350	701	1100	
	MIC_{TH_HYST}	V_{CC} = 3.7V		87		
Total Detection Time	t_{DET}	3 ramps max detection time		600		ms

Electrical Characteristics (continued)

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at V_{CC} = +3.7V, T_A = +25°C) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CC						
CC Disconnect Detection Threshold	$V_{CC\_DD\_TH}$	Audio Accessory mode, Rising	0.5		1.4	V
Leakage Current	I_{L_CC}	CC = 5V	-1		+1	µA
Time to MIC Open and SBU_ Discharge Time From CC High	$t_{CC\_MIC\_DIS}$	$C_{SBU\_}$ < 2µF		7		µs
SBU TO GROUND (GND SWITCH)						
Analog Signal Range	V_{SBU_G}		-0.3		V_{OVLO}	V
On-Resistance	R_{ON-SBU_G}	V_{CC} = 3.7V, I = 100mA		80	150	mΩ
Bandwidth	B_{WSBU_G}	V_{CC} = 3.7V, R_S = R_L = 50Ω		300		MHz
PSRR	P_{SRRSBU_G}	V_{CC} = 3.7V, $V_{SBU\_}$ = 400mV_{Pk-Pk}, f = 217Hz, R_S = R_L = 50Ω		-120		dB
SBU TO MIC (MIC SWITCH)						
Analog Signal Range	V_{SBU_MIC}		0		V_{OVLO}	V
On Resistance	R_{ON-SBU_MIC}	V_{CC} = 3.7V, I = 100mA		1.7	2.9	Ω
Turn-On Time	t_{ON-SBU_MIC}	$V_{SBU\_}$ = 1.5V, R_L = 50Ω, I^2C Control, time from last data bit processed to 90% of final value		20		µs
Turn-Off Time	$t_{OFF-SBU\_MIC}$	$V_{SBU\_}$ = 1.5V, R_L = 50Ω, I^2C Control, time from last data bit processed to 10% of initial value		5		µs
Bandwidth	BW_{SBU_MIC}	$V_{SBU\_}$ = 0dBm, R_S = R_L = 50Ω		30		MHz
THD+N	THD_{SBU_MIC}	500mV_{Pk-Pk}, DC bias = 2V with 2.2kΩ to MIC, f = 20Hz – 20kHz, R_L = 600Ω		100		dB
PSRR	$PSRR_{SBU\_MIC}$	V_{CC} = 3.7V, $V_{SBU\_}$ = 400mV_{Pk-Pk}, f = 217Hz, R_S = R_{SL} = 50Ω		-110		dB
Off Isolation	$V_{ISO-SBU\_MIC}$	$V_{D\_}$ = 400mV_{Pk-Pk}, f = 20kHz, R_L = 50Ω		-100		dB

Electrical Characteristics (continued)

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at V_{CC} = +3.7V, T_A = +25°C) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GROUND SENSE AND UART SWITCHES (GM_SR, GM_SL, MG_SR, MG_SL, TX, RX)						
Analog Signal Range	$V_{GM/MG}$	Ground sense switches	-0.3		+2.5	V
	V_{UART}	UART switches	-0.3		V_{OVLO}	
On Resistance	$R_{ON-GSNS\_}$	Ground Sense, $V_{GM\_/MG\_}$ = 0V, I_{LOAD} = 100mA		1.8	3	Ω
	$R_{ON-UART}$	UART, I_{LOAD} = 10mA		6.5	11.5	
Turn-On Time	$t_{ON-GSNS}$	$V_{COM\_}$ = 1.5V, R_L = 50Ω, I^2C control		45		µs
	$t_{ON-UART}$	$V_{COM\_}$ = 1.5V, R_L = 50Ω, I^2C control		20		
Turn-Off Time	$t_{OFF-GSNS/UART}$	$V_{COM\_}$ = 1.5V, R_L = 50Ω, OVLO event or I^2C control		5		µs
Bandwidth	BW_{GSNS}	R_S = R_L = 50Ω, C_L = 10pF		300		MHz
Crosstalk	$V_{CT-GSNS}$	V_{CC} = 3.7V, R_S = R_L = 50Ω, f = 20kHz		-100		dB
Off Isolation	$V_{ISO-GSNS}$	f = 20kHz, $V_{D\_}$ = 400mV_{Pk-Pk}, R_L = 50Ω		-100		dB
THD+N	THD_{GSNS}	V_{CC} = 3.7V, 10mV_{Pk-Pk}, DC bias = 0V, f = 20Hz – 20kHz, R_S = 50Ω, R_L = 200Ω		0.0004		%
PSRR	$PSRR_{GSNS}$	V = 400mV_{Pk-Pk}, f = 217Hz, R_S = R_L = 50Ω		-120		dB
DIGITAL SIGNALS (SCL, SDA, INT, MAX20328A ONLY)						
Output Voltage Low	V_{OL}	I_{SDA} = 4mA			0.4	V
Output Leakage	I_{LEAK}	V_{SDA} = 5.5V	-1		1	µA
Input Voltage High	V_{IH}		1.4			V
Input Voltage Low	V_{IL}				0.5	V
SCL Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
START Condition (Repeated) Hold Time	$t_{HD:STA}$		0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs

Electrical Characteristics (continued)

(V_{CC} = 2.7V to 5.5V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at V_{CC} = +3.7V, T_A = +25°C) (Note 3)

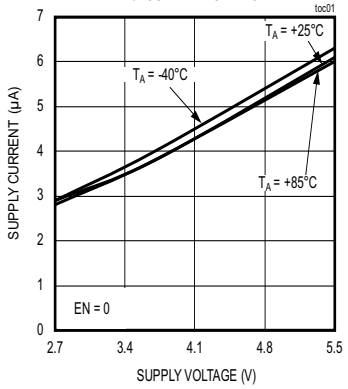
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		0.9	µs
Data Setup Time	$t_{SU:DAT}$		100			µs
Setup Time for a STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}			50		ns
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			135		
Thermal Hysteresis	T_{HYST}			20		
ESD PROTECTION						
HBM		DP_T, DM_T, DP_B, DM_B, SBU1_MG, SBU2_GM, MG_SL, MG_SR, GM_SL, GM_SR		±12		kV
Surge				±25		V
HBM		All other pins		±2		kV

Note 3: All devices are 100% production tested at T_A = +25°C. All temperature limits are guaranteed by design.
Note 4: The switch turns off for voltages above V_{OVLO}, protecting downstream circuits in case a fault condition occurs.
Note 5: $\Delta R_{ON}(MAX) = ABS (R_{ON\_CH1} – R_{ON\_CH2})$.
Note 6: Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over the specified analog signal range.
Note 7: Guaranteed by design.
Note 8: Between two switches.

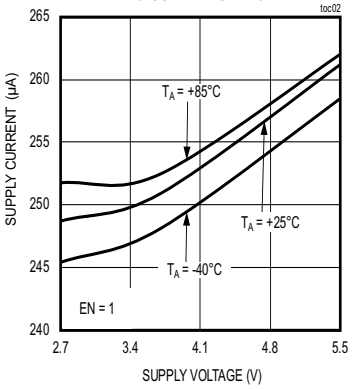
Typical Operating Characteristics

(V_{CC} = 3.7V, T_A = +25°C unless otherwise noted.)

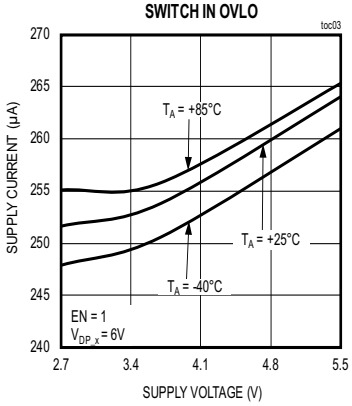
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



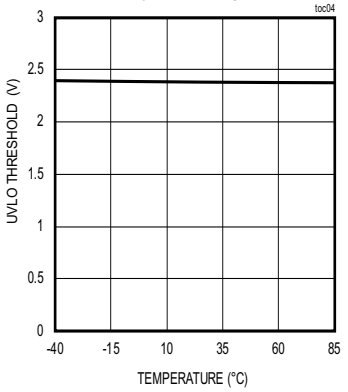
SUPPLY CURRENT vs. SUPPLY VOLTAGE



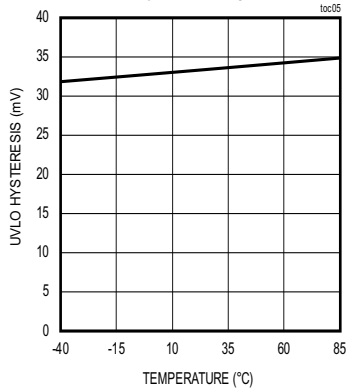
SUPPLY CURRENT vs. SUPPLY VOLTAGE SWITCH IN OVLO



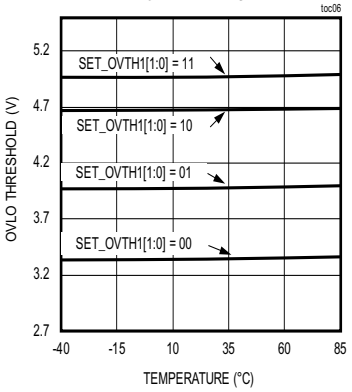
UVLO FALLING THRESHOLD vs. TEMPERATURE



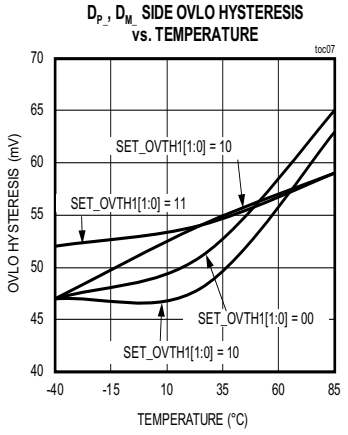
UVLO HYSTERESIS vs. TEMPERATURE



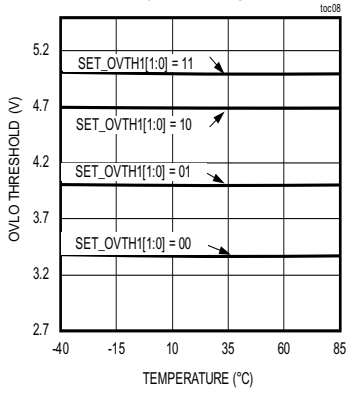
$D_{P\_}$, $D_{M\_}$ SIDE OVLO THRESHOLD vs. TEMPERATURE



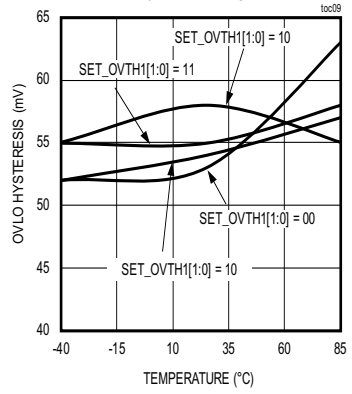
$D_{P\_}$, $D_{M\_}$ SIDE OVLO HYSTERESIS vs. TEMPERATURE



SBU SIDE OVLO THRESHOLD vs. TEMPERATURE



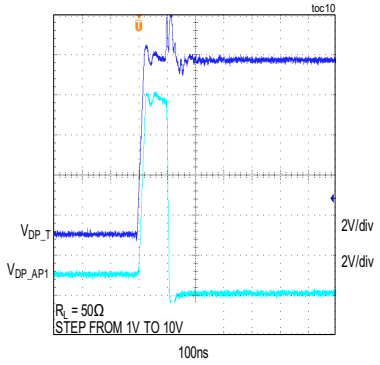
SBU SIDE OVLO HYSTERESIS vs. TEMPERATURE



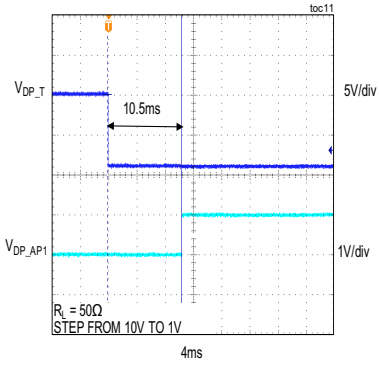
Typical Operating Characteristics (continued)

(V_{CC} = 3.7V, T_A = +25°C unless otherwise noted.)

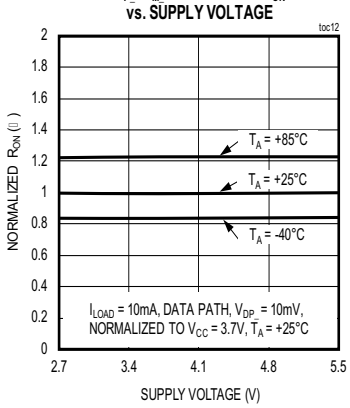
OVLO FAULT RESPONSE TIME



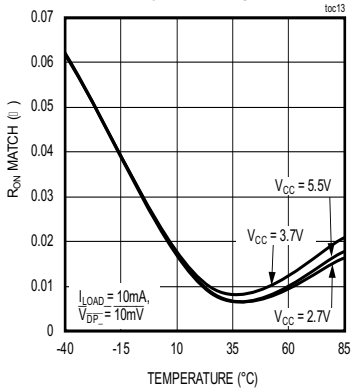
OVLO FAULT RECOVERY TIME



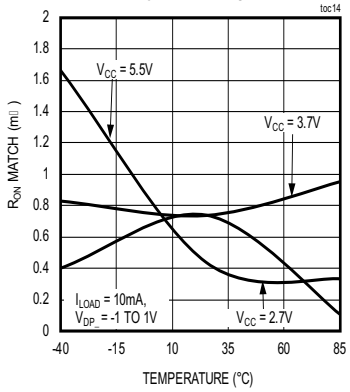
DP_, DM_ NORMALIZED RON vs. SUPPLY VOLTAGE



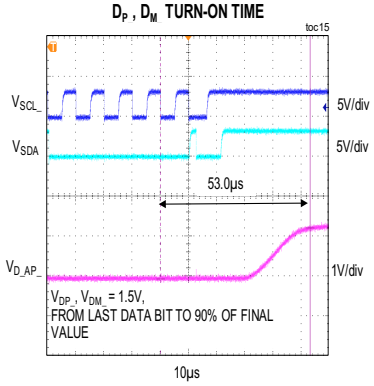
DP_, DM_ RON MATCH vs. TEMPERATURE



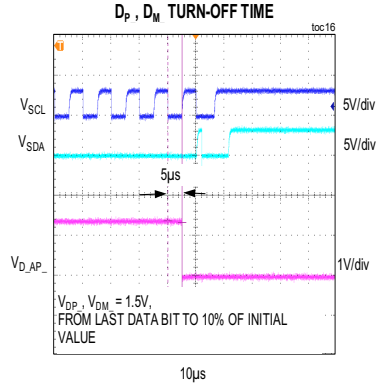
DP_, DM_ RON FLATNESS vs. TEMPERATURE



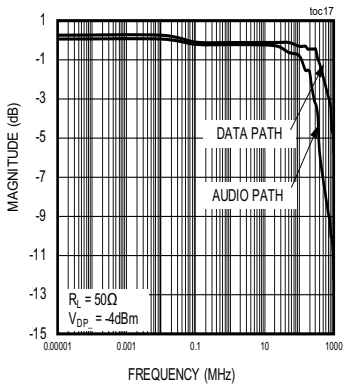
DP_, DM_ TURN-ON TIME



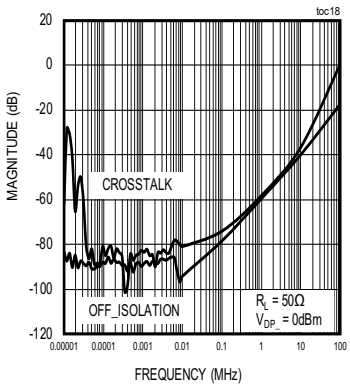
DP_, DM_ TURN-OFF TIME



DP_, DM_ BANDWIDTH DATA AND AUDIO PATHS



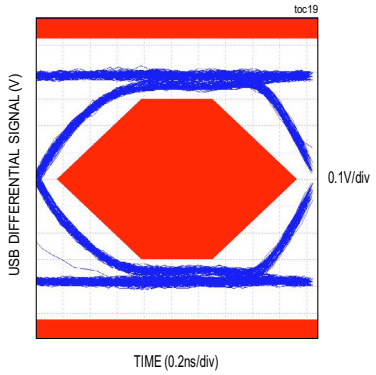
DP_, DM_ AUDIO AND DATA PATHS CROSSTALK AND OFF-ISOLATION



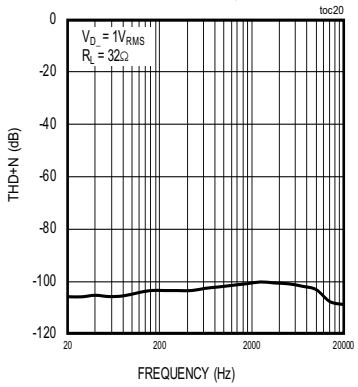
Typical Operating Characteristics (continued)

(V_{CC} = 3.7V, T_A = +25°C unless otherwise noted.)

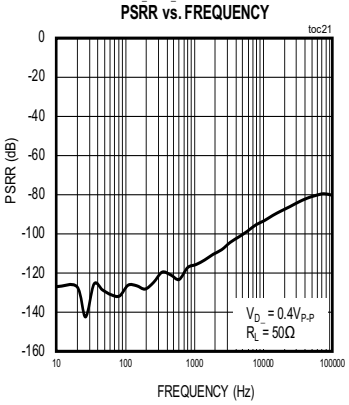
EYE DIAGRAM



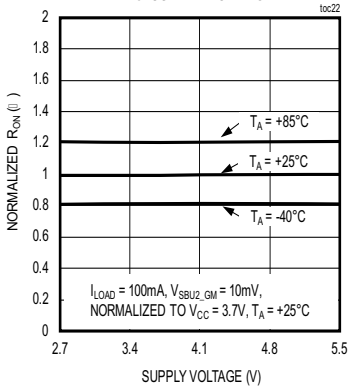
D_P , D_M AUDIO PATH
THD+N vs. FREQUENCY



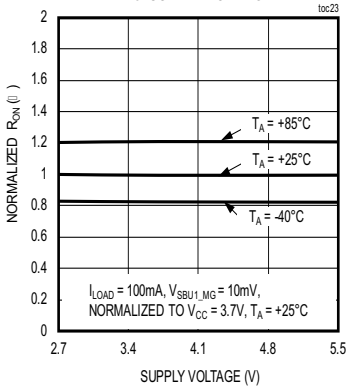
D_P , D_M AUDIO PATH
PSRR vs. FREQUENCY



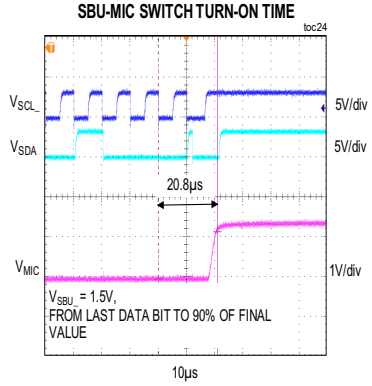
SBU2 - AGND NORMALIZED R_{ON}
vs. SUPPLY VOLTAGE



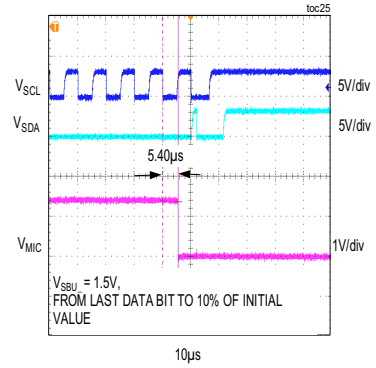
SBU1 - MIC NORMALIZED R_{ON}
vs. SUPPLY VOLTAGE



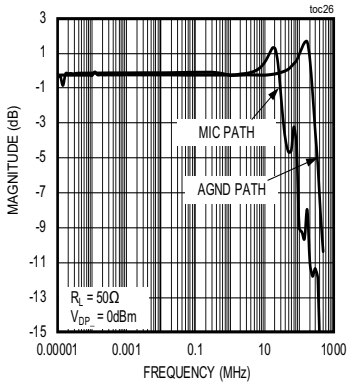
SBU-MIC SWITCH TURN-ON TIME



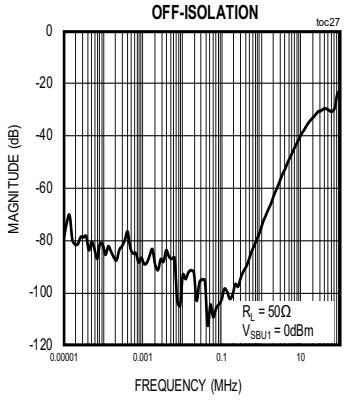
SBU-MIC SWITCH TURN-OFF TIME



SBU_ BANDWIDTH
MIC AND AGND PATHS



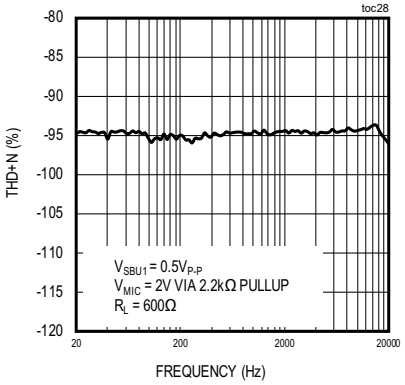
SBU_ MIC AND AGND PATHS
OFF-ISOLATION



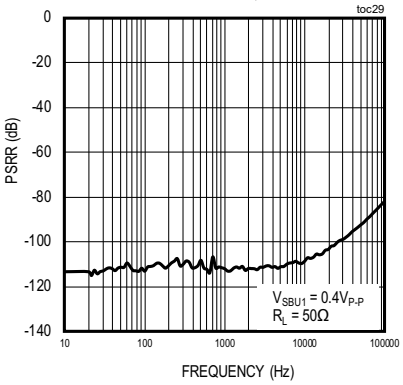
Typical Operating Characteristics (continued)

(V_{CC} = 3.7V, T_A = +25°C unless otherwise noted.)

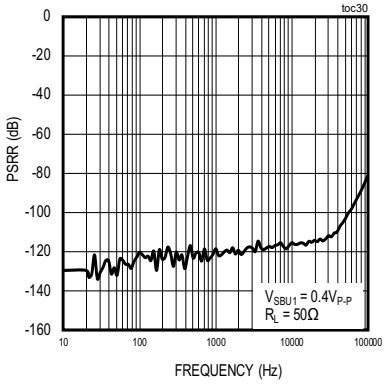
**SBU MIC PATH
THD+N vs. FREQUENCY**



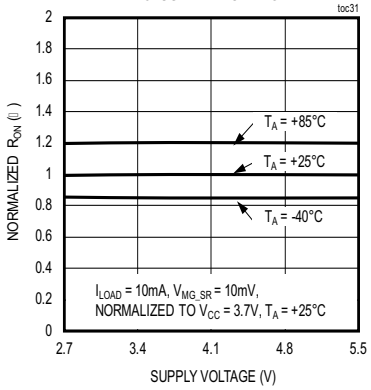
**SBU MIC PATH
PSRR vs. FREQUENCY**



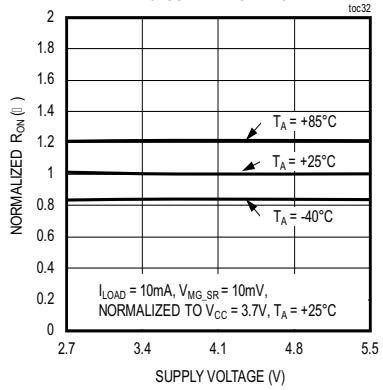
**SBU AGND PATH
PSRR vs. FREQUENCY**



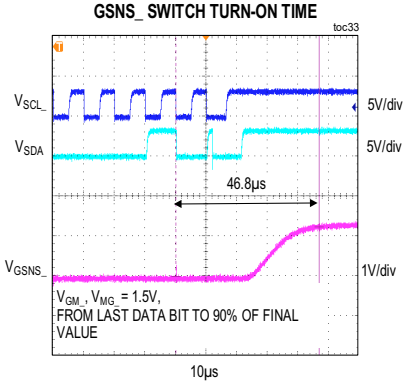
**GSNS NORMALIZED R_{ON}
vs. SUPPLY VOLTAGE**



**UART NORMALIZED R_{ON}
vs. SUPPLY VOLTAGE**



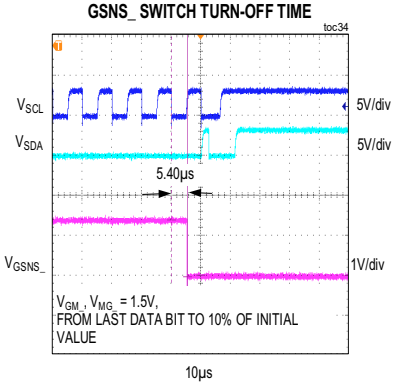
GSNS_ SWITCH TURN-ON TIME



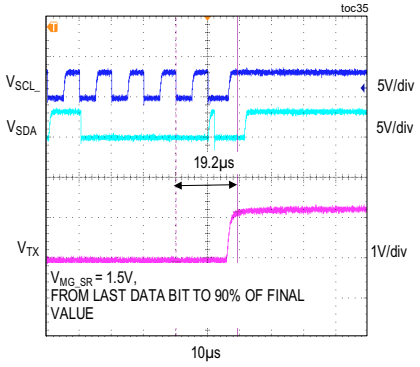
Typical Operating Characteristics (continued)

(V_{CC} = 3.7V, T_A = +25°C unless otherwise noted.)

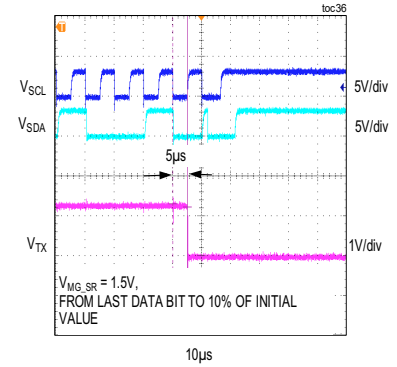
GSNS_ SWITCH TURN-OFF TIME



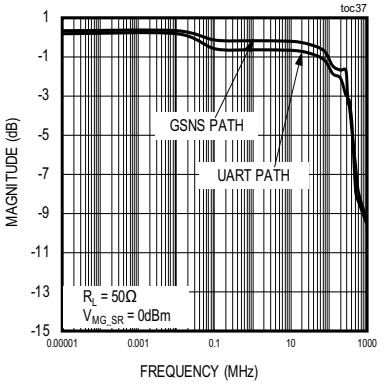
UART SWITCH TURN-ON TIME



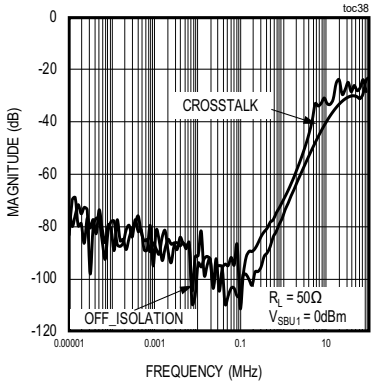
UART SWITCH TURN-OFF TIME



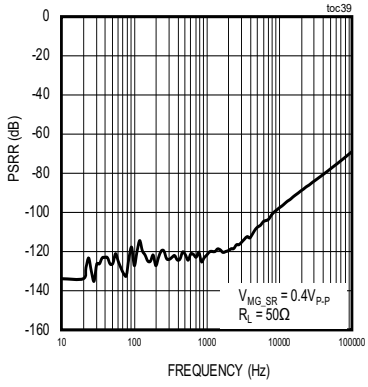
MG_S_BANDWIDTH
GSNS AND UART PATHS



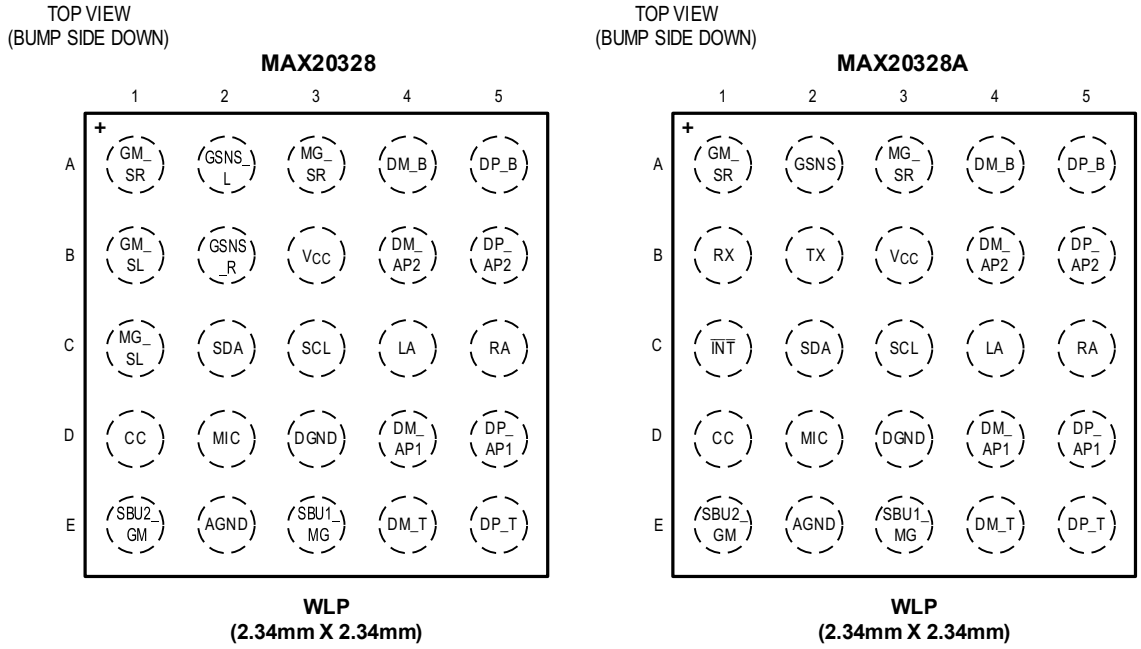
GSNS AND UART
OFF-ISOLATION AND CROSSTALK



GSNS PSRR vs. FREQUENCY



Bump Configurations



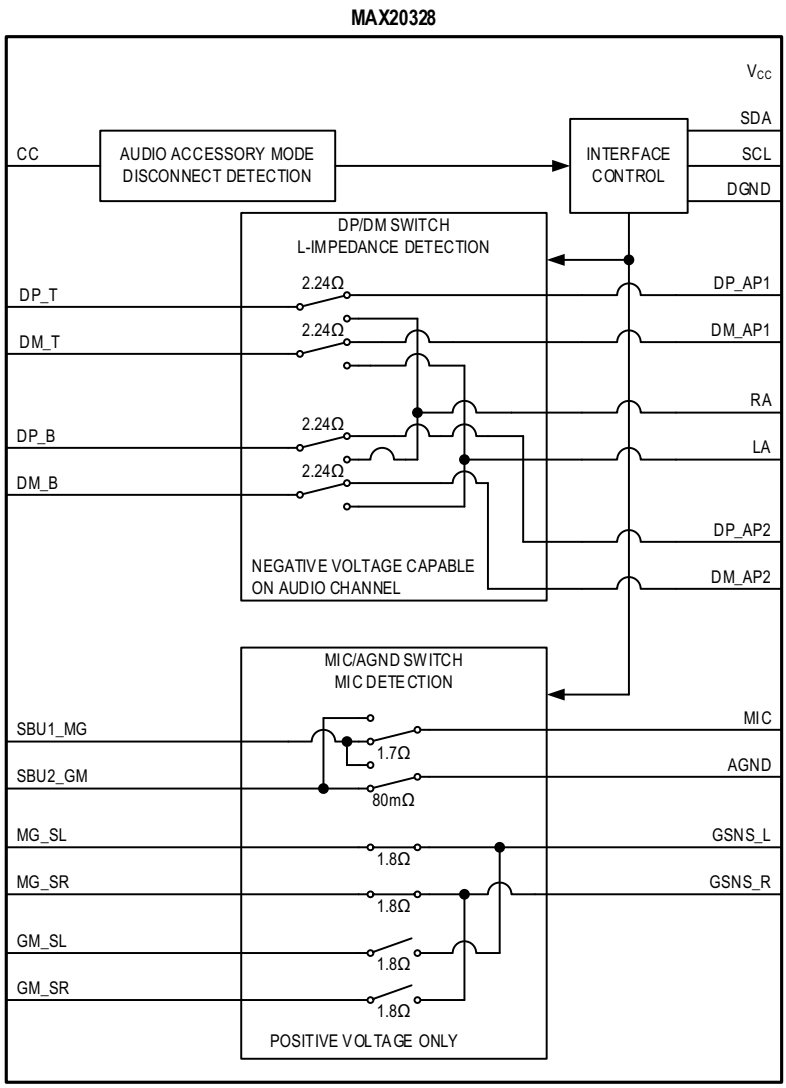
Bump Description

BUMP		NAME	FUNCTION
MAX20328	MAX20328A		
A1	A1	GM_SR	Analog Ground/MIC Sense Input for Right Audio Channel
A2	—	GSNS_L	Ground Sense Output for Left Audio Channel
—	A2	GSNS	Ground Sense Output
A3	A3	MG_SR	MIC/Analog Ground Sense Input for Right Audio Channel
A4	A4	DM_B	DM Bottom Side Data Line of the External USB Type-C Port
A5	A5	DP_B	DP Bottom Side Data Line of the External USB Type-C Port
B1	—	GM_SL	Analog Ground/MIC Sense Input for Left Audio Channel
—	B1	RX	UART RX Line
B2	—	GSNS_R	Ground Sense Output for Right Audio Channel
—	B2	TX	UART TX Line
B3	B3	V_{CC}	Power Supply. Bypass to ground with 1µF effective capacitance.
B4	B4	DM_AP2	DM Data Line to AP2
B5	B5	DP_AP2	DP Data Line to AP2

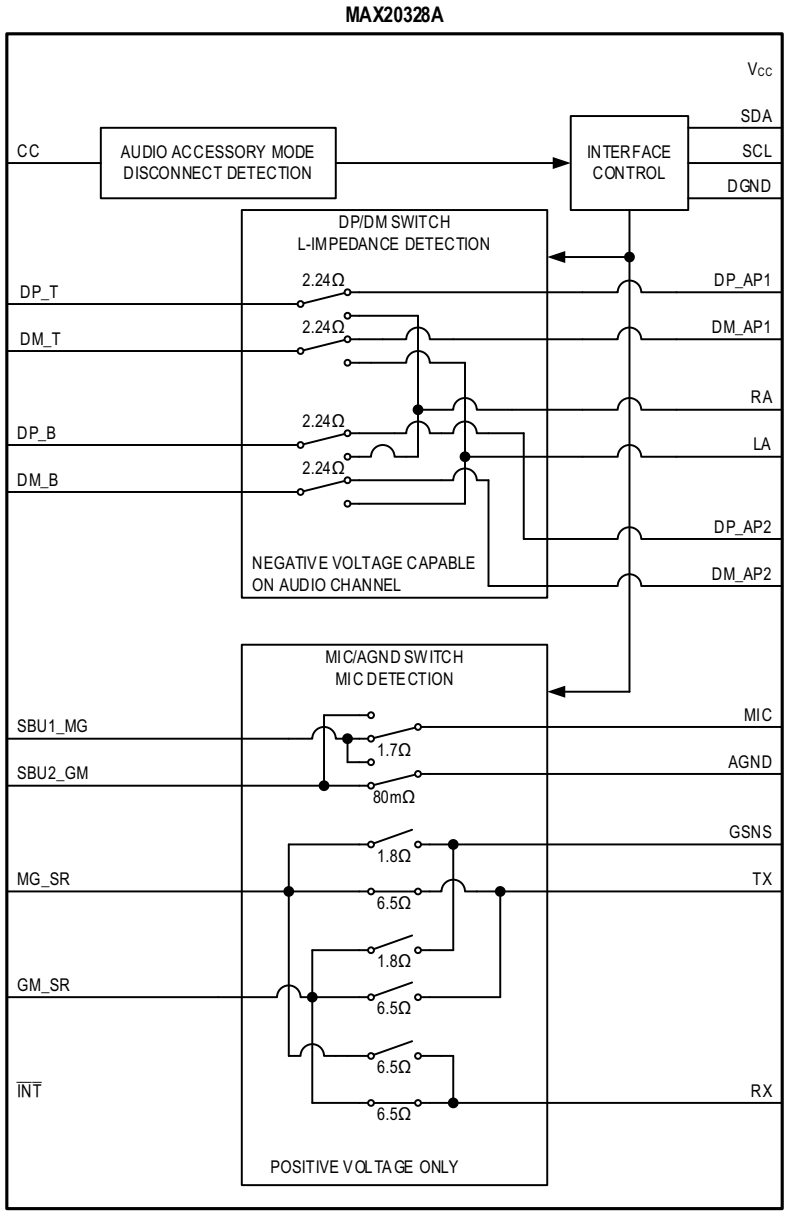
Bump Description (continued)

BUMP		NAME	FUNCTION
MAX20328	MAX20328A		
C1	—	MG_SL	MIC/Analog Ground Sense Input for Left Audio Channel
—	C1	$\overline{INT}$	Open Drain Output for Interrupt Signaling. Active low.
C2	C2	SDA	I^2C Data Line
C3	C3	SCL	I^2C Clock Line
C4	C4	LA	Left Audio Channel Output
C5	C5	RA	Right Audio Channel Output
D1	D1	CC	CC Line from the External USB Type-C Port
D2	D2	MIC	MIC Output
D3	D3	DGND	Digital Ground. Connect DGND and AGND together for correct operation.
D4	D4	DM_AP1	DM Data Line to AP1
D5	D5	DP_AP1	DP Data Line to AP1
E1	E1	SBU2_GM	Analog Ground/MIC, SBU2 Line
E2	E2	AGND	Analog Ground Substrate Connection. Connect DGND and AGND together for correct operation.
E3	E3	SBU1_MG	MIC/Analog Ground, SBU1 Line
E4	E4	DM_T	DM Top Side Data Line of the External USB Type-C Port
E5	E5	DP_T	DP Top Side Data Line of the External USB Type-C Port

Block Diagram



Block Diagram (continued)



Detailed Description

The MAX20328/MAX20328A are USB Type-C audio interface and protection ICs for use in portable devices. As USB power delivery makes a high-voltage charging solution readily available on Type-C connectors, the data and SBU lines are at risk of shorting to a high bus voltage, causing permanent damage to the portable device.

The MAX20328/MAX20328A route incoming signals through the USB Type-C data path or audio path based on information received from a Type-C controller IC or the application processor (AP) controller. The devices offer automatic microphone orientation and impedance detection for audio devices, pop-up noise suppression, and surge protection on pins connected directly to the USB Type-C port.

Operation

All switches are open until the MAX20328/MAX20328A are enabled. To enable the devices, write the EN bit (0x06[4]) high. Once enabled, the switches default to the behaviors selected by the MODE[2:0] bits (0x06[2:0]) in automatic mode. See Table 1 and Table 2 for the switch configurations of each MODE[2:0] setting.

Table 1. MAX20328 Switch Configurations

	SWITCH CONNECTION									
MODE[2:0]	**DP_T**	**DM_T**	**DP_B**	**DM_B**	**SBU1_MG**	**SBU2_GM**	**MG_SL**	**MG_SR**	**GM_SL**	**GM_SR**
OFF [000]	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
ON A [001]	DP_AP1	DM_AP1	DP_AP2	DM_AP2	MIC	AGND	OPEN	OPEN	GSNS_L	GSNS_R
ON B [010]	DP_AP1	DM_AP1	DP_AP2	DM_AP2	AGND	MIC	GSNS_L	GSNS_R	OPEN	OPEN
Set by 0x0D and 0x0E [011]	—	—	—	—	—	—	—	—	—	—
UART [100]	DP_AP1	DM_AP1	DP_AP2	DM_AP2	OPEN	OPEN	OPEN	GSNS_R	GSNS_L	OPEN
USB [101]	DP_AP1	DM_AP1	DP_AP2	DM_AP2	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN
Audio Accessory (Dual Ground Sense) [110]*	RA	LA	RA	LA	MIC *(1)	AGND *(1)	OPEN *(1)	OPEN *(1)	GSNS_L *(1)	GSNS_R *(1)
					AGND *(2)	MIC *(2)	GSNS_L *(2)	GSNS_R *(2)	OPEN *(2)	OPEN *(2)
Audio Accessory (Single Ground Sense) [111]*	RA	LA	RA	LA	MIC *(1)	AGND *(1)	OPEN *(1)	OPEN *(1)	GSNS_L *(1)	OPEN *(1)
					AGND *(2)	MIC *(2)	GSNS_L *(2)	OPEN *(2)	OPEN *(2)	OPEN *(2)

** Controlled by the state machine. Refer to the state diagram of Figure 1.*

**(1) When MG_CHK_DIS = 1 OR ADC_CTL ≠ 11, configuration valid when CC_POS = 0*

**(2) When MG_CHK_DIS = 1 OR ADC_CTL ≠ 11, configuration valid when CC_POS = 1*

Table 2. MAX20328A Switch Configurations

MODE[2:0]	SWITCH CONNECTION									
	DP_T	**DM_T**	**DP_B**	**DM_B**	**SBU1_MG**	**SBU2_GM**	**MG_SL**	**MG_SR**	**GM_SL**	**GM_SR**
OFF [000]	OPEN	OPEN	OPEN	OPEN	OPEN	OPEN	—	OPEN	—	OPEN
ON A [001]	DP_AP1	DM_AP1	OPEN	OPEN	MIC	AGND	—	TX	—	RX
Default Mode [010/011]	—	—	—	—	—	—	—	—	—	—
UART [100]	DP_AP1	DM_AP1	OPEN	OPEN	OPEN	OPEN	—	TX *(1) RX *(2)	—	RX *(1) TX *(2)
USB [101]	OPEN	OPEN	DP_AP2	DM_AP2	OPEN	OPEN	—	TX *(1) RX *(2)	—	RX *(1) TX *(2)
Audio Accessory (Single ground sense) SBU1_MG = MIC SBU1_MG = AGND [110/111]*	RA	LA	RA	LA	MIC *(3) AGND* (4)	AGND* (3) MIC *(4)	—	OPEN *(3) GSNS *(4)	—	GSNS *(3) OPEN *(4)

** Controlled by the state machine. Refer to the state diagram of Figure 1.*

**(1) CC_POS = 0*

**(2) CC_POS = 1*

**(3) When MG_CHK_DIS = 1 OR ADC_CTL ≠ 11, configuration valid when CC_POS = 0*

**(4) When MG_CHK_DIS = 1 OR ADC_CTL ≠ 11, configuration valid when CC_POS = 1*

Enable

Both the MAX20328 and MAX20328A are enabled by default (EN = 1). To disable a device, write EN = 0 (0x06[4] = 0). In the disable state, all switches are open and the devices enter a low-current mode to minimize the supply current. When a device is disabled, the ADC_VAL register (0x01) and bits 0x02[7:6] and 0x02[3:0] are reset to 0. These bits provide information regarding the audio accessory impedance and microphone orientation. When EN is set to 1, the device runs through the state machine diagrammed in Figure 1.

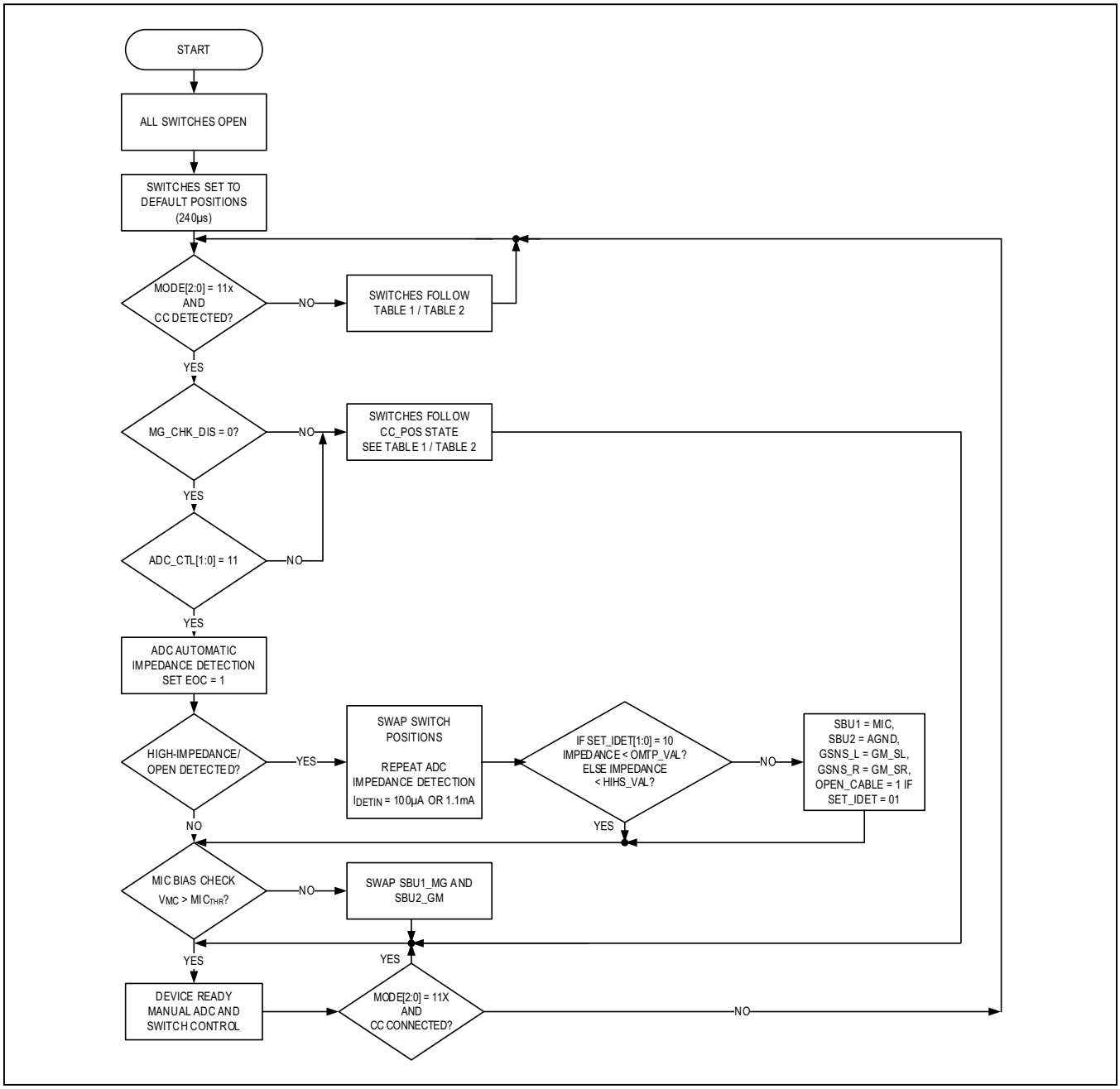


Figure 1. Startup State Machine (FSM)

Pop-Up Noise Suppression

If a 3.5mm jack is removed from a USB Type-C audio adapter when the adapter is connected to a portable device, pop-up noise may be heard due to the MIC line bias. When the CC pin goes high to signal an audio accessory removal, the MIC/AGND and AGND/MIC switches disconnect from the MIC bias and discharge to ground within 50µs.

Impedance Detection

The MAX20328/MAX20328A can perform an impedance detection to measure the impedance of a connected audio accessory or detect an open cable. This function uses a precision, 8-bit ADC to measure the voltage dropped across the left audio channel while the IDET current source is active. An impedance measurement triggers automatically when EN is set to 1 if ADC_CTL[1:0] = 11 and follows the state machine in Figure 1. Changing MODE[2:0] to 1xx while the device is enabled also triggers an automatic measurement. If ADC_CTL[1:0] = 01 or 10, impedance measurements are manually triggered by writing FORCE_ADC_START high.

When OPEN_DETECT = 1 (0x09[5]), the impedance detection starts with IDET = 100µA. Otherwise, the 1.1mA and 5.5mA current sources are used for low impedance detection. Figure 2 details the impedance detection process.

Current Sources

Three current source values are available for impedance detection. For high impedance audio accessories and open cable detection, a 100µA source is used. When the accessory impedance is low, i.e. ADC_VAL < HIHS_VAL after EOC goes high, IDET switches to 1.1mA. For very low impedance accessories, the 1.1mA source increases to 5.5mA. The value of the current source used in the latest impedance measurement is available in SET_IDET[1:0] (0x09[3:2]).

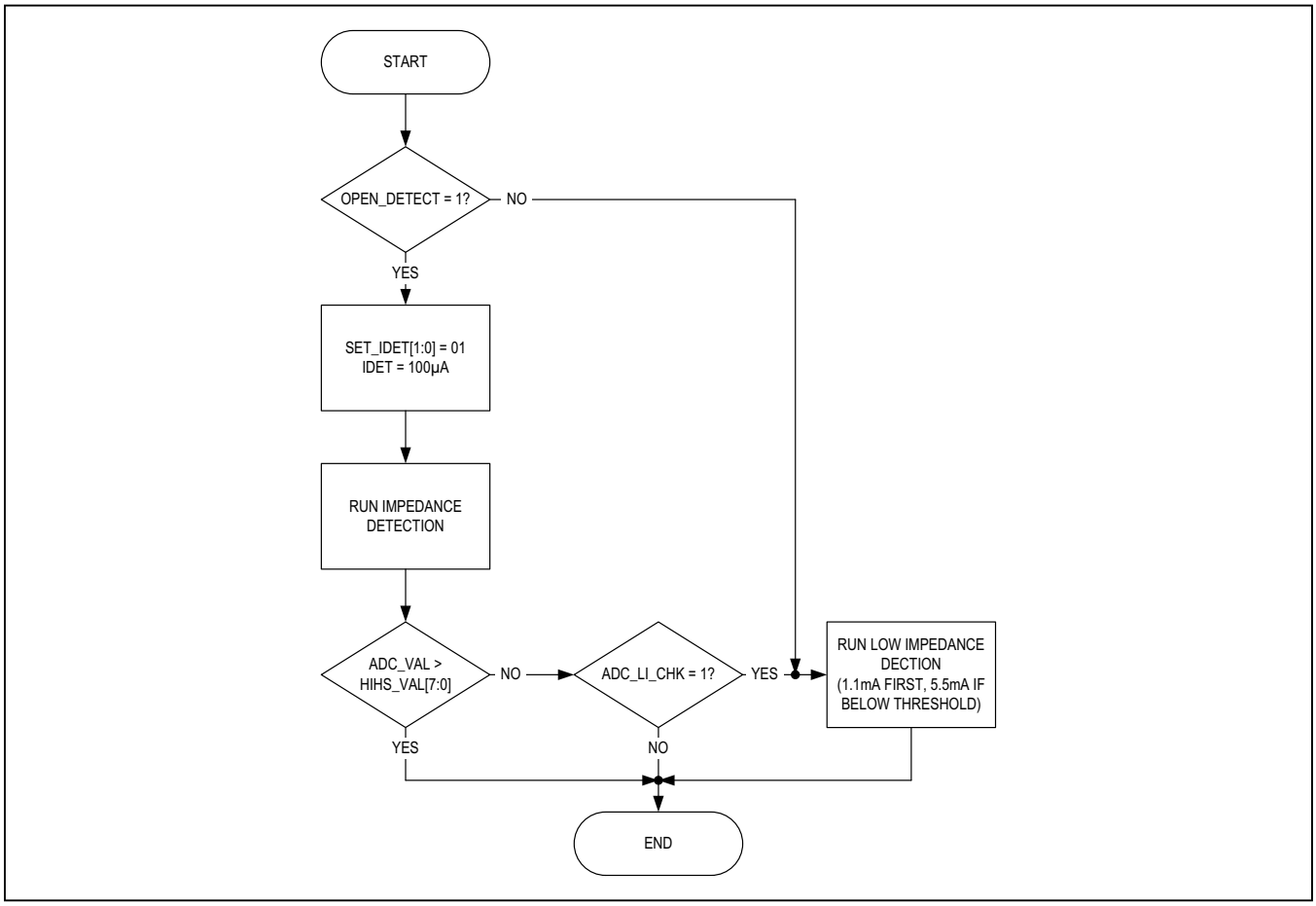


Figure 2.Impedance Detection Process

ADC Result

When the EOC bit goes high, the ADC result is available in ADC_VAL (register 0x01). The following conversion extracts the channel impedance from ADC_VAL and SET_IDET[1:0]

R = (ADC_VAL[7:0] x 4.746mV) / SET_IDET[1:0]

To account for potential offsets in the ADC and current source values, Table 3 provides the minimum and maximum values the ADC may provide for common headset impedance values.

Open Cable Check

The MAX20328/MAX20328A can perform an open cable check during the impedance measurement. If the 100µA current source detects a high impedance where ADC_VAL > HIHS_VAL, the OPEN_CABLE bit (0x02[3]) goes high to signal the open cable.

MIC/GND Detection

Because a USB Type-C audio accessory can be inserted in two orientations, it is necessary to identify the MIC and GND lines. After an impedance detection, the state machine determines if the MIC/AGND switches are in the correct orientations. If ADC_VAL is greater than the thresholds set in OMTP_VAL or HIHS_VAL, the switch positions are swapped and the impedance measurement is repeated.

In cases where the 3.5mm to USB Type-C adapter has a non-standard internal connection of one SBU to ground, there is the potential risk for the MIC line to be shorted to ground. To prevent this situation, the MAX20328/MAX20328A can check for the presence of a bias on the MIC line at the end of an automatic impedance detection. When MIC_CHK_DIS = 0 (0x07[1]), the devices check for a bias greater than MIC_{THR} on the MIC line. If no bias is detected, the states of the MIC/AGND switches are swapped immediately after the DEVICE_READY bit goes high. To prevent the bias check from incorrectly reassigning the switches, a bias voltage must be applied to MIC before running an impedance detection.

I^2C Interface

The MAX20328/MAX20328A use the two-wire I2C interface to communicate with a host application processor. The configuration settings and status information provided through this interface are detailed in the register descriptions (Tables 5 – 19). Both devices use the seven-bit slave address 0b0010101 (0x2A for writes, 0x2B for reads).

Applications Information

Applying Signals to an Open Switch

Due to the structure of the DP_/DM_ inputs, the switches will not close when a large, high frequency signal is applied to the open terminal. To ensure the desired path closes properly, avoid applying fast signals >1V to the DP_/DM_ pins before closing the switch.

Table 3. ADC to Impedance Range Conversion Guide

ACCESSORY IMPEDANCE (Ω)	RESISTOR RANGE (Ω)		ADC CODE (HEX)		SET_IDET[1:0]	
16	0	22.4	00	1A	1	1
32	25.0	40.6	1D	2F	1	1
64	44.9	87.2	34	65	1	1
150	94.9	189.8	16	2C	1	0
300	211.4	431.5	31	64	1	0
600	474.6	957.8	6E	DE	1	0
2000	1,001.4	12,150	15	FF	0	x

I²C Serial Interface

The I²C serial interface is used to configure the device. Figure 3 shows the I²C timing diagram.

Serial Addressing

When in I²C mode, the devices operate as slave devices that send and receive data through an I²C-compatible 2-wire interface. The interface uses a serial data line (SDA) and a serial-clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master (typically a microcontroller) initiates all data transfers to and from the MAX20328/MAX20328A and generates the SCL clock that synchronizes the data transfer. The SDA line operates as both an input and an open drain output. A pullup resistor is required on SDA. The SCL line operates only as an input. A pullup resistor is required on SCL if there are multiple masters on the 2-wire interface, or if the master in a single-master system has an open drain SCL output. Each transmission consists of a START condition sent by a master, followed by the MAX20328/MAX20328A 7-bit slave address plus R/W bit, a register address byte, one or more data bytes, and finally a STOP condition.

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high (Figure 4). When the master has finished communicating with the slave, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

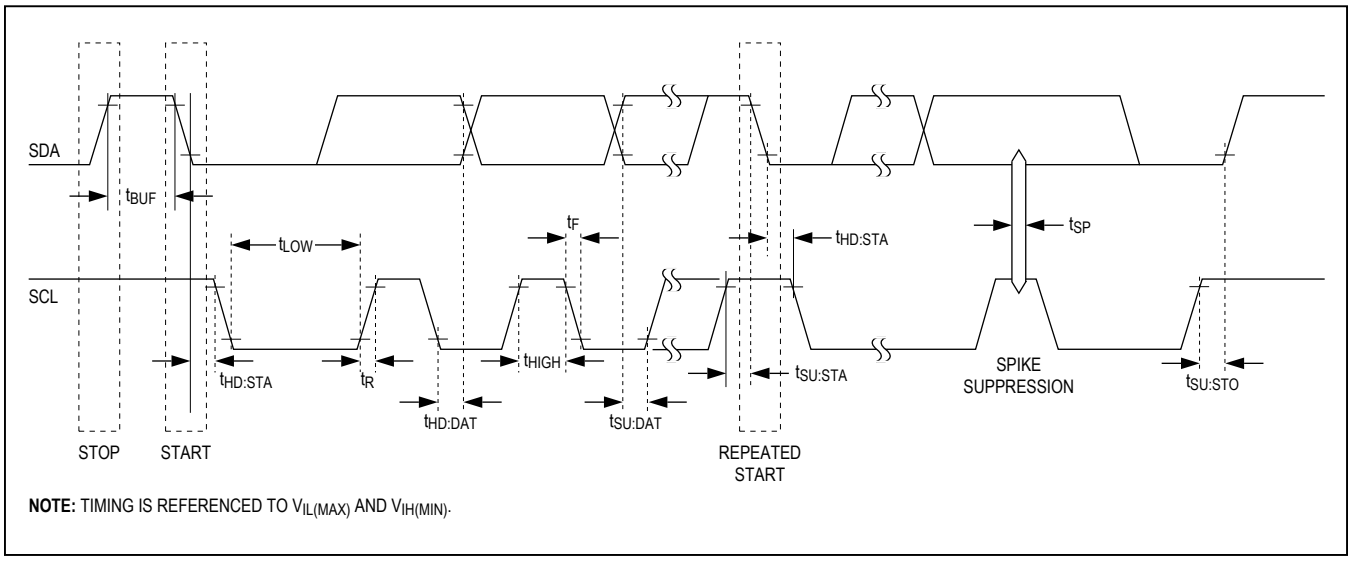


Figure 3. I²C Timing Diagram.

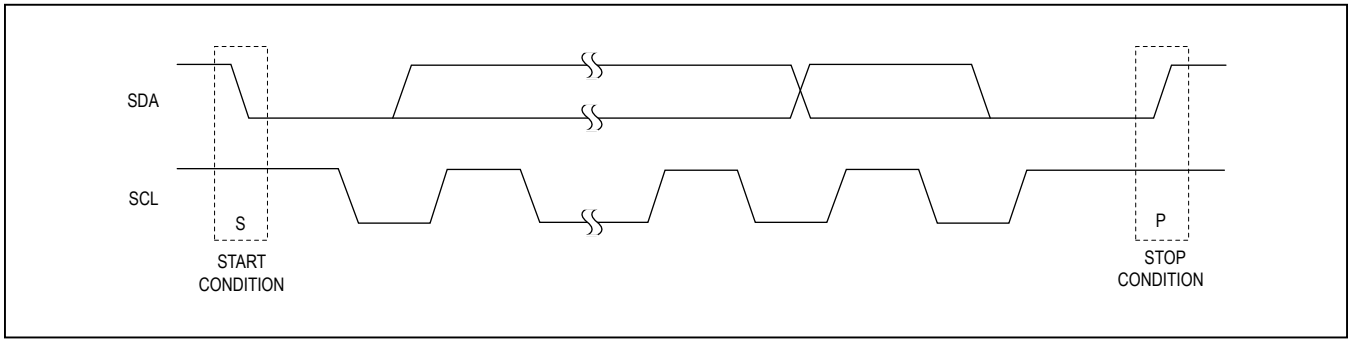


Figure 4. Start and Stop Conditions

Bit Transfer

One data bit is transferred during each clock pulse (Figure 5). The data on SDA must remain stable while SCL is high.

Acknowledge

The acknowledge bit is a clocked 9th bit (Figure 6), which the recipient uses to handshake receipt of each byte of data. Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse. The SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the devices, it generates the acknowledge bit because the device is the recipient. When the device is transmitting to the master, the master generates the acknowledge bit because the master is the recipient. If the device does not pull SDA low, a not acknowledge is indicated.

Slave Address

The devices have a 7-bit slave address. The bit following a 7-bit slave address is the R/$\overline{W}$ bit, which is low for a write command and high for a read command. The slave address for the device is 0b00101011 for read commands and 0b00101010 for write commands. This is summarized in Table 4.

Table 4. I²C Slave Addresses

ADDRESS FORMAT	VALUE	
	HEX	BINARY
7-BIT SLAVE ADDRESS	0x15	001 0101
WRITE ADDRESS	0x2A	0010 1010
READ ADDRESS	0x2B	0010 1011

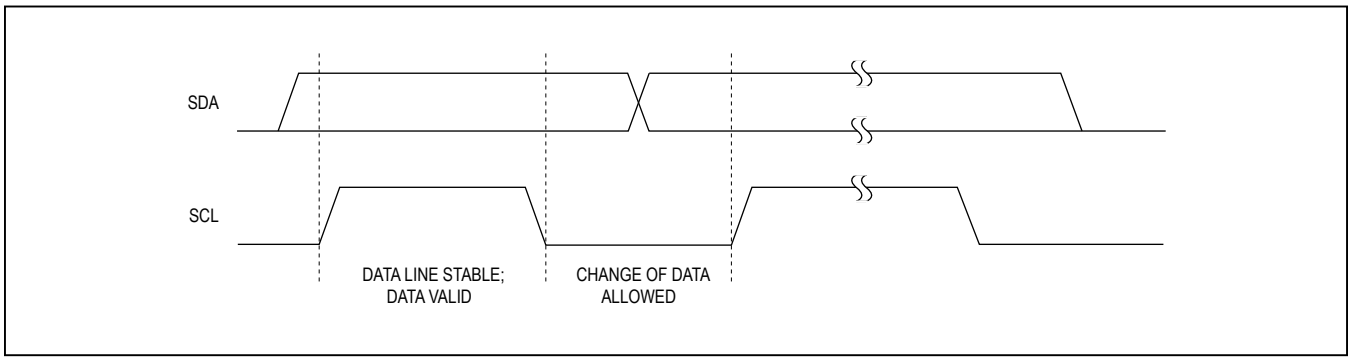


Figure 5. Bit Transfer

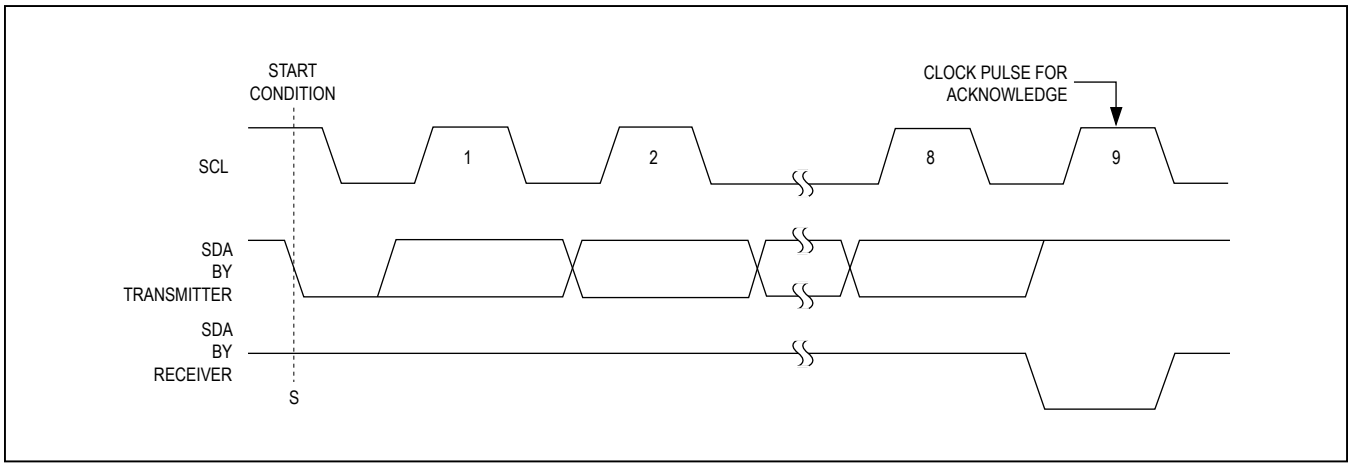


Figure 6. Acknowledge

Bus Reset

The MAX20328/MAX20328A resets the bus with the I²C start condition for reads. When the R/$\overline{W}$ bit is set to 1, the MAX20328/MAX20328A transmits data to the master, thus the master is reading from the device.

Format for Writing

A write to the devices comprises the transmission of the slave address with the R/$\overline{W}$ bit set to zero, followed by at least 1 byte of information. The first byte of information is the register address or command byte. The register address determines which register of the device is to be written by the next byte, if received. If a STOP (P) condition is detected after the register address is received, then the device takes no further action beyond storing the register address. Any bytes received after the register address are data bytes. The first data byte goes into the register selected by the register address and subsequent data bytes go into subsequent registers (Figure 7). If multiple data bytes are transmitted before a STOP condition, these bytes are stored in subsequent registers because the register addresses auto-increments (Figure 8).

Format for Reading

The MAX20328/MAX20328A is read using the internally stored register address as an address pointer, the same way the stored register address is used as an address pointer for a write. The pointer auto-increments after each data byte is read using the same rules as for a write. Thus, a read is initiated by first configuring the register address by performing a write (Figure 9). The master can now read consecutive bytes from the device, with the first data byte being read from the register addressed pointed by the previously written register address (Figure 10). Once the master sounds a NACK, the MAX20328/MAX20328A stop sending valid data.

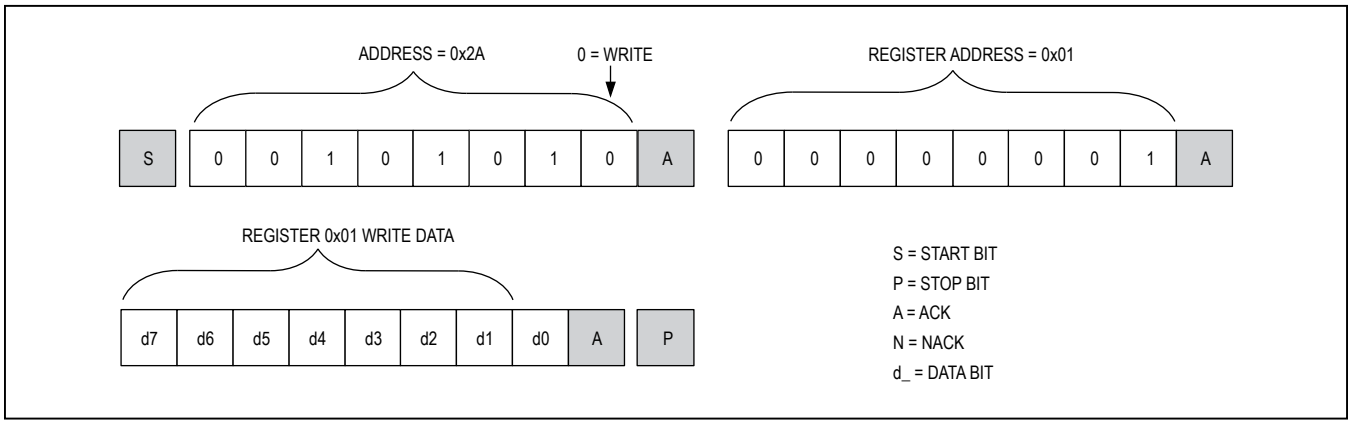


Figure 7. Format for I²C Write

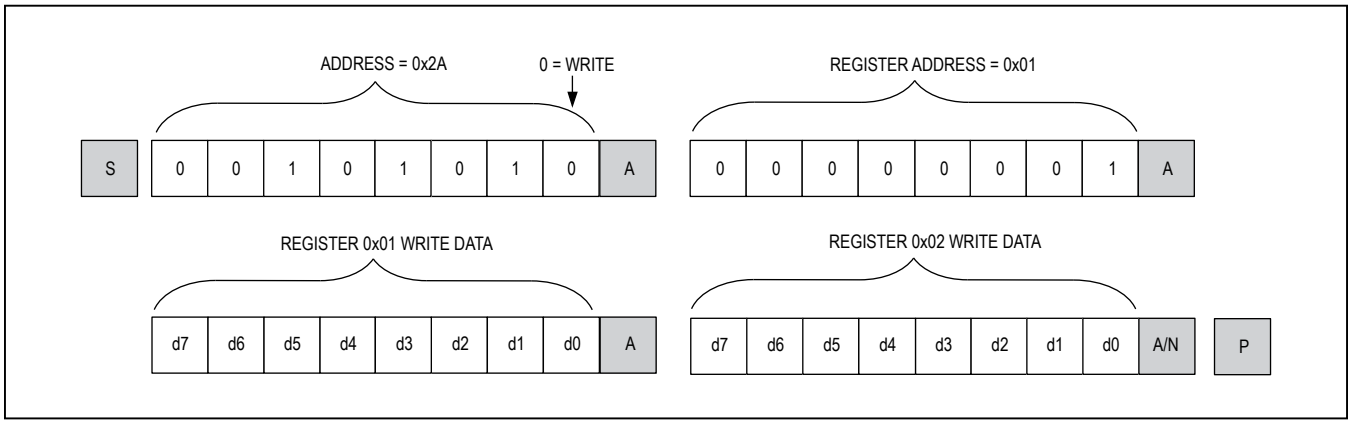


Figure 8. Format for Writing to Multiple Registers

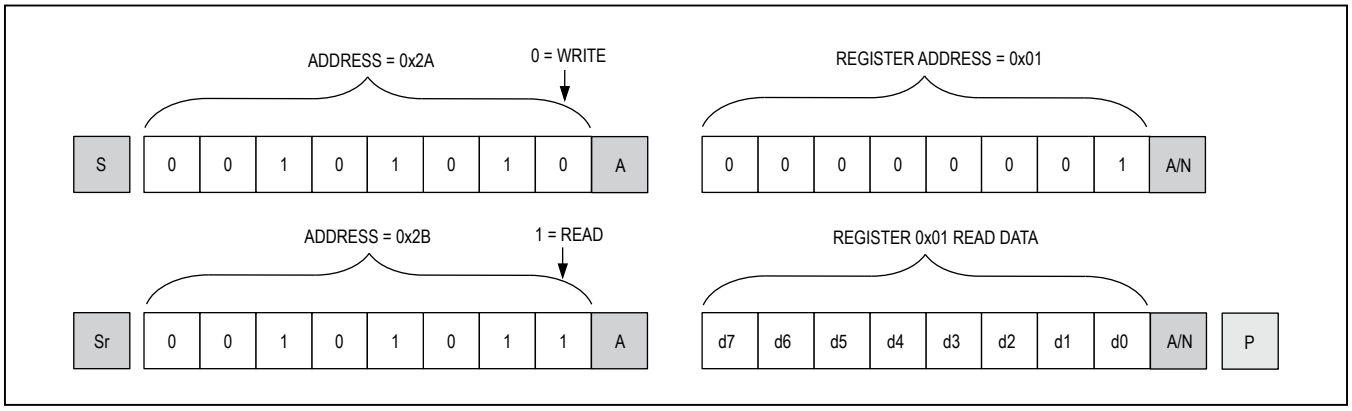


Figure 9. Format for Reads (Repeated Start)

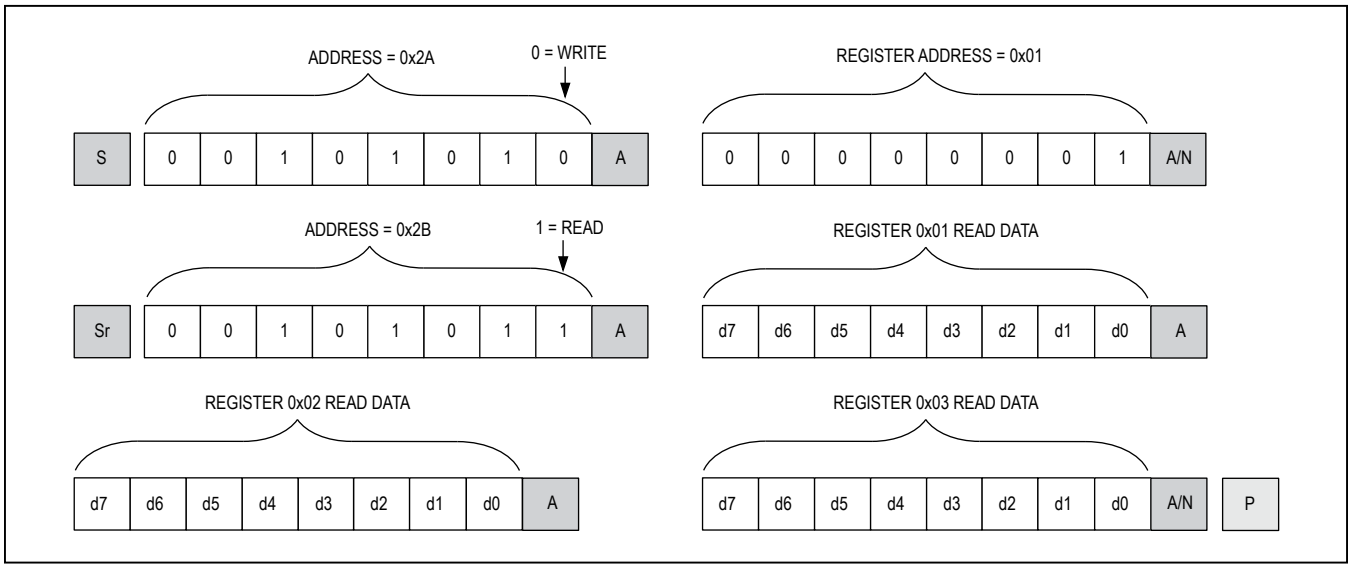


Figure 10. Format for Reading Multiple Registers