



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China





# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2064

## General Description

The MAX2064 high-linearity, dual analog variable-gain amplifier (VGA) operates in the 50MHz to 1000MHz frequency range. Each analog attenuator is controlled using an external voltage, or through the SPI™-compatible interface using an on-chip 8-bit DAC.

Since each of the stages has its own external RF input and RF output, this component can be configured to either optimize noise figure (NF) (amplifier configured first) or OIP3 (amplifier last). The device's performance features include 24dB amplifier gain (amplifier only), 4.4dB NF at maximum gain (includes attenuator insertion losses), and a high OIP3 level of +41dBm. Each of these features makes the device an ideal VGA for multipath receiver and transmitter applications.

In addition, the device operates from a single +5V supply with full performance, or a +3.3V supply for an enhanced power-savings mode with lower performance. The device is available in a compact 48-pin TQFN package (7mm x 7mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range, from  $T_C = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

## Applications

IF and RF Gain Stages  
 Temperature-Compensation Circuits  
 WCDMA, TD-SCDMA, and cdma2000® Base Stations  
 GSM 850/GSM 900 EDGE Base Stations  
 WiMAX™, LTE, and TD-LTE Base Stations and Customer-Premise Equipment  
 Fixed Broadband Wireless Access  
 Wireless Local Loop  
 Military Systems

*SPI is a trademark of Motorola, Inc.*

*cdma2000 is a registered trademark of Telecommunications Industry Association.*

*WiMAX is a trademark of WiMAX Forum.*

## Features

- ◆ Independently Controlled Dual Paths
- ◆ 50MHz to 1000MHz RF Frequency Range
- ◆ Pin-Compatible Family Includes  
     MAX2062 (Analog/Digital VGA)  
     MAX2063 (Digital-Only VGA)
- ◆ 22dB (typ) Maximum Gain
- ◆ 0.19dB Gain Flatness Over 100MHz Bandwidth
- ◆ 33dB Gain Range
- ◆ 49dB Path Isolation (at 200MHz)
- ◆ Built-In 8-Bit DACs for Analog Attenuation Control
- ◆ Excellent Linearity at 200MHz (Configured with Amp Last)
  - +41dBm OIP3
  - +59dBm OIP2
  - +19dBm Output 1dB Compression Point
- ◆ 4.4dB Typical Noise Figure (at 200MHz)
- ◆ Single +5V Supply (or +3.3V Operation)
- ◆ Amplifier Power-Down Mode for TDD Applications

## Ordering Information

| PART         | TEMP RANGE     | PIN-PACKAGE |
|--------------|----------------|-------------|
| MAX2064ETM+  | -40°C to +85°C | 48 TQFN-EP* |
| MAX2064ETM+T | -40°C to +85°C | 48 TQFN-EP* |

+ Denotes a lead (Pb)-free/RoHS-compliant package.

\*EP = Exposed pad.

T = Tape and reel.

# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

## ABSOLUTE MAXIMUM RATINGS

|  |                 |   |                 |
|--|-----------------|---|-----------------|
| VCC_AMP_1, VCC_AMP_2, VCC_RG to GND                        | -0.3V to +5.5V  | RF Input Power (AMP_IN_1, AMP_IN_2)       | +18dBm          |
| PD_1, PD_2, AMPSET to GND                                  | -0.3V to +3.6V  | $\theta_{JC}$ (Notes 1, 2)                | +12.3°C/W       |
| A_VCTL_1, A_VCTL_2 to GND                                  | -0.3V to +3.6V  | $\theta_{JA}$ (Notes 2, 3)                | +38°C/W         |
| DAT, CS, CLK, AA_SP to GND                                 | -0.3V to +3.6V  | Continuous Power Dissipation (Note 1)     | 5.3W            |
| AMP_IN_1, AMP_IN_2 to GND                                  | +0.95V to +1.2V | Operating Case Temperature Range (Note 4) | -40°C to +85°C  |
| AMP_OUT_1, AMP_OUT_2 to GND                                | -0.3V to +5.5V  | Junction Temperature                      | +150°C          |
| A_ATT_IN_1, A_ATT_IN_2, A_ATT_OUT_1,<br>A_ATT_OUT_2 to GND | 0V to +3.6V     | Storage Temperature Range                 | -65°C to +150°C |
| REG_OUT to GND   | -0.3V to +3.6V  | Lead Temperature (soldering, 10s)         | +300°C          |
| RF Input Power (A_ATT_IN_1, A_ATT_IN_2)                    | +20dBm          | Soldering Temperature (reflow)            | +260°C          |

- Note 1:** Based on junction temperature  $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$ . This formula can be used when the temperature of the exposed pad is known while the device is soldered down to a PCB. See the *Applications Information* section for details. The junction temperature must not exceed +150°C.
- Note 2:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).
- Note 3:** Junction temperature  $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$ . This formula can be used when the ambient temperature of the PCB is known. The junction temperature must not exceed +150°C.
- Note 4:**  $T_C$  is the temperature on the exposed pad of the package.  $T_A$  is the ambient temperature of the device and PCB.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## +5V SUPPLY DC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +4.75V$  to +5.25V, AMPSET = 0, PD\_1 = PD\_2 = 0,  $T_C = -40^\circ C$  to +85°C. Typical values are at  $V_{CC} = +5.0V$  and  $T_C = +25^\circ C$ , unless otherwise noted.)

| PARAMETER           | SYMBOL           | CONDITIONS                       | MIN  | TYP | MAX   | UNITS   |
|---------------------|------------------|----------------------------------|------|-----|-------|---------|
| Supply Voltage      | $V_{CC}$         |                                  | 4.75 | 5   | 5.25  | V       |
| Supply Current      | $I_{DC}$         |                                  |      | 143 | 210   | mA      |
| Power-Down Current  | $I_{DCPD}$       | PD_1 = PD_2 = 1, $V_{IH} = 3.3V$ |      | 5.3 | 8     | mA      |
| Input Low Voltage   | $V_{IL}$         |                                  |      |     | 0.5   | V       |
| Input High Voltage  | $V_{IH}$         |                                  | 1.7  |     | 3.465 | V       |
| Input Logic Current | $I_{IH}, I_{IL}$ |                                  | -1   |     | +1    | $\mu A$ |

## +3.3V SUPPLY DC ELECTRICAL CHARACTERISTICS

(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +3.135V$  to +3.465V, AMPSET = 1, PD\_1 = PD\_2 = 0,  $T_C = -40^\circ C$  to +85°C. Typical values are at  $V_{CC} = +3.3V$  and  $T_C = +25^\circ C$ , unless otherwise noted.)

| PARAMETER          | SYMBOL     | CONDITIONS                       | MIN   | TYP  | MAX   | UNITS |
|--------------------|------------|----------------------------------|-------|------|-------|-------|
| Supply Voltage     | $V_{CC}$   |                                  | 3.135 | 3.3  | 3.465 | V     |
| Supply Current     | $I_{DC}$   |                                  |       | 84.7 | 145   | mA    |
| Power-Down Current | $I_{DCPD}$ | PD_1 = PD_2 = 1, $V_{IH} = 3.3V$ |       | 4.5  | 8     | mA    |
| Input Low Voltage  | $V_{IL}$   |                                  |       | 0.5  |       | V     |
| Input High Voltage | $V_{IH}$   |                                  |       | 1.7  |       | V     |

# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2064

## RECOMMENDED AC OPERATING CONDITIONS

| PARAMETER    | SYMBOL   | CONDITIONS | MIN | TYP | MAX  | UNITS |
|--------------|----------|------------|-----|-----|------|-------|
| RF Frequency | $f_{RF}$ | (Note 5)   | 50  |     | 1000 | MHz   |

## +5V SUPPLY AC ELECTRICAL CHARACTERISTICS (each path, unless otherwise noted)

(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +4.75V$  to  $+5.25V$ , attenuators are set for maximum gain, RF ports are driven from  $50\Omega$  sources,  $AMPSET = 0$ ,  $PD\_1 = PD\_2 = 0$ ,  $100MHz \leq f_{RF} \leq 500MHz$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$ . Typical values are at maximum gain setting,  $V_{CC} = +5.0V$ ,  $P_{IN} = -20dBm$ ,  $f_{RF} = 350MHz$ , and  $T_C = +25^\circ C$ , unless otherwise noted.) (Note 6)

| PARAMETER                           | SYMBOL | CONDITIONS   | MIN  | TYP    | MAX  | UNITS          |
|-------------------------------------|--------|--|------|--------|------|----------------|
| Small-Signal Gain                   | G      | $f_{RF} = 50MHz$   |      | 22.4   |      | dB             |
|                                     |        | $f_{RF} = 100MHz$  |      | 22.3   |      |                |
|                                     |        | $f_{RF} = 200MHz$  |      | 22.2   |      |                |
|                                     |        | $f_{RF} = 350MHz, T_C = +25^\circ C$   | 19.5 | 21.9   | 23.5 |                |
|                                     |        | $f_{RF} = 450MHz$  |      | 21.7   |      |                |
|                                     |        | $f_{RF} = 750MHz$  |      | 21.4   |      |                |
|                                     |        | $f_{RF} = 900MHz$  |      | 20.6   |      |                |
| Gain vs. Temperature                |        |  |      | -0.006 |      | dB/ $^\circ C$ |
| Gain Flatness vs. Frequency         |        | From 100MHz to 200MHz  |      | 0.18   |      | dB             |
|                                     |        | Any 100MHz frequency band from 200MHz to 500MHz  |      | 0.19   |      |                |
| Noise Figure                        | NF     | $f_{RF} = 50MHz$   |      | 4.4    |      | dB             |
|                                     |        | $f_{RF} = 100MHz$  |      | 4.4    |      |                |
|                                     |        | $f_{RF} = 200MHz$  |      | 4.4    |      |                |
|                                     |        | $f_{RF} = 350MHz$  |      | 4.6    |      |                |
|                                     |        | $f_{RF} = 450MHz$  |      | 4.7    |      |                |
|                                     |        | $f_{RF} = 750MHz$  |      | 5.3    |      |                |
|                                     |        | $f_{RF} = 900MHz$  |      | 5.7    |      |                |
| Total Attenuation Range             |        | $f_{RF} = 350MHz, T_C = +25^\circ C$   | 30   | 32.9   |      | dB             |
| Output Second-Order Intercept Point | OIP2   | $P_{OUT} = 0dBm/$ tone, $\Delta f = 1MHz, f_1 + f_2$   |      | 53.7   |      | dBm            |
| Path Isolation                      |        | RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to $50\Omega$  |      | 48.7   |      | dB             |
|                                     |        | RF input 2 amplified signal measured at RF output 1 relative to RF output 2, all unused ports terminated to $50\Omega$ |      | 48.6   |      |                |
| Output Third-Order Intercept Point  | OIP3   | $P_{OUT} = 0dBm/$ tone, $\Delta f = 1MHz, f_{RF} = 50MHz$  |      | 46.3   |      | dBm            |
|                                     |        | $P_{OUT} = 0dBm/$ tone, $\Delta f = 1MHz, f_{RF} = 100MHz$   |      | 44.2   |      |                |
|                                     |        | $P_{OUT} = 0dBm/$ tone, $\Delta f = 1MHz, f_{RF} = 200MHz$   |      | 41.1   |      |                |
|                                     |        | $P_{OUT} = 0dBm/$ tone, $\Delta f = 1MHz, f_{RF} = 350MHz$   |      | 37.1   |      |                |
|                                     |        | $P_{OUT} = 0dBm/$ tone, $\Delta f = 1MHz, f_{RF} = 450MHz$   |      | 34.9   |      |                |
|                                     |        | $P_{OUT} = 0dBm/$ tone, $\Delta f = 1MHz, f_{RF} = 750MHz$   |      | 28.2   |      |                |
|                                     |        | $P_{OUT} = 0dBm/$ tone, $\Delta f = 1MHz, f_{RF} = 900MHz$   |      | 24.6   |      |                |

# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

## +5V SUPPLY AC ELECTRICAL CHARACTERISTICS (each path, unless otherwise noted) (continued)

(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +4.75V$  to  $+5.25V$ , attenuators are set for maximum gain, RF ports are driven from  $50\Omega$  sources,  $AMPSET = 0$ ,  $PD\_1 = PD\_2 = 0$ ,  $100MHz \leq f_{RF} \leq 500MHz$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$ . Typical values are at maximum gain setting,  $V_{CC} = +5.0V$ ,  $P_{IN} = -20dBm$ ,  $f_{RF} = 350MHz$ , and  $T_C = +25^\circ C$ , unless otherwise noted.) (Note 6)

| PARAMETER  | SYMBOL     | CONDITIONS   | MIN   | TYP   | MAX  | UNITS      |
|--|------------|--|---|-------|------|------------|
| Output -1dB Compression Point                                | $P_{1dB}$  | $f_{RF} = 350MHz$ , $T_C = +25^\circ C$ (Note 7)   | 17  | 18.7  |      | dBm        |
| Second Harmonic  |            | $P_{OUT} = +3dBm$  |   | -56.7 |      | dBc        |
| Third Harmonic   |            | $P_{OUT} = +3dBm$  |   | -72.4 |      | dBc        |
| Group Delay  |            | Includes EV kit PCB delays   |   | 0.9   |      | ns         |
| Amplifier Power-Down Time                                    |            | $PD\_1$ or $PD\_2$ from 0 to 1, amplifier DC supply current settles to within 0.1mA        |   | 0.5   |      | $\mu s$    |
| Amplifier Power-Up Time                                      |            | $PD\_1$ or $PD\_2$ from 1 to 0, amplifier DC supply current settles to within 1%           |   | 0.5   |      | $\mu s$    |
| Input Return Loss  | $RL_{IN}$  | $50\Omega$ source  |   | 16.8  |      | dB         |
| Output Return Loss   | $RL_{OUT}$ | $50\Omega$ load  |   | 30.7  |      | dB         |
| <b>ANALOG ATTENUATOR (each path, unless otherwise noted)</b> |            |  |   |       |      |            |
| Insertion Loss   | IL         |  |   | 2.2   |      | dB         |
| Input Second-Order Intercept Point                           | IIP2       | $P_{IN1} = 0dBm$ , $P_{IN2} = 0dBm$ (minimum attenuation), $\Delta f = 1MHz$ , $f_1 + f_2$ |   | 61.9  |      | dBm        |
| Input Third-Order Intercept Point                            | IIP3       | $P_{IN1} = 0dBm$ , $P_{IN2} = 0dBm$ (minimum attenuation), $\Delta f = 1MHz$               |   | 37.0  |      | dBm        |
| Attenuation Range  |            |  |   | 32.9  |      | dB         |
| Gain Control Slope   |            | Analog control input   |   | -13.3 |      | dB/V       |
| Maximum Gain Control Slope                                   |            | Over analog control input range  |   | -35.2 |      | dB/V       |
| Insertion Phase Change                                       |            | Over analog control input range  |   | 16.5  |      | Deg/V      |
| Attenuator Response Time                                     |            | RF settled to within $\pm 0.5dB$   | 31dB to 0dB, AA_SP = 0, from A_VCTL_ step         | 500   |      | ns         |
|  |            |  | 31dB to 0dB, AA_SP = 1, from $\overline{CS}$ step | 500   |      |            |
|  |            |  | 0dB to 31dB, AA_SP = 0, from A_VCTL_ step         | 500   |      |            |
|  |            |  | 0dB to 31dB, AA_SP = 1, from $\overline{CS}$ step | 500   |      |            |
| Group Delay vs. Control Voltage                              |            | Over analog control input from 0.25V to 2.75V  |   | -0.26 |      | ns         |
| Analog Control Input Range                                   |            |  | 0.25  |       | 2.75 | V          |
| Analog Control Input Impedance                               |            |  |   | 19.2  |      | k $\Omega$ |
| Input Return Loss  |            | $50\Omega$ source  |   | 16.0  |      | dB         |
| Output Return Loss   |            | $50\Omega$ load  |   | 15.9  |      | dB         |

## Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

### +5V SUPPLY AC ELECTRICAL CHARACTERISTICS (each path, unless otherwise noted) (continued)

(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +4.75V$  to  $+5.25V$ , attenuators are set for maximum gain, RF ports are driven from  $50\Omega$  sources,  $AMPSET = 0$ ,  $PD\_1 = PD\_2 = 0$ ,  $100MHz \leq f_{RF} \leq 500MHz$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$ . Typical values are at maximum gain setting,  $V_{CC} = +5.0V$ ,  $P_{IN} = -20dBm$ ,  $f_{RF} = 350MHz$ , and  $T_C = +25^\circ C$ , unless otherwise noted.) (Note 6)

| PARAMETER                                | SYMBOL | CONDITIONS          | MIN | TYP | MAX  | UNITS |
|--|--------|---------------------|-----|-----|------|-------|
| <b>D/A CONVERTER</b>                     |        |                     |     |     |      |       |
| Number of Bits                           |        |                     |     | 8   |      | Bits  |
| Output Voltage                           |        | DAC code = 00000000 |     |     | 0.35 | V     |
|  |        | DAC code = 11111111 | 2.7 |     |      |       |
| <b>SERIAL PERIPHERAL INTERFACE (SPI)</b> |        |                     |     |     |      |       |
| Maximum Clock Speed                      |        |                     |     | 20  |      | MHz   |
| Data-to-Clock Setup Time                 | tCS    |                     |     | 2   |      | ns    |
| Data-to-Clock Hold Time                  | tCH    |                     |     | 2.5 |      | ns    |
| Clock-to- $\overline{CS}$ Setup Time     | tES    |                     |     | 3   |      | ns    |
| $\overline{CS}$ Positive Pulse Width     | tEW    |                     |     | 7   |      | ns    |
| $\overline{CS}$ Setup Time               | tEWS   |                     |     | 3.5 |      | ns    |
| Clock Pulse Width                        | tCW    |                     |     | 5   |      | ns    |

### +3.3V SUPPLY AC ELECTRICAL CHARACTERISTICS (each path, unless otherwise noted)

(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +3.135V$  to  $+3.465V$ , attenuators are set for maximum gain, RF ports are driven from  $50\Omega$  sources,  $AMPSET = 1$ ,  $PD\_1 = PD\_2 = 0$ ,  $100MHz \leq f_{RF} \leq 500MHz$ ,  $T_C = -40^\circ C$  to  $+85^\circ C$ . Typical values are at maximum gain setting,  $V_{CC} = +3.3V$ ,  $P_{IN} = -20dBm$ ,  $f_{RF} = 350MHz$ , and  $T_C = +25^\circ C$ , unless otherwise noted.) (Note 6)

| PARAMETER                          | SYMBOL | CONDITIONS   | MIN | TYP  | MAX | UNITS |
|------------------------------------|--------|--|-----|------|-----|-------|
| Small-Signal Gain                  | G      |  |     | 21.8 |     | dB    |
| Output Third-Order Intercept Point | OIP3   | $P_{OUT} = 0dBm/$ tone   |     | 29.1 |     | dBm   |
| Noise Figure                       | NF     |  |     | 4.8  |     | dB    |
| Total Attenuation Range            |        |  |     | 32.9 |     | dB    |
| Path Isolation                     |        | RF input 1 amplified power measured at RF output 2 relative to RF output 1, all unused ports terminated to $50\Omega$  |     | 48.1 |     | dB    |
|                                    |        | RF input 2 amplified signal measured at RF output 1 relative to RF output 2, all unused ports terminated to $50\Omega$ |     | 48.2 |     |       |
| Output -1dB Compression Point      | P1dB   | (Note 7)   |     | 13.2 |     | dBm   |

**Note 5:** Operation outside this range is possible, but with degraded performance of some parameters. See the *Typical Operating Characteristics*.

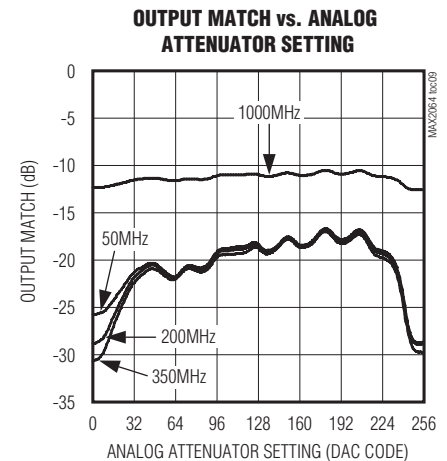
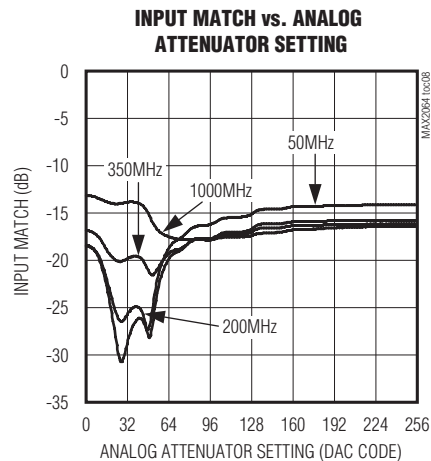
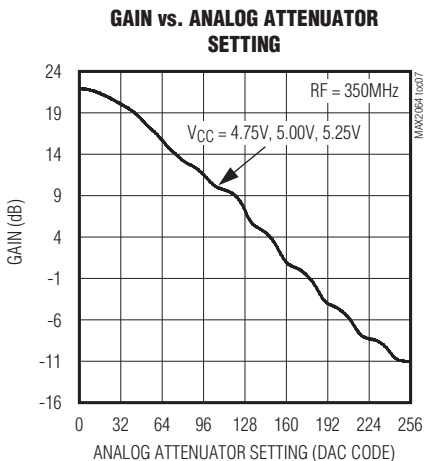
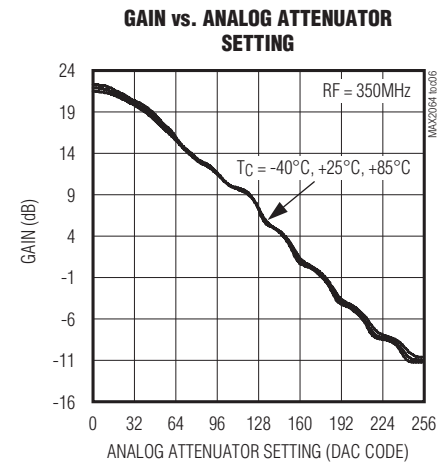
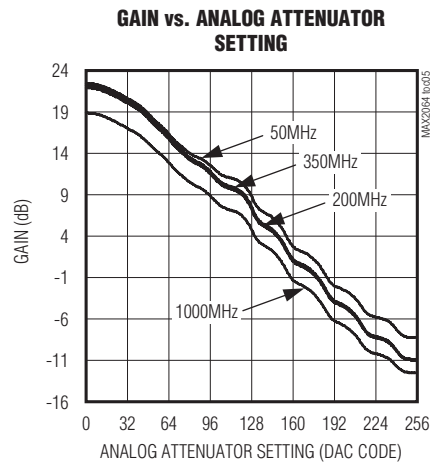
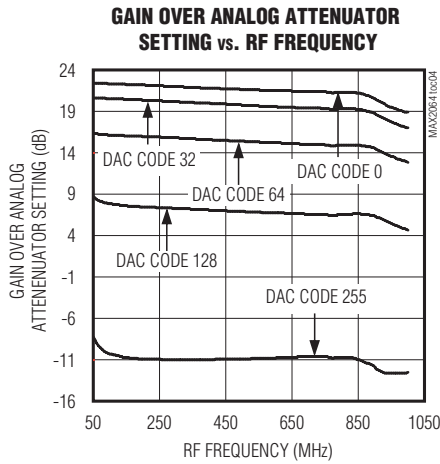
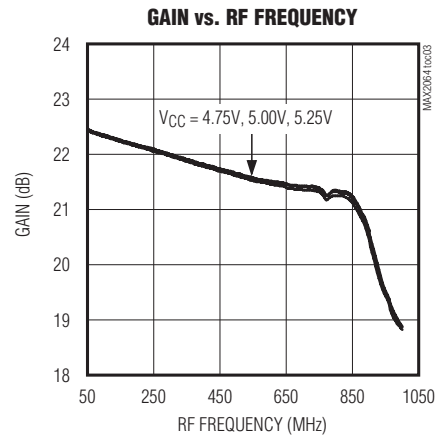
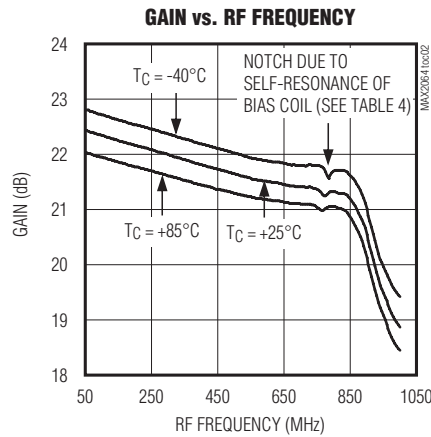
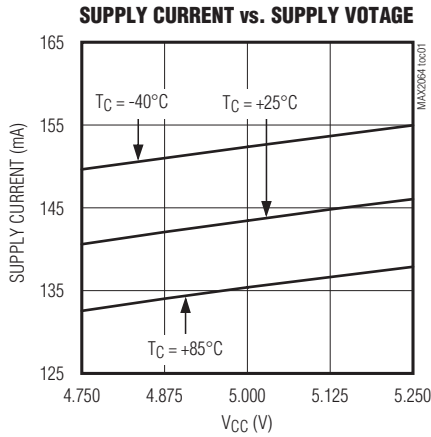
**Note 6:** All limits include external component losses. Output measurements are performed at the RF output port of the *Typical Application Circuit*.

**Note 7:** It is advisable not to continuously operate the RF input 1 or RF input 2 above  $+15dBm$ .

# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

## Typical Operating Characteristics

(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +5V$ , attenuators are set for maximum gain, RF ports are driven from  $50\Omega$  sources,  $AMPSET = 0$ ,  $PD\_1 = PD\_2 = 0$ ,  $P_{IN} = -20dBm$ ,  $f_{RF} = 350MHz$ , and  $T_C = +25^\circ C$ , unless otherwise noted.)

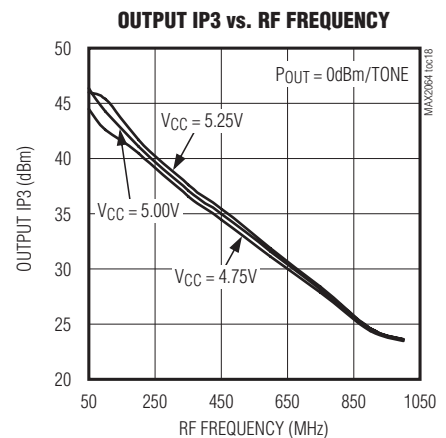
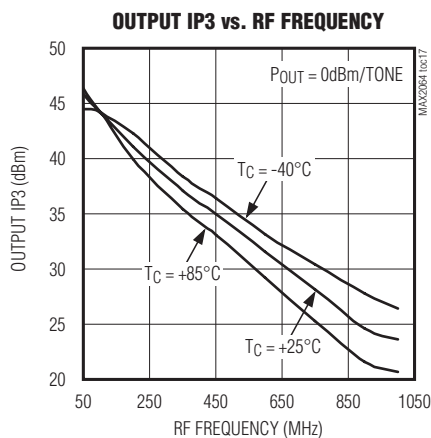
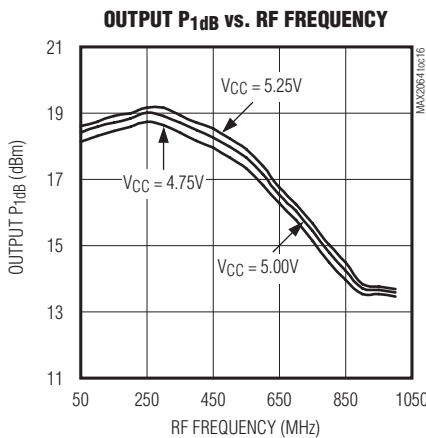
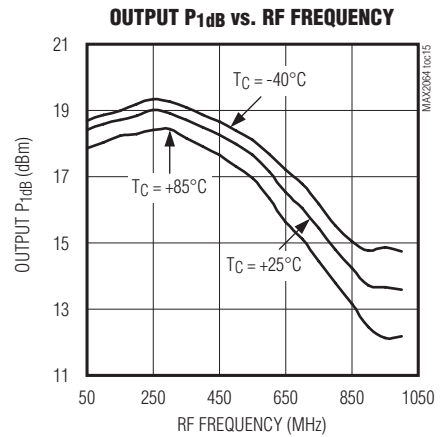
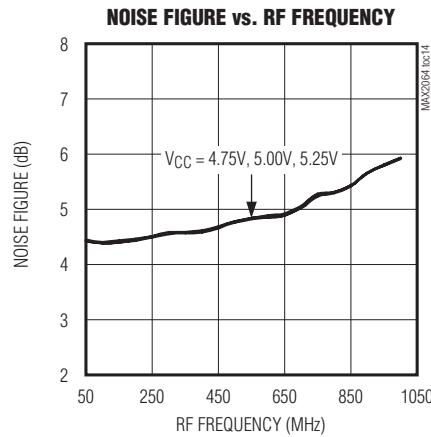
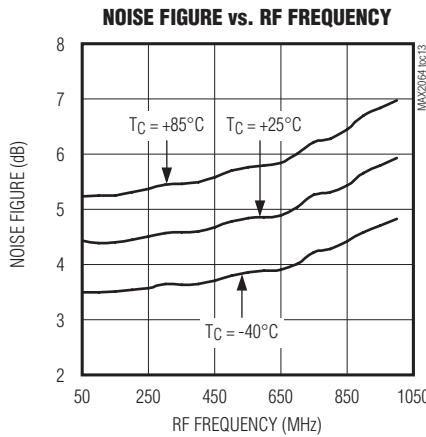
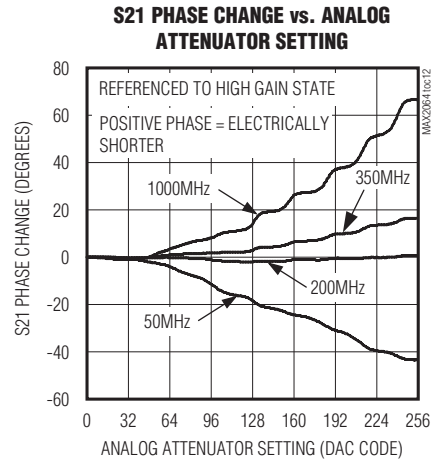
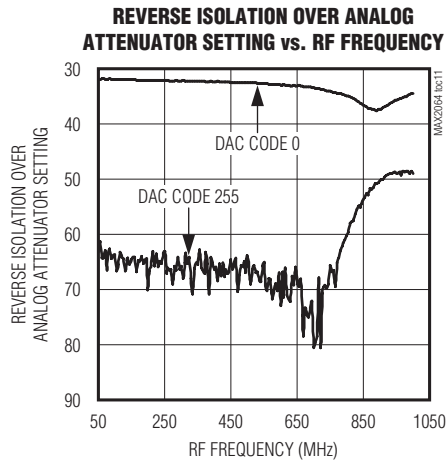
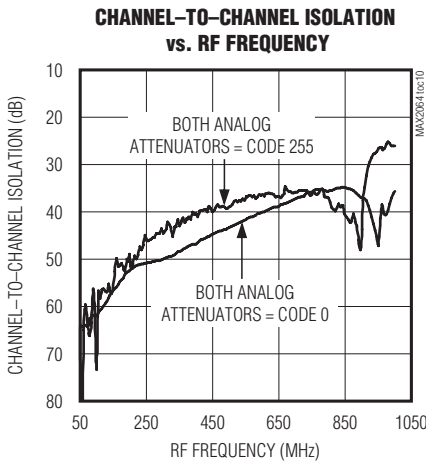


# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

MAX2064

## Typical Operating Characteristics (continued)

(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +5V$ , attenuators are set for maximum gain, RF ports are driven from  $50\Omega$  sources,  $AMPSET = 0$ ,  $PD\_1 = PD\_2 = 0$ ,  $P_{IN} = -20dBm$ ,  $f_{RF} = 350MHz$ , and  $T_C = +25^\circ C$ , unless otherwise noted.)



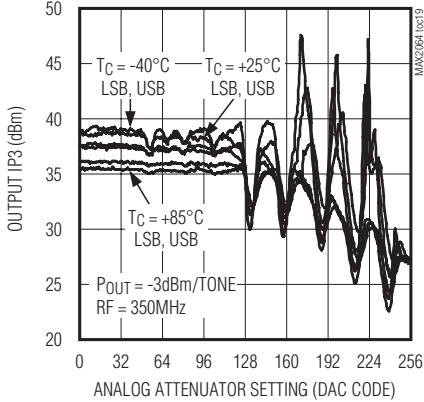


# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

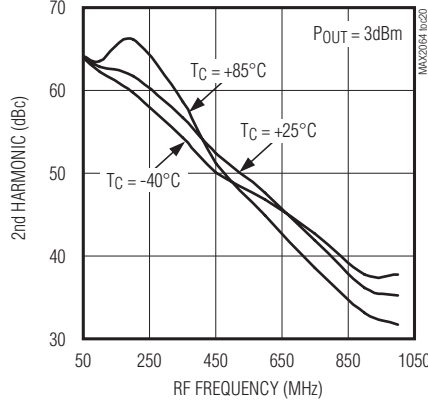
## Typical Operating Characteristics (continued)

(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +5V$ , attenuators are set for maximum gain, RF ports are driven from  $50\Omega$  sources,  $AMPSET = 0$ ,  $PD\_1 = PD\_2 = 0$ ,  $P_{IN} = -20dBm$ ,  $f_{RF} = 350MHz$ , and  $T_C = +25^\circ C$ , unless otherwise noted.)

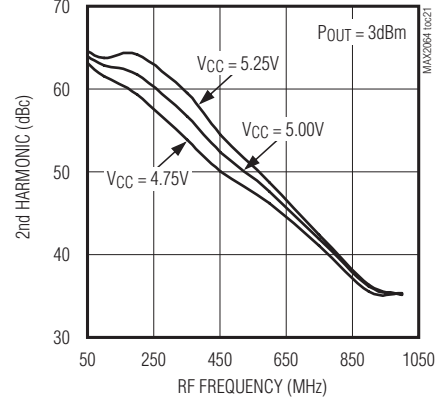
**OUTPUT IP3 vs. ANALOG ATTENUATOR SETTING**



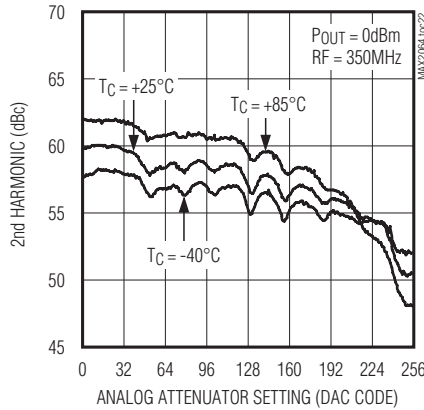
**2nd HARMONIC vs. RF FREQUENCY**



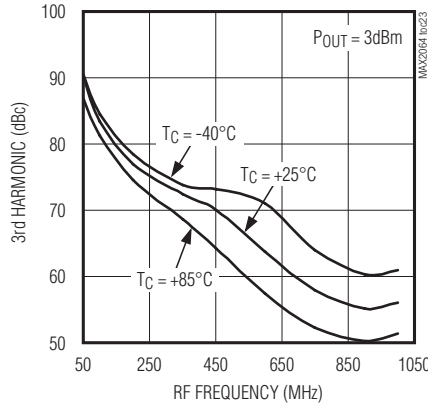
**2nd HARMONIC vs. RF FREQUENCY**



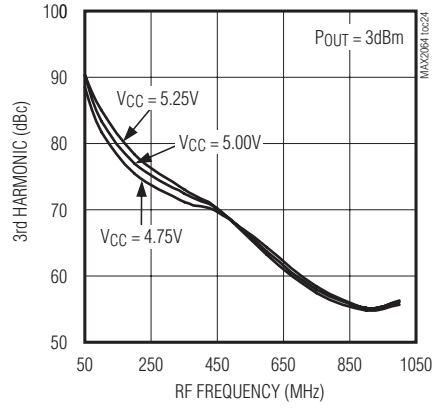
**2nd HARMONIC vs. ANALOG ATTENUATOR SETTING**



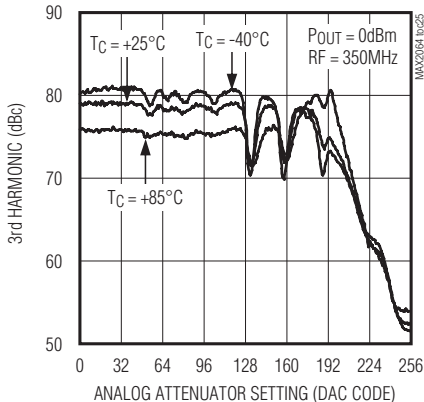
**3rd HARMONIC vs. RF FREQUENCY**



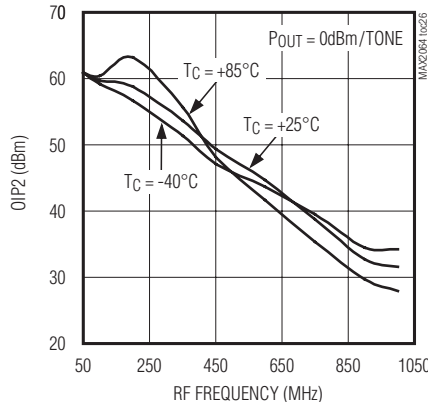
**3rd HARMONIC vs. RF FREQUENCY**



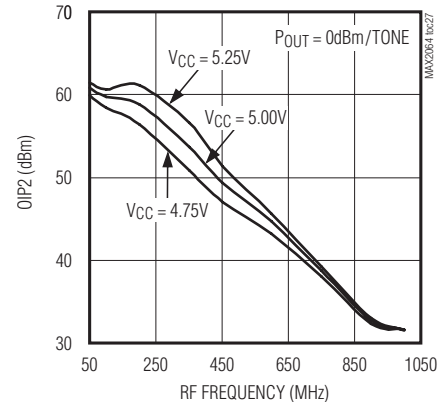
**3rd HARMONIC vs. ANALOG ATTENUATOR SETTING**



**OIP2 vs. RF FREQUENCY**



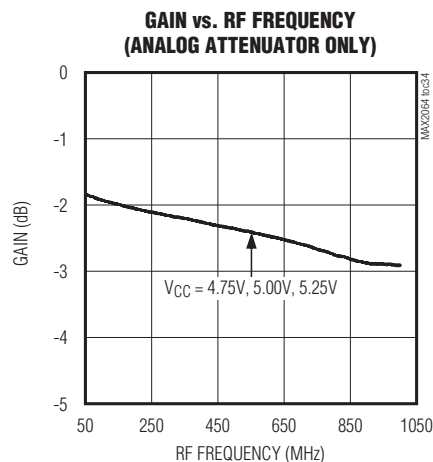
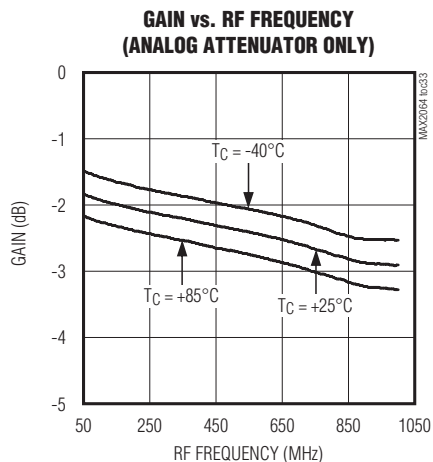
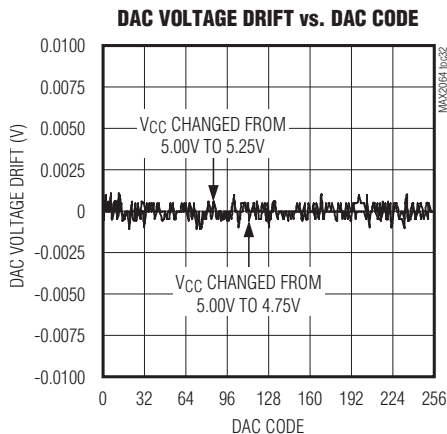
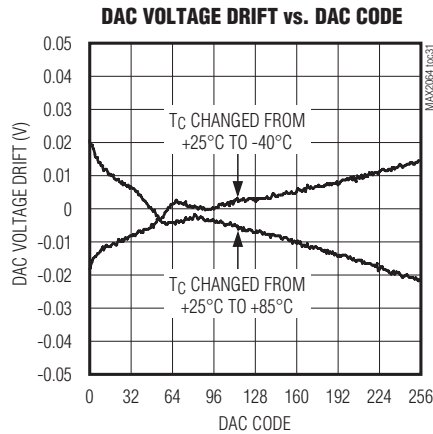
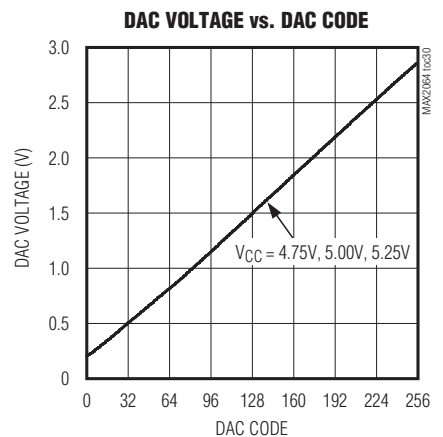
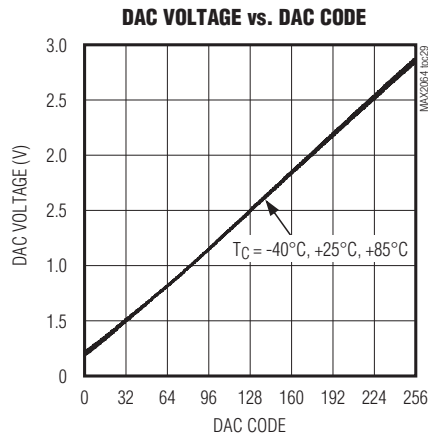
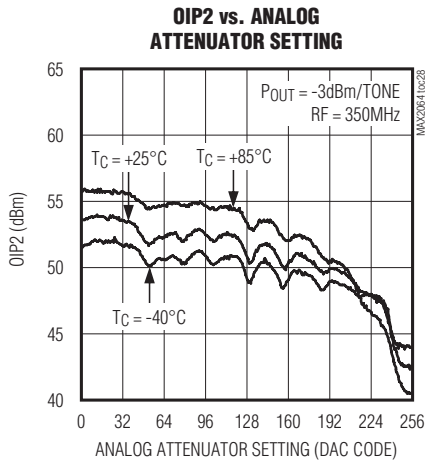
**OIP2 vs. RF FREQUENCY**



# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

## Typical Operating Characteristics (continued)

(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +5V$ , attenuators are set for maximum gain, RF ports are driven from  $50\Omega$  sources,  $AMPSET = 0$ ,  $PD\_1 = PD\_2 = 0$ ,  $P_{IN} = -20dBm$ ,  $f_{RF} = 350MHz$ , and  $T_C = +25^\circ C$ , unless otherwise noted.)

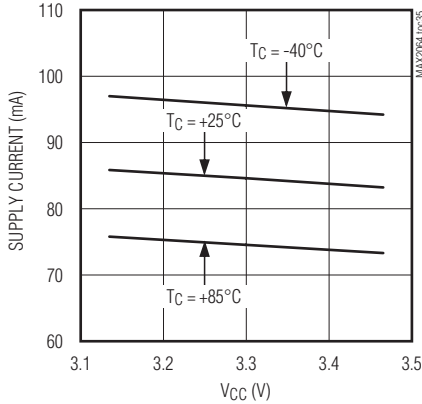


# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

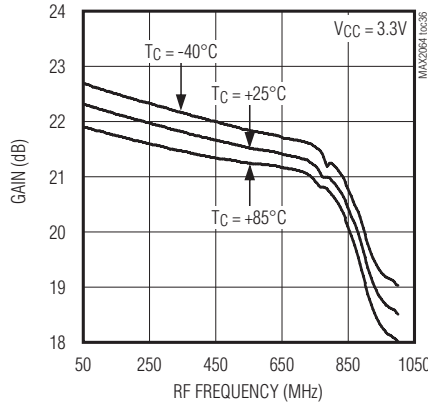
## Typical Operating Characteristics (continued)

(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +3.3V$ , attenuators are set for maximum gain, RF ports are driven from 50Ω sources, AMPSET = 1, PD\_1 = PD\_2 = 0, P<sub>IN</sub> = -20dBm, f<sub>RF</sub> = 350MHz, and T<sub>C</sub> = +25°C, unless otherwise noted.)

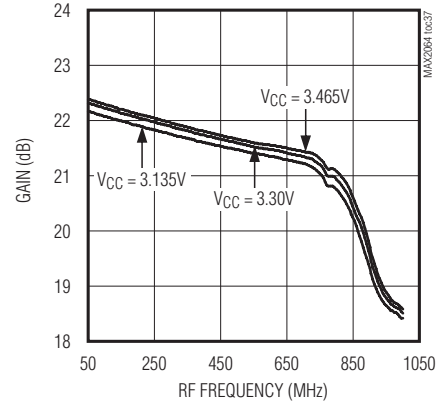
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



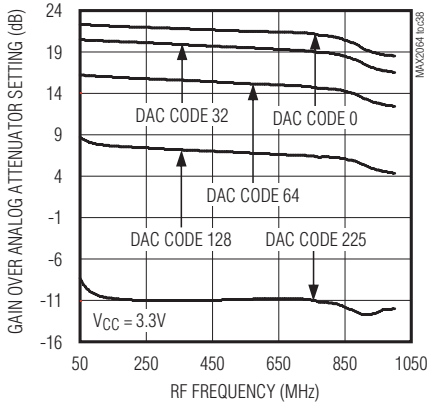
**GAIN vs. RF FREQUENCY**



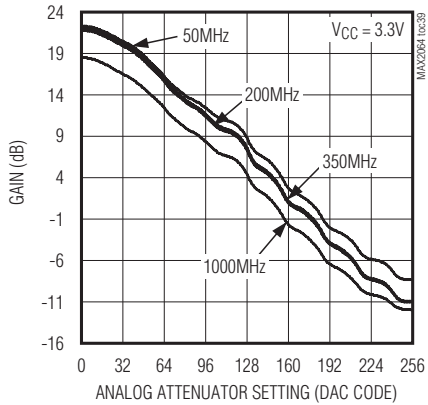
**GAIN vs. RF FREQUENCY**



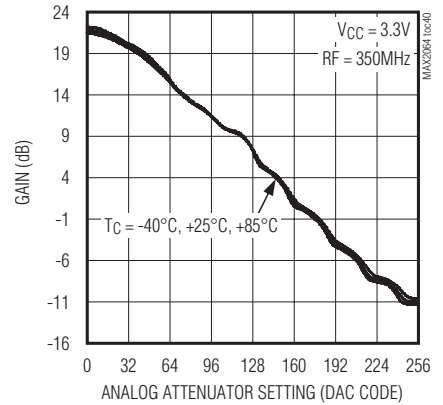
**GAIN OVER ANALOG ATTENUATOR SETTING vs. RF FREQUENCY**



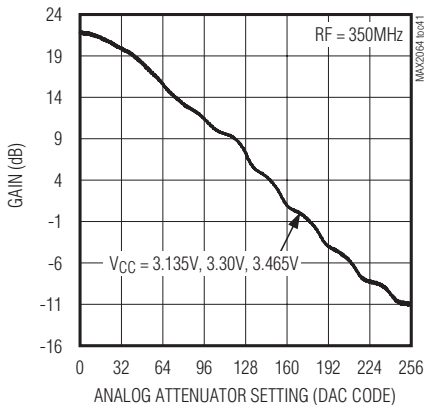
**GAIN vs. ANALOG ATTENUATOR SETTING**



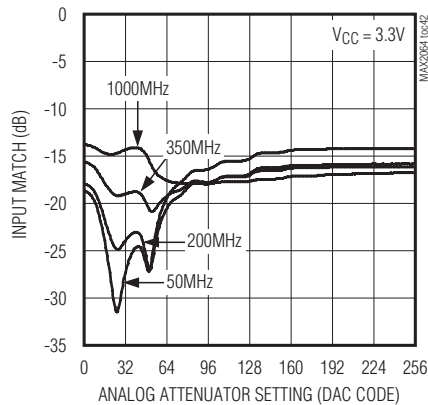
**GAIN vs. ANALOG ATTENUATOR SETTING**



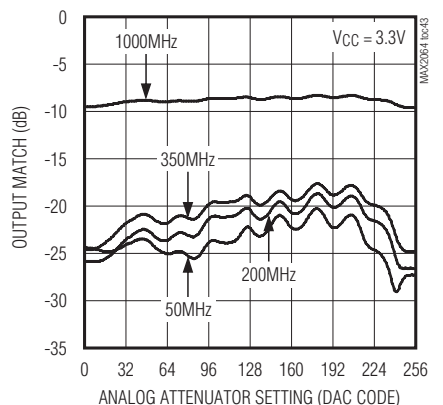
**GAIN vs. ANALOG ATTENUATOR SETTING**



**INPUT MATCH vs. ANALOG ATTENUATOR SETTING**



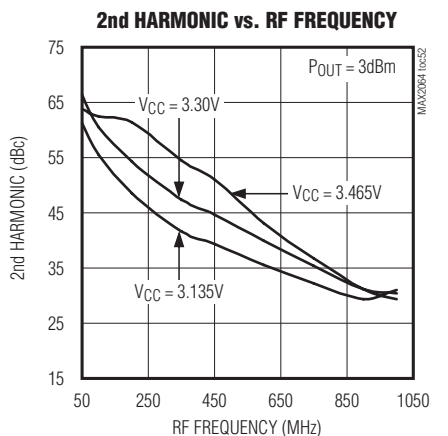
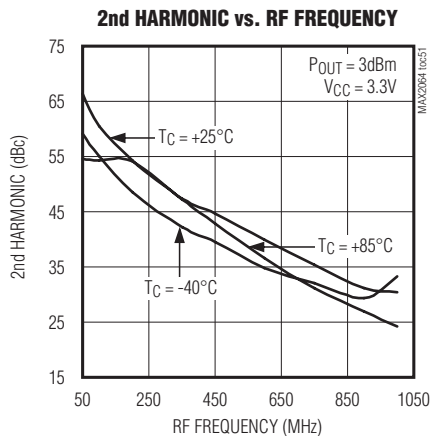
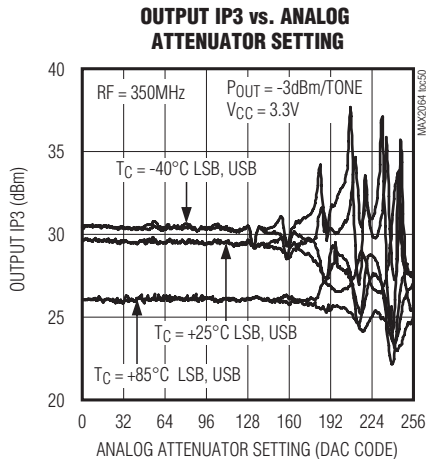
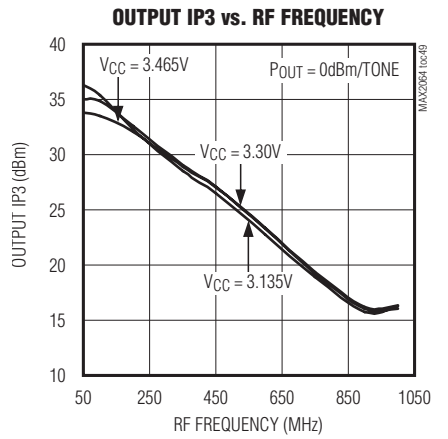
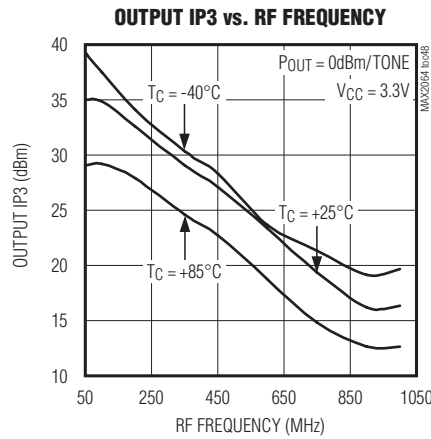
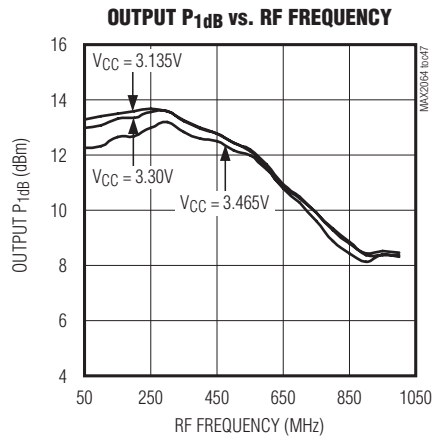
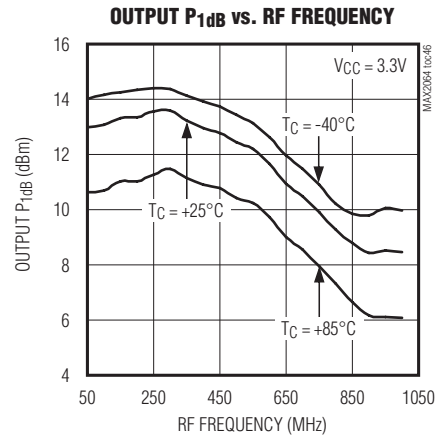
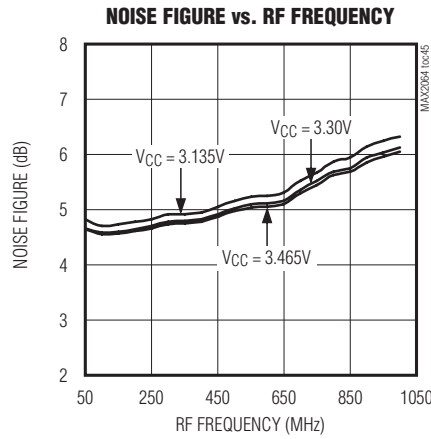
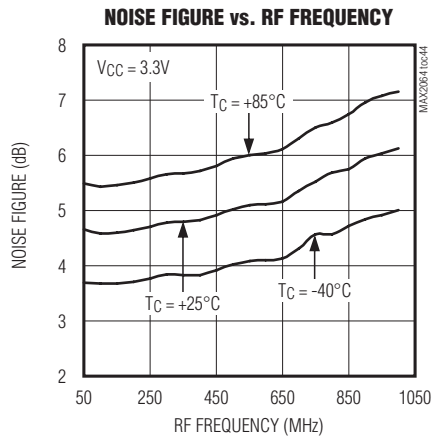
**OUTPUT MATCH vs. ANALOG ATTENUATOR SETTING**



# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

## Typical Operating Characteristics (continued)

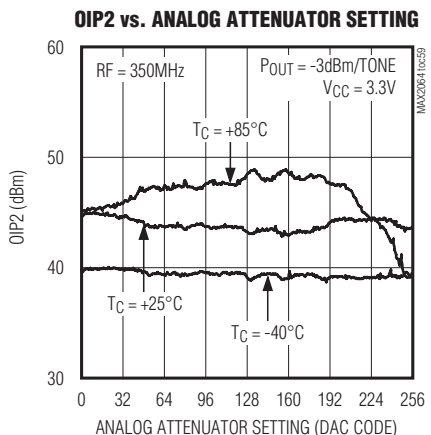
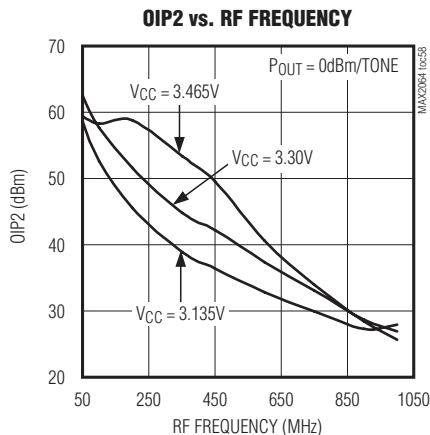
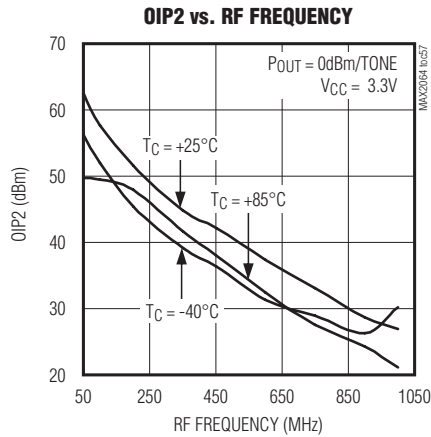
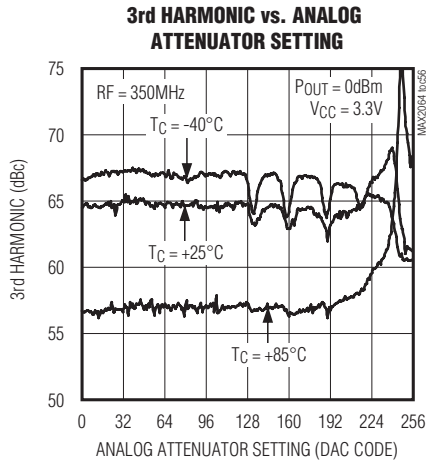
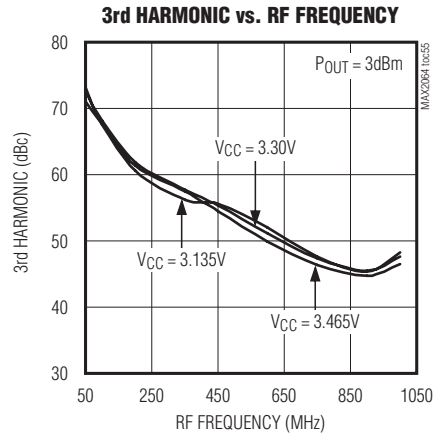
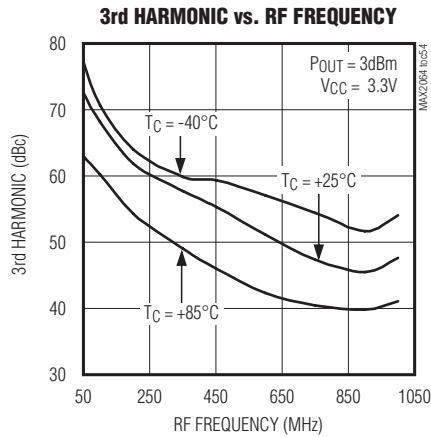
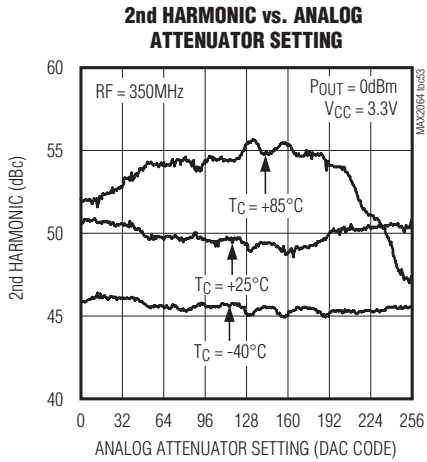
(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +3.3V$ , attenuators are set for maximum gain, RF ports are driven from  $50\Omega$  sources, AMPSET = 1, PD\_1 = PD\_2 = 0, P<sub>IN</sub> = -20dBm, f<sub>RF</sub> = 350MHz, and T<sub>C</sub> = +25°C, unless otherwise noted.)



# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

## Typical Operating Characteristics (continued)

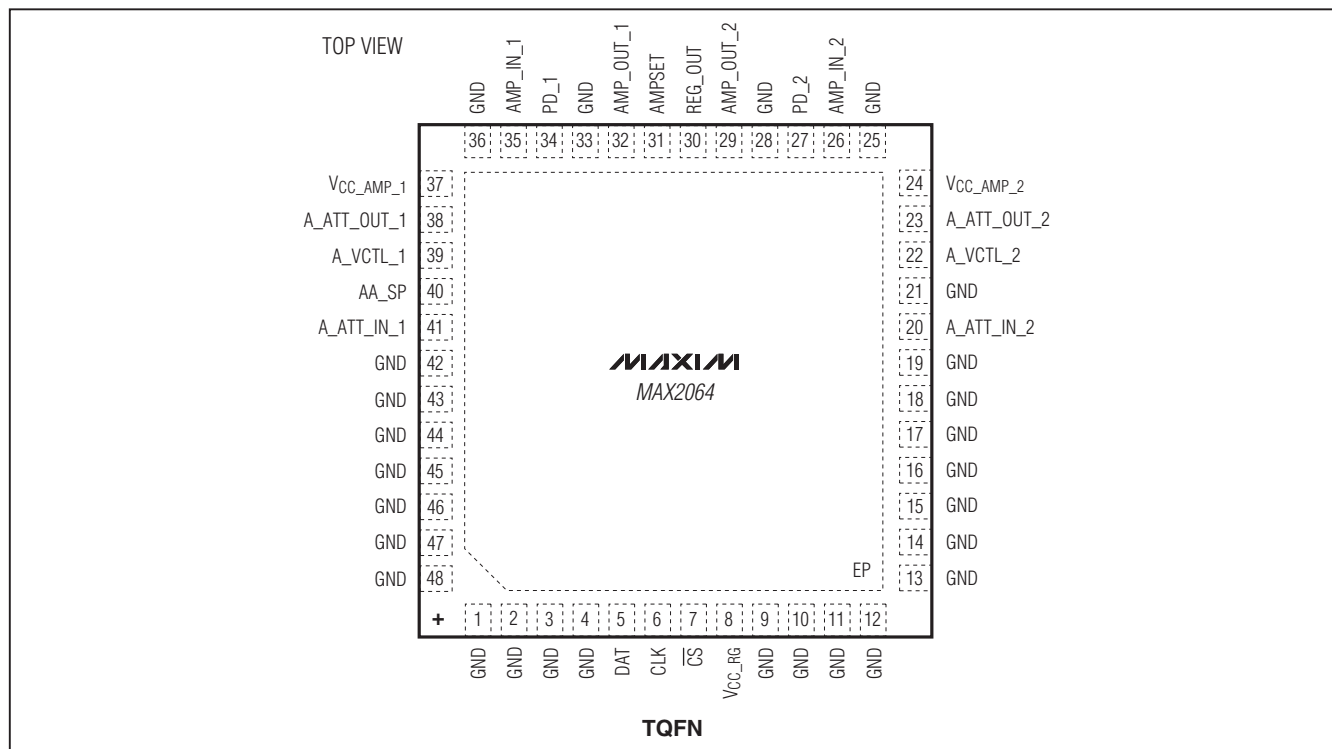
(Typical Application Circuit,  $V_{CC} = V_{CC\_AMP\_1} = V_{CC\_AMP\_2} = V_{CC\_RG} = +3.3V$ , attenuators are set for maximum gain, RF ports are driven from  $50\Omega$  sources,  $AMPSET = 1$ ,  $PD\_1 = PD\_2 = 0$ ,  $PIN = -20dBm$ ,  $f_{RF} = 350MHz$ , and  $T_C = +25^\circ C$ , unless otherwise noted.)



# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

## Pin Configuration

**MAX2064**



## Pin Description

| PIN                                  | NAME                   | FUNCTION  |
|--------------------------------------|------------------------|---|
| 1–4, 9–19, 21, 25, 28, 33, 36, 42–48 | GND                    | Ground  |
| 5                                    | DAT                    | SPI Data Digital Input  |
| 6                                    | CLK                    | SPI Clock Digital Input   |
| 7                                    | $\overline{\text{CS}}$ | SPI Chip-Select Digital Input   |
| 8                                    | VCC_RG                 | Regulator Supply Input. Connect to a 3.3V or 5V external power supply. VCC_RG powers all circuits except for the driver amplifiers. Bypass with a 10nF capacitor as close as possible to the pin. |
| 20                                   | A_ATT_IN_2             | Analog Attenuator Input (50Ω), Path 2. Requires a 1000pF DC-blocking capacitor.   |
| 22                                   | A_VCTL_2               | Analog Attenuator Voltage-Control Input, Path 2. Bypass to ground with a 150pF capacitor if DAC 2 is used (AA_SP = 1).  |
| 23                                   | A_ATT_OUT_2            | Analog Attenuator Output (50Ω), Path 2. Requires a DC-blocking capacitor. Connect to AMP_IN_2 through a 1000pF capacitor.   |
| 24                                   | VCC_AMP_2              | Driver Amplifier Supply-Voltage Input, Path 2. Bypass with a 10nF capacitor as close as possible to the pin.  |
| 26                                   | AMP_IN_2               | Driver Amplifier Input (50Ω), Path 2. Requires a DC-blocking capacitor. Connect to A_ATT_OUT_2 through a 1000pF capacitor.  |
| 27                                   | PD_2                   | Power-Down, Path 2. See Table 2 for operation details.  |
| 29                                   | AMP_OUT_2              | Driver Amplifier Output (50Ω), Path 2. Connect a pullup inductor from AMP_OUT_2 to VCC_.  |

# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

## Pin Description (continued)

| PIN | NAME        | FUNCTION  |
|-----|-------------|---|
| 30  | REG_OUT     | Regulator Output. Bypass with 1 $\mu$ F capacitor.  |
| 31  | AMPSET      | Driver Amplifier Bias Setting for 3.3V Operation. Set to logic 1 for 3.3V operation on pins VCC_AMP_1 and VCC_AMP_2. Set to logic 0 for 5V operation.   |
| 32  | AMP_OUT_1   | Driver Amplifier Output (50 $\Omega$ ), Path 1. Connect a pullup inductor from AMP_OUT_1 to VCC_.   |
| 34  | PD_1        | Power-Down, Path 1. See Table 2 for operation details.  |
| 35  | AMP_IN_1    | Driver Amplifier Input (50 $\Omega$ ), Path 1. Requires a DC-blocking capacitor. Connect to A_ATT_OUT_1 through a 1000pF capacitor.   |
| 37  | VCC_AMP_1   | Driver Amplifier Supply Voltage Input, Path 1. Bypass with a 10nF capacitor as close as possible to the pin.  |
| 38  | A_ATT_OUT_1 | Analog Attenuator Output (50 $\Omega$ ), Path 1. Requires a DC-blocking capacitor. Connect to AMP_IN_1 through a 1000pF capacitor.  |
| 39  | A_VCTL_1    | Analog Attenuator Voltage-Control Input, Path 1. Bypass to ground with a 150pF capacitor if on-chip DAC is used (AA_SP = 1).  |
| 40  | AA_SP       | DAC Enable/Disable Logic Input for Analog Attenuators. Set AA_SP to logic 1 to enable on-chip DAC circuit and digital SPI control. Set AA_SP to logic 0 to disable DAC circuit and digital SPI control. When AA_SP = 0, use analog control lines (A_VCTL_1 and A_VCTL_2). |
| 41  | A_ATT_IN_1  | Analog Attenuator Input (50 $\Omega$ ), Path 1. Requires a 1000pF DC-blocking capacitor.  |
| —   | EP          | Exposed Pad. Internally connected to GND. Connect to a large PCB ground plane for proper RF performance and enhanced thermal dissipation.   |

### Detailed Description

The MAX2064 high-linearity analog VGA is a general-purpose, high-performance amplifier designed to interface with 50 $\Omega$  systems operating in the 50MHz to 1000MHz frequency range.

Each channel of the device integrates an analog attenuator to provide 33dB of total gain control, as well as a driver amplifier optimized to provide high gain, high IP3, low NF, and low power consumption.

Each analog attenuator is controlled using an external voltage or through the SPI-compatible interface using an on-chip 8-bit DAC. See the *Applications Information* section and Table 3 for attenuator programming details.

Because each of the two stages in the separate signal paths has its own RF input and RF output, this component can be configured to either optimize NF (amplifier configured first) or OIP3 (amplifier last). The device's performance features include 24dB amplifier gain (amplifier only), 4.4dB NF at maximum gain (includes attenuator insertion losses), and a high OIP3 level of +41dBm. Each of these features makes the device an ideal VGA for multipath receiver and transmitter applications.

In addition, the device operates from a single +5V supply with full performance, or a +3.3V supply for an enhanced power-savings mode with lower performance. The device is available in a compact 48-pin TQFN package (7mm x 7mm) with an exposed pad. Electrical performance is guaranteed over the extended temperature range, from TC = -40°C to +85°C.

### Analog Attenuator Control

The device integrates two analog attenuators. Each analog attenuator has a 33dB range and is controlled using an external voltage, or through the 3-wire SPI interface using an on-chip 8-bit DAC. See the *Applications Information* section and Table 3 for attenuator programming details. The attenuators can be used for both static and dynamic power control.

Note that when the analog attenuators are controlled by the DACs through the SPI bus, the DAC output voltage shows on A\_VCTL\_1 and A\_VCTL\_2 (pins 39 and 22, respectively). Therefore, in SPI mode, the A\_VCTL\_1 and A\_VCTL\_2 pins must only connect to the resistor and capacitor to ground, as shown in the *Typical Application Circuit*.

# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

**Table 1. Control Logic**

| AA_SP | ANALOG ATTENUATOR                      | D/A CONVERTER   |
|-------|--|---|
| 0     | Controlled by external control voltage | Disabled  |
| 1     | Controlled by on-chip DAC              | Enabled (DAC output voltage shows on A_VCTL__ pins); DAC uses on-chip voltage reference |

**Table 2. Operating Modes**

| RESULT              | V <sub>CC</sub> (V) | AMP_SET | PD_1 | PD_2 |
|---------------------|---------------------|---------|------|------|
| All on              | 5                   | 0       | 0    | 0    |
|                     | 3.3                 | 1       | 0    | 0    |
| AMP1 off<br>AMP2 on | 5                   | 0       | 1    | 0    |
|                     | 3.3                 | 1       | 1    | 0    |
| AMP1 on<br>AMP2 off | 5                   | 0       | 0    | 1    |
|                     | 3.3                 | 1       | 0    | 1    |
| All off             | 5                   | 0       | 1    | 1    |
|                     | 3.3                 | 1       | 1    | 1    |

### Driver Amplifier

Each path of the device includes a high-performance driver with a fixed gain of 24dB. The driver amplifier circuits are optimized for high linearity for the 50MHz to 1000MHz frequency range.

### Applications Information

#### Operating Modes

The device features an optional +3.3V supply voltage operation with reduced linearity performance. The AMPSET pin needs to be biased accordingly in each mode, as listed in Table 2. In addition, the driver amplifiers can be shut down independently to conserve DC power. See the biasing scheme outlined in Table 2 for details.

#### SPI Interface and Attenuator Settings

The attenuators can be programmed through the 3-wire SPI/MICROWIRE™-compatible serial interface using 5-bit words. Fifty-six bits of data are shifted in MSB first and are framed by  $\overline{CS}$ . The first 28 bits set the first attenuator and the following 28 bits set the second attenuator. When  $\overline{CS}$  is low, the clock is active and data is shifted on the rising edge of the clock. When  $\overline{CS}$  transitions high, the data is latched and the attenuator setting changes (Figure 1). See Table 3 for details on the SPI data format.

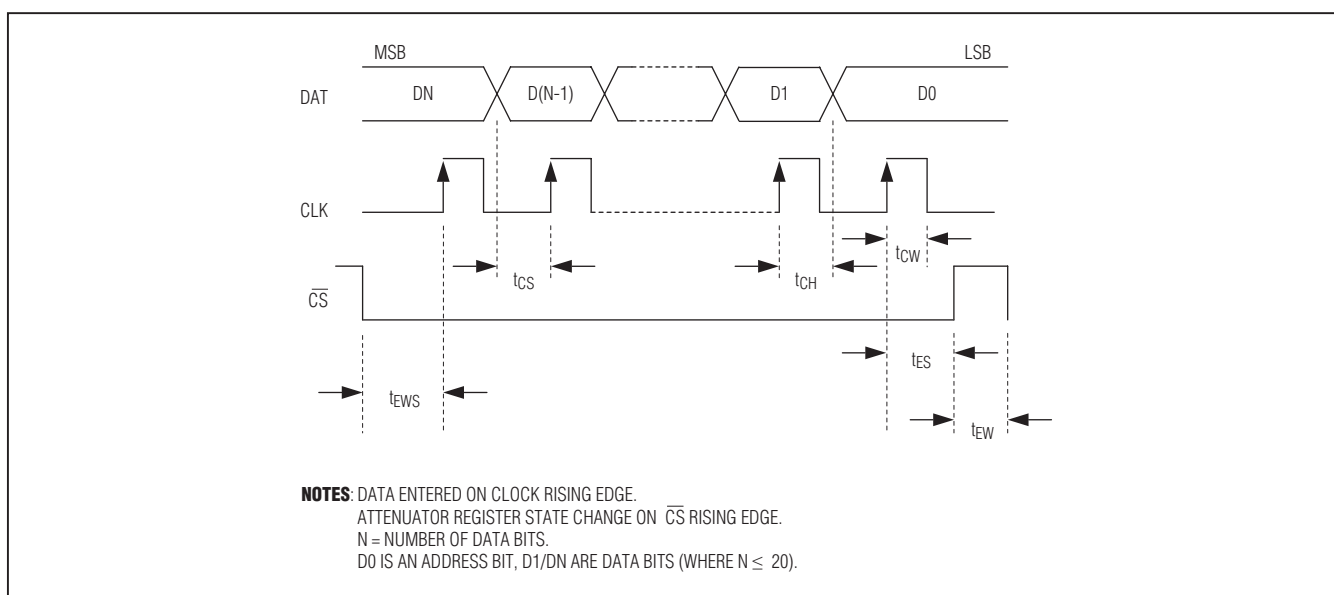


Figure 1. SPI Timing Diagram

MICROWIRE is a trademark of National Semiconductor Corp.



## Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

Table 3. SPI Data Format

| FUNCTION                | BIT       | DESCRIPTION   |
|-------------------------|-----------|---|
| Reserved                | D55 (MSB) | Bits D[55:36] are reserved. Set to logic 0.                             |
|                         | D54       |   |
|                         | D53       |   |
|                         | D52       |   |
|                         | D51       |   |
|                         | D50       |   |
|                         | D49       |   |
|                         | D48       |   |
|                         | D47       |   |
|                         | D46       |   |
|                         | D45       |   |
|                         | D44       |   |
|                         | D43       |   |
|                         | D42       |   |
|                         | D41       |   |
|                         | D40       |   |
|                         | D39       |   |
| D38                     |           |   |
| D37                     |           |   |
| D36                     |           |   |
| On-Chip DAC<br>(Path 2) | D35       | Bit 7 (MSB) of on-chip DAC used to program the Path 2 analog attenuator |
|                         | D34       | Bit 6 of DAC  |
|                         | D33       | Bit 5 of DAC  |
|                         | D32       | Bit 4 of DAC  |
|                         | D31       | Bit 3 of DAC  |
|                         | D30       | Bit 2 of DAC  |
|                         | D29       | Bit 1 of DAC  |
|                         | D28       | Bit 0 (LSB) of DAC  |

# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

**MAX2064**

**Table 3. SPI Data Format (continued)**

| FUNCTION                | BIT      | DESCRIPTION   |
|-------------------------|----------|---|
| Reserved                | D27      | Bits D[27:8] are reserved. Set to logic 0.                              |
|                         | D26      |   |
|                         | D25      |   |
|                         | D24      |   |
|                         | D23      |   |
|                         | D22      |   |
|                         | D21      |   |
|                         | D20      |   |
|                         | D19      |   |
|                         | D18      |   |
|                         | D17      |   |
|                         | D16      |   |
|                         | D15      |   |
|                         | D14      |   |
|                         | D13      |   |
| On-Chip DAC<br>(Path 1) | D7       | Bit 7 (MSB) of on-chip DAC used to program the Path 1 analog attenuator |
|                         | D6       | Bit 6 of DAC  |
|                         | D5       | Bit 5 of DAC  |
|                         | D4       | Bit 4 of DAC  |
|                         | D3       | Bit 3 of DAC  |
|                         | D2       | Bit 2 of DAC  |
|                         | D1       | Bit 1 of DAC  |
|                         | D0 (LSB) | Bit 0 (LSB) of DAC  |

# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

## Power-Supply Sequencing

The sequence to be used is:

- 1) Power supply
- 2) Control lines

## Layout Considerations

The pin configuration of the device is optimized to facilitate a very compact physical layout of the device and its associated discrete components. The exposed pad (EP) of the device's 48-pin TQFN-EP package provides a low thermal-resistance path to the die. It is important that

the PCB on which the device is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low inductance path to electrical ground. The EP **MUST** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes. The layout of the PCB should include proper top-layer ground shielding to isolate the amplifier's inputs and outputs from each other. Shielding between the paths (inputs and outputs) is important for channel-to-channel isolation.

**Table 4. Typical Application Circuit Component Values**

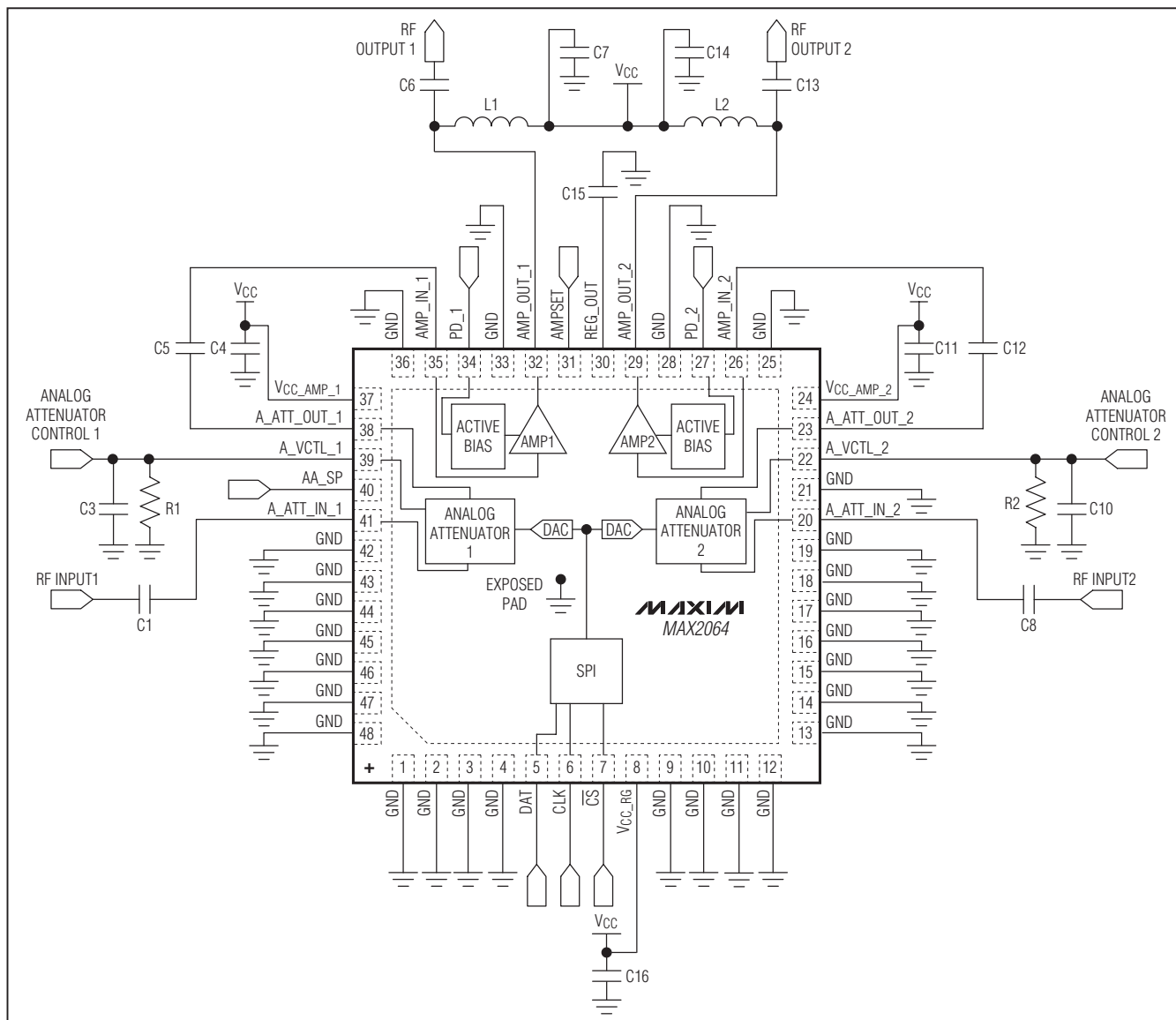
| DESIGNATION              | QTY | DESCRIPTION  | COMPONENT SUPPLIER                     |
|--------------------------|-----|--|--|
| C1, C5, C6, C8, C12, C13 | 6   | 1000pF ceramic capacitors (0402)<br>GRM1555C1H102J | Murata Electronics North America, Inc. |
| C3, C10                  | 2   | 150pF ceramic capacitors (0402)<br>GRM1555C1H151J  | Murata Electronics North America, Inc. |
| C4, C7, C11, C14, C16    | 5   | 10nF ceramic capacitors (0402)<br>GRM155R71E103K   | Murata Electronics North America, Inc. |
| C15                      | 1   | 1μF ceramic capacitor (0603)<br>GRM188R71C105K     | Murata Electronics North America, Inc. |
| L1, L2*                  | 2   | 820nH inductors (1008)<br>Coilcraft 1008CS-821XJLC | Coilcraft, Inc.                        |
| R1, R2                   | 2   | 47.5kΩ resistors (0402)                            | —                                      |
| U1                       | 1   | 48 TQFN-EP (7mm x 7mm)<br>Maxim MAX2064ETM+        | Maxim Integrated Products, Inc.        |

\*Select the inductors to ensure that self-resonance of the inductors is outside the band of operation.

# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

## Typical Application Circuit

MAX2064



### Chip Information

PROCESS: SiGe BiCMOS

### Package Information

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO.             | LAND PATTERN NO.        |
|--------------|--------------|-------------------------|-------------------------|
| 48 TQFN-EP   | T4877+7      | <a href="#">21-0144</a> | <a href="#">90-0133</a> |

# Dual 50MHz to 1000MHz High-Linearity, Serial/Analog-Controlled VGA

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION     | PAGES CHANGED |
|-----------------|---------------|-----------------|---------------|
| 0               | 12/10         | Initial release | —             |

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

20 \_\_\_\_\_ **Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600**