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19-4696; Rev 1; 9/09

Octal-Channel Ultrasound Front-End

General Description

The MAX2077 octal-channel ultrasound front-end is a fully integrated, bipolar, high-density, octal-channel ultrasound receiver optimized for low-cost, high-channel count, high-performance portable and cart-based ultrasound systems. The easy-to-use IC allows the user to achieve high-end 2D and PW imaging capability using substantially less space and power. The highly compact imaging receiver lineup, including a low-noise amplifier (LNA), variable-gain amplifier (VGA), and anti-alias filter (AAF), achieves an ultra-low 2.4dB noise figure at $R_S = R_{IN} = 200\Omega$ at a very low 64.8mW per-channel power dissipation. The full imaging receiver channel has been optimized for second-harmonic imaging with -64dBFS second-harmonic distortion performance with a $1V_{P-P}$ 5MHz output signal and broadband SNR of > 68dB* at 20dB gain. The bipolar front-end has also been optimized for excellent low-velocity PW and color-flow Doppler sensitivity with an exceptional near-carrier SNR of 140dBc/Hz at 1kHz offset from a 5MHz $1V_{P-P}$ output clutter signal.

The MAX2077 octal-channel ultrasound front-end is available in a small 8mm x 8mm, 56-pin thin QFN or 10mm x 10mm, 68-pin thin QFN package with an exposed pad and is specified over a 0°C to +70°C temperature range. To add CW Doppler capability, replace the MAX2077 with the MAX2078.

Applications

Medical Ultrasound Imaging

Sonar

Pin Configurations and Typical Application Circuits appear at end of data sheet.

Features

- ♦ **8 Full Channels of LNA, VGA, and AAF in a Small, 8mm x 8mm, 56-Pin or 10mm x 10mm, 68-Pin TQFN Package**
- ♦ **Ultra-Low Full-Channel Noise Figure of 2.4dB at $R_{IN} = R_S = 200\Omega$**
- ♦ **Low Output-Referred Noise of $23nV/\sqrt{Hz}$ at 5MHz, 20dB Gain, Yielding a Broadband SNR of 68dB* for Excellent Second-Harmonic Imaging**
- ♦ **High Near-Carrier SNR of 140dBc/Hz at 1kHz Offset from a 5MHz, $1V_{P-P}$ Output Signal, and 20dB of Gain for Excellent Low-Velocity PW and Color-Flow Doppler Sensitivity in a High-Clutter Environment**
- ♦ **Ultra-Low Power 64.8mW per Full-Channel (LNA, VGA, and AAF) Normal Imaging Mode**
- ♦ **Selectable Active Input-Impedance Matching of 50Ω, 100Ω, 200Ω, and 1kΩ**
- ♦ **Wide Input-Voltage Range of $330mV_{P-P}$ in High LNA Gain Mode and $550mV_{P-P}$ in Low LNA Gain Mode**
- ♦ **Integrated Selectable 3-Pole 9MHz, 10MHz, 15MHz, and 18MHz Butterworth AAF**
- ♦ **Fast-Recovery, Low-Power Modes (< 2µs)**
- ♦ **Pin Compatible with the MAX2078 Ultrasound Front-End with CW Doppler (MAX2077 68-Pin Package Variant)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2077CTN+	0°C to +70°C	56 Thin QFN-EP**
MAX2077CTK+	0°C to +70°C	68 Thin QFN-EP**

+Denotes a lead(Pb)-free/RoHS-compliant package.
***EP = Exposed pad.*

**When coupled with the MAX1437B ADC.*

Octal-Channel Ultrasound Front-End

ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to GND ....-0.3V to +5.5V
V_{CC2} - V_{CC1} ....> -0.3V
ZF_, IN_, AG to GND ....-0.3V to ($V_{CC\_}$ + 0.3V)
INC_ ....20mA DC
V_{REF} to GND...-0.3V to +3V
IN_ to AG ....-0.6V to +0.6V
OUT_, DIN, DOUT, VG_, NP, $\overline{CS}$, CLK,
PD to GND ....-0.3V to (V_{CC1} + 0.3V)
$V_{CC\_}$, V_{REF} analog and digital control signals must be applied in this order
Input Differential Voltage ....2.0V_{P-P} differential

Continuous Power Dissipation (T_A = +70°C)
56-Pin TQFN (derate 47.6mW/°C above +70°C) 3.8W
68-Pin TQFN (derate 40.0mW/°C above +70°C) 4.0W
Operating Temperature Range (Note 1)................0°C to +70°C
Junction Temperature ....+150°C
θ_{JC} (Notes 2, 3) (56-Pin TQFN)..1°C/W
θ_{JC} (Notes 2, 3) (68-Pin TQFN)......................................0.3°C/W
θ_{JA} (Notes 3, 4) (56-Pin TQFN).......................................21°C/W
θ_{JA} (Notes 3, 4) (68-Pin TQFN).......................................20°C/W
Storage Temperature Range ....-40°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: T_C is the temperature on the exposed pad of the package. T_A is the ambient temperature of the device and PCB.
Note 2: Junction temperature $T_J = T_C + (\theta_{JC} \times V_{CC} \times I_{CC})$. This formula can only be used if the component is soldered down to a printed circuit board pad containing multiple ground vias to remove the heat. The junction temperature must not exceed 150°C.
Note 3: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.
Note 4: Junction temperature $T_J = T_A + (\theta_{JA} \times V_{CC} \times I_{CC})$, assuming there is no heat removal from the exposed pad. The junction temperature must not exceed 150°C.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, no RF signals applied. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
3.3V Supply Voltage	V_{CC1}		3.13	3.3	3.47	V
4.75V/5V Supply Voltage	V_{CC2}		4.5	4.75	5.25	V
External Reference Voltage Range	V_{REF}	(Note 6)	2.475		2.525	V
CMOS Input High Voltage	V_{IH}	Applies to CMOS control inputs	2.5			V
CMOS Input Low Voltage	V_{IL}	Applies to CMOS control inputs			0.8	V
CMOS Input Leakage Current	I_{IN}	0V to 3.3V			10	µA
Data Output High Voltage	DOUT_HI	10MΩ load		V_{CC1}		V
Data Output Low Voltage	DOUT_LO	10MΩ load		0		V
4.75V/5V Supply Standby Current	I_NP_5V_TOT	NP = 1, all channels		3.9	6	mA
3V Supply Standby Current	I_NP_3V_TOT	NP = 1, all channels		1.7	3	mA
4.75V/5V Power-Down Current	I_PD_5V_TOT	PD = 1, all channels (Note 7)		0.4	10	µA
3V Power-Down Current	I_PD_3V_TOT	PD = 1, all channels (Note 7)		0.3	10	µA
3V Supply Current per Channel	I_3V_NM	Total I divided by 8, VG+ - VG- = -2V		11	18	mA
4.75V/5V Supply Current per Channel	I_5V_NM	Total I divided by 8		6.0	8.3	mA
DC Power per Channel	P_NM			64.8	105	mW
Differential Analog Control Voltage Range	VGAIN_RANG	VG+ - VG-		±3		V

DC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, no RF signals applied. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Common-Mode Voltage for Difference Analog Control	VGAIN_COMM	(VG+ + VG-)/2		1.65 ±5%		V
Source/Sink Current for Gain Control Pins	I_ACONTROL	Per pin		±1.6	±4	µA
Reference Current	I_{REF}	All channels		9.7	13	µA
Output Common-Mode Level	V_{CMO}			1.73		V

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Impedance	D1/D0 = 0/0, R_{IN} = 50Ω, f_{RF} = 2MHz	47.5	50	60	Ω
	D1/D0 = 0/1, R_{IN} = 100Ω, f_{RF} = 2MHz	90	100	115	
	D1/D0 = 1/0, R_{IN} = 200Ω, f_{RF} = 2MHz	185	200	220	
	D1/D0 = 1/1, R_{IN} = 1000Ω, f_{RF} = 2MHz	600	830	1000	
Noise Figure	R_S = R_{IN} = 50Ω, LNA gain = 18.5dB, VG+ - VG- = +3V		4.5		dB
	R_S = R_{IN} =100Ω, LNA gain = 18.5dB, VG+ - VG- = +3V		3.4		
	R_S = R_{IN} = 200Ω, LNA gain = 18.5dB, VG+ - VG- = +3V		2.4		
	R_S = R_{IN} = 1000Ω, LNA gain = 18.5dB, VG+ - VG- = +3V		2.2		
Low-Gain Noise Figure	D3/D2/D1/D0 = 0/0/0/1, LNA gain = 12.5dB, R_S = R_{IN} = 200Ω, VG+ - VG- = +3V		3.9		dB
Input-Referred Noise Voltage	D3/D2/D1/D0 = 1/1/1/0		0.9		nV/√Hz
Input-Referred Noise Current	D3/D2/D1/D0 = 1/1/1/0		2.1		pA/√Hz
Maximum Gain, High Gain Setting	VG+ - VG- = +3V	41	42.4	45	dB
Minimum Gain, High Gain Setting	VG+ - VG- = -3V	9	10.1	12	dB
Maximum Gain, Low Gain Setting	D3/D2/D1/D0 = 0/0/0/1, R_{IN} = 200Ω, LNA gain = 12.5dB, VG+ - VG- = +3V	35	37.6	39	dB
Minimum Gain, Low Gain Setting	D3/D2/D1/D0 = 0/0/0/1, R_{IN} = 200Ω, LNA gain = 12.5dB, VG+ - VG- = -3V	3	5.4	8	dB
Anti-Aliasing Filter 3dB Corner Frequency	D5/D4 = 0/0, f_C = 9MHz		9		MHz
	D5/D4 = 0/1, f_C = 10MHz		10		
	D5/D4 = 1/0, f_C = 15MHz		15		
	D5/D4 = 1/1, f_C = 18MHz		18		
Gain Range	VG+ - VG- = -3V to +3V		33		dB

Octal-Channel Ultrasound Front-End

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Absolute Gain Error	VG+ - VG- = -2V		±0.4		dB
	VG+ - VG- = 0V		±0.4		
	VG+ - VG- = +2V		±0.4		
Input Gain Compression	VG+ - VG- = -3V (VGA minimum gain), gain ratio with 330mV$_{P-P}$/50mV$_{P-P}$ input tones		1.4		dB
	LNA low gain = 12.5dB, VG+ - VG- = -3V (VGA minimum gain), gain ratio with 600mV$_{P-P}$/50mV$_{P-P}$		0.8		
VGA Gain Response Time	Gain step up (V_{IN} = 5mV$_{P-P}$, gain changed from 10dB to 44dB, settling time is measured within 1dB final value)		1.4		µs
	Gain step down (V_{IN} = 5mV$_{P-P}$, gain changed from 44dB to 10dB, settling time is measured within 1dB final value)		1.6		
VGA Output Offset Under Pulsed Overload	Overdrive is ±10mA in clamping diodes, gain at 30dB, 16 pulses at 5MHz, repetition rate 20kHz; offset is measured at output when RF duty cycle is off		180		mV
Small-Signal Output Noise	20dB of gain, VG+ - VG- = -0.85V, no input signal		23		nV/√Hz
Large-Signal Output Noise	20dB of gain, VG+ - VG- = -0.85V, f_{RF} = 5MHz, f_{NOISE} = f_{RF} + 1kHz, V_{OUT} = 1V$_{P-P}$ differential		35		nV/√Hz
Second Harmonic (HD2)	V_{IN} = 50mV$_{P-P}$, f_{RF} = 2MHz, V_{OUT} = 1V$_{P-P}$		-67		dBc
	V_{IN} = 50mV$_{P-P}$, f_{RF} = 5MHz, V_{OUT} = 1V$_{P-P}$		-64.2		
High-Gain IM3 Distortion	D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), V_{IN} = 50mV$_{P-P}$, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, V_{OUT} = 1V$_{P-P}$ (Note 8)	-52	-61		dBc
Low-Gain IM3 Distortion	D3/D2/D1/D0 = 0/0/0/1 (R_{IN} = 200Ω, LNA gain = 12.5dB), V_{IN} = 100mV$_{P-P}$, f_{RF1} = 5MHz, f_{RF2} = 5.01MHz, V_{OUT} = 1V$_{P-P}$ (Note 8)	-50	-60		dBc
Standby Mode Power-Up Response Time	Gain set for 26dB, f_{RF} = 5MHz, V_{OUT} = 1V$_{P-P}$, settled within 1dB from transition on NP pin		2.1		µs
Standby Mode Power-Down Response Time	To reach DC current target ±10%		2.0		µs
Power-Up Response Time	Gain set for 28dB, f_{RF} = 5MHz, V_{OUT} = 1V$_{P-P}$, settled within 1dB from transition on PD		2.7		ms
Power-Down Response Time	Gain set for 28dB, f_{RF} = 5MHz, DC power reaches 6mW/channel, from transition on PD		5		ns
Adjacent Channel Crosstalk	V_{OUT} = 1V$_{P-P}$ differential, f_{RF} = 10MHz, 28dB of gain		-58		dBc
Nonadjacent Channel Crosstalk	V_{OUT} = 1V$_{P-P}$ differential, f_{RF} = 10MHz, 28dB of gain		-71		dBc
Phase Matching Between Channels	Gain = 28dB, VG+ - VG- = 0.4V, V_{OUT} = 1V$_{P-P}$, f_{RF} = 10MHz		±1.2		Degrees

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.13V to 3.47V, V_{CC2} = 4.5V to 5.25V, T_A = 0°C to +70°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/$\sqrt{Hz}$ from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF. Typical values are at V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, unless otherwise noted.) (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3V Supply Modulation Ratio	Gain = 28dB, VG+ - VG- = 0.4V, V_{OUT} = $1V_{P-P}$, f_{RF} = 5MHz, f_{MOD} = 1kHz, V_{MOD} = $50mV_{P-P}$, ratio of output sideband at 5.001MHz, $1V_{P-P}$		-73		dBc
4.75V/5V Supply Modulation Ratio	Gain = 28dB, VG+ - VG- = 0.4V, V_{OUT} = $1V_{P-P}$, f_{RF} = 5MHz, f_{MOD} = 1kHz, V_{MOD} = $50mV_{P-P}$, ratio of output sideband at 5.001MHz, $1V_{P-P}$		-82		dBc
Gain Control Lines Common-Mode Rejection Ratio	Gain = 28dB, VG+ - VG- = 0.4V, V_{OUT} = $1V_{P-P}$, f_{RF} = 5MHz, $f_{MOD(CM)}$ = 1kHz, $V_{MOD(CM)}$ = $50mV_{P-P}$, ratio of output sideband at 5.001MHz to $1V_{P-P}$		-74		dBc
Overdrive Phase Delay	VG+ - VG- = -3V, delay between V_{IN} = $300mV_{P-P}$ and V_{IN} = $30mV_{P-P}$ differential		5		ns
Output Impedance	Differential		100		Ω

AC ELECTRICAL CHARACTERISTICS—SERIAL PERIPHERAL INTERFACE

(DOUT loaded with 60pF and 10MΩ, 2ns rise and fall edges on CLK.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Speed					10	MHz
Mininimum Data-to-Clock Setup Time	t_{CS}			5		ns
Mininimum Data-to-Clock Hold Time	t_{CH}			0		ns
Mininimum Clock-to-$\overline{CS}$ Setup Time	t_{ES}			5		ns
$\overline{CS}$ Positive Mininimum Pulse Width	t_{EW}			1		ns
Mininimum Clock Pulse Width	t_{CW}			2		ns

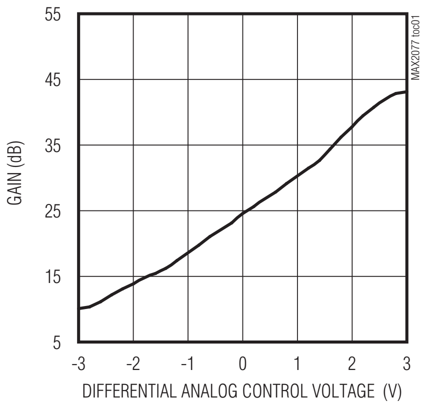
Note 5: Minimum and maximum limits at T_A = +25°C and +70°C are guaranteed by design, characterization, and/or production test.
Note 6: Noise performance of the device is dependent on the noise contribution from V_{REF}. Use a low-noise supply for V_{REF}. The reference input noise is given for 8 channels, knowing that the reference-noise contributions are correlated in all 8 channels. If more channels are used, the reference noise must be reduced to get the best noise performance.
Note 7: Not applicable to the MAX2077CTK+.
Note 8: See the *Ultrasound-Specific IMD3 Specification* section.

Octal-Channel Ultrasound Front-End

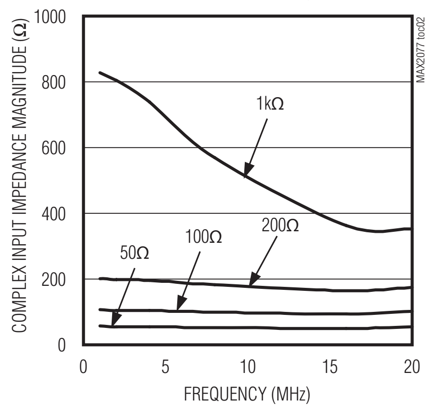
Typical Operating Characteristics

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/$\sqrt{Hz}$ from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF, unless otherwise noted. All typical operating curves have been taken with the MAX2077CTN+ package variant.)

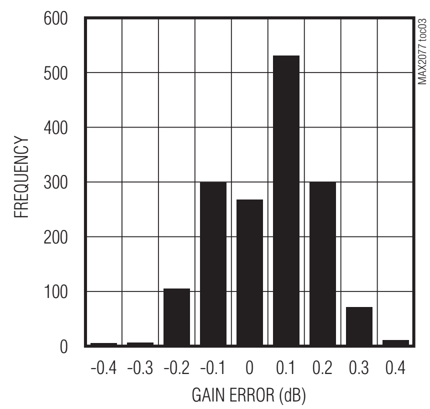
GAIN vs. DIFFERENTIAL ANALOG CONTROL VOLTAGE



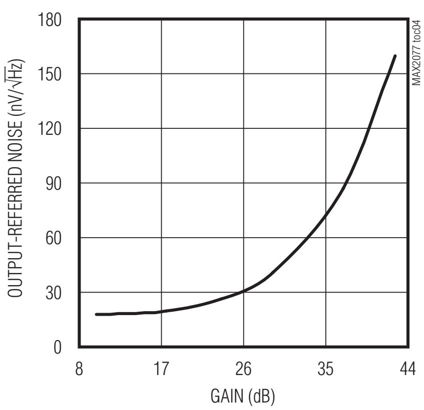
COMPLEX INPUT IMPEDANCE MAGNITUDE vs. FREQUENCY



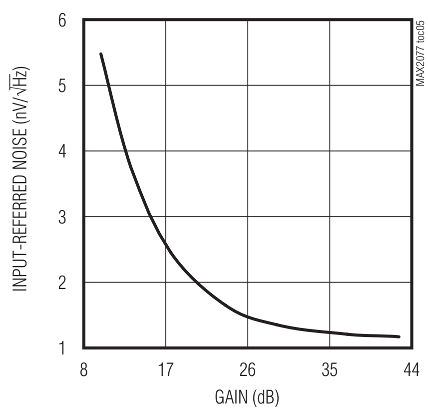
GAIN ERROR HISTOGRAM



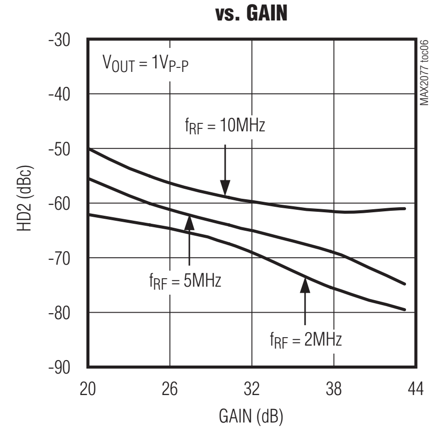
OUTPUT-REFERRED NOISE vs. GAIN



INPUT-REFERRED NOISE vs. GAIN



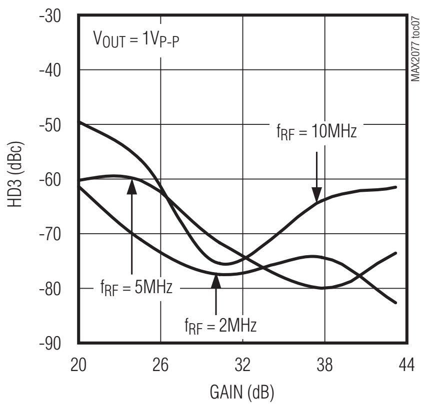
SECOND-HARMONIC DISTORTION vs. GAIN



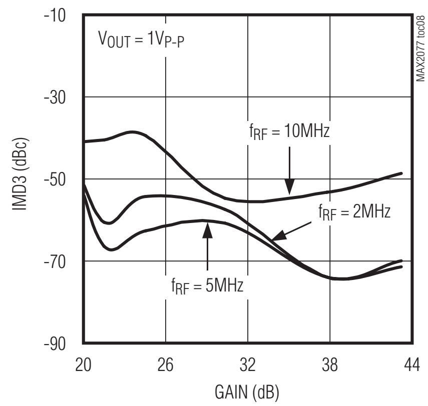
Typical Operating Characteristics (continued)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/$\sqrt{Hz}$ from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF, unless otherwise noted. All typical operating curves have been taken with the MAX2077CTN+ package variant.)

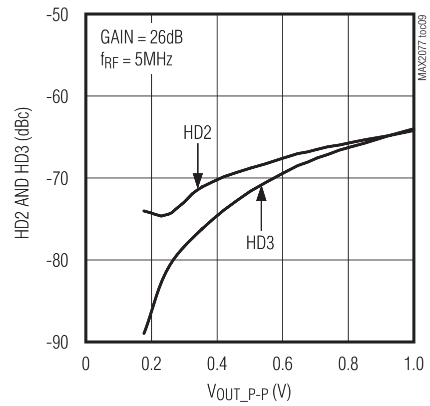
THIRD-HARMONIC DISTORTION vs. GAIN



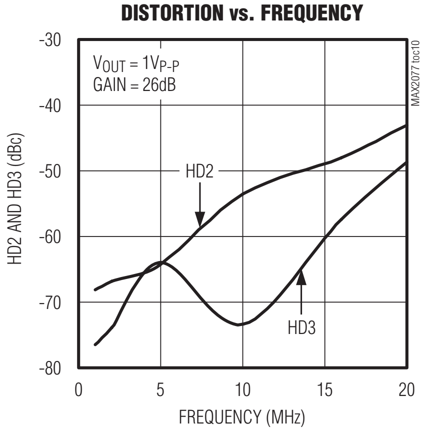
TWO-TONE ULTRASOUND-SPECIFIC IMD3 vs. GAIN



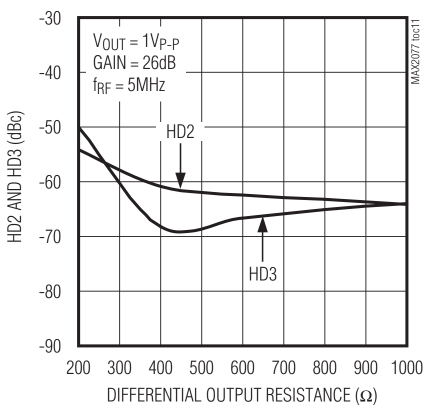
SECOND- AND THIRD-HARMONIC DISTORTION vs. V_{OUT_P-P}



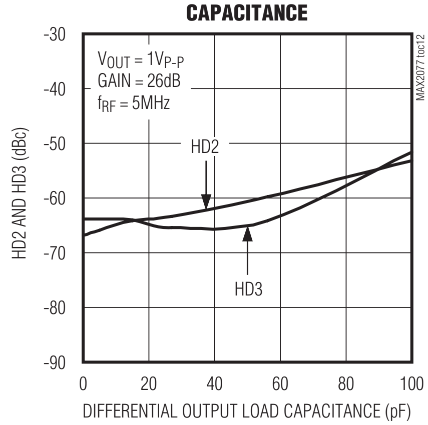
SECOND- AND THIRD-HARMONIC DISTORTION vs. FREQUENCY



SECOND- AND THIRD-HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT RESISTANCE



SECOND- AND THIRD-HARMONIC DISTORTION vs. DIFFERENTIAL OUTPUT LOAD CAPACITANCE

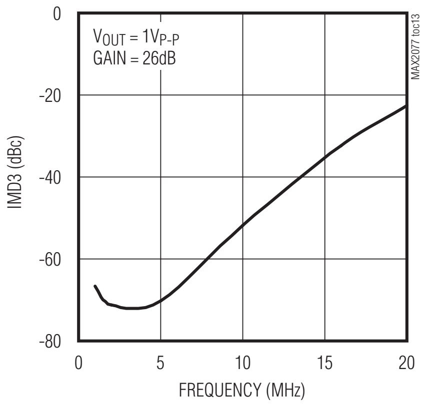


Octal-Channel Ultrasound Front-End

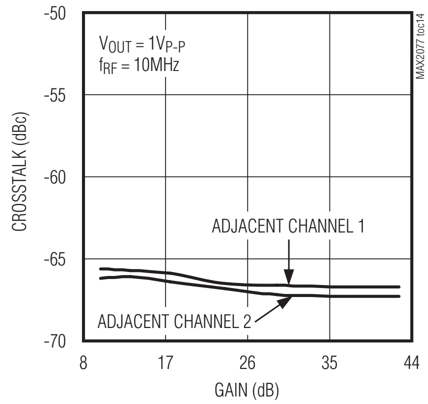
Typical Operating Characteristics (continued)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/$\sqrt{Hz}$ from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF, unless otherwise noted. All typical operating curves have been taken with the MAX2077CTN+ package variant.)

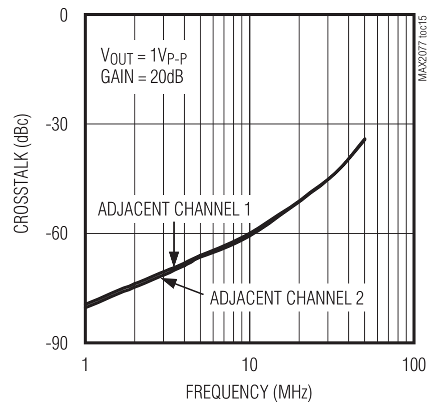
TWO-TONE ULTRASOUND-SPECIFIC IMD3 vs. FREQUENCY



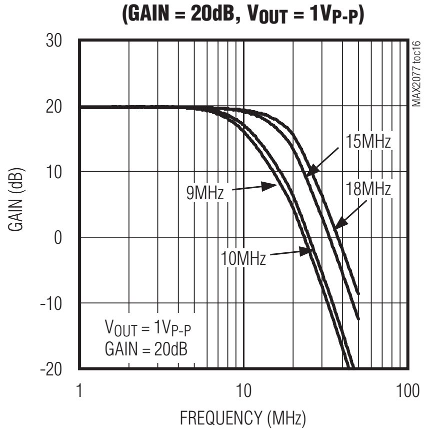
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. GAIN



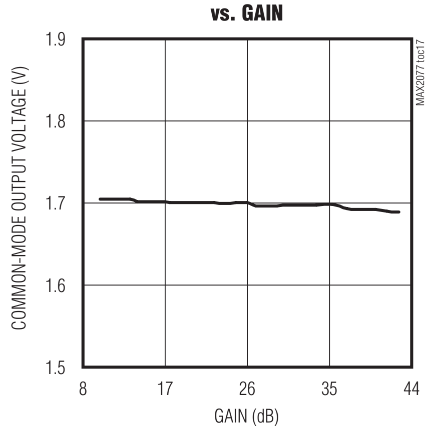
ADJACENT CHANNEL-TO-CHANNEL CROSSTALK vs. FREQUENCY



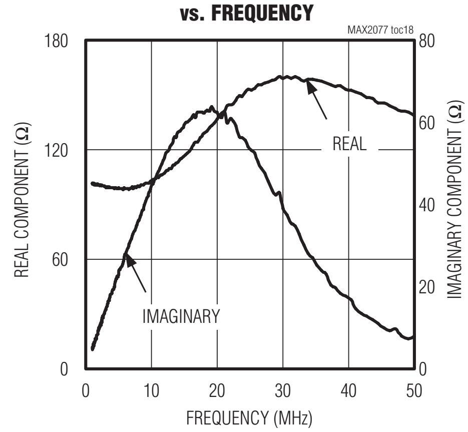
LARGE-SIGNAL BANDWIDTH vs. FREQUENCY (GAIN = 20dB, V_{OUT} = $1V_{P-P}$)



COMMON-MODE OUTPUT VOLTAGE vs. GAIN



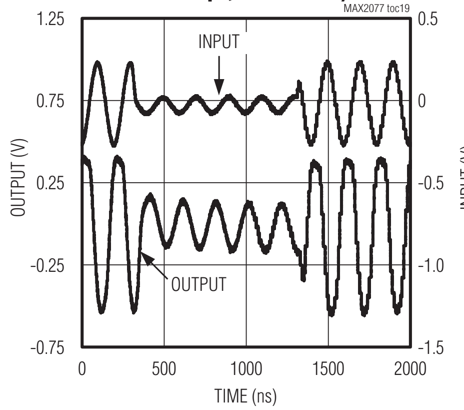
DIFFERENTIAL OUTPUT IMPEDANCE vs. FREQUENCY



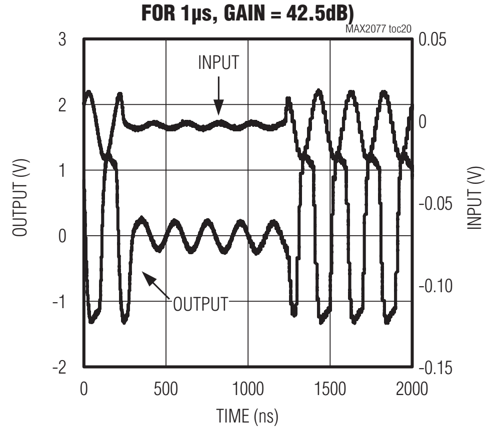
Typical Operating Characteristics (continued)

(*Typical Application Circuits*, V_{REF} = 2.475V to 2.525V, V_{CC1} = 3.3V, V_{CC2} = 4.75V, T_A = +25°C, V_{GND} = 0V, NP = 0, PD = 0, D3/D2/D1/D0 = 1/0/1/0 (R_{IN} = 200Ω, LNA gain = 18.5dB), D5/D4 = 1/1 (f_C = 18MHz), f_{RF} = 5MHz, R_S = 200Ω, capacitance to GND at each of the VGA differential outputs is 25pF, differential capacitance across VGA outputs is 15pF, R_L = 1kΩ differential, reference noise less than 10nV/√Hz from 1kHz to 20MHz, DOUT loaded with 10MΩ and 60pF, unless otherwise noted. All typical operating curves have been taken with the MAX2077CTN+ package variant.)

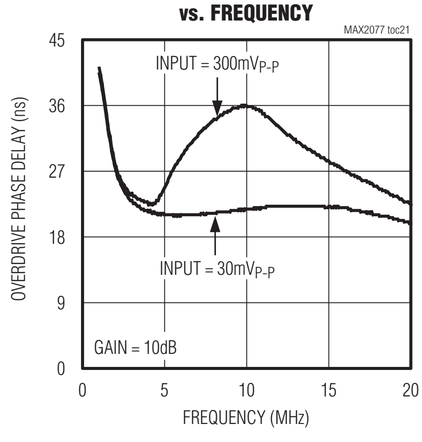
LNA OVERLOAD RECOVERY TIME (V_{IN} = 500mV$_{P-P}$ FOR 0.5µs TO 100mV$_{P-P}$ FOR 1µs AND BACK TO 500mV$_{P-P}$ FOR 0.5µs, GAIN =10dB)



VGA OVERLOAD RECOVERY TIME (V_{IN} = 40mV$_{P-P}$ FOR 1µs TO 4mV$_{P-P}$ FOR 1µs AND BACK TO 40mV$_{P-P}$ FOR 1µs, GAIN = 42.5dB)



OVERDRIVE PHASE DELAY vs. FREQUENCY



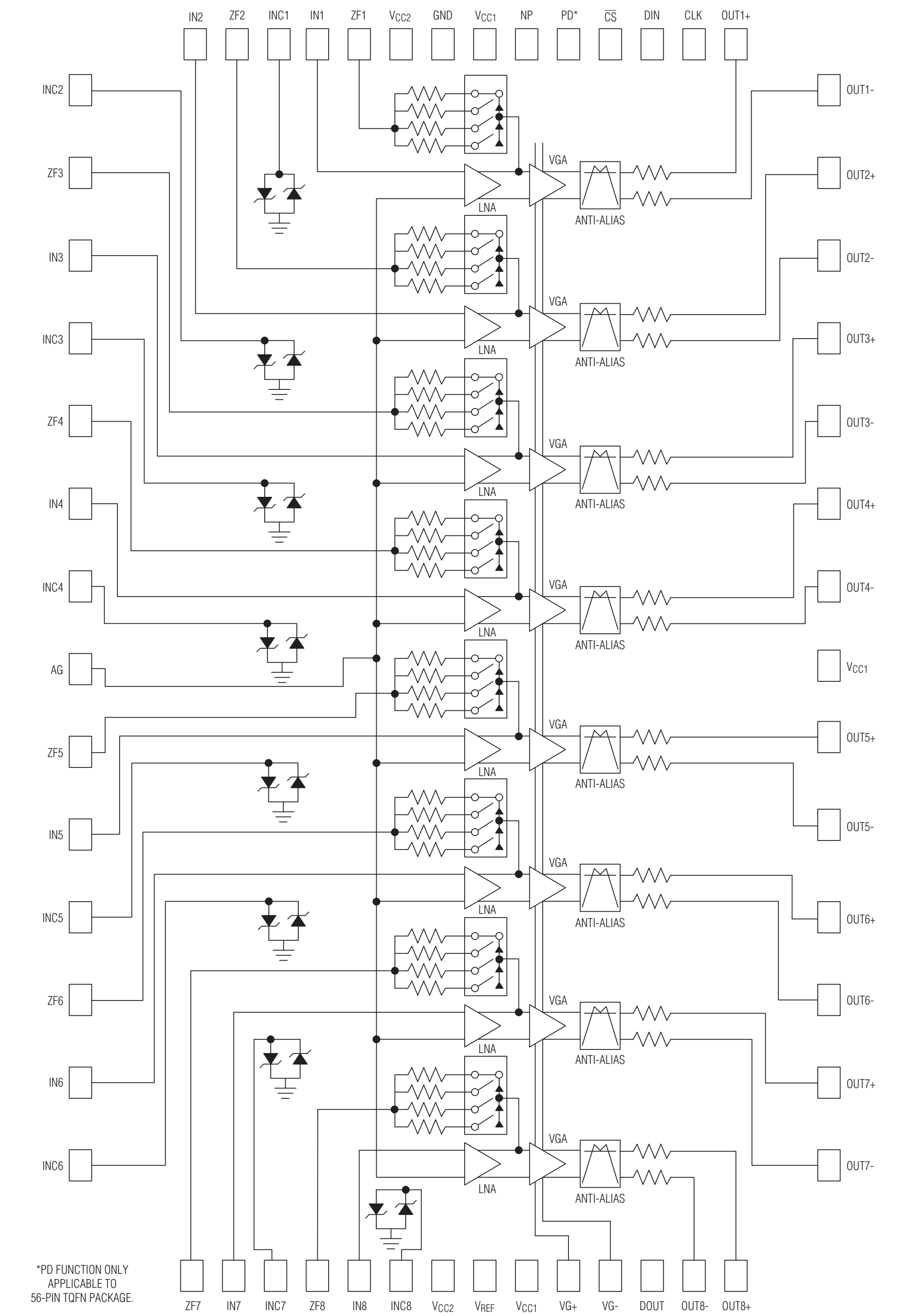
Pin Description

PIN		NAME	FUNCTION
56 TQFN	68 TQFN		
1	2	INC2	Channel 2 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuits* for details.
2	3	ZF3	Channel 3 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
3	4	IN3	Channel 3 Input
4	5	INC3	Channel 3 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuits* for details.
5	6	ZF4	Channel 4 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
6	7	IN4	Channel 4 Input
7	8	INC4	Channel 4 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuits* for details.
8	10	AG	AC Ground. Connect a low-ESR 1µF capacitor to ground.
9	11	ZF5	Channel 5 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
10	12	IN5	Channel 5 Input
11	13	INC5	Channel 5 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuits* for details.
12	14	ZF6	Channel 6 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
13	15	IN6	Channel 6 Input
14	16	INC6	Channel 6 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuits* for details.
15	17	ZF7	Channel 7 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
16	18	IN7	Channel 7 Input
17	19	INC7	Channel 7 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuits* for details.
18	20	ZF8	Channel 8 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
19	21	IN8	Channel 8 Input
20	22	INC8	Channel 8 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuits* for details.
21, 51	23, 64	V_{CC2}	4.75V Power Supply. Connect to an external 4.75V power supply. Connect all 4.75V supply pins together externally and bypass with 100nF capacitors as close as possible to the pin.
22	24	V_{REF}	External 2.5V Reference Supply. Connect to a low-noise power supply. Bypass to GND with a 0.1µF capacitor as close as possible to the pins. Note that noise performance of the device is dependent on the noise contribution from V_{REF}. Use a supply with noise lower than $5nV/\sqrt{Hz}$ from 1kHz to 20MHz.
23, 35, 49	25, 44, 63	V_{CC1}	3.3V Power Supply. Connect to an external 3.3V power supply. Connect all 3.3V supply pins together externally and bypass with 100nF capacitors as close as possible to the pin.
24	26	VG+	VGA Analog Gain Control Differential Input. Set the differential voltage to -3V for minimum gain and to +3V for maximum gain.
25	27	VG-	
26	32	DOUT	Serial Port Data Output. Data output for ease of daisy-chain programming. The level is 3.3V CMOS.

Pin Description (continued)

PIN		NAME	FUNCTION
56 TQFN	68 TQFN		
27	34	OUT8-	Channel 8 Negative Differential Output
28	35	OUT8+	Channel 8 Positive Differential Output
29	36	OUT7-	Channel 7 Negative Differential Output
30	37	OUT7+	Channel 7 Positive Differential Output
31	38	OUT6-	Channel 6 Negative Differential Output
32	39	OUT6+	Channel 6 Positive Differential Output
33	40	OUT5-	Channel 5 Negative Differential Output
34	41	OUT5+	Channel 5 Positive Differential Output
36	45	OUT4-	Channel 4 Negative Differential Output
37	46	OUT4+	Channel 4 Positive Differential Output
38	47	OUT3-	Channel 3 Negative Differential Output
39	48	OUT3+	Channel 3 Positive Differential Output
40	49	OUT2-	Channel 2 Negative Differential Output
41	50	OUT2+	Channel 2 Positive Differential Output
42	51	OUT1-	Channel 1 Negative Differential Output
43	52	OUT1+	Channel 1 Positive Differential Output
44	54	CLK	Serial Port Data Clock (Positive Edge Triggered). 3.3V CMOS. Clock input for programming the serial shift registers.
45	55	DIN	Serial Port Data Input Line. 3.3V CMOS. Data input to program the serial shift registers.
46	56	$\overline{CS}$	Active-Low Serial Port Chip Select. 3.3V CMOS. Used to store programming bits in registers, as well as in CW mode, synchronizing all channel phases (on a rising edge).
47	—	PD	Power-Down Mode Select Input (56-Pin TQFN Only). Drive PD high to place the entire device in power-down mode. Drive PD low for normal operation. This mode overrides the standby mode.
48	57	NP	VGA Standby Mode Select Input. Set NP to 1 to place the entire device in standby mode. Overrides soft channel shutdown in serial shift register, but not general power-down (PD).
50	9, 28, 31	GND	Ground
52	65	ZF1	Channel 1 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
53	66	IN1	Channel 1 Input
54	67	INC1	Channel 1 Clamp Input. Connect to a coupling capacitor. See the *Typical Application Circuits* for details.
55	68	ZF2	Channel 2 Active Impedance Matching Line. AC-couple to source with a 10nF capacitor.
56	1	IN2	Channel 2 Input
—	29, 30, 33, 42, 43, 53, 58–62	N.C.	No Connection. Internally not connected.
—	—	EP	Exposed pad. Internally connected to ground. Connect to a large ground plane using multiple vias to maximize thermal and electrical performance. Not intended as an electrical connection point.

Functional Diagram



*PD FUNCTION ONLY APPLICABLE TO 56-PIN TQFN PACKAGE.

Detailed Description

The MAX2077 is a high-density, octal-channel ultrasound receiver optimized for low-cost, high-channel count, high-performance portable and cart-based ultrasound applications. The integrated octal LNA, VGA, and AAF offer a complete ultrasound imaging path receiver solution.

Imaging path dynamic range has been optimized for exceptional second-harmonic performance. The complete imaging receive channel exhibits an exceptional 68dBFS* SNR at 5MHz. The bipolar front-end has also been optimized for exceptionally low near-carrier modulation noise for exceptional low-velocity pulsed and color-flow Doppler sensitivity under high-clutter conditions, achieving an impressive near-carrier SNR of 140dBc/Hz at 1kHz offset from a V_{OUT} = $1V_{P-P}$, 5MHz clutter signal. To add CW Doppler capability, replace the MAX2077 with the MAX2078.

Modes of Operation

The MAX2077 requires programming before it can be used. The operating modes are controlled by the D0–D6 programming bits. Tables 1 and 2 show the functions of these programming bits.

Low-Noise Amplifier (LNA)

The MAX2077's LNA is optimized for excellent dynamic range and linearity performance characteristics, making it ideal for ultrasound imaging applications. When the LNA is placed in low-gain mode, the input resistance (R_{IN}), being a function of the gain A (R_{IN} = $R_F/(1+A)$), increases by a factor of approximately 2.

Table 1. Summary of Programming Bits

BIT NAME	DESCRIPTION
D0, D1, D2	Input-impedance programming
D3	LNA gain (D3 = 0 is low gain)
D4, D5	Anti-alias filter f_C programming
D6	Don't care

Table 2. Logic Functions of Programming Bits

D6	D5	D4	D3	D2	D1	D0	MODE
X	X	X	1	0	0	0	R_{IN} = 50Ω, LNA gain = 18.5dB
X	X	X	1	0	0	1	R_{IN} = 100Ω
X	X	X	1	0	1	0	R_{IN} = 200Ω
X	X	X	1	0	1	1	R_{IN} = 1000Ω
X	X	X	0	0	0	0	R_{IN} = 100Ω, LNA gain = 12.5dB
X	X	X	0	0	0	1	R_{IN} = 200Ω
X	X	X	0	0	1	0	R_{IN} = 400Ω
X	X	X	0	0	1	1	R_{IN} = 2000Ω
X	X	X	1	1	X	X	Open feedback, LNA gain = 18.5dB
X	0	0	X	X	X	X	f_C = 9MHz
X	0	1	X	X	X	X	f_C = 10MHz
X	1	0	X	X	X	X	f_C = 15MHz
X	1	1	X	X	X	X	f_C = 18MHz

X = Don't care.

**When coupled with the MAX1437B ADC.*

Consequently, the switches that control the feedback resistance (R_F) have to be changed. For instance, the 100Ω mode in high gain becomes the 200Ω mode in low gain (see Table 2).

Variable-Gain Amplifier (VGA)

The MAX2077's VGAs are optimized for high linearity, high dynamic range, and low output-noise performance, all of which are critical parameters for ultrasound imaging applications. Each VGA path includes circuitry for adjusting analog gain, as well as an output buffer with differential output ports (OUT_+, OUT_-) for driving ADCs.

The VGA gain can be adjusted through the differential gain control input VG+ and VG-. Set the differential gain control input voltage at -3V for minimum gain and +3V for maximum gain. The differential analog control common-mode voltage is 1.65V (typ).

Overload Recovery

The device is also optimized for quick overload recovery for operation under the large input signal conditions that are typically found in ultrasound imaging applications. See the *Typical Operating Characteristics* for an illustration of the rapid recovery time from a transmit-related overload.

Power-Down Mode

The MAX2077CTN+ can also be powered down with PD (the same feature is not available in the MAX2077CTK+). Set PD to logic-high for power-down mode. In power-down mode, the device consumes 3.0µW (typ) power. Set PD to logic-low for normal operation.

Setting NP to logic-high places the MAX2077 in standby mode. In standby mode, the device consumes less power (5.6mW typ), but input/output pins remain biased to provide quick power-up response time. Standby mode is available for both MAX2077CTN+ and MAX2077CTK+ versions.

Applications Information

Serial Interface

The MAX2077 is programmed using a serial shift register arrangement. This greatly simplifies the complexity of the program circuitry, reduces the number of IC pins necessary for programming, and reduces the PCB layout complexity. The data in (DIN) and data out (DOUT) can be daisy-chained from device to device and all front-ends can run off a single programming clock.

The data can be entered after $\overline{CS}$ goes low. Once a whole word is entered, $\overline{CS}$ needs to rise. When programming the part, enter LSB first and MSB last. The chip-select line ($\overline{CS}$) is used to load the programming information in multiple MAX2077 devices at the same time. The line is pulled down before the programming begins and pulled up after it is complete for all devices used. On the rising edge, the information is stored in internal registers.

Active Impedance Matching

To provide exceptional noise-figure characteristics, the input impedance of each amplifier uses a feedback topology for active impedance matching. A feedback resistor of the value (1 + (A/2)) x R_S is added between the inverting input of the amplifier to the output. The input impedance is the feedback resistor (Z_F) divided by 1 + (A/2). The factor of two is due to the gain of the amplifier (A) being defined with a differential output. For common input impedances, the internal digitally programmed impedances can be used (see Table 2). For other input impedances, use an externally supplied resistor in series with the existing programmable feedback impedances to set the input impedance according to the above formula.

Noise Figure

The MAX2077 is designed to provide maximum input sensitivity with exceptionally low noise figure. The input active devices are selected for very low-equivalent input-noise voltage and current, optimized for source impedances from 50Ω to 1000Ω. Additionally, the noise contribution of the matching resistor is effectively divided by 1 + (A/2). Using this scheme, typical noise figure of the amplifier is approximately 2.4dB for R_{IN} = R_S = 200Ω. Table 3 illustrates the noise figure for other input impedances.

Input Clamp

The MAX2077 includes configurable integrated input-clamping diodes. The diodes are clamped to ground at ±0.8V. The input-clamping diodes can be used to prevent large transmit signals from overdriving the inputs of the amplifiers. Overdriving the inputs could possibly place charge on the input-coupling capacitor, causing longer transmit overload recovery times. Input signals are AC-coupled to the single-ended inputs IN1–IN8, but are clamped with the INC1–INC8 inputs. See the *Typical Application Circuits*. If external clamping devices are preferred, simply leave INC1–INC8 unconnected.

Table 3. Noise Figure vs. Source and Input Impedances

R_S (Ω)	R_{IN} (Ω)	NF (dB)
50	50	4.5
100	100	3.4
200	200	2.4
1000	1000	2.2

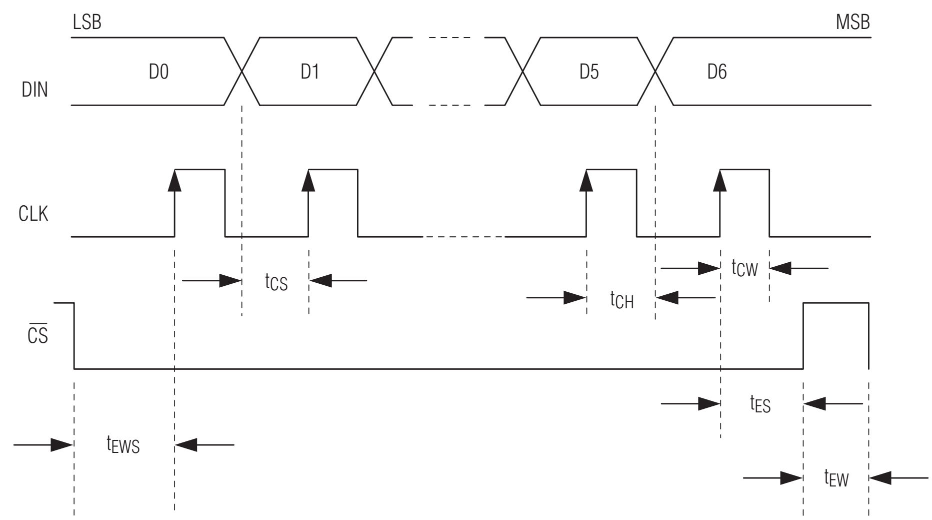


Figure 1. Shift Register Timing Diagram

Analog Output Coupling

Each of the VGA output pins can drive 25pF to GND and 15pF || 1kΩ differentially. The differential outputs have a common-mode bias of approximately 1.73V. AC-couple these differential outputs if the next stage has a different common-mode input range.

Power-Supply Sequencing

Use the following power-on sequence:

1) 4.75V supply
2) 3.3V supply
3) 2.5V reference voltage
4) Control signals

Before a signal is turned on, it should be either at 0V or in an open state.

Ultrasound-Specific IMD3 Specification

Unlike typical communications applications, the two input tones are not equal in magnitude for the ultrasound-specific IMD3 two-tone specification. In this measurement, f_1 represents reflections from tissue and f_2 represents reflections from blood. The latter reflections are typically 25dB lower in magnitude, and hence the measurement is defined with one input tone 25dB lower than the other. The IMD3 product of interest (f_1 - (f_2 - f_1)) presents itself as an undesired Doppler error signal in ultrasound applications (see Figure 2).

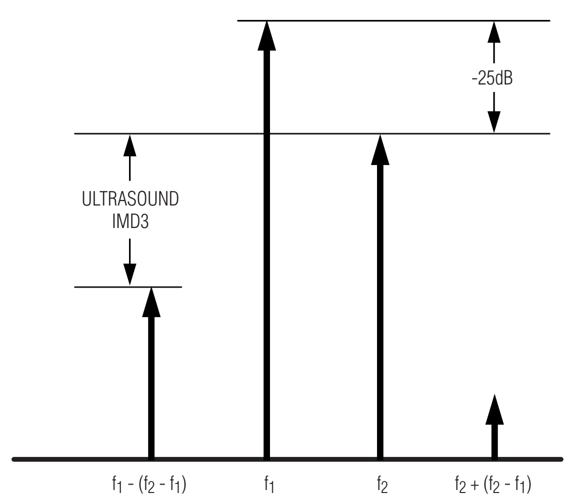


Figure 2. Ultrasound IMD3 Measurement Technique

PCB Layout

The pin configuration of the MAX2077 is optimized to facilitate a very compact physical layout of the device and its associated discrete components. A typical application for this device might incorporate several devices in close proximity to handle multiple channels of signal processing.

The exposed pad (EP) of the MAX2077's TQFN-EP packages provide a low thermal-resistance path to the die. It is important that the PCB on which the MAX2077 is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP **MUST** be soldered to a ground plane on the PCB, either directly or through an array of plated via holes.

Chip Information

PROCESS: Complementary BiCMOS

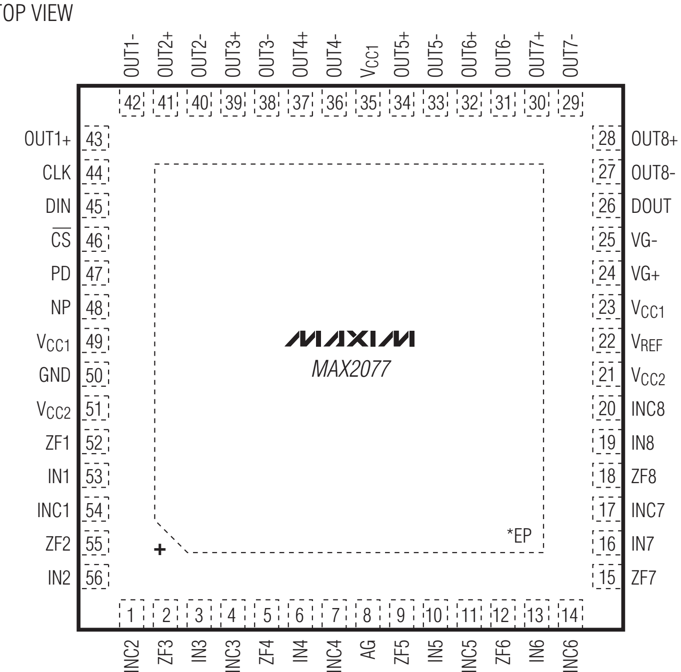
Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
56 TQFN-EP	T5688+2	**21-0135**
68 TQFN-EP	T6800+2	**21-0142**

Pin Configurations

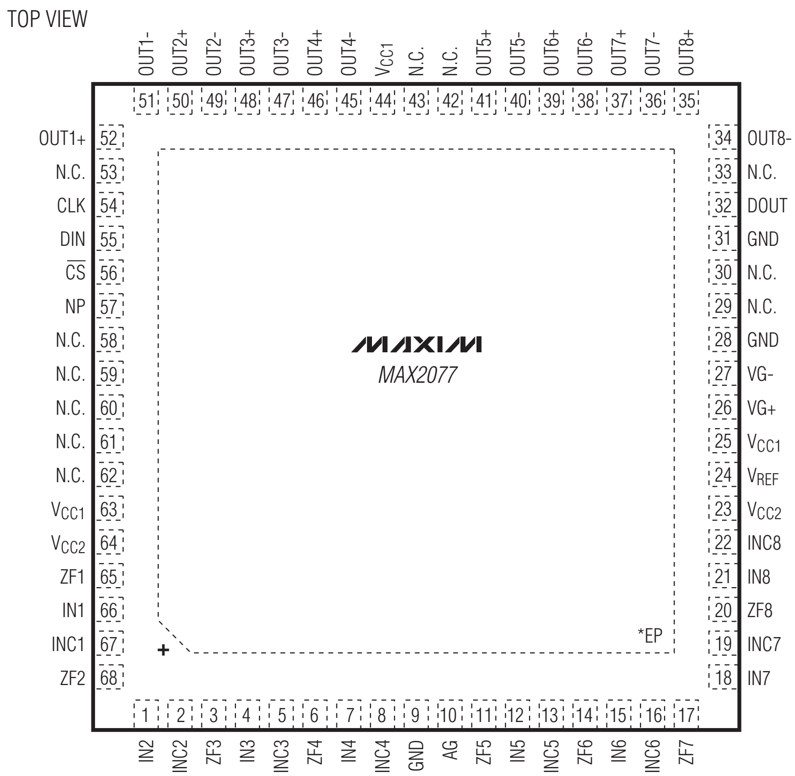
TOP VIEW



TQFN
(8mm × 8mm)

*EP = EXPOSED PAD.

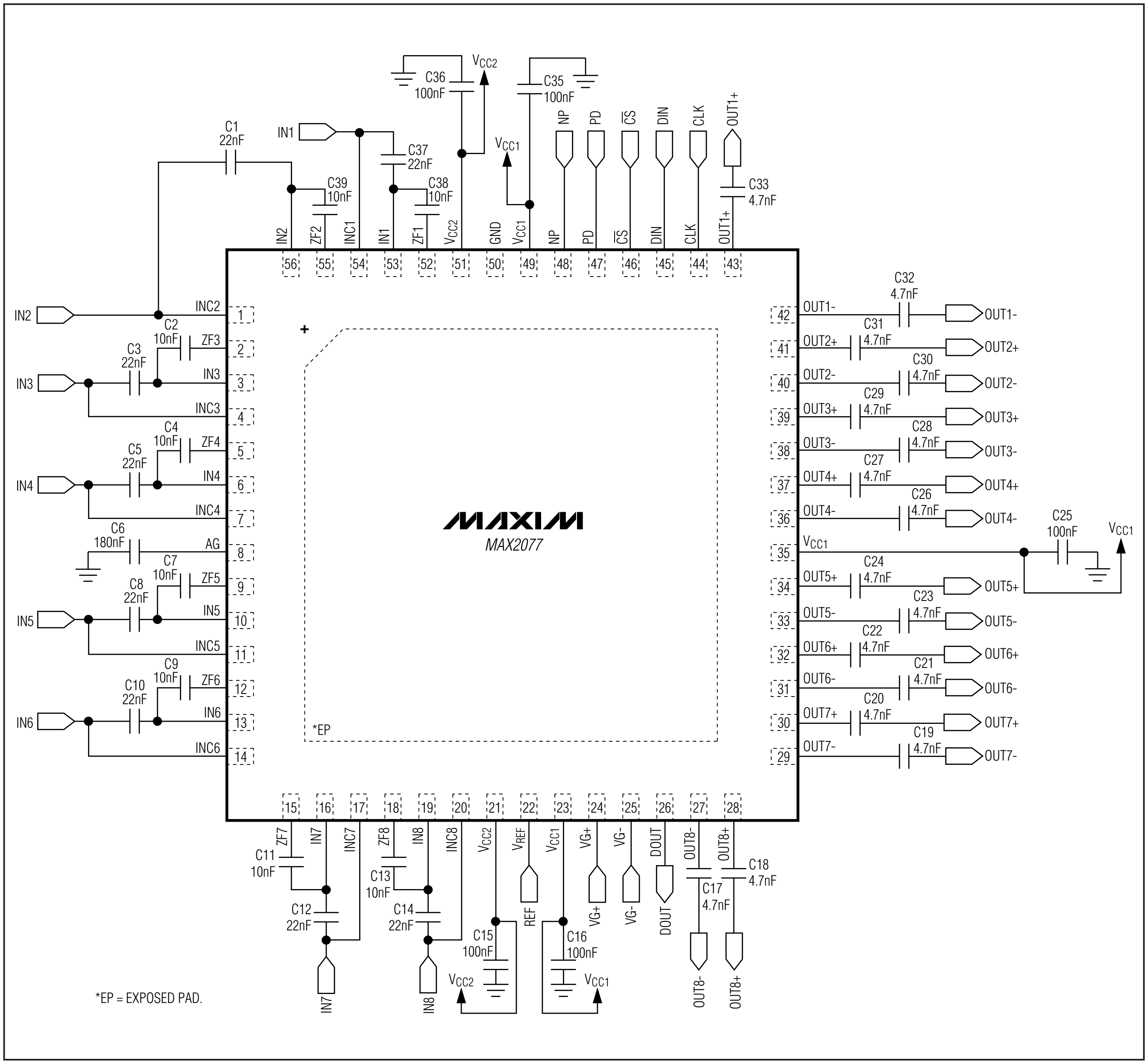
Pin Configurations (continued)



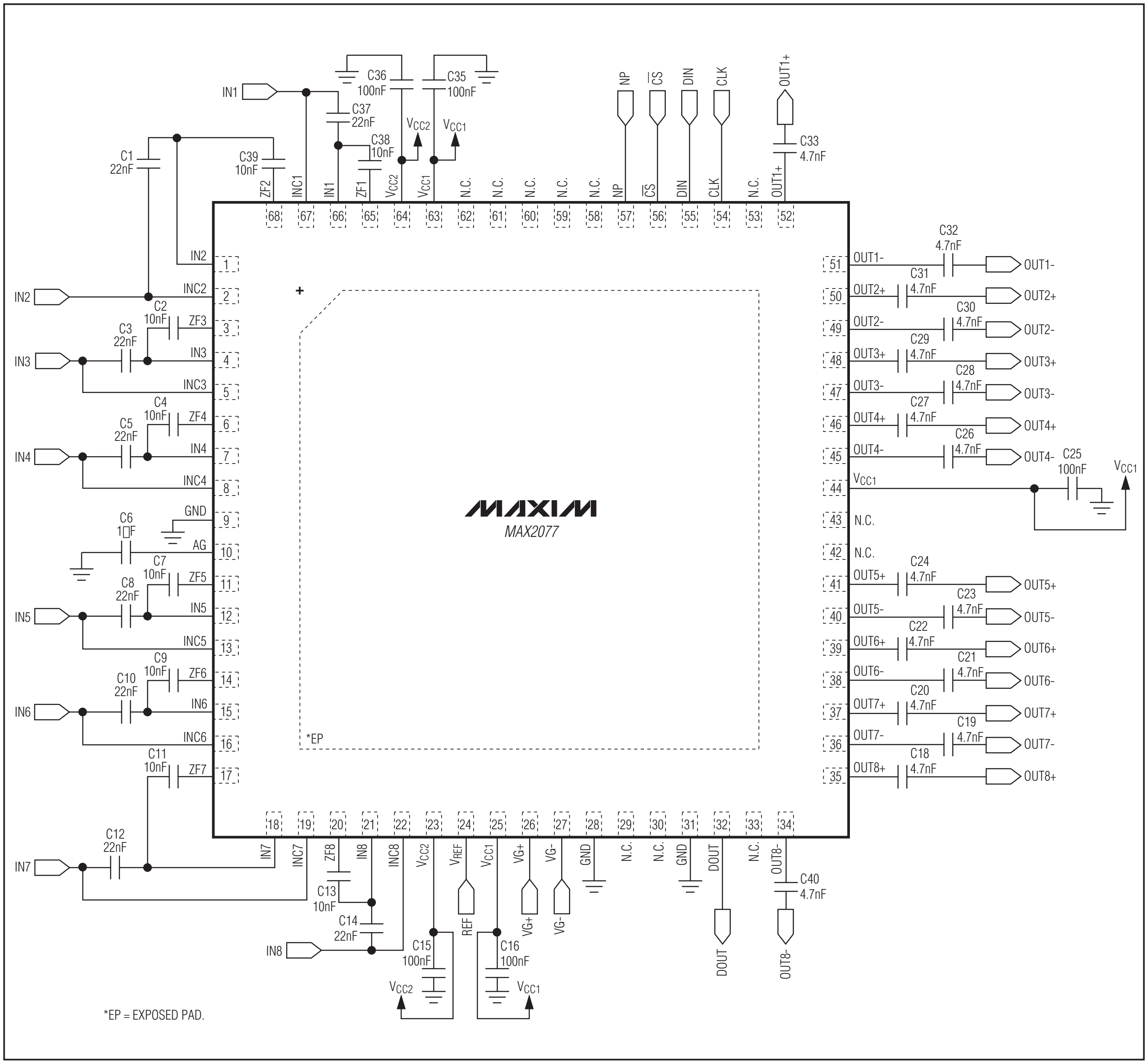
TQFN
(10mm × 10mm)

*EP = EXPOSED PAD.

Typical Application Circuits



Typical Application Circuits (continued)



Octal-Channel Ultrasound Front-End

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/09	Initial release	—
1	9/09	Removed future product reference for MAX2077CTK+ package and made minor corrections	1, 6–9, 12