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19-1912; Rev 3; 11/03

EVALUATION KIT AVAILABLE

MAXIM

2.4GHz to 2.5GHz Linear Power Amplifier

MAX2242

General Description

The MAX2242 low-voltage linear power amplifier (PA) is designed for 2.4GHz ISM-band wireless LAN applications. It delivers +22.5dBm of linear output power with an adjacent-channel power ratio (ACPR) of <-33dBc 1st-side lobe and <-55dBc 2nd-side lobe, compliant with the IEEE 802.11b 11MB/s WLAN standard with at least 3dB margin. The PA is packaged in the tiny 3x4 chip-scale package (UCSP™), measuring only 1.5mm x 2.0mm, ideal for radios built in small PC card and compact flash card form factors.

The MAX2242 PA consists of a three-stage PA, power detector, and power management circuitry. The power detector provides over 20dB of dynamic range with ±0.8dB accuracy at the highest output power level. An accurate automatic level control (ALC) function can be easily implemented using this detector circuit.

The PA also features an external bias control pin. Through the use of an external DAC, the current can be throttled back at lower output power levels while maintaining sufficient ACPR performance. As a result, the highest possible efficiency is maintained at all power levels. The device operates over a single +2.7V to +3.6V power-supply range. An on-chip shutdown feature reduces operating current to 0.5µA, eliminating the need for an external supply switch.

Applications

IEEE 802.11b DSSS Radios

Wireless LANs

HomeRF

2.4GHz Cordless Phones

2.4GHz ISM Radios

Actual Size

■

1.5mm × 2.0mm

Typical Application Circuit appears at end of data sheet.

UCSP is a trademark of Maxim Integrated Products, Inc.

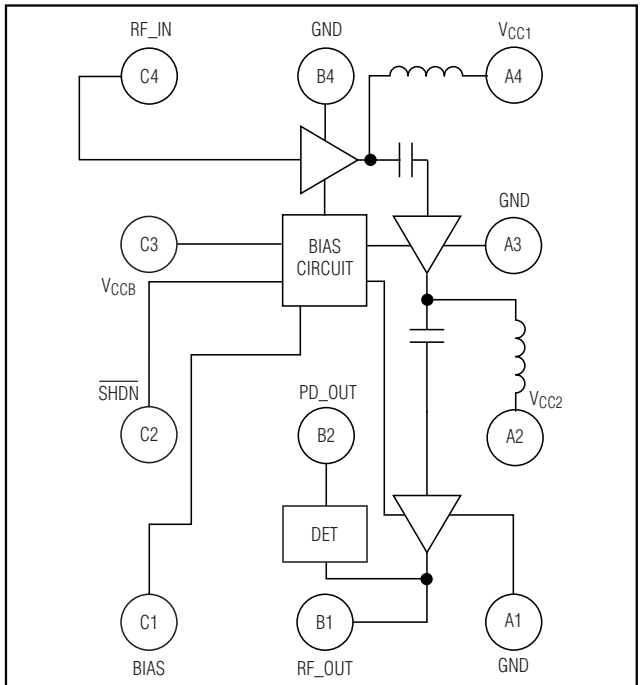
Features

- **2.4GHz to 2.5GHz Operating Range**
- **+22.5dBm Linear Output Power (ACPR of <-33dBc 1st-Side Lobe and <-55dbc 2nd-Side Lobe)**
- **28.5dB Power Gain**
- **On-Chip Power Detector**
- **External Bias Control for Current Throttleback**
- **+2.7V to +3.6V Single-Supply Operation**
- **0.5µA Shutdown Mode**
- **Tiny Chip-Scale Package (1.5mm × 2.0mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX2242EBC-T	-40°C to +85°C	3 × 4 UCSP	AAE

Pin Configuration



3×4 UCSP

2.4GHz to 2.5GHz Linear Power Amplifier

ABSOLUTE MAXIMUM RATINGS

V_{CC1}, V_{CC2} to GND (no RF signal applied) .....-0.3V to +5.5V
RF Input Power .....+10dBm
$\overline{SHDN}$, BIAS, PD_OUT, RF_OUT .....-0.3V to (V_{CC} + 0.3V)
DC Input Current at RF_IN Port.....-1mA to +1mA
Maximum VSWR Without Damage 10:1
Maximum VSWR for Stable Operation.....5:1
Continuous Power Dissipation (T_A = +85°C)
3×4 UCSP (derate 80mW/°C above +85°C) 1.6W
Operating Temperature Range .....-40°C to +85°C
Thermal Resistance .....25°C/W
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +125°C
Lead Temperature (soldering, 10s) .....+260°C
Continuous Operating Lifetime.....10yrs × $0.92^{(T_A - 60°C)}$
(For Operating Temperature, $T_A \geq +60°C$)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.6V, f_{IN} = 2.4GHz to 2.5GHz, $V_{\overline{SHDN}} = V_{CC}$, RF_IN = RF_OUT = connected to 50Ω load, T_A = -40°C to +85°C. Typical values are measured at V_{CC} = +3.3V, f_{IN} = 2.45GHz, T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.7		3.6	V
Supply Current (Notes 2, 3, 6)	P_{OUT} = +22dBm, V_{CC} = +3.3V, idle current = 280mA		300	335	mA
	P_{OUT} = +13dBm, idle current = 55mA		90		
	P_{OUT} = +5dBm, idle current = 25mA		50		
Shutdown Supply Current	$V_{\overline{SHDN}}$ = 0, no RF input		0.5	10	µA
Logic Input Voltage High		2.0			V
Logic Input Voltage Low				0.8	V
Logic Input Current High		-1		5	µA
Logic Input Current Low		-1		1	µA

AC ELECTRICAL CHARACTERISTICS

(MAX2242 Evaluation Kit, V_{CC} = +3.3V, $V_{\overline{SHDN}}$ = V_{CC}, 50Ω source and load impedance, f_{IN} = 2.45GHz, T_A = +25°C, unless otherwise noted.) (Note 6)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Range (Notes 3, 4)		2.4		2.5	GHz
Power Gain (Notes 1, 3)	T_A = +25°C	26.5	28.5		dB
	T_A = -40°C to +85°C	25.5			
Gain Variation Over Temperature (Note 3)	T_A = -40°C to +85°C		±1.2		dB
Gain Variation Over V_{CC} (±10%) (Note 3)	V_{CC} = +3.0V to +3.6V		±0.3		dB
Output Power (Notes 3, 5, 8)	ACPR, 1st-side lobe < -33dBc, 2nd-side lobe < -55dBc	21.5	22.5		dBm
Saturated Output Power	P_{IN} = +5dBm		26.5		dBm
Harmonic Output (2f, 3f, 4f)			-40		dBc
Input VSWR	Over full P_{IN} range		1.5:1		
Output VSWR	Over full P_{OUT} range		2.5:1		
Power Ramp Turn-On Time (Note 7)	$\overline{SHDN}$ from low to high		1	1.5	µs
Power Ramp Turn-Off Time (Note 7)	$\overline{SHDN}$ from high to low		1	1.5	µs
RF Output Detector Response TIme			2.5	5	µs
RF Output Detector Voltage	P_O = +22dBm (Note 9)		1.8		V
	P_O = +13dBm (Note 9)		0.9		
	P_O = +5dBm (Note 9)		0.55		

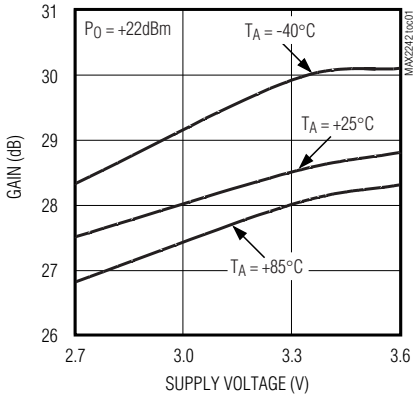
Note 1: Specifications over T_A = -40°C to +85°C are guaranteed by design. Production tests are performed at T_A = +25°C.
Note 2: Idle current is controlled by external DAC for best efficiency over the entire output power range.
Note 3: Parameter measured with RF modulation based on IEEE 802.11b standard.
Note 4: Power gain is guaranteed over this frequency range. Operation outside this range is possible, but is not guaranteed.
Note 5: Output two-tone third-order intercept point (OIP3) is production tested at T_A = +25°C. The OIP3 is tested with two signals at f1 = 2.450GHz and f2 = 2.451GHz with fixed P_{IN}.
Note 6: Min/max limits are guaranteed by design and characterization.
Note 7: The total turn-on and turn-off times required for PA output power to settle to within 0.5dB of the final value.
Note 8: Excludes PC board loss of approximately 0.15dB.
Note 9: See *Typical Operating Characteristics* for statistical variation.

2.4GHz to 2.5GHz Linear Power Amplifier

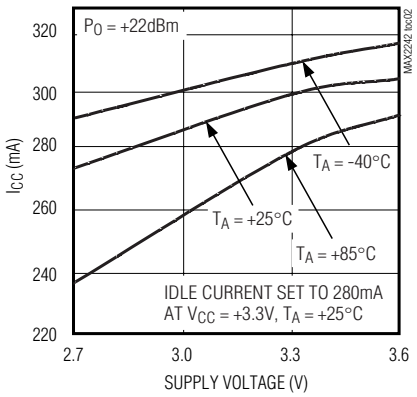
Typical Operating Characteristics

(V_{CC} = +3.3V, f_{IN} = 2.45MHz, RF modulation = IEEE 802.11b, $V_{\overline{SHDN}}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

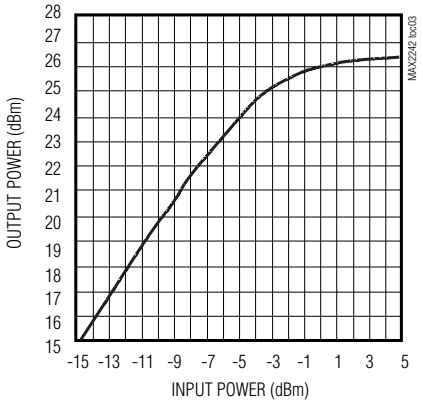
GAIN vs. SUPPLY VOLTAGE



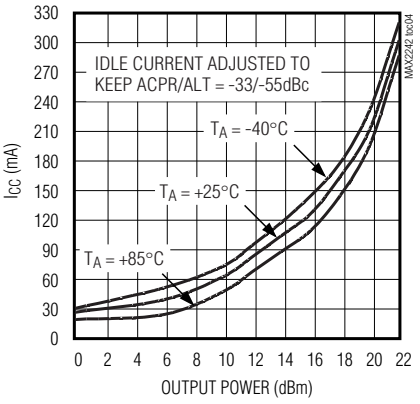
I_{CC} vs. SUPPLY VOLTAGE



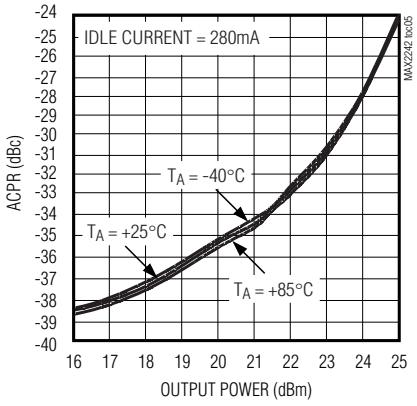
OUTPUT POWER vs. INPUT POWER



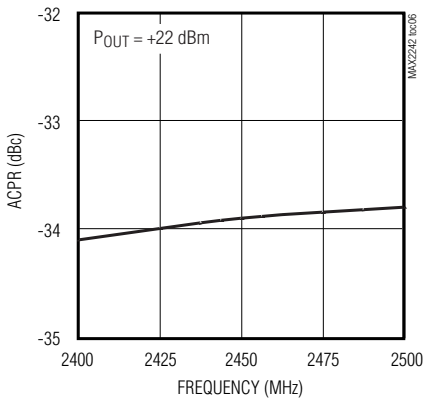
I_{CC} vs. OUTPUT POWER



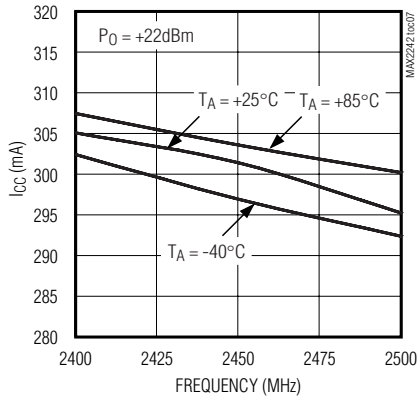
ACPR vs. OUTPUT POWER



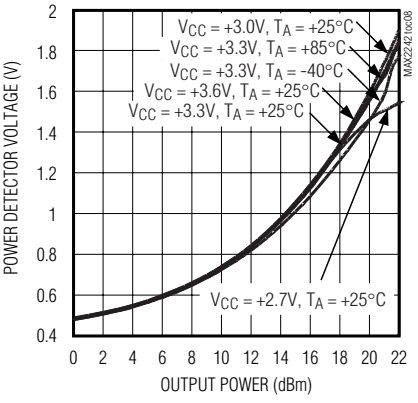
ACPR vs. FREQUENCY



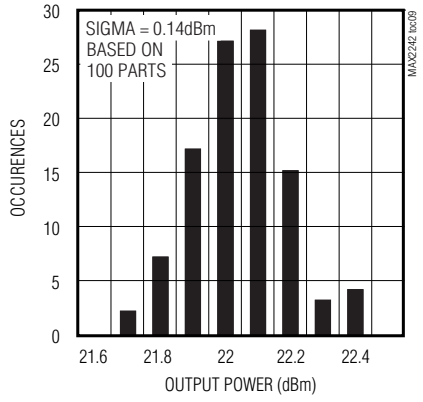
I_{CC} vs. FREQUENCY



POWER DETECTOR VOLTAGE vs. OUTPUT POWER



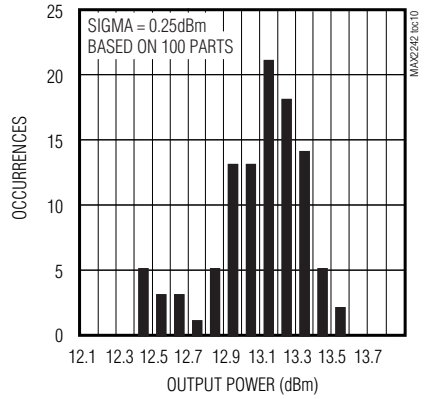
OUTPUT POWER HISTOGRAM AT FIXED 1.6V POWER DETECTOR VOLTAGE



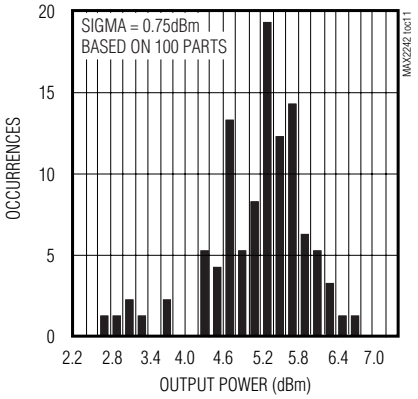
Typical Operating Characteristics (continued)

(V_{CC} = +3.3V, f_{IN} = 2.45MHz, RF modulation = IEEE 802.11b, $V_{\overline{SHDN}}$ = V_{CC}, T_A = +25°C, unless otherwise noted.)

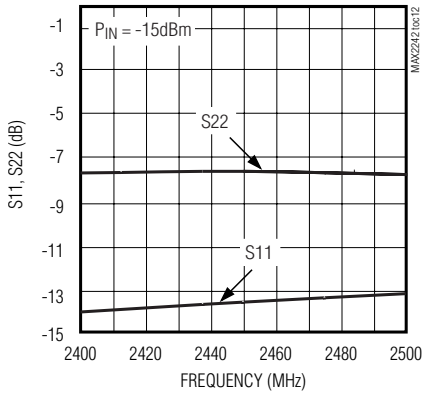
OUTPUT POWER HISTOGRAM AT FIXED 0.8V POWER DETECTOR VOLTAGE



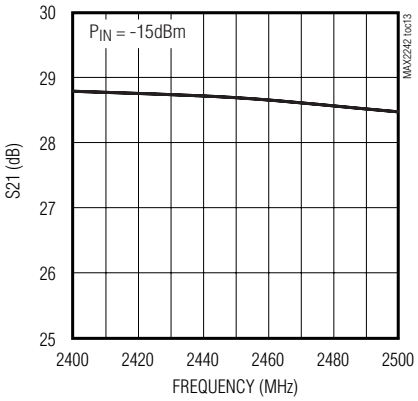
OUTPUT POWER HISTOGRAM AT FIXED 0.5V POWER DETECTOR VOLTAGE



S11, S22, vs. FREQUENCY



MAX2242 S21 vs. FREQUENCY



2.4GHz to 2.5GHz Linear Power Amplifier

Pin Description

PIN	NAME	FUNCTION
A1	GND	3rd Stage Ground. Refer to *Application Information* section for detailed PC-board layout information.
A2	V_{CC2}	2nd Stage Supply Voltage. Bypass to ground using configuration in the typical operating circuit.
A3	GND	3rd Stage Ground. Refer to *Application Information* section for detailed PC-board layout information.
A4	V_{CC1}	1st Stage Supply Voltage. Bypass to ground using configuration in the typical operating circuit.
B1	RF_OUT	RF Output. Requires external matching.
B2	PD_OUT	Power Detector Output. This output is a DC voltage indicating the PA output power. Connect a 47kΩ resistor to GND.
B4	GND	1st Stage and Bias Control Circuit Ground
C1	BIAS	Bias Control. Connect one 8kΩ resistor from BIAS to GND and one 8kΩ resistor from BIAS to DAC block to set the idle current.
C2	$\overline{SHDN}$	Shutdown Input. Drive logic low to place the device in shutdown mode. Drive logic high for normal operation.
C3	V_{CCB}	Bias Circuit DC Supply Voltage. Bypass to ground using configuration in the typical operating circuit.
C4	RF_IN	RF Input. Requires external matching.

Detailed Description

The MAX2242 is a linear PA intended for 2.4GHz ISM-band wireless LAN applications. The PA is fully characterized in the 2.4GHz to 2.5GHz ISM band. The PA consists of two driver stages and an output stage. The MAX2242 also features an integrated power detector and power shutdown control mode.

Dynamic Power Control

The MAX2242 is designed to provide optimum power-added efficiency (PAE) in both high and low power applications. For a +3.3V supply at high output power level, the output power is typically +22.5dBm with an idle current of 280mA. At low output-power levels, the DC current can be reduced by an external DAC to increase PAE while still maintaining sufficient ACPR performance. This is achieved by using external resistors connected to the BIAS pin to set the bias currents of the driver and output stages. The resistors are typically 8kΩ. Typically, a DAC voltage of 1.0V will give a 280mA bias current. Increasing the DAC voltage will decrease the idle current. Similarly, decreasing the DAC voltage will increase the idle current.

The BIAS pin is maintained at a constant voltage of 1.0V, allowing the user to set the desired idle current using only two off-chip 1% resistors: a shunt resistor, R2, from BIAS to ground; and a series resistor, R1, to the DAC voltage, as shown in the *Typical Application Circuit*. Resistor values R1 and R2 are determined as follows:

$$V_{MAX} = 1.0 + (1.0 \times R1) / R2; \quad (I_{CC} = 0, V_{DAC} = V_{MAX}) \quad (1)$$

$$I_{MAX} = (1.0 \times 1867) \times (R1 + R2) / (R1 \times R2); \quad (I_{CC} = I_{MAX} = \text{max value}, V_{DAC} = 0) \quad (2)$$

$$I_{DAC} = (V_{DAC} - 1.0) / R1 \quad (3)$$

$$I_{MID} = (1.0 \times 1867) / R2; \quad (V_{DAC} = 1.0V \text{ or floating}) \quad (4)$$

$$I_{CC} = 1867 \times I_{BIAS} \quad (5)$$

where

V_{MAX} = is the maximum DAC voltage

I_{MAX} = is the maximum idle current

I_{MID} = is the idle current with V_{DAC} = 1.0V or not connected

V_{DAC} = is the DAC voltage

I_{DAC} = is the DAC current

If no DAC is used and a constant idle current is desired, use equation 4 to determine the resistor values for a given total bias current. Only R2 is required.

For a DAC capable of both sourcing and sinking currents, the full voltage range of the DAC (typically from 0 to +3V) can be used. By substituting the desired values of V_{MAX} and I_{MAX} into equations 1 and 2, R1 and R2 can be easily calculated.

For a DAC capable of sourcing current only, use equation 4 to determine the value of resistor R2 for the desired maximum current. Use equation 1 to determine the value of resistor R1 for the desired minimum current.

For a DAC capable of sinking current only, set resistors R1 and R2 to 0 and connect the DAC directly to the BIAS pin. Use equation 5 to determine the DAC current required for a given I_{CC}.

Shutdown Mode

Apply logic low to $\overline{SHDN}$ (pin C2) to place the MAX2242 into shutdown mode. In this mode, all gain stages are disabled and supply current typically drops to 0.5µA. Note that the shutdown current is lowest when $V_{\overline{SHDN}} = 0$.

Power Detector

The power detector generates a voltage proportional to the output power by monitoring the output power using an internal coupler. It is fully temperature compensated and allows the user to set the bandwidth with an external capacitor. For maximum bandwidth, connect a 47kΩ resistor from PD_OUT to GND and do not use any external capacitor.

Applications Information

Interstage Matching and Bypassing

V_{CC1} and V_{CC2} provide bias to the first and second stage amplifiers, and are also part of the interstage matching networks required to optimize performance between the three amplifier stages. See the *Typical Application Circuit* for the lumped and discrete component values used on the MAX2242 EV kit for optimum interstage matching and RF bypassing. In addition to RF bypass capacitors on each bias line, a global bypass capacitor of 22µF is necessary to filter any noise on the supply line. Route separate V_{CC} bias paths from the global bypass capacitor (star topology) to avoid coupling between PA stages. Use the MAX2242 EV kit PC board layout as a guide.

External Matching

The RFIN port requires a matching network. The RFIN port impedance is 16–j30 at 2.45GHz. See the *Typical Application Circuit* for recommended component values.

The RFOUT port is an open-collector output that must be pulled to V_{CC} through a 10nH RF choke for proper biasing. A shunt 33pF capacitor to ground is required at the supply side of the inductor. In addition, a matching network is required for optimum gain, efficiency, ACPR, and output power. The load impedance seen at the RFOUT port of the MAX2242 on the EV kit is approximately 8 + j5Ω. This should serve as a good starting point for your layout. However, optimum performance is layout dependent and some component optimization may be required. See the *Typical Application Circuit* for the lumped and discrete component values used on the MAX2242 EV kit to achieve this impedance.

Ground Vias

Placement and type of ground vias are important to achieve optimum gain and output power and ACPR performance. Each ground pin requires its own throughhole via (via diameter = 10mils) placed as near to the device pin as possible to reduce ground inductance and feedback between stages. Use the MAX2242 EV kit PC board layout as a guide.

Layout and Thermal Management Issues

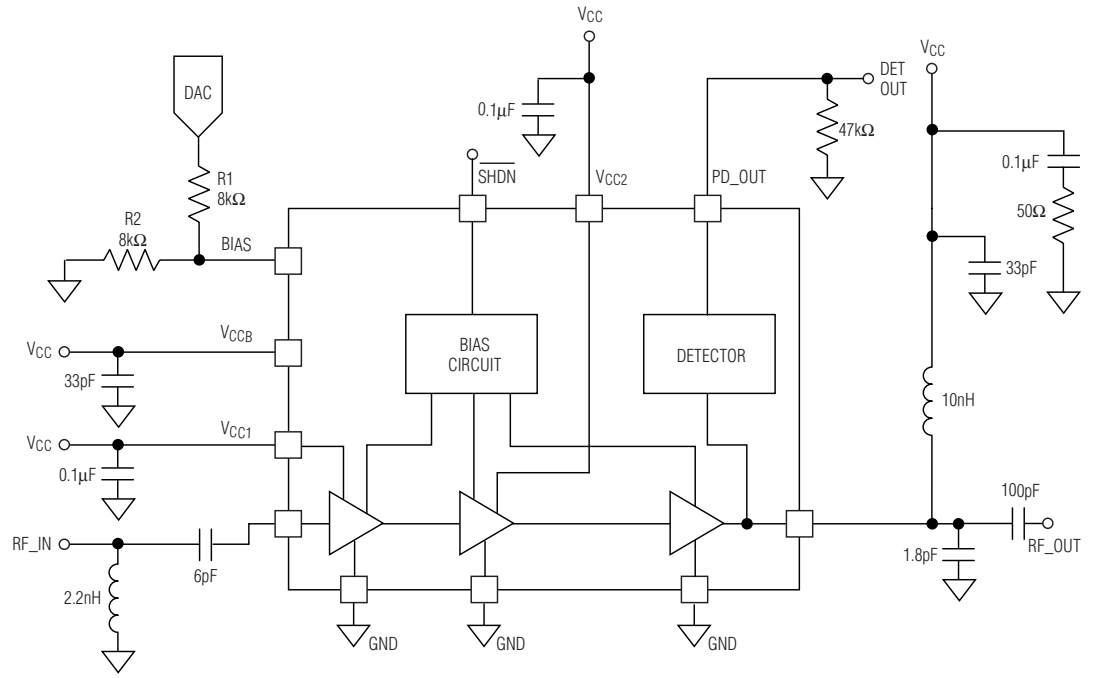
The MAX2242 EV kit serves as a layout guide. Use controlled-impedance lines on all high-frequency inputs and outputs. The GND pins also serve as heat sinks. Connect all GND pins directly to the topside RF ground. On boards where the ground plane is not on the component side, connect all GND pins to the ground plane with plated multiple throughholes close to the package. PC board traces connecting the GND pins also serve as heat sinks. Make sure that the traces are sufficiently wide.

UCSP Reliability

UCSP represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit-board material, and usage environment. The user should closely review these areas when considering use of a UCSP. Performance through the operating-life test and moisture resistance remains uncompromised as it is primarily determined by the wafer-fabrication process. Mechanical stress performance is a greater consideration for a UCSP. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged-product lead frame. Solder joint contact integrity must be considered. Testing done to characterize the

2.4GHz to 2.5GHz Linear Power Amplifier

Typical Application Circuit



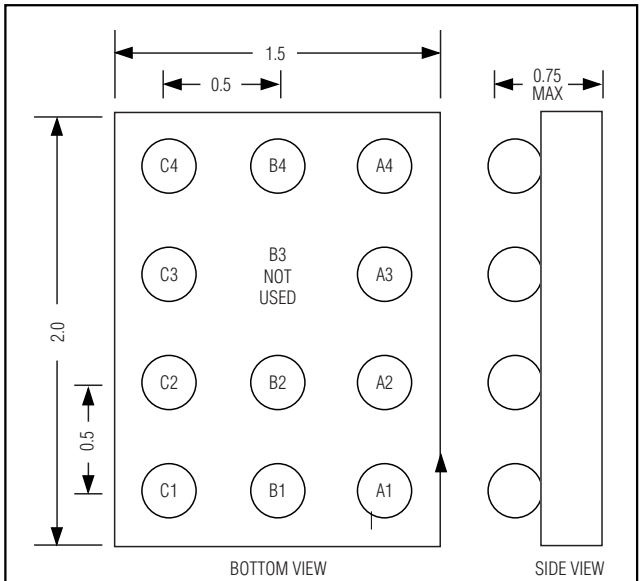
NOTE: REFER TO MAX2242 EV KIT DATA SHEET FOR DETAILED LAYOUT INFORMATION.

UCSP reliability performance shows that it is capable of performing reliably through environmental stresses. Users should also be aware that as with any interconnect system there are electromigration-based current limits that, in this case, apply to the maximum allowable current in the bumps. Reliability is a function of this current, the duty cycle, lifetime, and bump temperature. See the *Absolute Maximum Ratings* section for any specific limitations listed under Continuous Operating Lifetime.Results of environmental stress tests and additional usage data and recommendations are detailed in the UCSP application note, which can be found on Maxim's website at www.maxim-ic.com.

Chip Information

TRANSISTOR COUNT: 486

Package Diagram

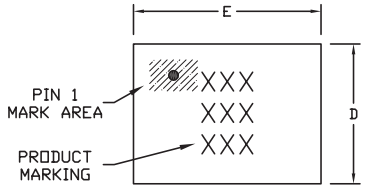


CHIP-SCALE PACKAGE (ALL DIMENSIONS IN mm)

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

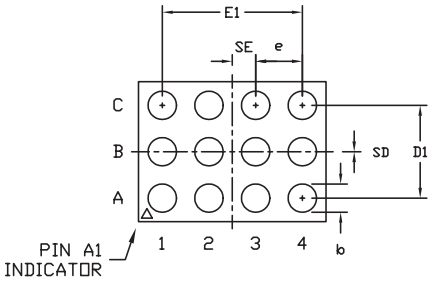
12L, UCSP 4x3.EPS



TOP VIEW

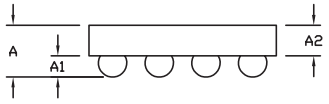
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 4x3 UCSP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0104	F	1/1

Note: *MAX2242 does not use bump B3.*