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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



MAX2248

1.9GHz Power Amplifier

General Description

The MAX2248 single-supply, low-voltage power amplifier (PA) IC is designed specifically for applications in the 1880MHz to 1930MHz frequency band. The PA provides a +20dBm (100mW) output power in the highest power mode.

The PA includes a digital power control circuit to greatly simplify control of the output power. Four digitally controlled output power levels are provided: from +4dBm to +20dBm. A digital input controls the active or shutdown operating modes of the PA. In the shutdown mode, the current reduces to 0.5µA.

The MAX2248 integrates the RF input and inter-stage matching to simplify application of the IC. Temperature and supply-independent biasing are also included to provide stable performance under all operating conditions.

The IC operates from a +2.7V to +5V single-supply voltage. No negative bias voltage is required. Current consumption is a modest 105mA at the highest power level.

This part is packaged in a 3mm x 3mm, 16-pin TQFN.

Benefits and Features

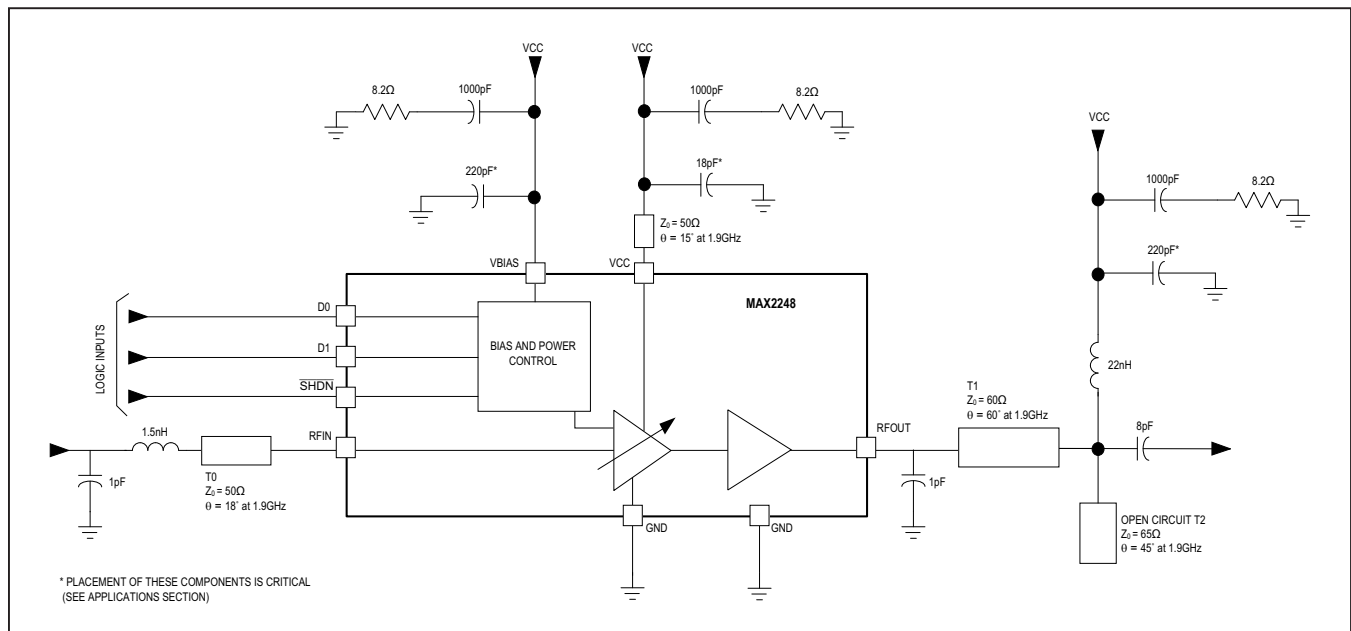
- Frequency Range: 1880MHz–1930MHz
- High +20dBm Output Power
- 2-Bit Digital Power Control: Four Output Levels
- Low 105mA Operating Current
- 0.5µA Low-Power Shutdown Mode Current
- +2.7V to +5V Single-Supply Operation
- Small 3mm x 3mm, 16-Pin TQFN Package

Applications

- 1.9GHz DECT (Cordless Phones and Wireless Headsets)

Ordering Information appears at end of data sheet.

Typical Application Circuit/Functional Block Diagram



Absolute Maximum Ratings

BIAS, V _{CC} , RFOUT to GND.....	-0.3V to +6V
SHDN, D0, D1 to GND.....	-0.3V to V _{BIAS} + 0.3V
RFIN to GND.....	-0.7V to +0.7V
RF Input Power (RFIN).....	+10dBm
Input Current (SHDN, D0, D1).....	-10mA to +10mA

Continuous Power Dissipation (T _A = +70°C)	
16-Pin TQFN.....	1176.5mW
Deration above T _A = +70°C.....	14.70mW/°C
Operating Temperature Range.....	-40°C to +85°C
Storage Temperature Range.....	-65°C to +150°C
Soldering Temperature (reflow).....	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 TQFN

PACKAGE CODE	T1633+5
Outline Number	21-0136
Land Pattern Number	90-0032
THERMAL RESISTANCE, SINGLE-LAYER BOARD:	
Junction to Ambient (θ _{JA})	68°C/W
Junction to Case (θ _{JC})	10°C/W
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ _{JA})	48°C/W
Junction to Case (θ _{JC})	10°C/W

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Electrical Characteristics

(Using Typical Application Circuit, V_{CC} = +2.7V to +5V, P_{RFIN} = 0dBm to +4dBm, f_{RFIN} = 1880MHz to 1930MHz, SHDN = V_{CC}, T_A = -40°C to +85°C, Typical values measured at V_{CC} = +3.2V, P_{RFIN} = +3dBm, f_{RFIN} = 1.9GHz, T_A = +25°C, unless otherwise noted. (Note 1))

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS					
Supply Current (Note 2, Note 3)	D1 = Low, D0 = Low, T _A = +25°C, P _{RFIN} = +3dBm, V _{CC} = 3.2V, f _{RFIN} = 1.9GHz		73	90	mA
	D1 = Low, D0 = Low (Note 8)			126	
	D1 = Low, D0 = High, T _A = +25°C, P _{RFIN} = +3dBm, V _{CC} = 3.2V, f _{RFIN} = 1.9GHz		76	95	
	D1 = Low, D0 = High (Note 8)			130	
	D1 = High, D0 = Low, T _A = +25°C, P _{RFIN} = +3dBm, V _{CC} = 3.2V, f _{RFIN} = 1.9GHz		82	105	
	D1 = High, D0 = Low (Note 8)			150	
	D1 = High, D0 = High, T _A = +25°C, P _{RFIN} = +3dBm, V _{CC} = 3.2V, f _{RFIN} = 1.9GHz		105	125	
	D1 = High, D0 = High (Note 8)			202	

Electrical Characteristics (continued)

(Using Typical Application Circuit, $V_{CC} = +2.7V$ to $+5V$, $P_{RFIN} = 0dBm$ to $+4dBm$, $f_{RFIN} = 1880MHz$ to $1930MHz$, $\overline{SHDN} = V_{CC}$, $T_A = -40^{\circ}C$ to $+85^{\circ}C$, Typical values measured at $V_{CC} = +3.2V$, $P_{RFIN} = +3dBm$, $f_{RFIN} = 1.9GHz$, $T_A = +25^{\circ}C$, unless otherwise noted. (Note 1))

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown Supply Current	$\overline{SHDN} = \text{Low}$, D0 = Low, D1 = Low, no input signal		0.5	20	μA
Input Logic Voltage High		2			V
Input Logic Voltage Low				0.8	V
Input Current	$GND \leq V_{IN} \leq V_{BIAS}$	-2		2	μA
AC ELECTRICAL CHARACTERISTICS					
Frequency Range		1880		1930	MHz
Input Power Range		0		4	dBm
Output Power	D1 = Low, D0 = Low		4		dBm
	D1 = Low, D0 = High		12		
	D1 = High, D0 = Low		18		
	$V_{CC} = 3.2V$, $P_{RFIN} = 3dBm$, $f_{RFIN} = 1.9GHz$, D1 = High, D0 = High, $T_A = +25^{\circ}C$ (Note 8)	18	20		
	D1 = High, D0 = High, $T_A = -40^{\circ}C$ to $85^{\circ}C$ (Note 1)	15.8	20	27	
Power Control Steps	D1 = Low, D0 = Low to D1 = Low, D0 = High		7		dB
	D1 = Low, D0 = High to D1 = High, D0 = Low		6		
	D1 = High, D0 = Low to D1 = High, D0 = High		2		
Harmonic Output (Note 3)			-15		dBm
Input VSWR	$R_S = 50\Omega$		1.5:1		
In-Band Spurious Noise (Note 4)	Frequency offset = $\pm 550kHz$		-22		dBc
	Frequency offset = $\pm 1.5MHz$		-40		dBm
	Frequency offset = $\pm 2.5MHz$		-60		
Power Ramp Turn-On Time (Notes 5, 8)	$\overline{SHDN} = 0$ to 1, D0 = D1 = logic-low-to-high transition			2	μs
Power Ramp Turn-Off Time (Notes 6, 8)	$\overline{SHDN} = 1$ to 0, D0 = D1 = logic-high-to-low transition			2	μs
Nonharmonic Spurious Output (Note 8)	All power levels set by D0, D1; load VSWR $\leq 3:1$; $P_{RFIN} = +4dBm$			-30	dBm
Input to Output Isolation in Shutdown			45		dB
Maximum Output VSWR Without Damage (Note 7)	All power levels set by D0, D1; any load phase angle, any duration		6:1		

Note 1: Limits are 100% production tested at $T_A = +25^{\circ}C$. Limits over the entire operating temperature range are guaranteed by design and characterization but are not production tested.

Note 2: Supply current is measured with RF power applied to the input.

Note 3: Measured with an output-matching network to minimize the 2nd and 3rd harmonics (see Applications Information section).

Note 4: Output measured in 100kHz RBW. Test signal modulation shall comply with GFSK, BT = 0.5, 1-bit/symbol, 1Mbps, frequency deviation = 175kHz.

Note 5: The total turn-on time for the PA output power to settle within 1dB of the final value.

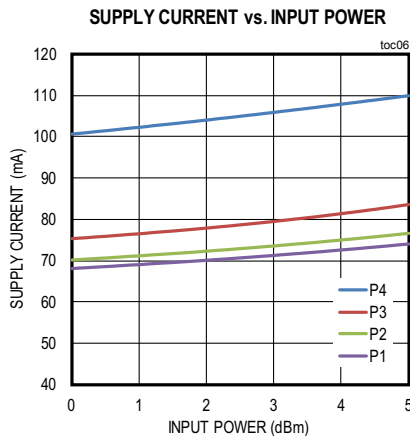
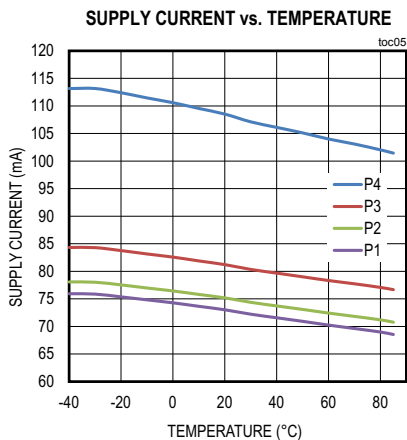
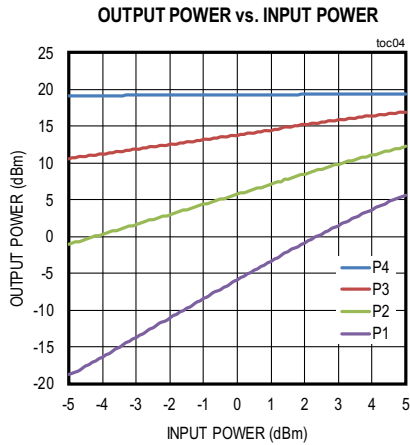
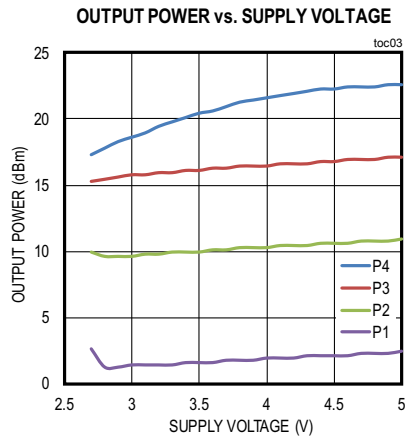
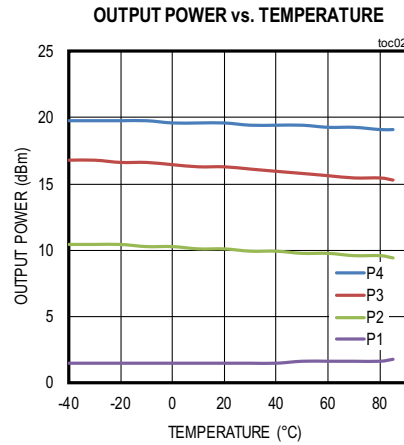
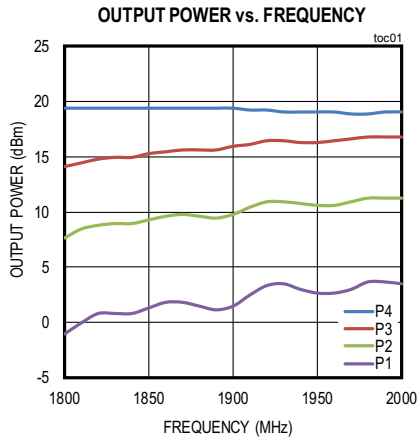
Note 6: The total turn-off time for the PA output power to drop to -10dBm.

Note 7: After removal of the load mismatch, the PA returns to operation under normal conditions.

Note 8: Guaranteed by design and characterization.

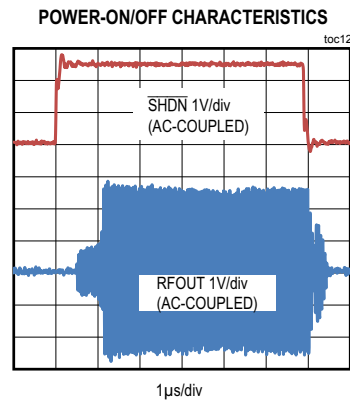
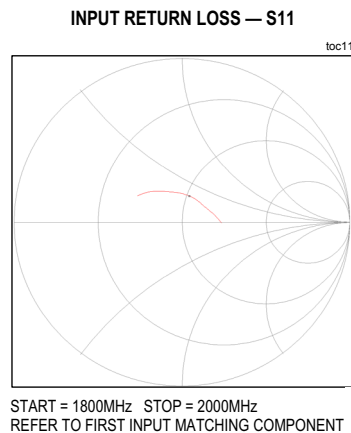
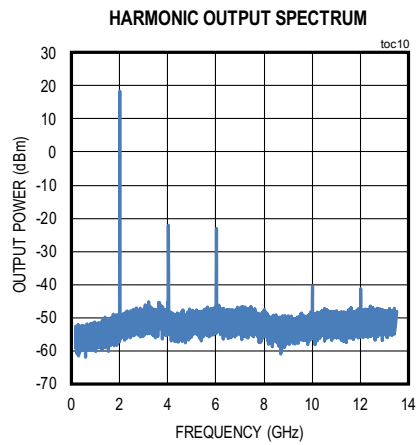
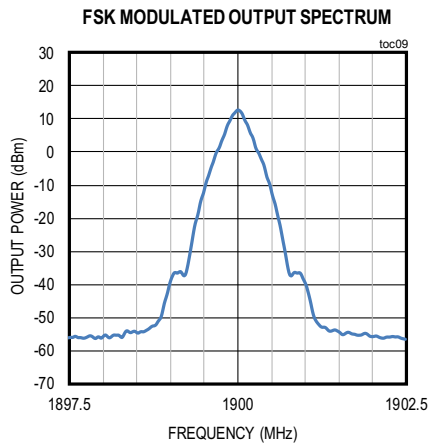
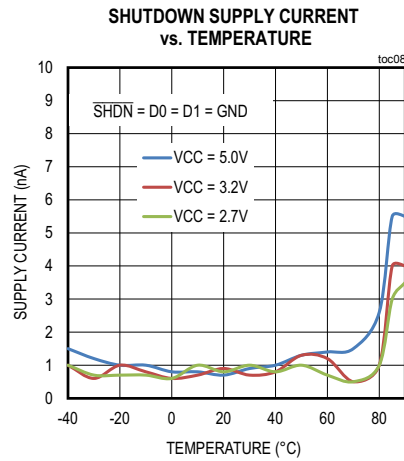
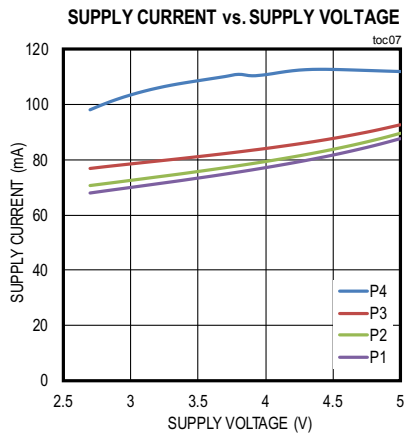
Typical Operating Characteristics

(MAX2248 EV kit, $V_{CC} = +3.2V$, $P_{RFIN} = +3dBm$, $f_{RFIN} = 1.9GHz$, $\overline{SHDN} = V_{CC}$, $T_A = +25^\circ C$, unless otherwise noted. See [Table 1](#) for power level settings P1, P2, P3, P4.)($T_A = +25^\circ C$, unless otherwise noted.)

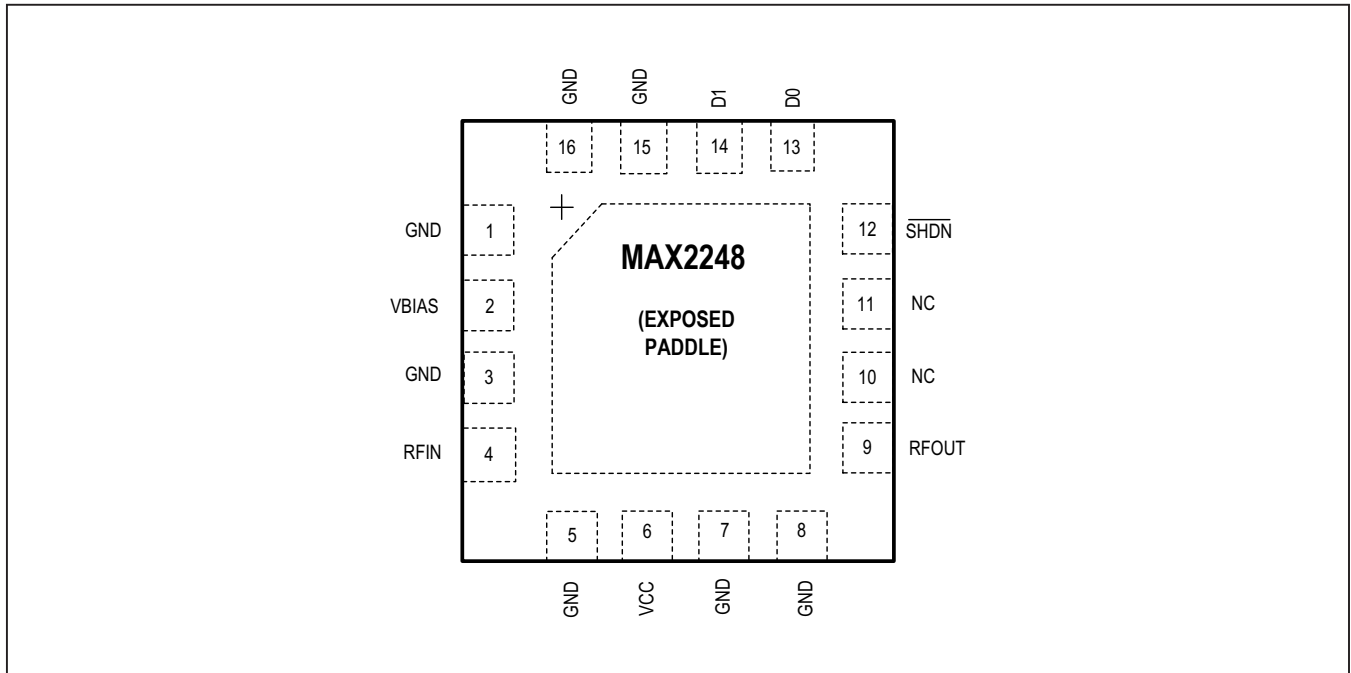


Typical Operating Characteristics (continued)

(MAX2248 EV kit, $V_{CC} = +3.2V$, $P_{RFIN} = +3dBm$, $f_{RFIN} = 1.9GHz$, $\overline{SHDN} = V_{CC}$, $T_A = +25^{\circ}C$, unless otherwise noted. See Table 1 for power level settings P1, P2, P3, P4.)($T_A = +25^{\circ}C$, unless otherwise noted.)



Pin Configuration



Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 7, 8, 15, 16	GND	Ground Pin. Requires a low-inductance/low thermal resistance path to the ground plane with multiple vias.
10, 11	N.C.	No Connection. Leave unconnected.
4	RFIN	Power Amplifier RF Input. Internally DC blocked.
2	V _{BIAS}	DC Voltage Supply for Bias and Control Circuitry. An external RF bypass capacitor to ground is required. Place capacitor as close to the pin as possible.
6	V _{CC}	DC Voltage Supply for 1st Stage. Refer to Inter-stage Match section for external component requirements.
9	RFOUT	Power Amplifier RF Output. Open-collector output requires external pullup inductor to V _{CC} . Requires an external matching network for optimum output power and efficiency.
12	SHDN	Power Amplifier Shutdown Control Input. Drive SHDN low to enable low-power shutdown mode. Drive SHDN high for normal operation.
13	D0	Digital Power Control Input (LSB) (Table 1)
14	D1	Digital Power Control Input (MSB) (Table 1)
—	EP	Exposed Paddle. Must be connected to ground.

Detailed Description

The MAX2248 PA is guaranteed to operate over a 1880MHz to 1930MHz frequency range with a +2.7V to +5V single supply. The PA provides a nominal +20dBm output power in the highest power mode setting (D0 = D1 = 1). The signal path consists of two amplifier stages: an input amplifier stage and a PA stage. A matching circuit is provided between the two stages to match their impedances. The PA also contains bias circuits that interface to external logic commands (D0, D1, and $\overline{\text{SHDN}}$) to control output power and power-up/shutdown of the amplifier. The input amplifier is a variable gain amplifier (VGA). The amplifier is AC-coupled; therefore, a DC blocking capacitor is not required at the RFIN port. The VGA gain is varied by changing the bias current through a current driver circuit. Depending on power control digital inputs D0 and D1, the current-driver circuit provides four levels of precisely controlled currents to the VGA. Each current level presents a different power level to the final amplifier stage, therefore controlling the output power. The digital power control circuit of the PA greatly simplifies control of the output power.

[Table 1](#) shows D0 and D1 digital control states, the corresponding nominal output power and the typical current consumption of the IC. The bias circuit provides separate bias voltages and currents to the amplifier stages. An

internal lowpass RC filter isolates the bias circuit from being corrupted by the RF signals. The bias circuit is optimized to minimize output power variations due to the variations in temperature, V_{CC} and RF input power. The bias circuit design also ensures the stability of the PA when connected to high VSWR loads over all power levels. A digital low at the $\overline{\text{SHDN}}$ port turns the amplifier down with a current consumption of less than 1 μ A. The MAX2248 PA requires an external match at the RFOUT port to optimize the amplifier for output power and efficiency. There are numerous ways of transforming 50 Ω to the optimum impedance. The output matching in the typical operating circuit is implemented using a series transmission line of 60 Ω and electrical length of 60°, and an open-ended shunt stub of 65 Ω and 45° in length at 1.9GHz. The shunt stub also reduces the second harmonic at the output.

Applications Information

Overview

The MAX2248 is a high-frequency power amplifier that requires a relatively small number of external components. The placement and layout of these components is critical. These components are small, low-cost, surface-mount passive elements. All transmission lines are simple microstrip structures printed on the PC board. See [Typical Application Circuit/Functional Block Diagram](#).

Table 1. Control Input Settings

DIGITAL CONTROL INPUTS			OUTPUT POWER AND SUPPLY CURRENT			
$\overline{\text{SHDN}}$	D1	D0	Power Level	P_{IN} (dBm)	P_{OUT} (dBm)	I_{CC} (mA)
0	X	X	PA OFF-	3	—	<1 μ A
1	0	0	P1	3	4	73
1	0	1	P2	3	12	76
1	1	0	P3	3	18	82
1	1	1	P4	3	20	105

X = Don't care.

Output Match

The output stage of the MAX2248 power amplifier is the collector of a transistor. The DC bias and impedance matching network are off-chip as shown in the [Typical Application Circuit/Functional Block Diagram](#). An off-chip external network, as with most PA ICs, is used to achieve higher efficiency and output power than is typically achieved using low-Q on-chip matching elements.

The primary power-matching structure is a low-pass network formed by the series transmission line section T1 and the open-stub transmission line section T2. The transmission line network acts like a series inductance and shunt capacitance. T1 and T2 are expressed as electrical lengths of a particular characteristic impedance line, but could be designed with different impedance lines. Choose the length of T2 to provide a short at the 2nd harmonic frequency of the fundamental, and significantly attenuate its amplitude at the output—1/4 wave at the 2nd harmonic frequency of 3.8GHz. The 3rd harmonic is attenuated through the clever use of the parasitic capacitance in the choke. This capacitance rolls off the choke impedance at higher frequencies and appears as a low impedance at the 3rd harmonic frequency. The output series capacitor is used as a DC-blocking capacitor and a final matching element. A value of 8pF is recommended. For proper DC biasing, the PA requires a connection to V_{CC} through an inductor, serving as a choke. Locate the inductor on the load side of transmission line T1. The recommended inductor value is 22nH. However, its value is not critical but must provide an impedance that is several hundred ohms. Choose an inductor with a self-resonant frequency at, or slightly below, 1880MHz. The inductor Q is not critical; a moderate Q (>25) is sufficient. Remember to provide sufficient current-handling capability for the inductor, in this case at least 200mA. Also, a 220pF bypass capacitor is recommended at the supply-voltage end of the inductor.

Interstage Match

The off chip network connected to pin V_{CC} , shown in the [Typical Application Circuit/Functional Block Diagram](#), forms part of the interstage match for the PA. The performance of the PA is sensitive to the impedance of this network. For best results, the trace should be a 50Ω transmission line, electrical length = 15° at 1.9GHz, and the capacitor ground connection should follow a low inductance path to IC GND.

Layout

Design the layout for the PA IC to be as compact as possible to minimize the magnitude of parasitics. Connect multiple vias from the ground plane as close to the ground pins as possible. As already described, locate the capacitors as close as possible to the IC supply voltage pin or supply end of the series inductor. Place the ground end of these capacitors near the IC GND pins to provide a low impedance return path for the signal current.

Ordering Information

PART NUMBER	TEMP RANGE	PINPACKAGE
MAX2248ETE+	-40°C to +85°C	16 TQFN
MAX2248ETE+T	-40°C to +85°C	16 TQFN

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T Denotes tape-and-reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/17	Initial release	—
1	8/17	Added bulk part number to Ordering Information table, EP information, and derated abs max power	1, 2, 4–8

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