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EVALUATION KIT
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W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

General Description

The MAX2390–MAX2393/MAX2396/MAX2400/MAX2401 (referred to as the “MAX2390 family”) fully integrated direct-conversion receiver ICs are designed for W-CDMA and TD-SCDMA applications.

The MAX2390 family of receiver ICs have over 90dB of dynamic gain control, and typical noise figure of 2.7dB referred to LNA input. Each receiver consists of an ultra-low-current low-noise amplifier (LNA) with on-chip output matching and a two-step gain control. The zero-IF demodulator has a differential circuit topology for minimum LO leakage to receiver’s input. The channel selectivity is done completely in the baseband section of the receiver with an on-chip lowpass filter. The AGC section has over 50dB of gain-control range. LO quadrature generation is done on-chip through a divide-by-2 prescaler. The DC offset cancellation in the I/Q baseband channels is done fully on-chip using a DC servo loop. To quickly correct for large DC offset transients in minimal time, very fast settling time is obtained by optimization of the DC-offset-cancellation circuit’s time constant.

The MAX2390 family includes a 3-wire serial bus for configuring the different receiver modes. They also include a SHDN pin for full device shutdown. The receivers are fabricated using an advanced high-frequency SiGe BiCMOS process. The ICs operate from a single +2.7V to +3.3V supply and are housed in a small 28-pin leadless QFN-EP and thin QFN-EP packages (5mm x 5mm).

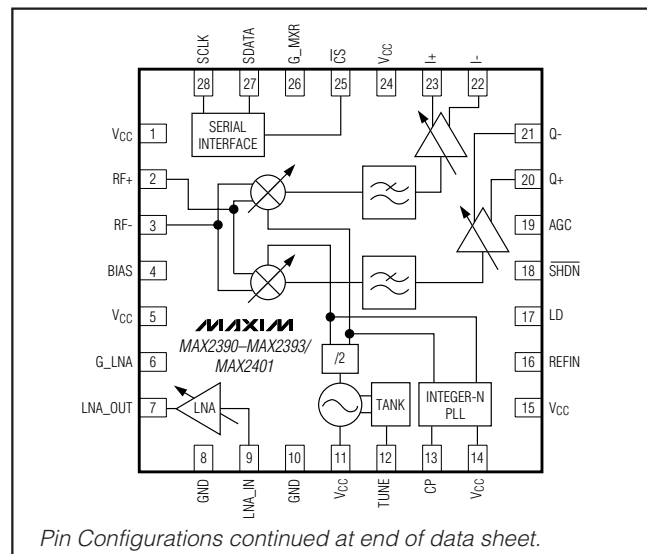
Applications

IMT2000 Handsets	TD-SCDMA Handsets
UMTS Handsets	W-CDMA TDD Handsets
W-CDMA Band II (PCS) Handsets	W-CDMA Band III (DCS) Handsets

Features

- ◆ Fully Monolithic Direct-Conversion Receivers
- ◆ Eliminate External IF SAW + IF AGC + I/Q Demod
- ◆ Meet all 3GPP Receiver’s Standard Requirements with at Least 3dB Margin on Eb/No
- ◆ Operate from a +2.7V to +3.3V Single Supply
- ◆ Over 90dB of RF+ Baseband Gain-Control Range
- ◆ Channel Selectivity Over 40dB
- ◆ Receiver Current Consumption \approx 32mA
- ◆ On-Chip DC Offset Cancellation
- ◆ Compatible with Various CMOS Logic Levels

Pin Configurations/ Functional Diagrams



Ordering Information/Selector Guide

PART	TEMP RANGE	PIN-PACKAGE	APPLICATION	CHIP RATE (Mcps)	RF BAND (MHz)	SYNTHESIZER
MAX2390ETI	-40°C to +85°C	28 Thin QFN-EP*	W-CDMA Band II	3.84	1930 to 1990	On-Chip
MAX2391ETI	-40°C to +85°C	28 Thin QFN-EP*	IMT2000/UMTS	3.84	2110 to 2170	On-Chip
MAX2391ETI+	-40°C to +85°C	28 Thin QFN-EP*	IMT2000/UMTS	3.84	2110 to 2170	On-Chip
MAX2392ETI	-40°C to +85°C	28 Thin QFN-EP*	TD-SCDMA	1.28	2010 to 2025	On-Chip
MAX2392ETI+	-40°C to +85°C	28 Thin QFN-EP*	TD-SCDMA	1.28	2010 to 2025	On-Chip
MAX2393EGI	-40°C to +85°C	28 QFN-EP*	W-TDD/TD-SCDMA	3.84 or 1.28	1900 to 1920	On-Chip
MAX2396EGI	-40°C to +85°C	28 QFN-EP*	IMT2000/UMTS	3.84	2110 to 2170	External
MAX2400ETI	-40°C to +85°C	28 Thin QFN-EP*	W-CDMA Band II	3.84	1930 to 1990	External
MAX2401ETI	-40°C to +85°C	28 Thin QFN-EP*	W-CDMA Band III	3.84	1805 to 1880	On-Chip
MAX2401ETI+	-40°C to +85°C	28 Thin QFN-EP*	W-CDMA Band III	2.84	1805 to 1880	On-Chip

*EP = Exposed paddle. + Denotes lead-free package.



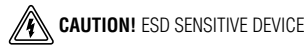
For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim’s website at www.maxim-ic.com.

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND-0.3V to +3.6V
 All Other Pins to GND-0.3V to (V_{CC} + 0.3V)
 LNA_IN+15dBm
 Digital Input Current±10mA
 Digital Output Open-Collector Current1mA
 Continuous Power Dissipation (T_A = +70°C)
 28-Pin QFN (derate 20.8mW/°C above +70°C)1666.7mW

Operating Temperature Range-40°C to +85°C
 Junction Temperature+150°C
 Storage Temperature Range-65°C to +160°C
 Lead Temperature (soldering, 10s)+300°C



Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7V to 3.3V, V_{SHDN} = V_{DH} (Note 1), G_{LNA} = G_{MXR} = V_{IH}, HGML mode (see Table 6), no RF input signals, RF input and output ports are terminated into 50Ω, baseband I and Q outputs loaded with 10kΩ || 5pF, V_{AGC} = 2.2V, T_A = -40°C to +85°C. Typical values are for V_{CC} = 2.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Supply Voltage	V _{CC}		2.7	2.8	3.3	V	
Operating Supply Current	I _{CC}	MAX2391, MAX2392, MAX2393, MAX2400	HGML mode		33	39	mA
			HGHL mode		34	40	
			LG mode		29	35	
			IDLE mode		11.5	13	
		MAX2396	HGML mode		31	38	
			LG mode		27	34	
			IDLE mode		10.5	12	
		MAX2390, MAX2401	HGML mode		35	42	
			HGHL mode		36	43	
			LG mode		31	37	
IDLE mode			12	14			
All versions	SHDN mode		0.5	15	μA		
Gain-Control Input Bias Current	I _{AGC}	0.3V ≤ V _{AGC} ≤ 2.4V	-10		+10	μA	
		V _{AGC} ≤ 0.3V; V _{SHDN} = V _{DL}			3		
Common-Mode Output Voltage at I and Q Outputs	V _{CM}	V _{I(CM)} = (V _{I+} + V _{I-}) / 2, V _{Q(CM)} = (V _{Q+} + V _{Q-}) / 2	(V _{CM} = 0 in OPCTRL register)	1.10	1.20	1.30	V
			(V _{CM} = 1 in OPCTRL register)	1.30	1.42	1.55	
Lock Indicator High Leakage Current		PLL locked, V _{LD} = V _{CC} (MAX2390-MAX2393, MAX2401)			0.1	μA	
Lock Indicator Low Sink Voltage		Sinking 100μA, PLL unlocked (MAX2390-MAX2393, MAX2401)			0.4	V	
SHDN Input-Logic High	V _{DH}	MAX2390-MAX2393, MAX2401	1.5		V _{CC}	V	
		MAX2396/MAX2400	V _{CC} - 0.5		V _{CC}		
SHDN Input-Logic Low	V _{DL}		0		0.5	V	
SHDN Input Resistance		Resistance to GND	50			kΩ	

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

MAX2390-MAX2393/MAX2396/MAX2400/MAX2401

DC ELECTRICAL CHARACTERISTICS (continued)

($V_{CC} = 2.7V$ to $3.3V$, $V_{SHDN} = V_{DH}$ (Note 1), $G_{LNA} = G_{MXR} = V_{IH}$, HGML mode (see Table 6), no RF input signals, RF input and output ports are terminated into 50Ω , baseband I and Q outputs loaded with $10k\Omega$ || $5pF$, $V_{AGC} = 2.2V$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are for $V_{CC} = 2.8V$, $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IDLE Input-Logic High	V_{IH}	MAX2396, MAX2400 only	$V_{CC} - 0.5$		V_{CC}	V
IDLE Input-Logic Low	V_{IL}		0		0.5	V
IDLE Input Resistance			Resistance to GND	50		
Digital Input-Logic High	V_{IH}	\overline{CS} , SDATA, SCLK, G_{MXR} , G_{LNA} (Note 1)	0.7 × V_{DH} or 1.2V, whichever is greater		V_{CC}	V
Digital Input-Logic Low	V_{IL}		0	0.3 × V_{DH}		
Input-Logic High Current	I_{IH}				1	μA
Input-Logic Low Current	I_{IL}			-1		μA

AC ELECTRICAL CHARACTERISTICS

(Devices tested on their respective evaluation kits (EV kits); LNA input port is driven with a 50Ω source; LNA output port is terminated with 50Ω load, mixer differential input port is driven through a 1:4 impedance balun with a 50Ω source; baseband I/Q output differential load = $10k\Omega$ || $5pF$; reference oscillator input: 19.2MHz (MAX2390/MAX2391/MAX2392/MAX2393), 26MHz (MAX2401), 15.36MHz (MAX2396/MAX2400); AGC is set to result in a 0.3V_{p-p} differential output-voltage swing at the baseband I/Q output; registers set to power-up defaults (Table 2); $T_A = -40^\circ C$ to $+85^\circ C$. Typical values are for $V_{CC} = 2.8V$ and $T_A = +25^\circ C$, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LNA PERFORMANCE						
RF Frequency Range (Note 2)	f_{RF}	MAX2391/MAX2396	2110	2140	2170	MHz
		MAX2392	2010	2017	2025	
		MAX2393	1900	1910	1920	
		MAX2390/MAX2400	1930	1960	1990	
		MAX2401	1805	1842	1880	
Signal Phase Change	$\Delta\phi$	Switching between any of the LNA modes		8		Degrees
LNA HIGH GAIN ("HGLNA", $G_{LNA} = V_{IH}$)						
Power Gain	G_{LNA}	(Note 3)	13	16	18	dB
Noise Figure	NF_{LNA}	(Note 3)		1.5	2.0	dB
Input -1dB Compression Point	IP-1dB	(Note 3)	-20	-16		dBm
3rd-Order Input Intercept Point (Note 4)	IIP3 _{LNA}	MAX2391/MAX2396	-4.5	-2.5		dBm
		MAX2392/MAX2393	-6	-4		
		MAX2390/MAX2400/MAX2401	-7	-4		
Input Return Loss	dB[S11]	On EV kit, externally matched to 50Ω		-14		dB
Output Return Loss	dB[S22]	On EV kit, internally matched to 50Ω		-14		dB
Reverse Isolation	dB[S12]	On EV kit		-35		dB
LNA LOW GAIN ($G_{LNA} = V_{IL}$)						
Power Gain	G_{LNA}	(Note 3)	-12	-8.0	-5	dB
Noise Figure	NF_{LNA}	(Note 3)		18	22	dB
Input -1dB Compression Point	IP-1dB	(Note 3)	-6	-3		dBm

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

AC ELECTRICAL CHARACTERISTICS (continued)

(Devices tested on their respective evaluation kits (EV kits); LNA input port is driven with a 50Ω source; LNA output port is terminated with 50Ω load, mixer differential input port is driven through a 1:4 impedance balun with a 50Ω source; baseband I/Q output differential load = 10kΩ || 5pF; reference oscillator input: 19.2MHz (MAX2390/MAX2391/MAX2392/MAX2393), 26MHz (MAX2401), 15.36MHz (MAX2396/MAX2400); AGC is set to result in a 0.3V_{P-P} differential output-voltage swing at the baseband I/Q output; registers set to power-up defaults (Table 2); T_A = -40°C to +85°C. Typical values are for V_{CC} = 2.8V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
Input Return Loss	dB[S11]	On EV kit, externally matched to 50Ω		-11		dB	
Output Return Loss	dB[S22]	On EV kit, internally matched to 50Ω		-11		dB	
Reverse Isolation	dB[S12]	On EV kit		-30		dB	
ZERO-IF DEMODULATOR PERFORMANCE (RF+/RF- TO BASEBAND I AND Q OUTPUTS)							
Voltage Gain (Note 5)	AV	HGML mode, V _{AGC} = 2.2V	80	86		dB	
		MG or LG mode, V _{AGC} = 2.2V	68	76			
Baseband Gain-Control Range	ΔAV	V _{AGC} = 0.3V to 2.4V (Note 3)	53	60		dB	
Baseband Gain-Control Slope	dAV/dV	V _{AGC} = 0.3V to 2.4V (Note 3)	25	29	33	dB/V	
DSB Noise Figure (Notes 3, 6)	NF	HGML or HGHL mode, V _{AGC} ≥ 1.8V	MAX2391/MAX2392/ MAX2393/MAX2396		10.5	14	dB
			MAX2390/MAX2400/ MAX2401		9.5	13	
		MG or LG mode, V _{AGC} ≥ 1.8V			18.5	25	
3rd-Order Input Intercept Point	IIP3	HGML mode, V _{AGC} = 2.2V (Note 7)		-5	-1	dBm	
		HGHL mode, V _{AGC} = 2.2V (Note 3, 7)		-3.5	0		
		MAX2390/MAX2400/MAX2401 HGML or HGHL mode (Note 8)			-16		
Input -1dB Compression Point	I _{P-1dB}	LG mode, V _{AGC} = 0.5V			-23	dBm	
-1dB Output Compression Differential Voltage	O _{V-1dB}	All modes (Note 3)	V _{AGC} ≥ 1.3V		1.0	1.5	V _{P-P}
			V _{AGC} = 0.5V		0.6	1.0	
2nd-Order Input Intercept Point	IIP2	(MAX2391/MAX2396) 190MHz offset; all modes, V _{AGC} ≥ 0.5V (Note 9)			+34	dBm	
		(MAX2390/MAX2400) 80MHz offset; all modes, V _{AGC} ≥ 0.5V (Note 9)			+33		
		(MAX2401) 95MHz offset; all modes, V _{AGC} ≥ 0.5V (Note 9)			+33		
		V _{AGC} = 2.2V, HGML mode (Note 10)	(MAX2390/MAX2391/ MAX2393/MAX2396/ MAX2400/MAX2401) 15MHz offset		+25		+33
(MAX2392) 4.8MHz offset			+25	+33			
LO Leakage	X _{LO}	At LNA_IN, HGML mode, RX band (Note 3)		-100	-95	dBm	
I/Q Gain Imbalance	ΔG _{I/Q}	All modes, V _{AGC} = 0.5V to 2.2V		0.2	1.5	dB	

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

AC ELECTRICAL CHARACTERISTICS (continued)

(Devices tested on their respective evaluation kits (EV kits); LNA input port is driven with a 50Ω source; LNA output port is terminated with 50Ω load, mixer differential input port is driven through a 1:4 impedance balun with a 50Ω source; baseband I/Q output differential load = 10kΩ || 5pF; reference oscillator input: 19.2MHz (MAX2390/MAX2391/MAX2392/MAX2393), 26MHz (MAX2401), 15.36MHz (MAX2396/MAX2400); AGC is set to result in a 0.3V_{p-p} differential output-voltage swing at the baseband I/Q output; registers set to power-up defaults (Table 2); T_A = -40°C to +85°C. Typical values are for V_{CC} = 2.8V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/Q Quadrature Phase Imbalance	$ \Delta\Phi_{I/Q} $	All modes, V _{AGC} = 0.5V to 2.2V			4	Degrees
Error Vector Magnitude (Note 11)	EVM	MAX2391/MAX2392/MAX2393/MAX2396		15		%
		MAX2390/MAX2400/MAX2401		17		
Differential DC Offset at I/Q Baseband Output	ΔDC	Including DC servo loop; V _{AGC} = 2.2V			±25	mV
BASEBAND CHANNEL RESPONSE (W-CDMA); MAX2391/MAX2393/MAX2396						
-3dB Lowpass Corner Frequency	f _{-3dB}			2.4		MHz
Filter Attenuation Relative to 180kHz	A _{dB}	At 5MHz offset	51	58		dB
		At 10MHz offset	59	67		
		At 15MHz offset	64	75		
Passband Gain Flatness	ΔA _{dB}	100kHz to 1.92MHz (Note 3)		1.2	1.7	dB
BASEBAND CHANNEL RESPONSE (W-CDMA); MAX2390/MAX2400/MAX2401						
-3dB Lowpass Corner Frequency	f _{-3dB}	MAX2390/MAX2400		2.1		MHz
		MAX2401		2.2		
Filter Attenuation Relative to 180kHz	A _{dB}	At 2.7MHz offset, MAX2390/MAX2400	36	56	50	56
		At 2.8MHz offset, MAX2401				
		At 3.5MHz offset, MAX2390/MAX2400				
		At 3.6MHz offset, MAX2401				
		At 5MHz offset	57	65		
At 15MHz offset	65	75				
Passband Gain Flatness	ΔA _{dB}	100kHz to 1.92MHz (Note 3)		1.9	2.5	dB
BASEBAND CHANNEL RESPONSE (TD-SCDMA); MAX2392/MAX2393						
-3dB Lowpass Corner Frequency	f _{-3dB}			0.75		MHz
Filter Attenuation Relative to 180kHz	A _{dB}	At 1.6MHz offset	51	57		dB
		At 3.2MHz offset	56	65		
		At 6.4MHz offset	64	76		
Passband Gain Flatness	ΔA _{dB}	50kHz to 0.64MHz (Note 3)		1.2	1.7	dB

MAX2390-MAX2393/MAX2396/MAX2400/MAX2401

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

AC ELECTRICAL CHARACTERISTICS (continued)

(Devices tested on their respective evaluation kits (EV kits); LNA input port is driven with a 50Ω source; LNA output port is terminated with 50Ω load, mixer differential input port is driven through a 1:4 impedance balun with a 50Ω source; baseband I/Q output differential load = 10kΩ || 5pF; reference oscillator input: 19.2MHz (MAX2390/MAX2391/MAX2392/MAX2393), 26MHz (MAX2401), 15.36MHz (MAX2396/MAX2400); AGC is set to result in a 0.3V_{P-P} differential output-voltage swing at the baseband I/Q output; registers set to power-up defaults (Table 2); T_A = -40°C to +85°C. Typical values are for V_{CC} = 2.8V and T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	
ON-CHIP VCO							
VCO Frequency (VCO Range is 2x the LO Range)	f _{OSC}	MAX2391/MAX2396	4220		4340	MHz	
		MAX2392	4020		4050		
		MAX2393	3800		3840		
		MAX2390/MAX2400	3860		3980		
		MAX2401	3610		3760		
Phase Noise	Φ _N	At 10MHz offset; locked (Note 3)		-139	-133	dBc/Hz	
Pulling		From IDLE mode to ON mode (Note 3)		0.5	1	MHz _{P-P}	
Pushing		V _{CC} stepped 3.3V to 2.7V (Note 3)			13	MHz/V	
VCO INTERFACE TO EXTERNAL SYNTHESIZER (MAX2396/MAX2400)							
VCO Tuning Gain	K _{VCO}	Referred to the VCO frequency (2x RFLO)	MAX2396	130		300	MHz/V
			MAX2400	100		270	
VCO Output Frequency		Output to synthesizer is f _{VCO} / 3 = 2f _{RFLO} / 3	MAX2396	1406.67	1426.67	1446.67	MHz
			MAX2400	1286.67	1306.67	1326.67	
VCO Output Differential Voltage		(Note 12)	180			mV _{P-P}	
VCO Tuning Voltage Range	V _{TUNE}		0.4		2.3	V	
INTEGER-N RF SYNTHESIZER (MAX2390-MAX2393, MAX2401)							
Main PLL Integer Division Ratio		15-bit register (64/65 dual-modulus prescaler), f _{COMP} = 200kHz	4032	10700	32767		
Reference Frequency Range	f _{REF}		10	19.2	40	MHz	
REFDIV Reference-Divider Ratio		9-bit register	16	96	511		
Charge-Pump Output Current (Sink or Source)	I _{CP}	CONFIG:CP1 = 1, CONFIG:CP0 = 1, V _{CPOUT} = V _{CC} / 2	2.0	2.5	3.0	mA	
Charge-Pump Leakage Current	I _{L_CP}				10	nA	
SYSTEM TIMING							
Turn-On Time Including DC Offset Cancellation	t _{ON}	From IDLE mode to ON mode VGA set to maximum gain with -40dBm signal at demodulator input (Note 3)		30	60	μs	
3-WIRE SERIAL INTERFACE TIMING							
Data to Clock Setup	t _{CS}	Per timing diagram	20			ns	
Data to Clock Hold Time	t _{CH}	Per timing diagram	10			ns	
Clock Pulse-Width High	t _{CWH}	Per timing diagram	20			ns	
Clock Pulse-Width Low	t _{CWL}	Per timing diagram	20			ns	
Clock to Load Enable/Setup Time	t _{ES}	Per timing diagram	20			ns	
Clock Frequency					20	MHz	

Note 1: Logic thresholds track V_{SHDN}. This allows the digital interface to operate with logic levels from 1.2V to V_{CC}.

Note 2: All min and max specifications are measured over this frequency range.

Note 3: Guaranteed by design and characterization.

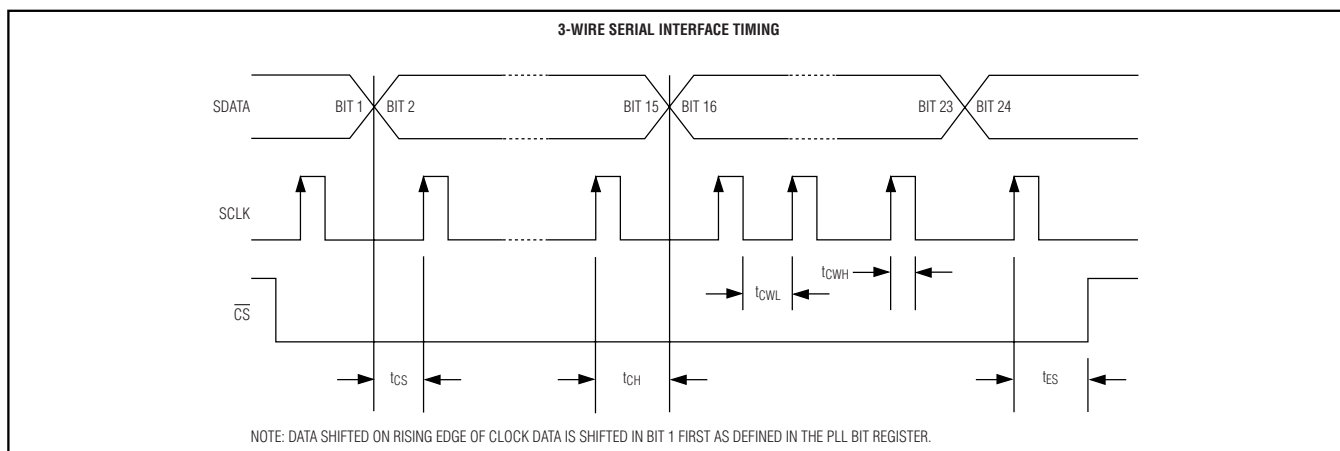
W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

AC ELECTRICAL CHARACTERISTICS (continued)

(Devices tested on their respective evaluation kits (EV kits); LNA input port is driven with a 50Ω source; LNA output port is terminated with 50Ω load, mixer differential input port is driven through a 1:4 impedance balun with a 50Ω source; baseband I/Q output differential load = 10kΩ || 5pF; reference oscillator input: 19.2MHz (MAX2390/MAX2391/MAX2392/MAX2393), 26MHz (MAX2401), 15.36MHz (MAX2396/MAX2400); AGC is set to result in a 0.3V_{p-p} differential output-voltage swing at the baseband I/Q output; registers set to power-up defaults (Table 2); T_A = -40°C to +85°C. Typical values are for V_{CC} = 2.8V and T_A = +25°C, unless otherwise noted.)

- Note 4:** MAX2391/MAX2396: tones at 2025.0MHz and 1930.0MHz (-28dBm/tone); receiver tuned for input RF of 2120.0MHz.
MAX2392: tones at 2020.6MHz and 2023.8MHz (-35dBm/tone); receiver tuned for input RF of 2017.4MHz.
MAX2393: tones at 1910.0MHz and 1920.0MHz (-35dBm/tone); receiver tuned for input RF of 1900.0MHz.
MAX2390/MAX2400: tones at 1963.5MHz and 1965.9MHz (-35dBm/tone); receiver tuned for input RF of 1960.0MHz.
MAX2401: tones at 1846MHz and 1848.4MHz (-35dBm/tone); receiver tuned for input RF of 1842.4MHz.
- Note 5:** Voltage gain defined as the differential baseband RMS I or Q output voltage, measured across the 10kΩ load, divided by the RMS differential input voltage at RF+/RF-.
- Note 6:** NF is constant or flattens out for AGC voltage ≥1.75V.
- Note 7:** MAX2391/MAX2396: tones at 2150.0MHz and 2160.18MHz (-35dBm/tone); receiver tuned for input RF of 2140MHz.
MAX2392: tones at 2020.6MHz and 2023.98MHz (-35dBm/tone); receiver tuned for input RF of 2017.4MHz.
MAX2393: tones at 1910.0MHz and 1919.82MHz (-35dBm/tone); receiver tuned for input RF of 1900.0MHz.
MAX2390/MAX2400: tones at 1970.0MHz and 1980.18MHz (-35dBm/tone); receiver tuned for input RF of 1960.0MHz.
MAX2401: tones at 1852.4MHz and 1862.58MHz (-35dBm/tone); receiver tuned for input RF of 1842.4MHz.
Measure IM3 product at 180kHz.
- Note 8:** MAX2390/MAX2400: tones at 1963.5MHz and 1965.9MHz (-35dBm/tone); receiver tuned for input RF of 1960.0MHz, IM3 at 1.1MHz baseband.
MAX2401: tones at 1846MHz and 1848.4MHz (-35dBm/tone); receiver tuned for input RF of 1842.4MHz. IM3 at 1.2 MHz baseband.
- Note 9:** MAX2391/MAX2396: tones at 1950.0MHz and 1950.18MHz (-35dBm/tone); receiver tuned for input RF of 2140MHz.
MAX2390/MAX2400: tones at 1880.0MHz and 1880.18MHz (-35dBm/tone); receiver tuned for input RF of 1960.0MHz.
MAX2401: tones at 1747.4MHz and 1747.58MHz (-35dBm/tone); receiver tuned for input RF of 1842.4MHz.
Measure IM2 product at 180kHz.
- Note 10:** MAX2391/MAX2396: tones at 2155.0MHz and 2155.18MHz (-35dBm/tone); receiver tuned for input RF of 2140MHz.
MAX2392: tones at 2022.2MHz and 2022.38MHz (-35dBm/tone); receiver tuned for input RF of 2017.4MHz.
MAX2393: tones at 1915.0MHz and 1915.18MHz (-35dBm/tone); receiver tuned for input RF of 1900.0MHz.
MAX2390/MAX2400: tones at 1975.0MHz and 1975.18MHz (-35dBm/tone); receiver tuned for input RF of 1960.0MHz.
MAX2401: tones at 1857.4MHz and 1857.58MHz (-35dBm/tone); receiver tuned for input RF of 1842.4MHz.
Measure IM2 product at 180kHz.
- Note 11:** The receiver is tested using the DL reference measurement channel (12.2kbps) as specified in subclause C.3.1 in the 3GPP 25.101 standard document.
- Note 12:** I/Q differential output load impedance is 5kΩ minimum (10kΩ typical) in parallel with 5pF.

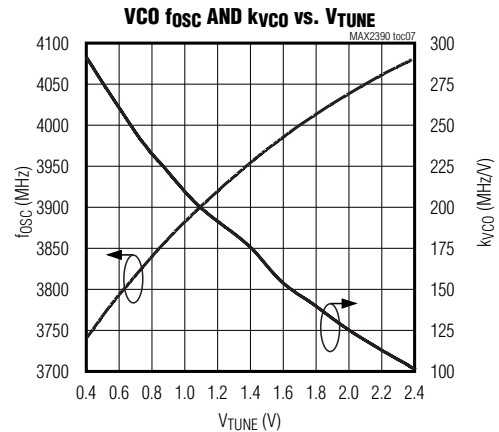
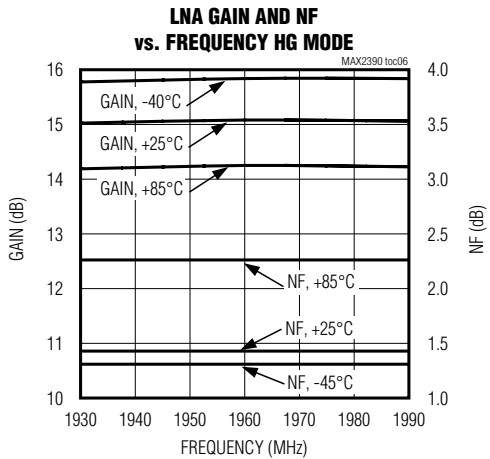
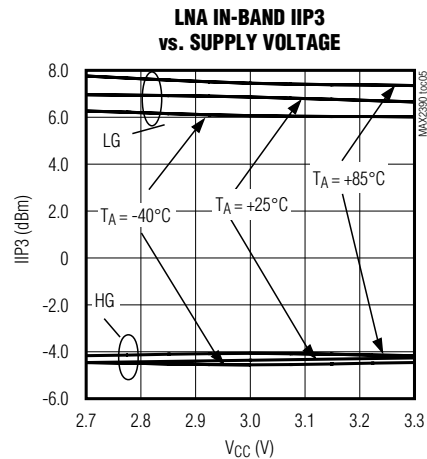
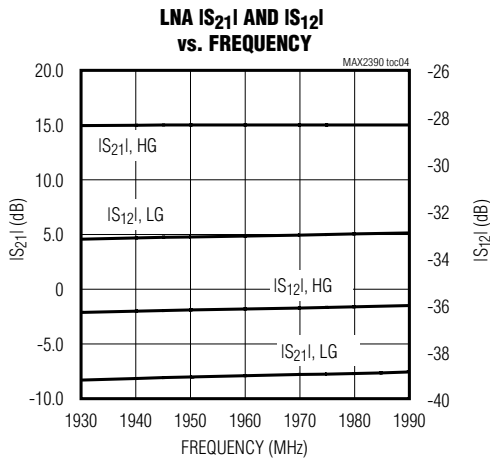
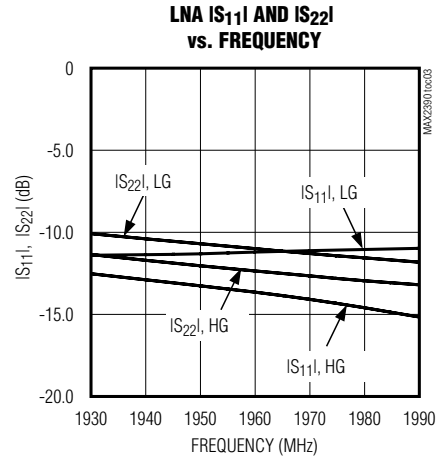
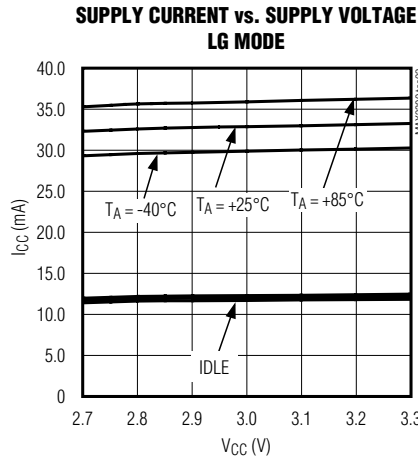
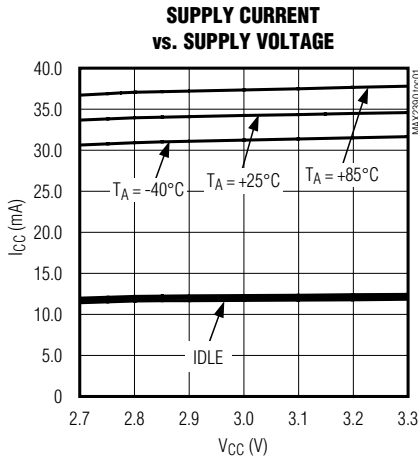
Timing Diagram



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

MAX2390 Typical Operating Characteristics

(MAX2390 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1960MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

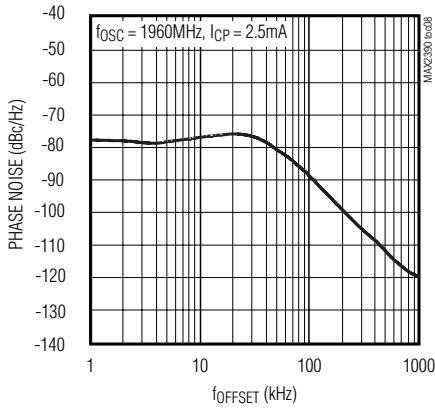


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

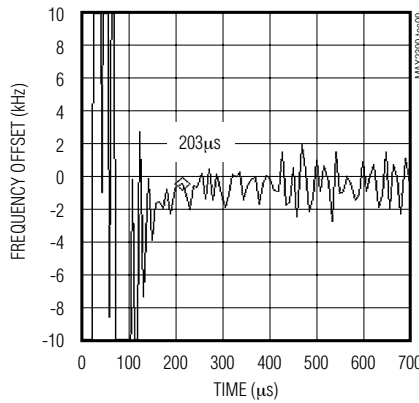
MAX2390 Typical Operating Characteristics (continued)

(MAX2390 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1960MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

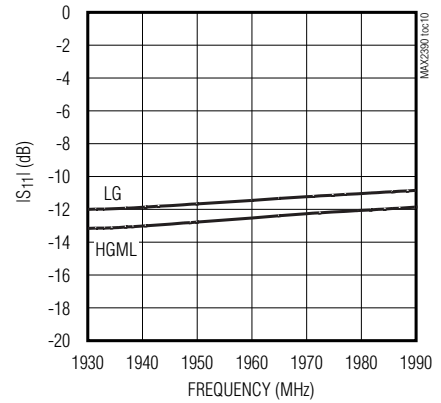
SYNTHESIZER CLOSED-LOOP PHASE NOISE



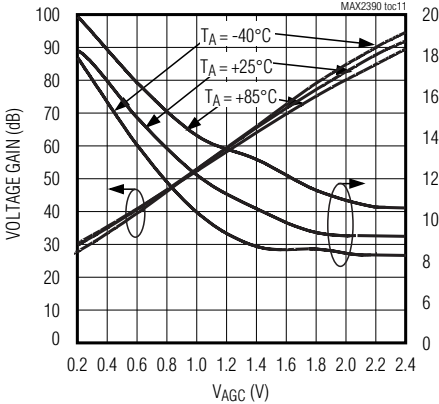
PLL SETTLING TIME 60MHz STEP



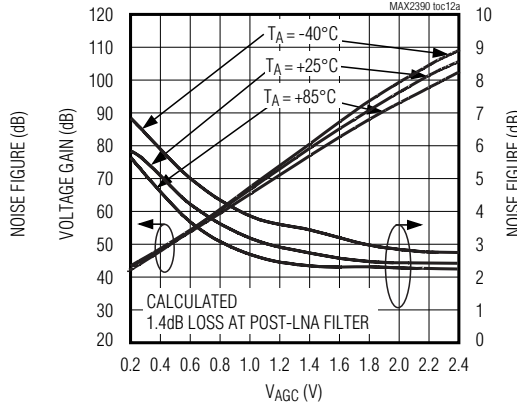
DEMODULATOR IS₁₁ vs. FREQUENCY



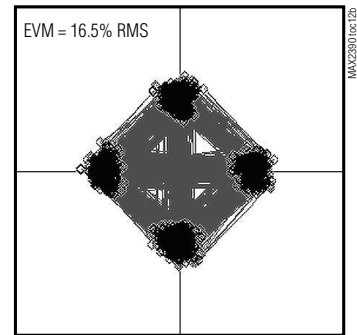
DEMODULATOR GAIN AND NF vs. V_{AGC}



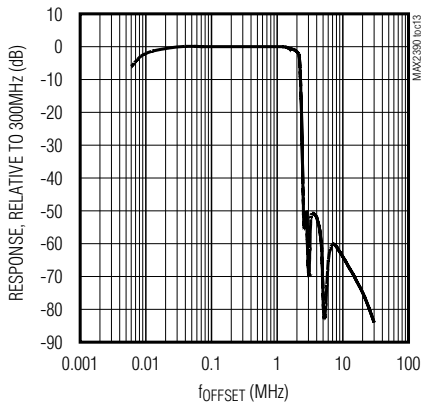
CASCADED GAIN AND NF vs. V_{AGC}



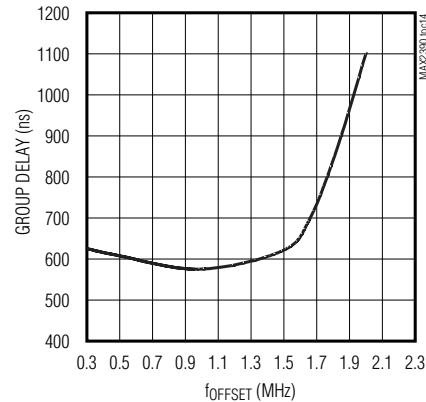
**COMPOSITE EVM
W-CDMA: PCCPCH + SCH**



BASEBAND CHANNEL RESPONSE vs. FREQUENCY



BASEBAND CHANNEL GROUP DELAY vs. FREQUENCY

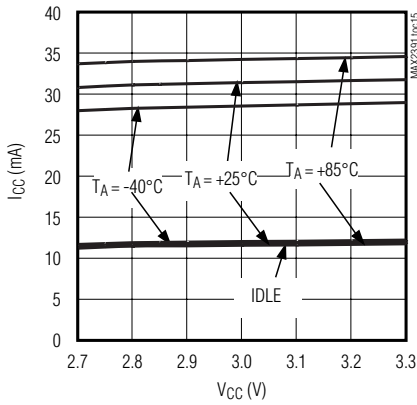


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

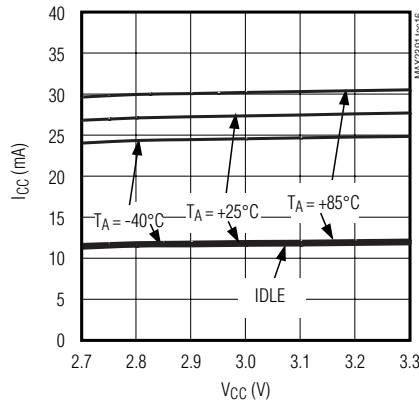
MAX2391 Typical Operating Characteristics

(MAX2391 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 2140MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

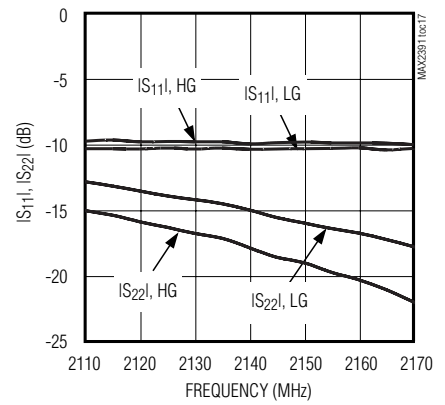
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
HGML MODE**



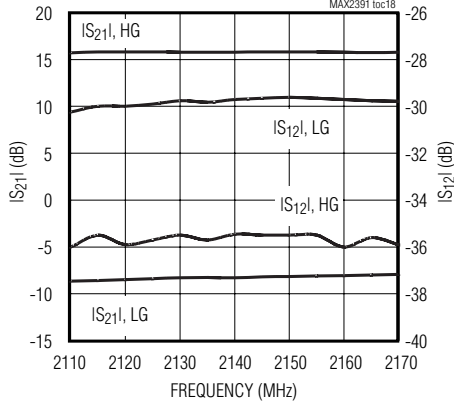
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
LG MODE**



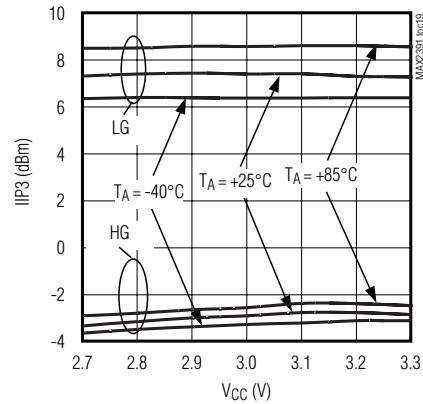
LNA IS11 AND IS22 vs. FREQUENCY



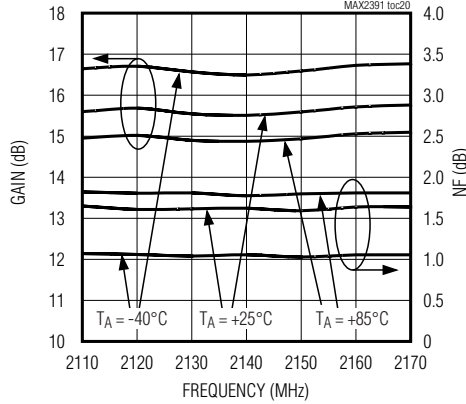
LNA IS21 AND IS12 vs. FREQUENCY



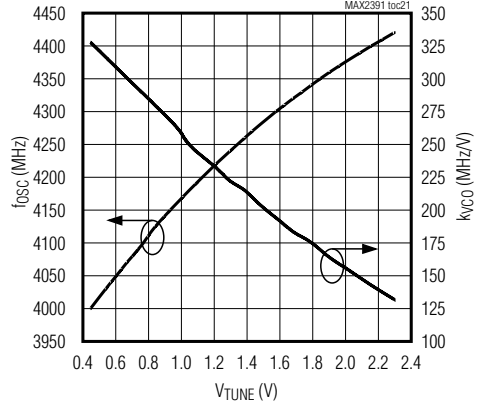
LNA IN-BAND IIP3 vs. SUPPLY VOLTAGE



LNA GAIN (HG MODE) AND NF vs. FREQUENCY



VCO fosc vs. VTUNE

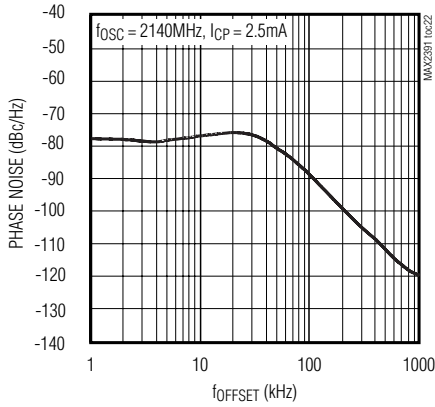


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

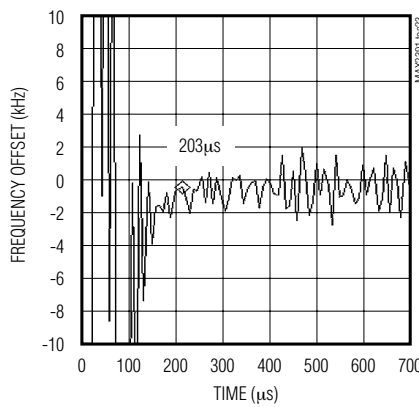
MAX2391 Typical Operating Characteristics (continued)

(MAX2391 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 2140MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

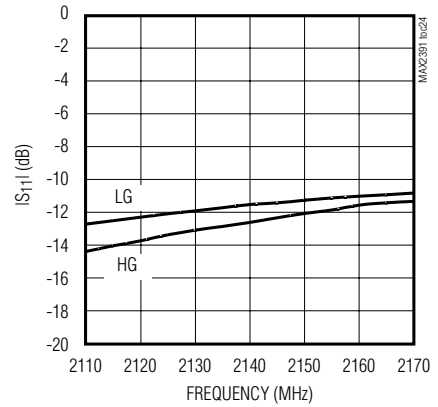
SYNTHESIZER CLOSED-LOOP PHASE NOISE



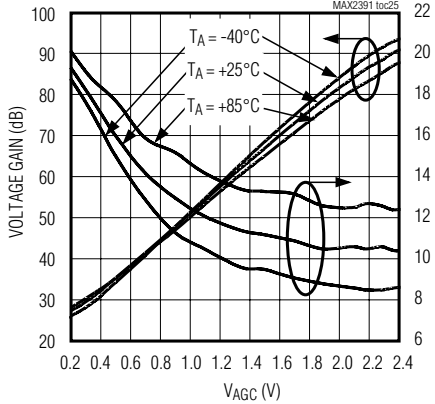
PLL SETTLING TIME 60MHz STEP



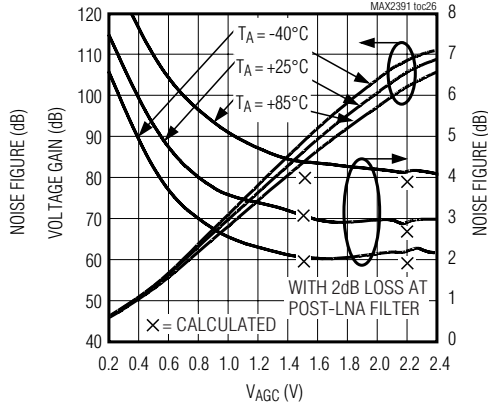
DEMODULATOR $|S_{11}|$ vs. FREQUENCY



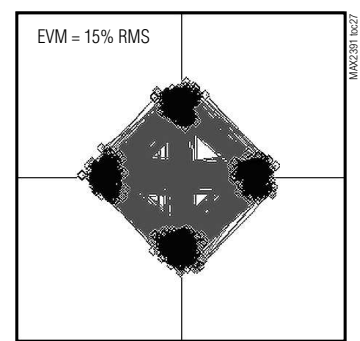
DEMODULATOR GAIN (HGML MODE) AND NF vs. V_{AGC}



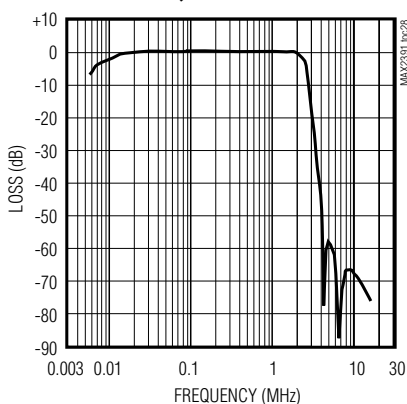
CASCADED GAIN (HGML MODE) AND NF vs. V_{AGC}



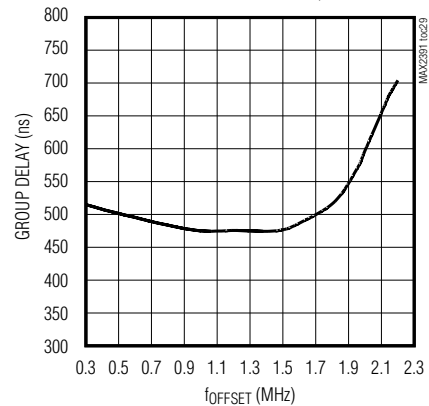
COMPOSITE EVM W-CDMA: PCCPCH + SCH



BASEBAND CHANNEL FREQUENCY RESPONSE



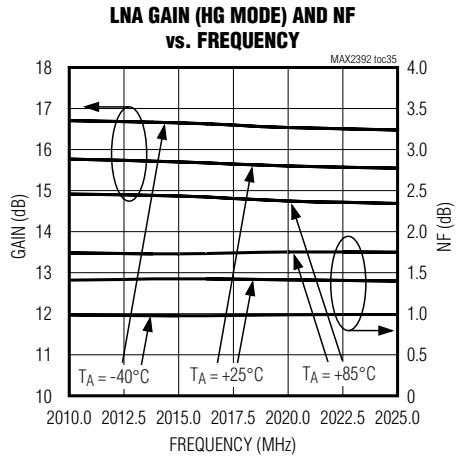
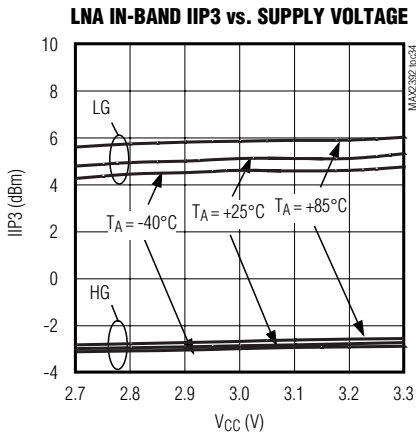
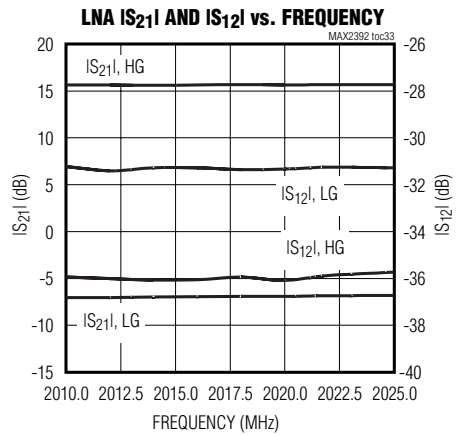
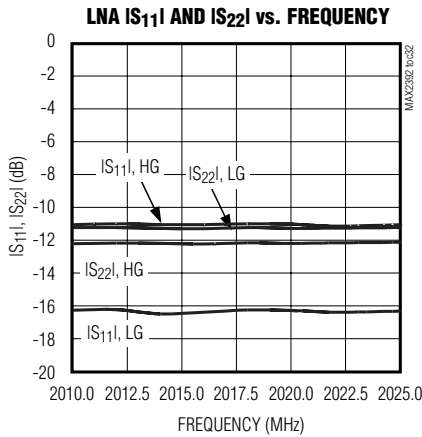
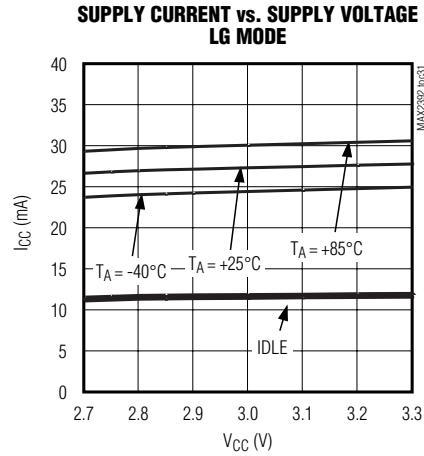
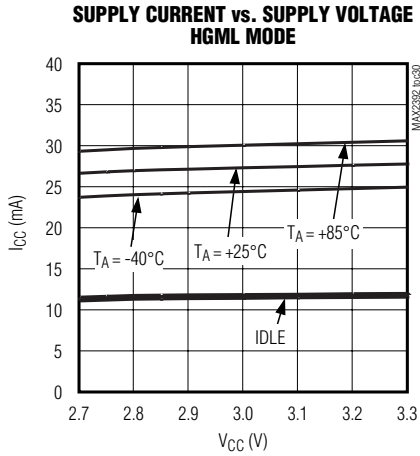
BASEBAND CHANNEL GROUP DELAY vs. FREQUENCY



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

MAX2392 Typical Operating Characteristics

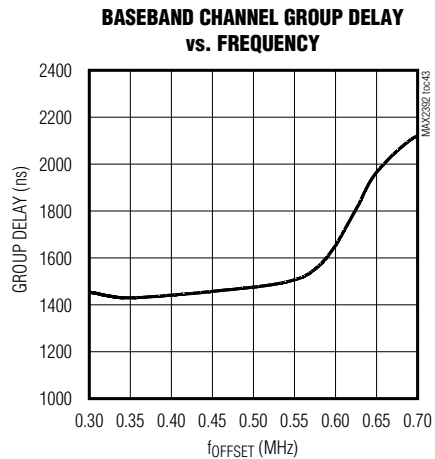
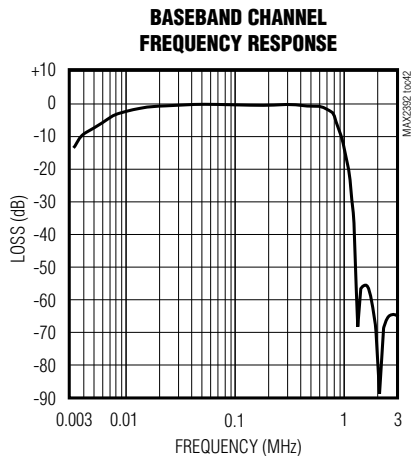
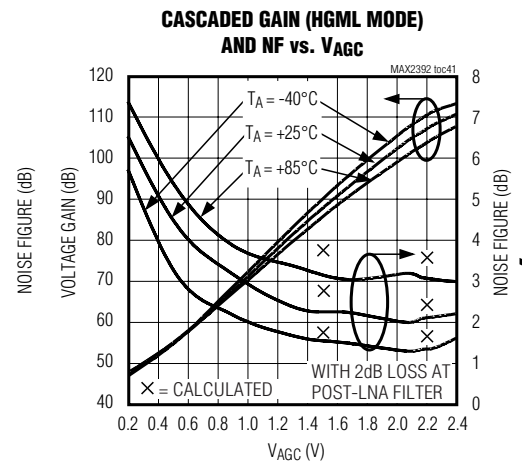
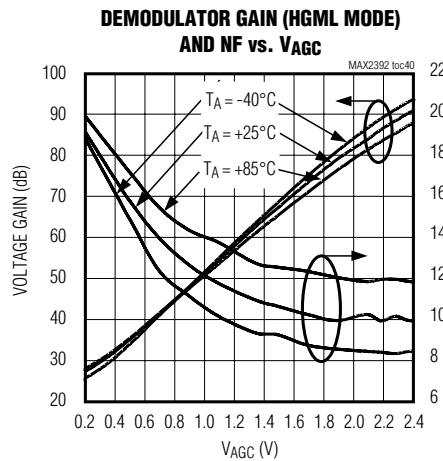
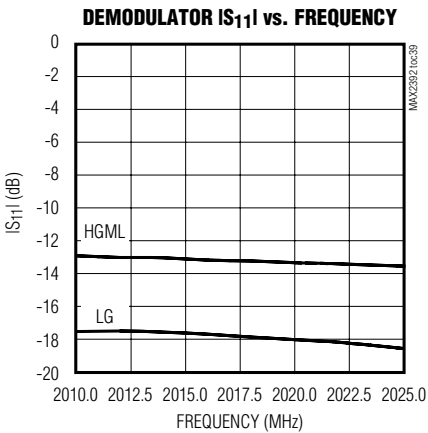
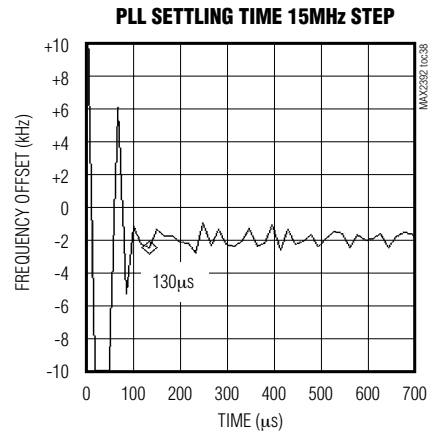
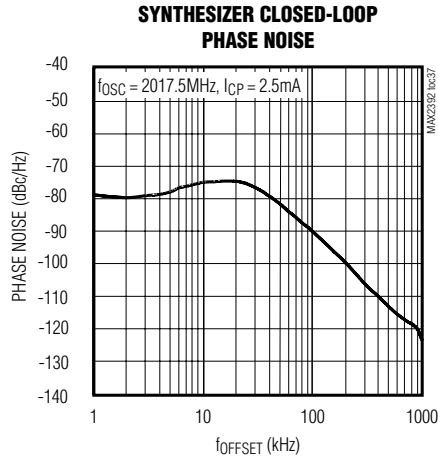
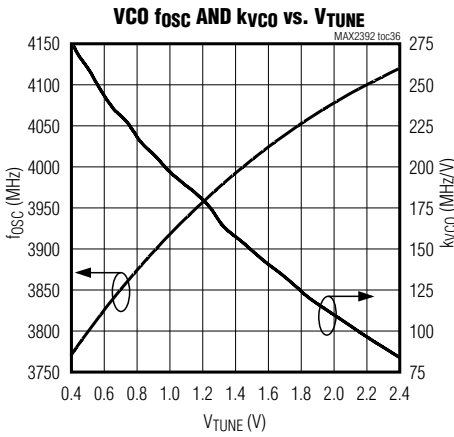
(MAX2392 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 2017MHz$, $T_A = +25^\circ C$, unless otherwise noted.)



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

MAX2392 Typical Operating Characteristics (continued)

(MAX2392 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 2017MHz$, $T_A = +25^\circ C$, unless otherwise noted.)



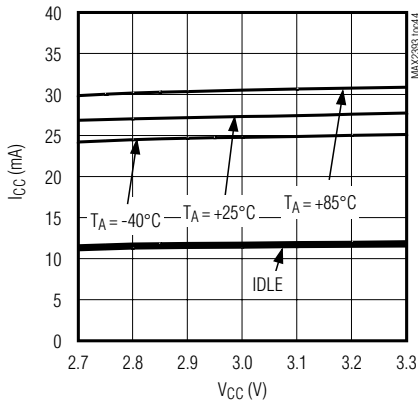
MAX2390-MAX2393/MAX2396/MAX2400/MAX2401

W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

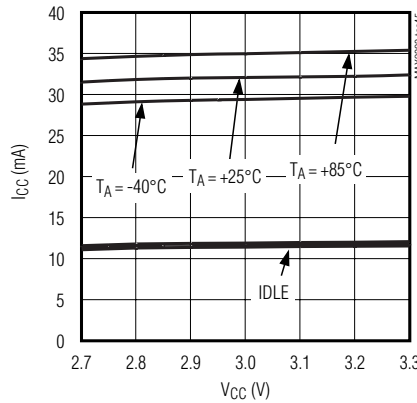
MAX2393 Typical Operating Characteristics

(MAX2393 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1910MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

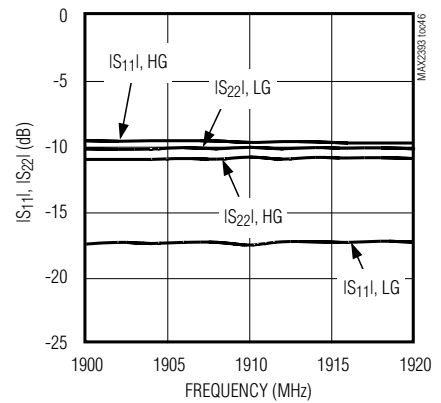
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
LG MODE**



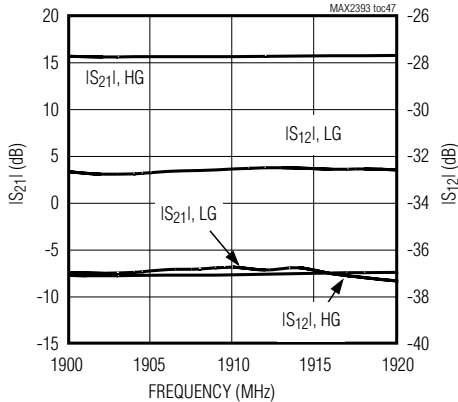
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
HGML MODE**



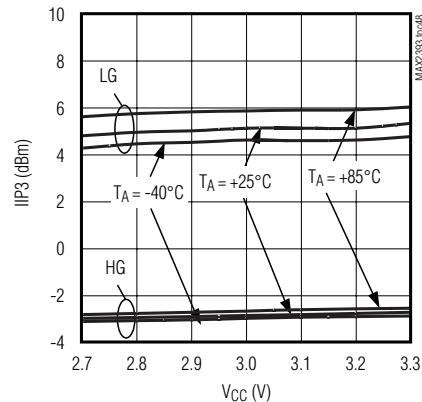
LNA IS11| AND IS22| vs. FREQUENCY



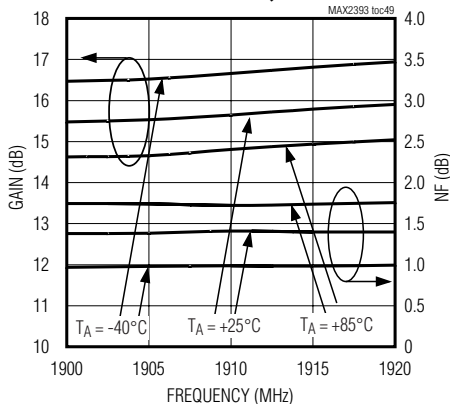
LNA IS21| AND IS12| vs. FREQUENCY



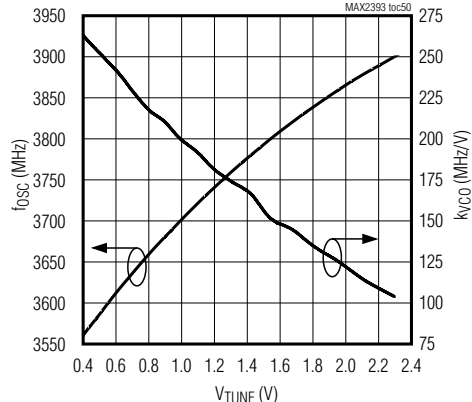
LNA IN-BAND IIP3 vs. SUPPLY VOLTAGE



**LNA GAIN (HG MODE)
AND NF vs. FREQUENCY**



VCO fosc AND kvco vs. VTUNE

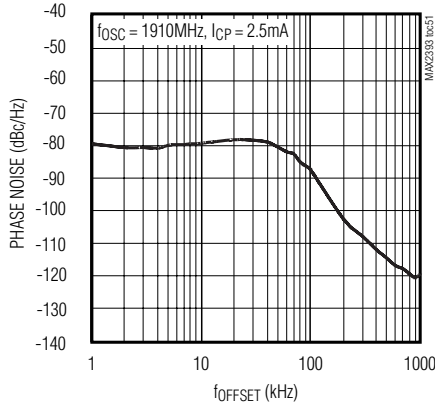


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

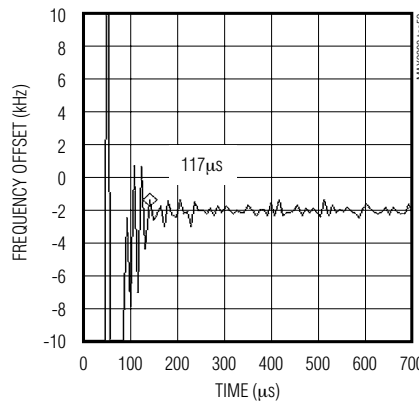
MAX2393 Typical Operating Characteristics (continued)

(MAX2393 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1910MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

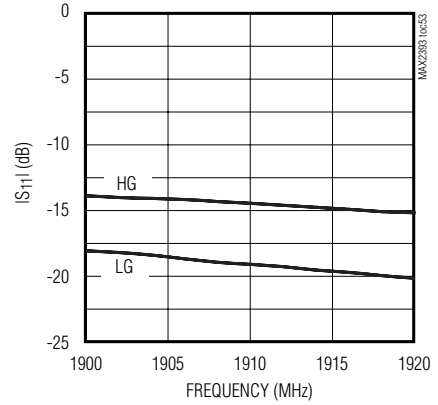
SYNTHESIZER CLOSED-LOOP PHASE NOISE



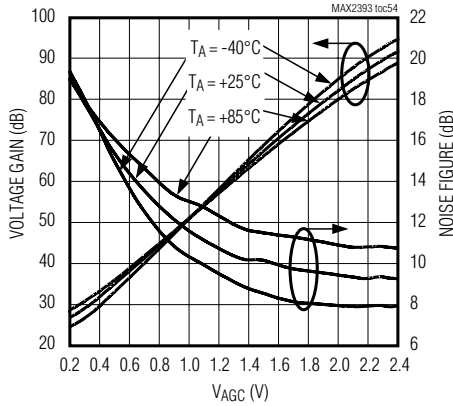
PLL SETTLING TIME 20MHz STEP



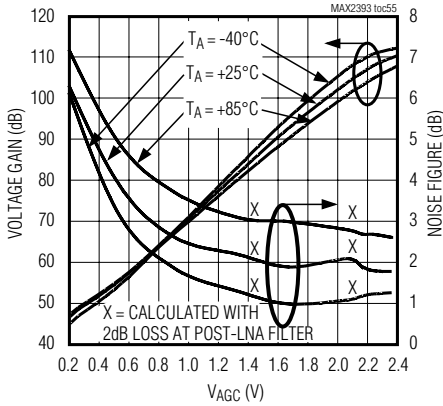
DEMODULATOR IS_{11} vs. FREQUENCY



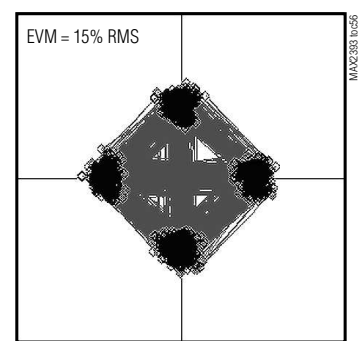
DEMODULATOR GAIN (HGML MODE) AND NF vs. V_{AGC}



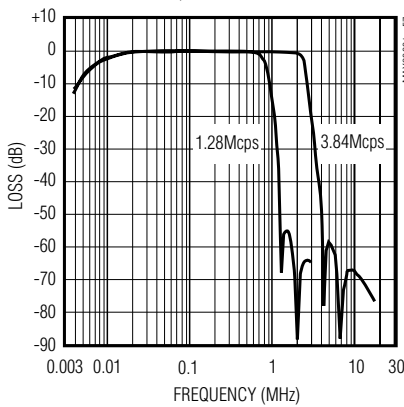
CASCADED GAIN (HGML MODE) AND NF vs. V_{AGC}



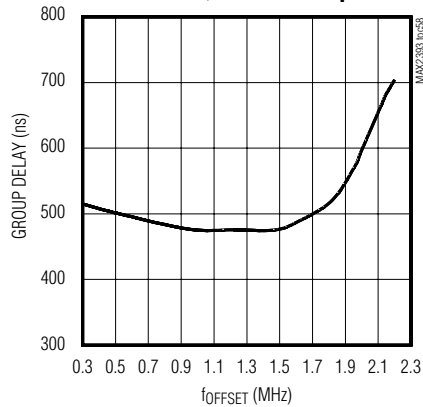
COMPOSITE EVM W-CDMA: PCCPCH + SCH



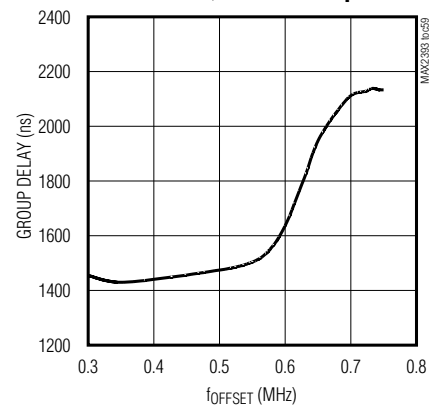
BASEBAND CHANNEL FREQUENCY RESPONSE



BASEBAND CHANNEL GROUP DELAY vs. FREQUENCY 3.84Mcps



BASEBAND CHANNEL GROUP DELAY vs. FREQUENCY 1.28Mcps

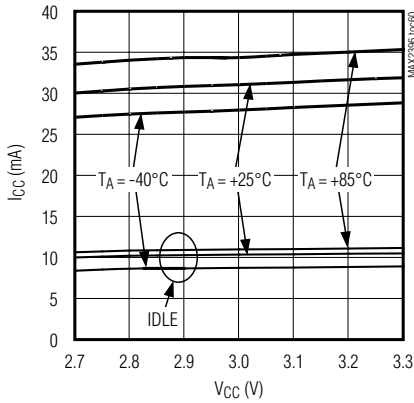


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

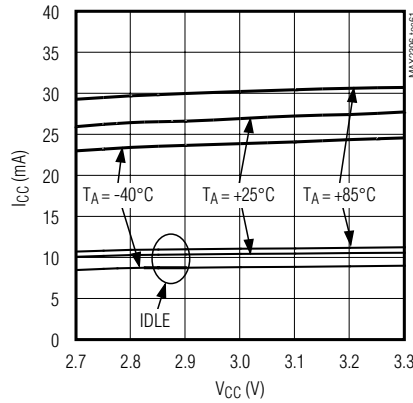
MAX2396 Typical Operating Characteristics

(MAX2396 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 2140MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

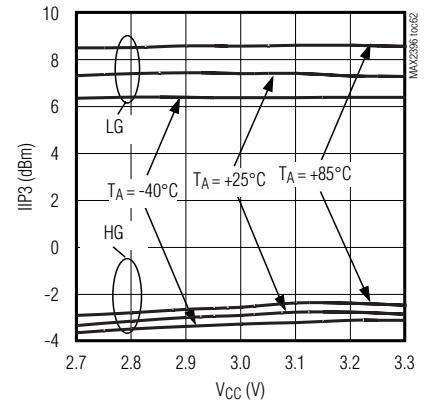
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
HGHL MODE**



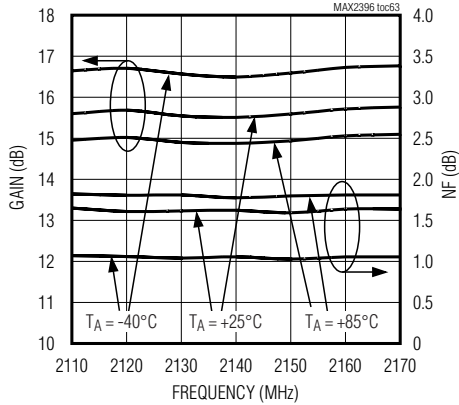
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
LG MODE**



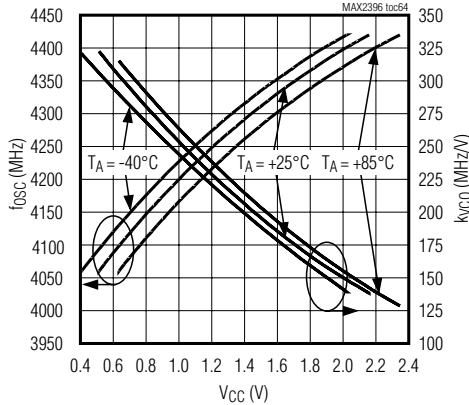
LNA IN-BAND IIP3 vs. SUPPLY VOLTAGE



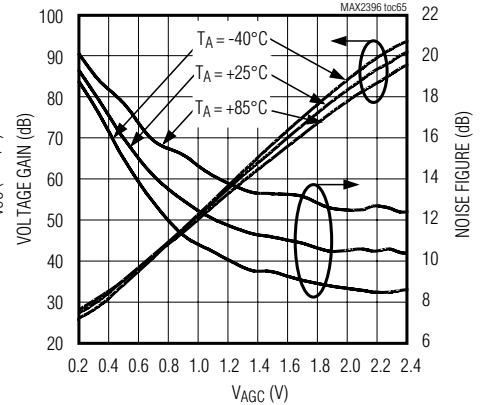
LNA GAIN AND NF (HG MODE) vs. FREQUENCY



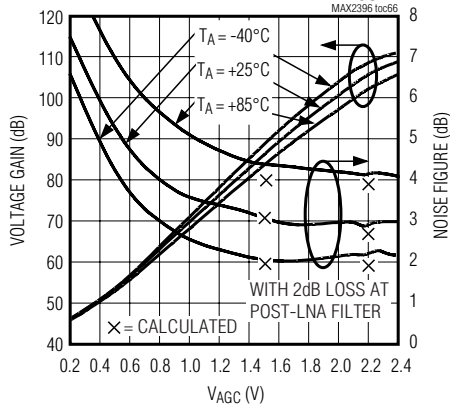
VCO f_{OSC} AND k_{VCO} vs. V_{TUNE}



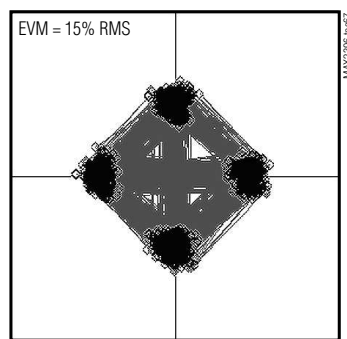
DEMODULATOR GAIN AND NF vs. V_{AGC}



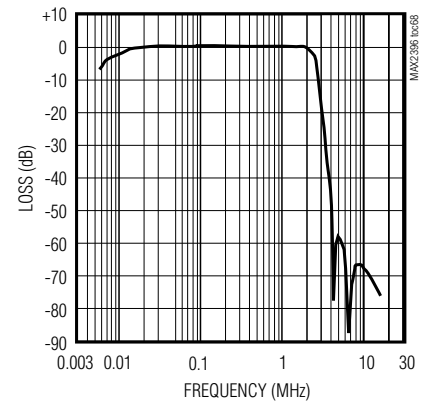
CASCADED GAIN AND NF vs. V_{AGC}



**COMPOSITE EVM
W-CDMA: PCCPCH + SCH**



FREQUENCY RESPONSE

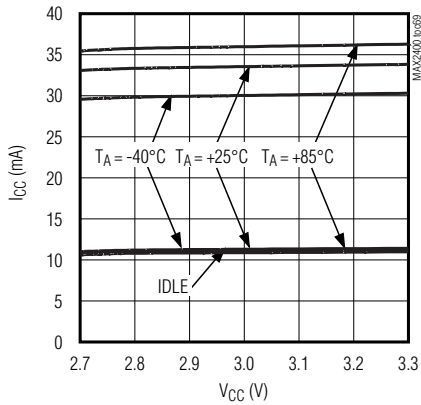


W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

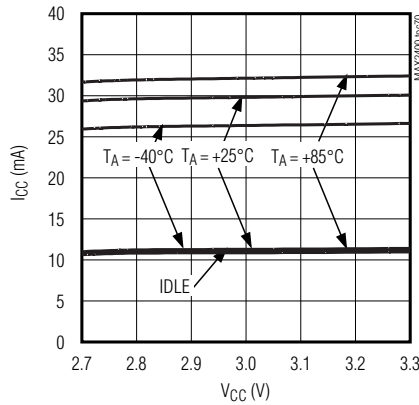
MAX2400 Typical Operating Characteristics

(MAX2400 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1960MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

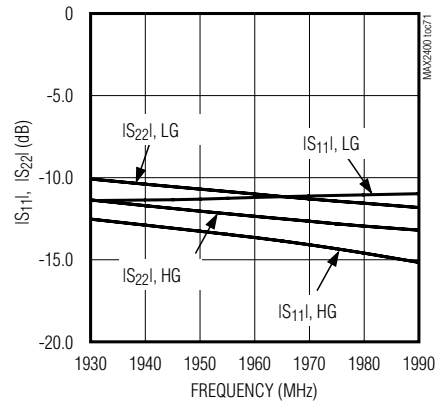
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
HGML MODE**



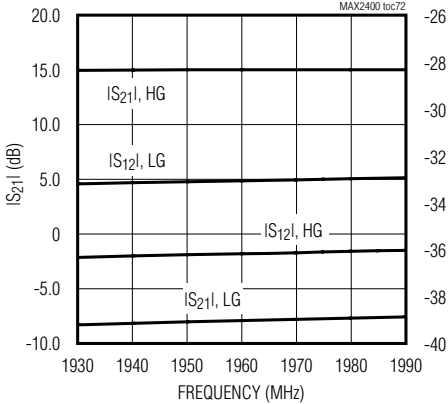
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
LG MODE**



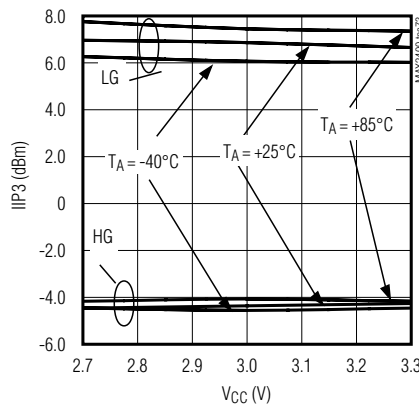
**LNA IS_{11} AND IS_{22}
vs. FREQUENCY**



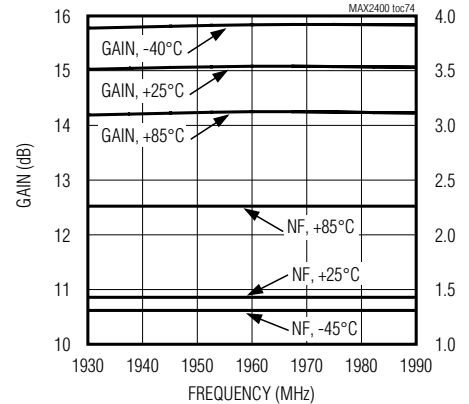
**LNA IS_{21} AND IS_{12}
vs. FREQUENCY**



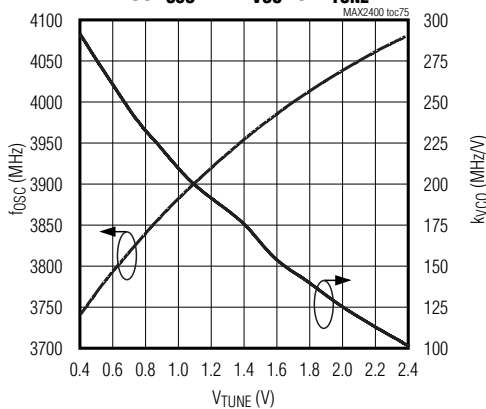
**LNA IN-BAND IIP3
vs. SUPPLY VOLTAGE**



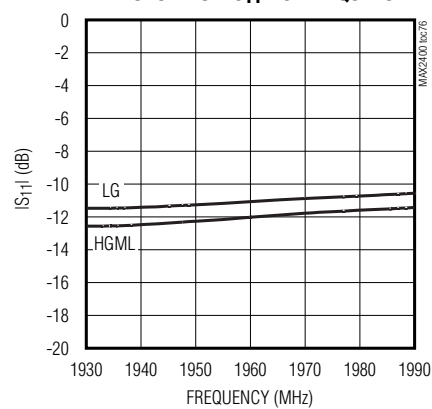
**LNA GAIN AND NF
vs. FREQUENCY HG MODE**



VCO f_{osc} AND k_{VCO} vs. V_{TUNE}



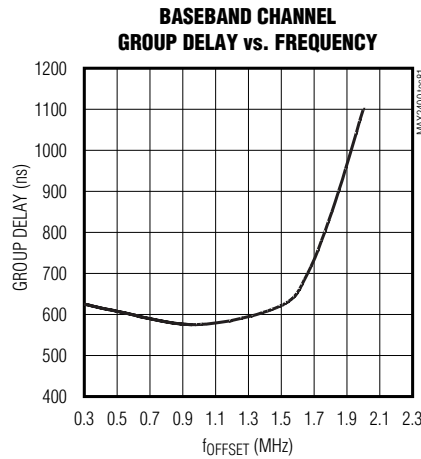
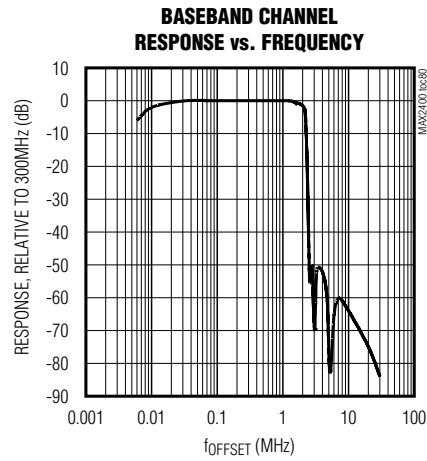
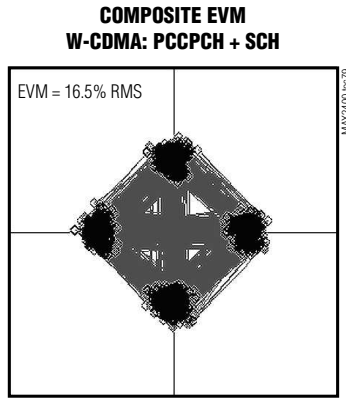
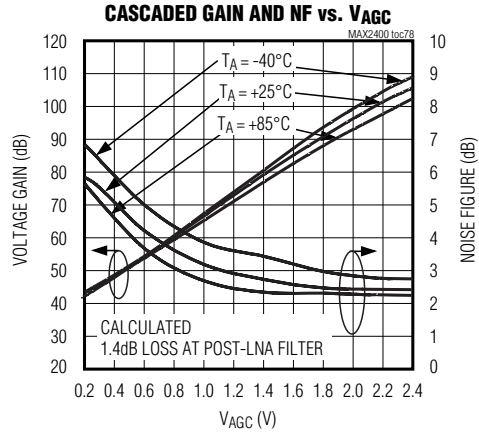
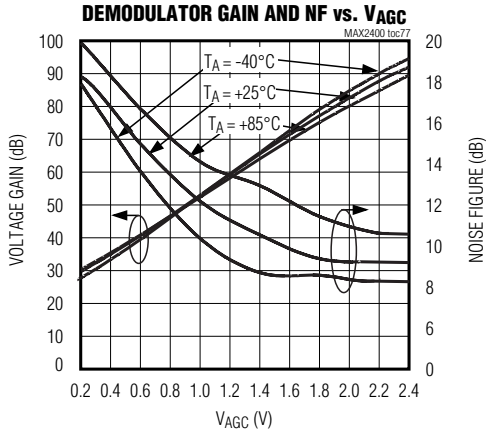
DEMODULATOR IS_{11} vs. FREQUENCY



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

MAX2400 Typical Operating Characteristics (continued)

(MAX2400 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1960MHz$, $T_A = +25^\circ C$, unless otherwise noted.)



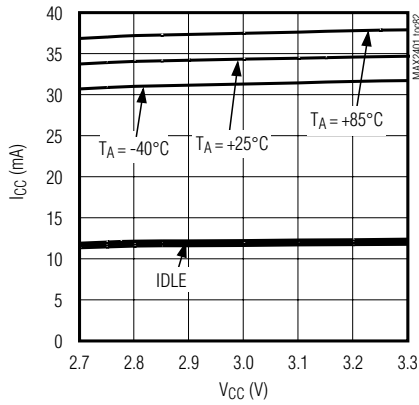
W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

MAX2401 Typical Operating Characteristics

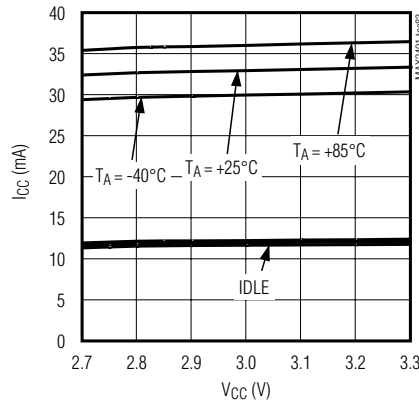
(MAX2401 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1842.4MHz$, $T_A = +25^\circ C$, unless otherwise noted.)

MAX2390-MAX2393/MAX2396/MAX2400/MAX2401

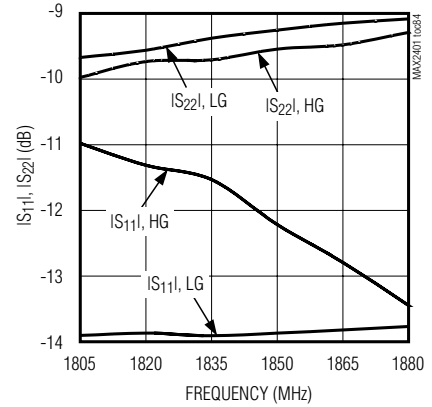
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
HGML MODE**



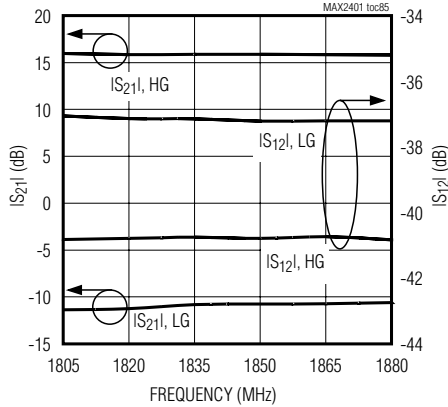
**SUPPLY CURRENT vs. SUPPLY VOLTAGE
LG MODE**



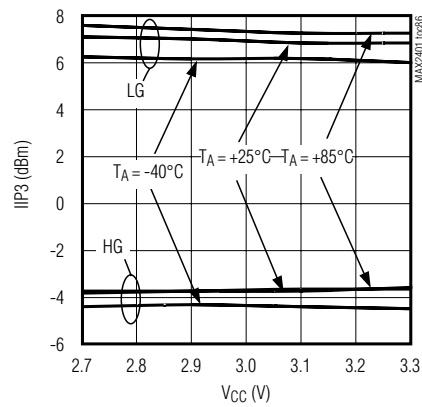
LNA IS11I AND IS22I vs. FREQUENCY



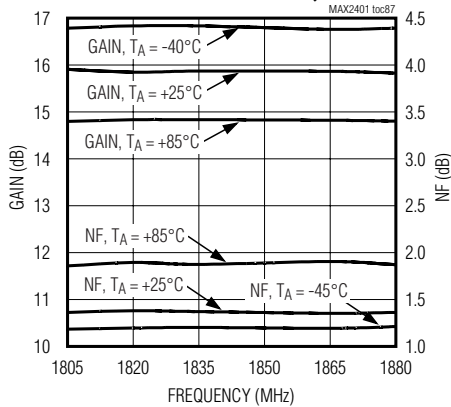
LNA IS21I AND IS12I vs. FREQUENCY



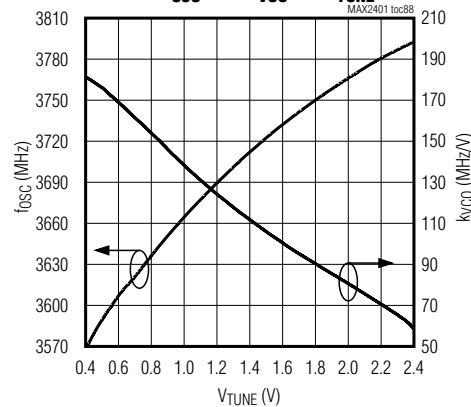
LNA IN-BAND IIP3 vs. SUPPLY VOLTAGE



LNA GAIN AND NF vs. FREQUENCY



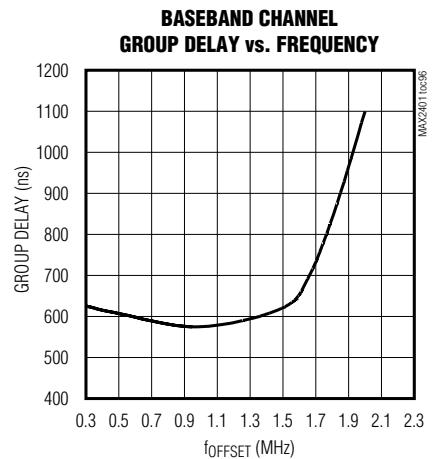
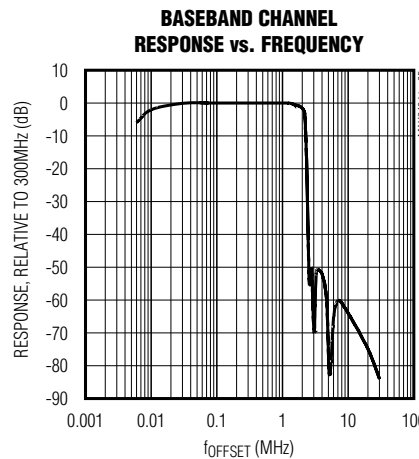
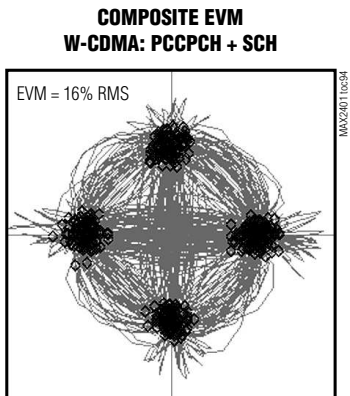
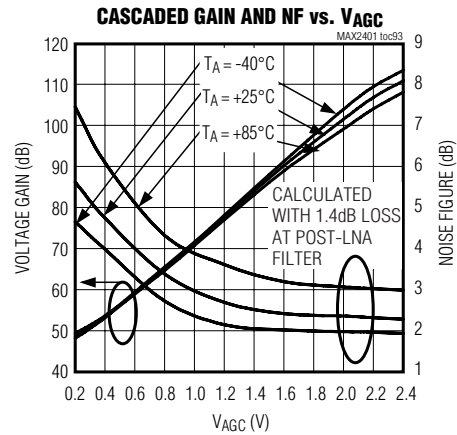
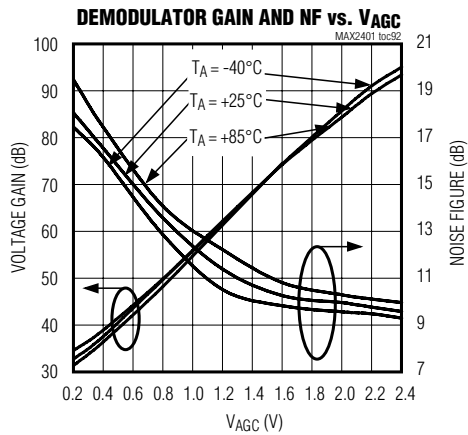
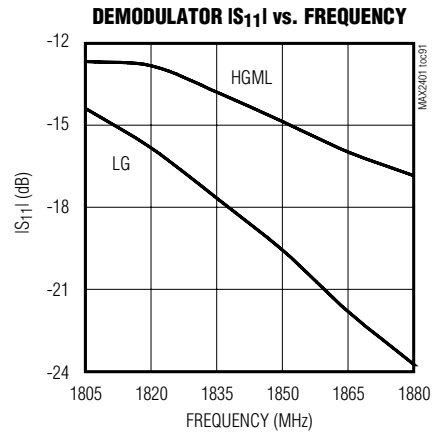
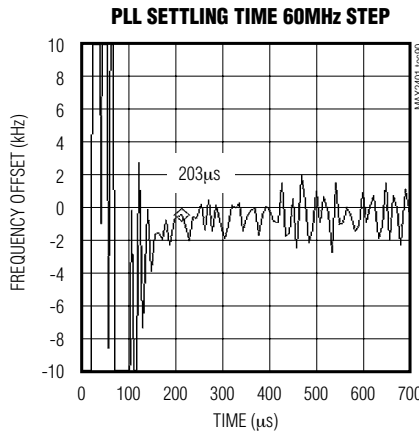
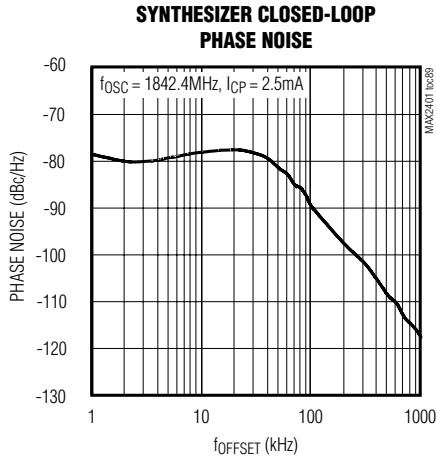
VCO fosc AND kvco vs. VTUNE



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

MAX2401 Typical Operating Characteristics (continued)

(MAX2401 EV kit, $V_{CC} = 2.8V$, HGML mode (see Table 6), $f_{RF} = 1842.4MHz$, $T_A = +25^\circ C$, unless otherwise noted.)



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

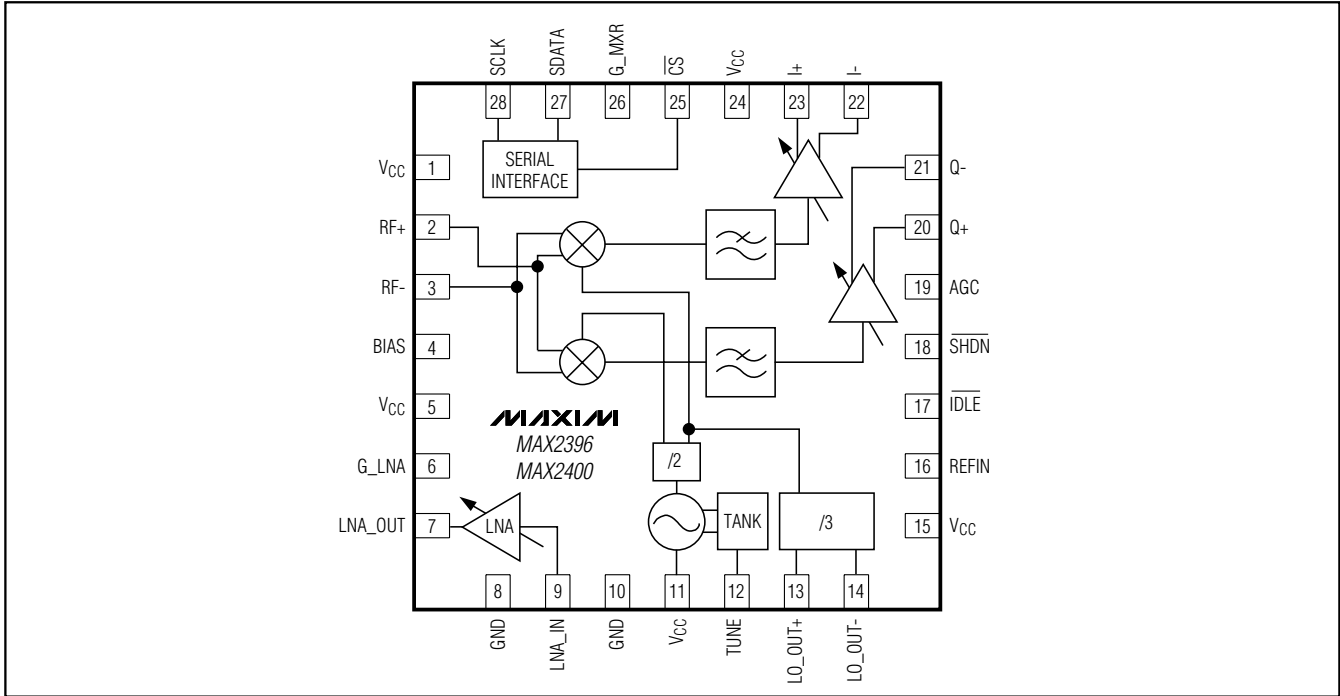
Pin Description

PIN	NAME	FUNCTION
1	VCC	Supply Pin for I/Q Mixers. This pin must be bypassed to system ground as close to the pin as possible. The ground vias for the bypass capacitor should not be shared by any other branch. Use 100pF for RF bypassing to GND.
2	RF+	Noninverting RF Input to Zero-IF Demodulator (200Ω Differential Nominal Impedance Between RF+ and RF-)
3	RF-	Inverting RF Input to Zero-IF Demodulator (200Ω Differential Nominal Impedance Between RF+ and RF-)
4	BIAS	External Bias Resistor Connection
5	VCC	Supply Pin for LNA. This pin must be bypassed to system ground as close to the pin as possible. The ground vias for the bypass capacitor should not be shared by any other branch. Use 100pF for RF bypassing to GND.
6	G_LNA	LNA Gain Mode Logic-Control Pin
7	LNA_OUT	LNA Output. Internally matched to 50Ω.
8	GND	RF Ground Return for LNA. Provide multiple vias to the system ground plane as close to the pin as possible.
9	LNA_IN	LNA Input. Externally matched to 50Ω. See the <i>Applications Information</i> section for more information.
10	GND	RF VCO Varactor Ground Return. Provide multiple vias to the system ground plane as close to the pin as possible.
11	VCC	Supply Pin for VCO. This pin must be bypassed to system ground as close to the pin as possible. The ground vias for the bypass capacitor should not be shared by any other branch. Use 100pF for RF bypassing to GND.
12	TUNE	RF VCO Varactor TUNE Input. Connect PLL loop filter between CP and TUNE.
13	CP	(MAX2390–MAX2393, MAX2401) High-Impedance Output of the RF Charge Pump. The RF PLL's loop filter is connected between this pin and TUNE.
	LO_OUT+	(MAX2396/MAX2400) VCO Divide-by-3 Noninverting Output to Synthesizer
14	VCC	(MAX2390–MAX2393, MAX2401) Supply Pin for Synthesizer Charge Pump. Use 100nF for bypassing to GND.
	LO_OUT-	(MAX2396/MAX2400) VCO Divide-by-3 Inverting Output to Synthesizer
15	VCC	Supply Pin for On-Chip Digital Circuitry. Use 100nF for bypassing to GND.
16	REFIN	Synthesizer Reference Frequency Input. AC-couple to the reference source through 1nF.
17	LD	(MAX2390–MAX2393, MAX2401) Open-Drain Output Indicating LOCK Status of the RF PLL. It is open drain to wire-OR with LD from TX chip.
	$\overline{\text{TDLE}}$	(MAX2396/MAX2400) Idle Mode Enable. Drive $\overline{\text{TDLE}}$ low to disable all blocks except serial bus, VCO, and divide-by-3 prescaler to PLL.
18	$\overline{\text{SHDN}}$	Shutdown Logic Pin for Entire Receiver (Active Low)
19	AGC	Analog Input Pin Controlling the Baseband VGA Gain
20	Q+	Noninverting Baseband Output for Q Channel
21	Q-	Inverting Baseband Output for Q Channel
22	I-	Inverting Baseband Output for I Channel
23	I+	Noninverting Baseband Output for I Channel
24	VCC	Supply Pin for Baseband Circuitry. Use 100nF for bypassing to GND.
25	$\overline{\text{CS}}$	3-Wire Serial Bus Enable Input (Active Low)
26	G_MXR	Mixer Gain Mode Logic-Control Pin
27	SDATA	3-Wire Serial Bus Data Input
28	SCLK	3-Wire Serial Bus Clock Input

MAX2390–MAX2393/MAX2396/MAX2400/MAX2401

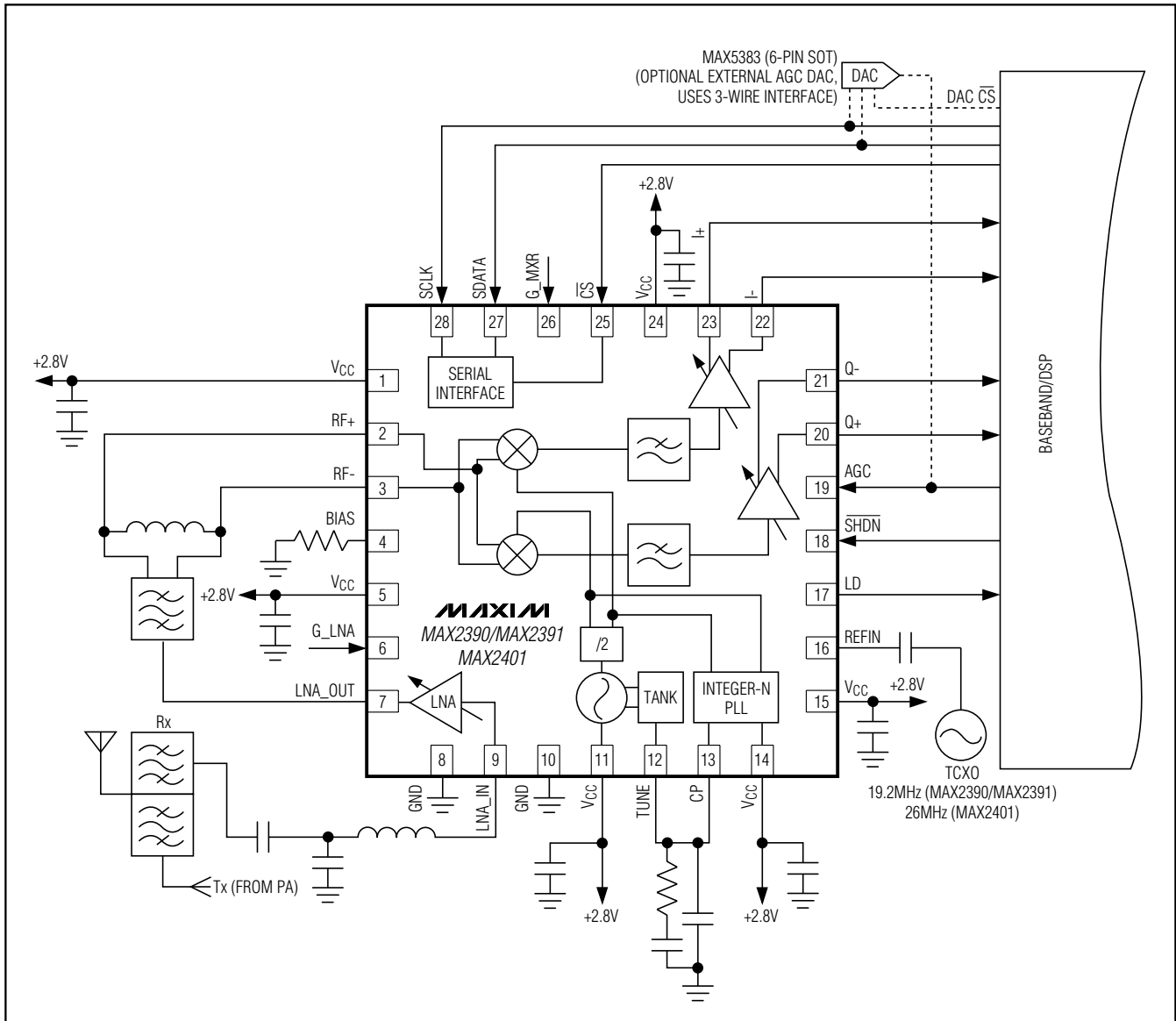
W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

Pin Configuration/Functional Diagram for MAX2396/MAX2400



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

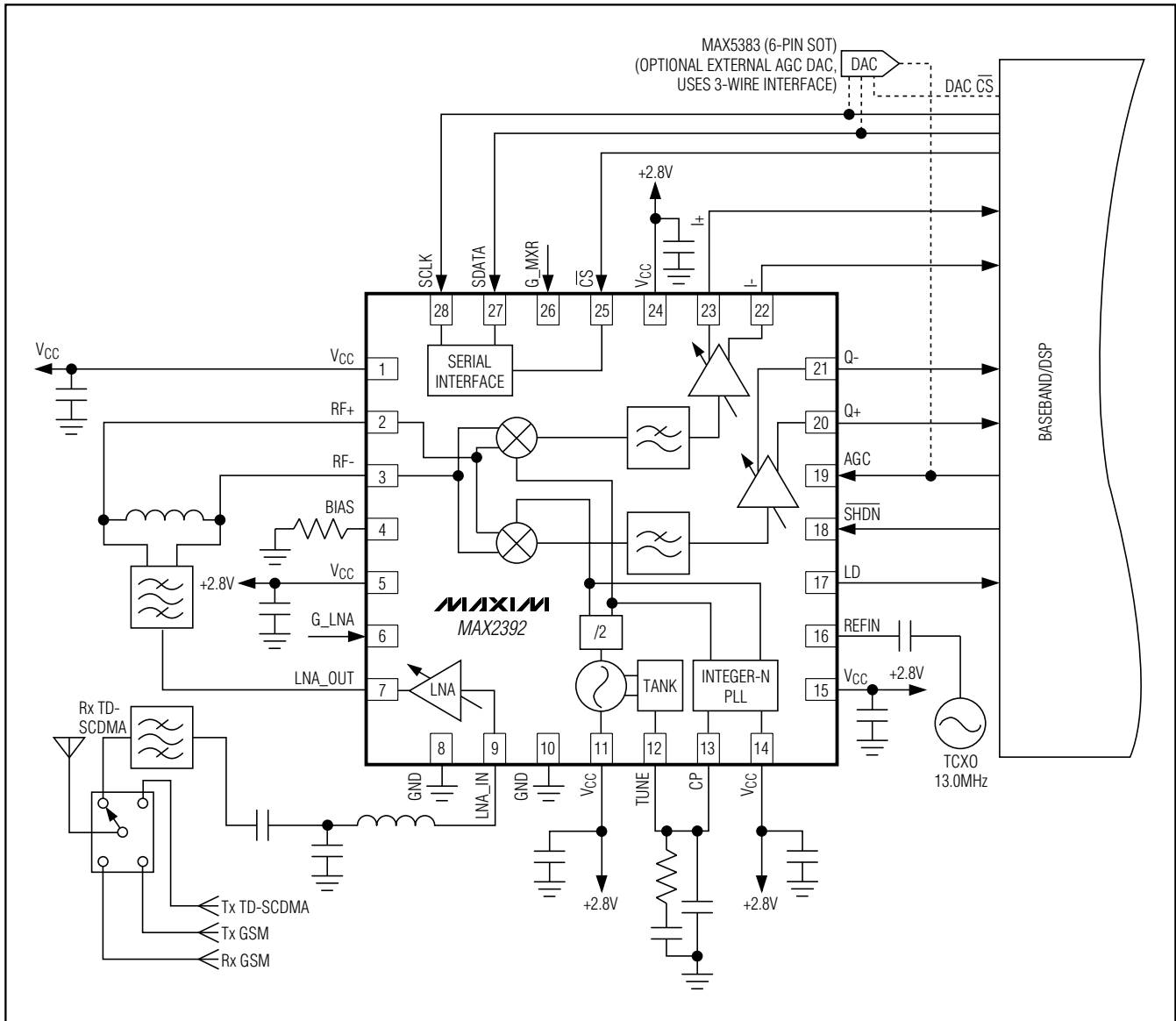
W-CDMA FDD Receiver Operating Circuit (MAX2390/MAX2391/MAX2401)



MAX2390-MAX2393/MAX2396/MAX2400/MAX2401

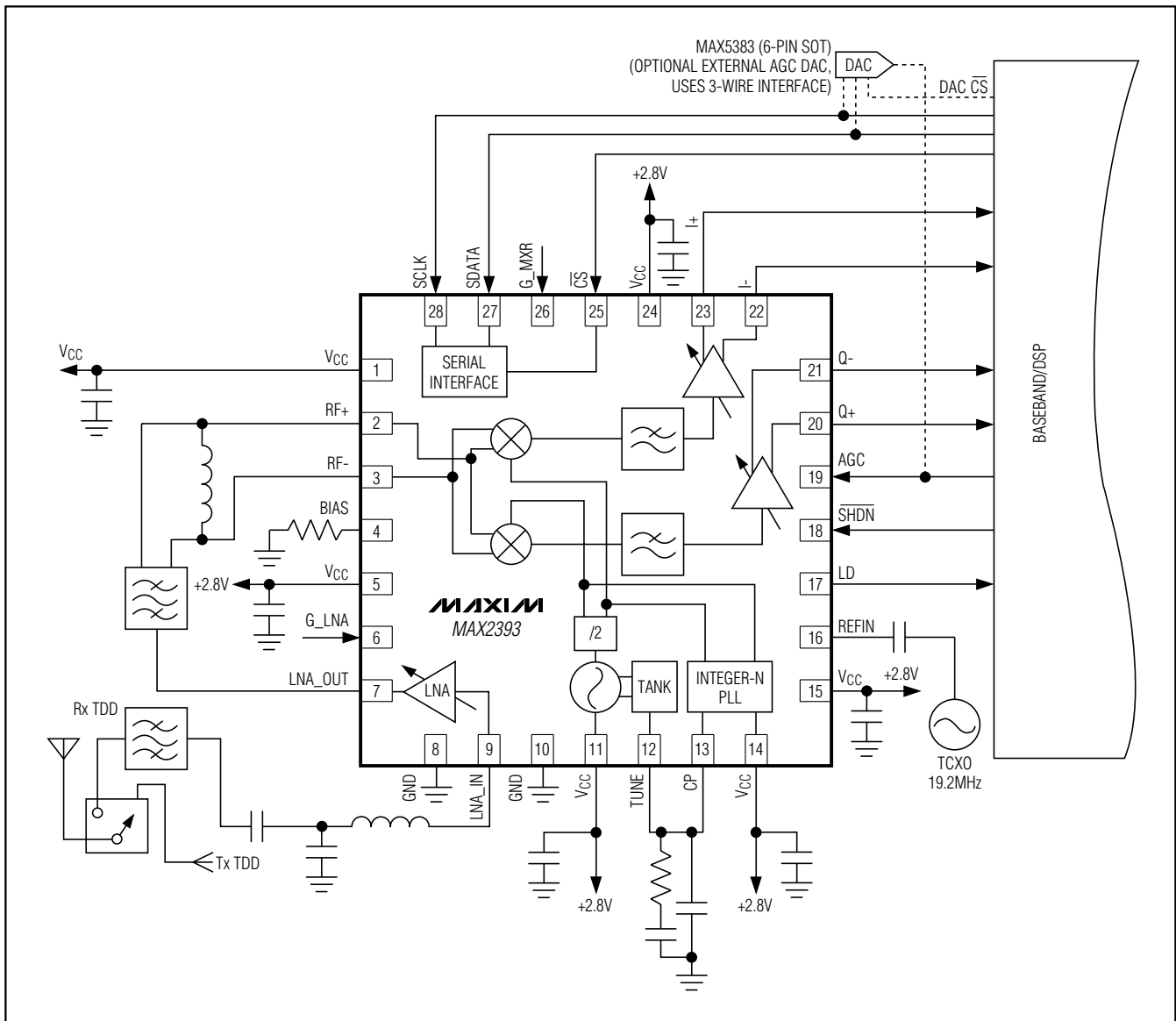
W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

TD-SCDMA Receiver Operating Circuit (MAX2392)



W-CDMA/W-TDD/TD-SCDMA Zero-IF Receivers

W-TDD Receiver Operating Circuit (MAX2393)



MAX2390-MAX2393/MAX2396/MAX2400/MAX2401