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MAX24001

2.5Gbps Tx Burst-Mode Laser Transceiver

General Description

The MAX24001 is a complete burst-mode laser driver transmitter and limiting amplifier receiver for use within fiber optic modules for FTTx applications. A fully compliant GPON/GEPON module with digital diagnostics can be realized when used with a 2KB EEPROM and suitable optics. Alternatively, a microcontroller can be used in conjunction with the MAX24001; however, this is not a necessity in order to achieve SFF-8472 compliance.

The 2.5Gbps limiting receive path features programmable output swing control, rate selection, and OMA-based loss-of-signal detection. Functions are also provided which facilitate the implementation of APD biasing without the need for an external DC-DC converter.

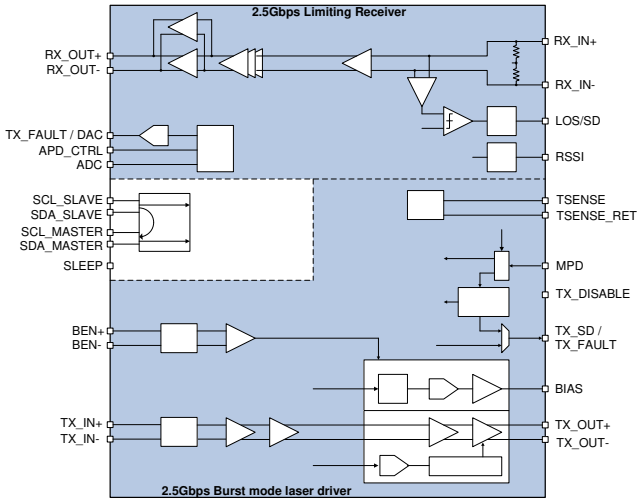
The burst-mode laser driver has temperature compensated modulation control using a lookup table. Closed-loop control of laser power incorporates tracking error compensation and has multiple options for rapidly settling the laser power thus enabling fast registration and shutdown on the network. Diagnostics are enhanced with the inclusion of programmable transmit signal detection during bursts, and rogue ONU detection between bursts. This is linked to a laser safety system which allows the modulation and bias currents to be shut off in response to a range of different fault conditions detected on-chip.

The transmit and receive systems are independently powered and can respond separately to the SLEEP pin. The MAX24001 is highly configurable from either EEPROM or low-cost MCU using a two-wire interface.

Applications

GPON, GEPON, Gigabit Ethernet

Functional Diagram



Features

- **2.5Gbps Limiting Receiver**
- **Integrated APD Bias Loop With Overvoltage And Overcurrent Protection**
- **OMA-Based LOS Detection**
- **1.25Gbps to 2.5Gbps Laser Driver**
- **CML, LVPECL, HSTL, SSTL-Compatible Inputs**
- **Open and Closed-Loop Bias Control**
- **Temperature-Compensated I_{MOD} Control**
- **Highly Configurable Laser Safety System**
- **Transmit TX_SD and Rogue ONU Detection**
- **SFP MSA and SFF-8472 Digital Diagnostics**
- **Integrated Temperature Sensor**
- **Power-Saving SLEEP Modes**
- **External DAC, ADC, and PWM Interfaces**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX24001TL+	-40°C to +95°C	40 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

19-6460; Rev 0; 11/12

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V_{DD_TX}, V_{DD_TXO}, V_{DD_RX}, V_{DD_RXO} ..... -0.3V to +3.65V
Voltage Range on Any Pin Not Otherwise Specified (with respect to V_{SS_*}) ..... -0.5V to (V_{DD_*} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 35.7mW/°C above +70°C) 2857.1mW
Operating Temperature Range ..... -40°C to +95°C
Junction Temperature ..... +150°C
Storage Temperature ..... -70°C to +150°C
Lead Temperature (soldering 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage	V_{DD}		3.0	3.3	3.6	V
RSSI Pin Compliance		ROSA sourcing to RSSI pin			V_{DD} - 0.75	V
		ROSA sinking from RSSI pin	0.75			V
BIAS Pin Compliance			0.8			V
TX_OUT Pin Compliance			0.8			V
MPD Input Current		For correct APC loop operation	40		2000	µA
MPD Input Capacitance		For correct APC loop operation	4		20	pF
Junction Temperature			-40		+120	°C
Case Temperature			-40		+95	°C

Device not guaranteed to meet parametric specifications when operated beyond these conditions. Permanent damage may be incurred by operating beyond these limits.

ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.97V to 3.63V, T_A = -40°C to +95°C.) (Note 1)

Note 1: Electrical specifications are production tested at T_A = +25°C. Specifications over the entire operating temperature range are guaranteed by design and characterization. Typical specifications are at T_A = +25°C, 3.3V.

CONTINUOUS RATINGS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	IDD	Excluding laser bias and modulation currents, 20mA bias and modulation current, Rx CML output 400mV_{P-P}		136		mA

RECEIVER CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Differential Input Impedance			80	100	120	Ω
Maximum Input Data Rate				2.5		Gbps
Minimum Input Data Rate				1.25		Gbps
Input Sensitivity		Differential, BER = 1E-10, 2.5Gbps, PRBS 2^{23}-1 pattern		6.5	13	mV_{P-P}
Deterministic Jitter		2.5Gbps, V_{OUT} = $800mV_{P-P}$, V_{IN} between $25mV_{P-P}$ differential and $1000mV_{P-P}$		40		ps_{P-P}
Random Jitter		2.5Gbps, V_{OUT} = $800mV_{P-P}$, V_{IN} between $25mV_{P-P}$ differential and $1000mV_{P-P}$		2.7		ps_{RMS}
Output Rise/Fall Times		2.5Gbps, V_{OUT} = $800mV_{P-P}$, V_{IN} = $25mV_{P-P}$ differential and $1000mV_{P-P}$		60		ps
Low-Frequency Cutoff				30		kHz
Output Impedance		1MHz differential	80	100	120	Ω
Minimum Output Swing		Differential, 4-bit programmable (Note 2)		200	240	mV_{P-P}
Maximum Output Swing		Differential, 4-bit programmable (Note 2)	800	880		mV_{P-P}

Note 2: Measured with 1111111100000000 pattern.

LOSS OF SIGNAL AND RSSI CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum OMA LOS Assert Time				11		µs
Maximum OMA LOS Deassert Time				11		µs
Maximum LOS Threshold Setting				400		mV_{P-P}
LOS Assert/Deassert Level		LOS DAC = 50 (Note 3)		67		mV_{P-P}
		LOS DAC = 105 (Note 3)		143		mV_{P-P}
Maximum RSSI Current Level		Sourced or sunk from RSSI pin		1200		µA

Note 3: LOS assert and deassert levels can be set independently to define hysteresis.

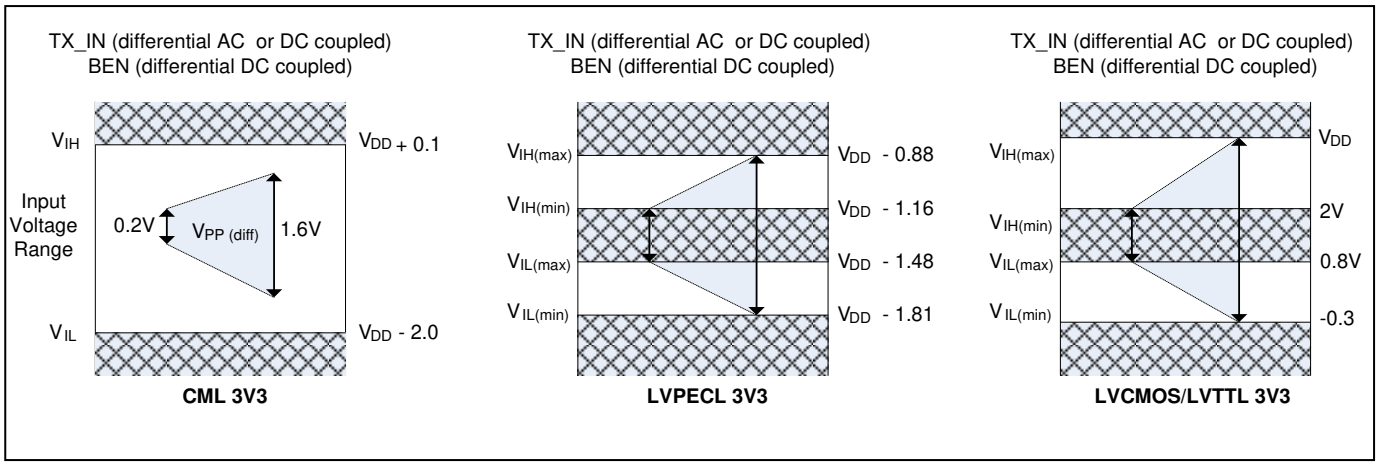
TRANSMITTER CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Input Data Rate		PRBS23		2.488		Gbps
Minimum Input Data Rate		PRBS23		1.25		Gbps
Maximum Modulation Current			80			mA_{P-P}
Minimum Modulation Current				8		mA_{P-P}
Maximum Electrical Rise/Fall Time (20% to 80%)		Measured using 15Ω effective termination, I_{MOD} = $8mA_{P-P}$ to $80mA_{P-P}$		96		ps
Total Jitter		PRBS15, 2.488Gbps, I_{MOD} = $8mA_{P-P}$ to $80mA_{P-P}$, differential electrical measurement		65	175	mUI_{P-P}
Deterministic Jitter		PRBS15, 2.488Gbps, I_{MOD} = $8mA_{P-P}$ to $80mA_{P-P}$, differential electrical measurement		45		mUI_{P-P}
Random Jitter		PRBS15, 2.488Gbps, I_{MOD} = $8mA_{P-P}$ to $80mA_{P-P}$, differential electrical measurement		1.11		mUI_{RMS}
Maximum Bias Current				90		mA

BURST TIMINGS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Burst Enable/Disable Time (Electrical)		Disable: Bias current reduced to 20% of its maximum value. Enable: Bias current increased to 90% of desired bias plus modulation current Target bias current > 3mA		7	12	ns
Minimum Burst Length to Update APC Loop		During closed-loop operation		90		ns
Minimum Burst Gap		During closed-loop operation		75		ns
Maximum Initial Mean Power Control Settling Time (APC Loop)		From power-on, negation of TX_DISABLE, or negation of SLEEP to 90% of desired optical power. Fast settling algorithm enabled, no fast start LUT. Bias current overshoot < 10% Bias current > 4mA		1.2		µs

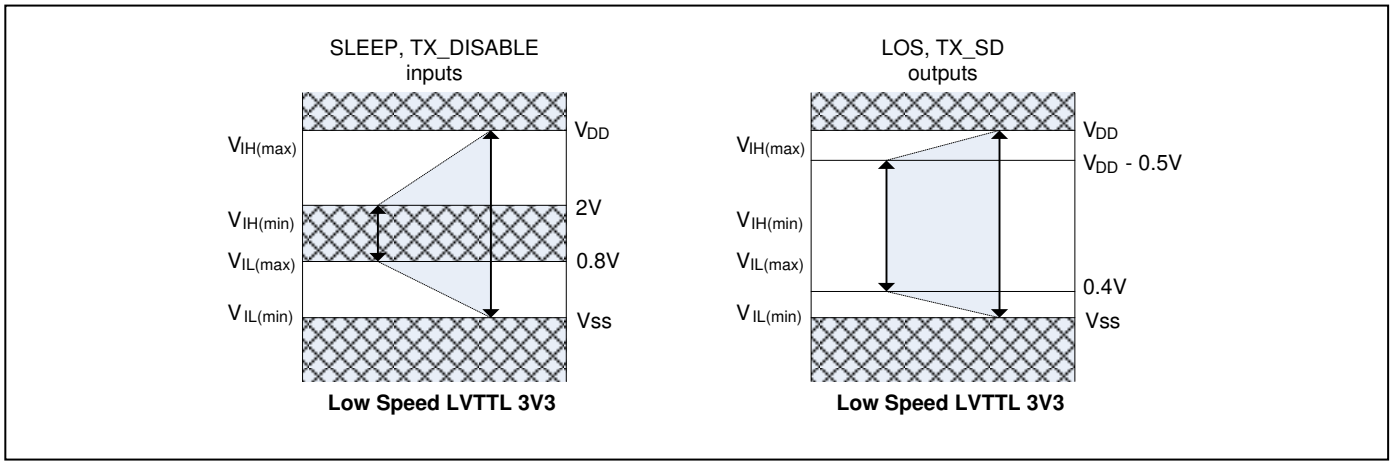
TRANSMITTER INPUT CHARACTERISTICS



Typical I/O ranges for TX_IN and BEN are shown. TX_IN and BEN inputs are also compatible with HSTL and SSTL for low-voltage operation.

DIGITAL I/O CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Time To Initialise		From power-up or hot plug		71		ms
TX_DISABLE Assert		TX_DISABLE assert to optical disable		0.3		µs
TX_DISABLE Negate		TX_DISABLE negate to optical enable		0.5		ms
TX_DISABLE to Reset		Time TX_DISABLE must be held high to reset TX_FAULT		0.155		µs
Maximum Delay BEN Change to TX_SD Response		Rising or falling edge		100		ns
Light During Gap to Laser Shutdown		Rogue ONU		100		µs



Typical I/O Ranges for SLEEP, TX_DISABLE, LOS and TX_SD

PERIPHERAL FUNCTIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-On-Reset (POR) Voltage		Module 3V3 supply voltage above which reset will not be asserted			2.5	V
		Module 3V3 supply voltage below which reset is guaranteed	2.2			V

APD Control

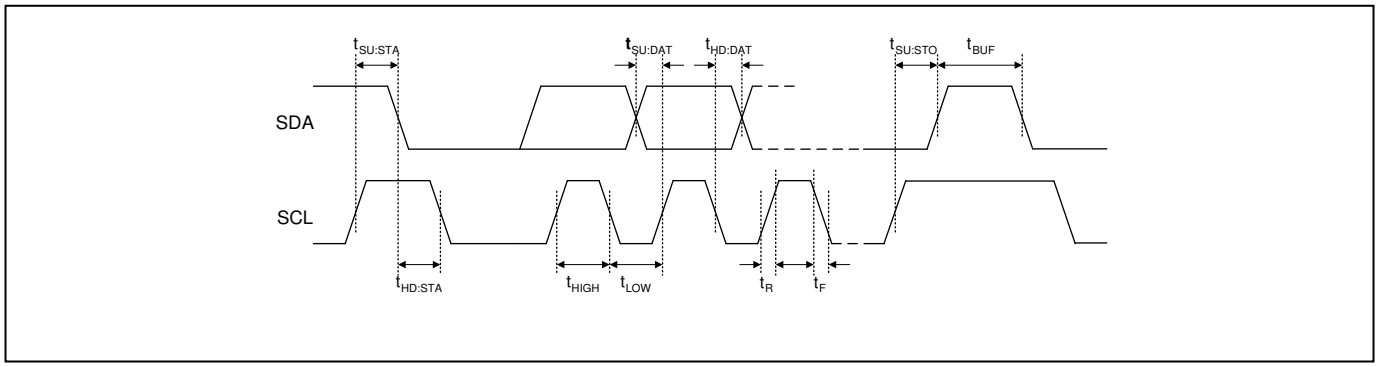
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Pin Minimum Voltage					1.30	V
ADC Pin Maximum Voltage			2.25			V
DAC Pin Minimum Current				0		mA
DAC Pin Maximum Current				0.45		mA
DAC Pin Compliance				1.5		V
PWM Frequency		Minimum PWM frequency		250		kHz
		Maximum PWM frequency		2		MHz
Step Response Settling Time		Load current change from 20µA to 1mA		2		ms

SLEEP

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Sleep Assert/Deassert		Time to allow first operation or enter sleep from deassertion of sleep pin		100		ns

TWO-WIRE INTERFACE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum SCL Clock Frequency				400		kHz
Minimum SCL Clock LOW Period	t_{LOW}			1200		ns
Minimum SCL Clock HIGH Period	t_{HIGH}			600		ns
Minimum Setup Time For A Repeated START Condition	$t_{SU:STA}$			600		ns
Minimum Hold Time (Repeated) START Condition	$t_{HD:STA}$			600		ns
Minimum Data Hold Time	$t_{HD:DAT}$			0		ns
Minimum Data Setup Time	$t_{SU:DAT}$			100		ns
Minimum Setup Time for STOP Condition	$t_{SU:STO}$			600		ns
Minimum Bus Free Time Between a STOP and START Condition	t_{BUF}			1200		ns
Maximum Rise and Fall Times of Both SDA and SCL Signals	t_R, t_F			300		ns
Minimum Rise and Fall Times of Both SDA and SCL Signals	t_R, t_F	C_b = capacitance of a single bus line $C_x = 20 + 0.1 \times Cb$		Cx		ns
Maximum Capacitance for Each I/O Pin				10		pF

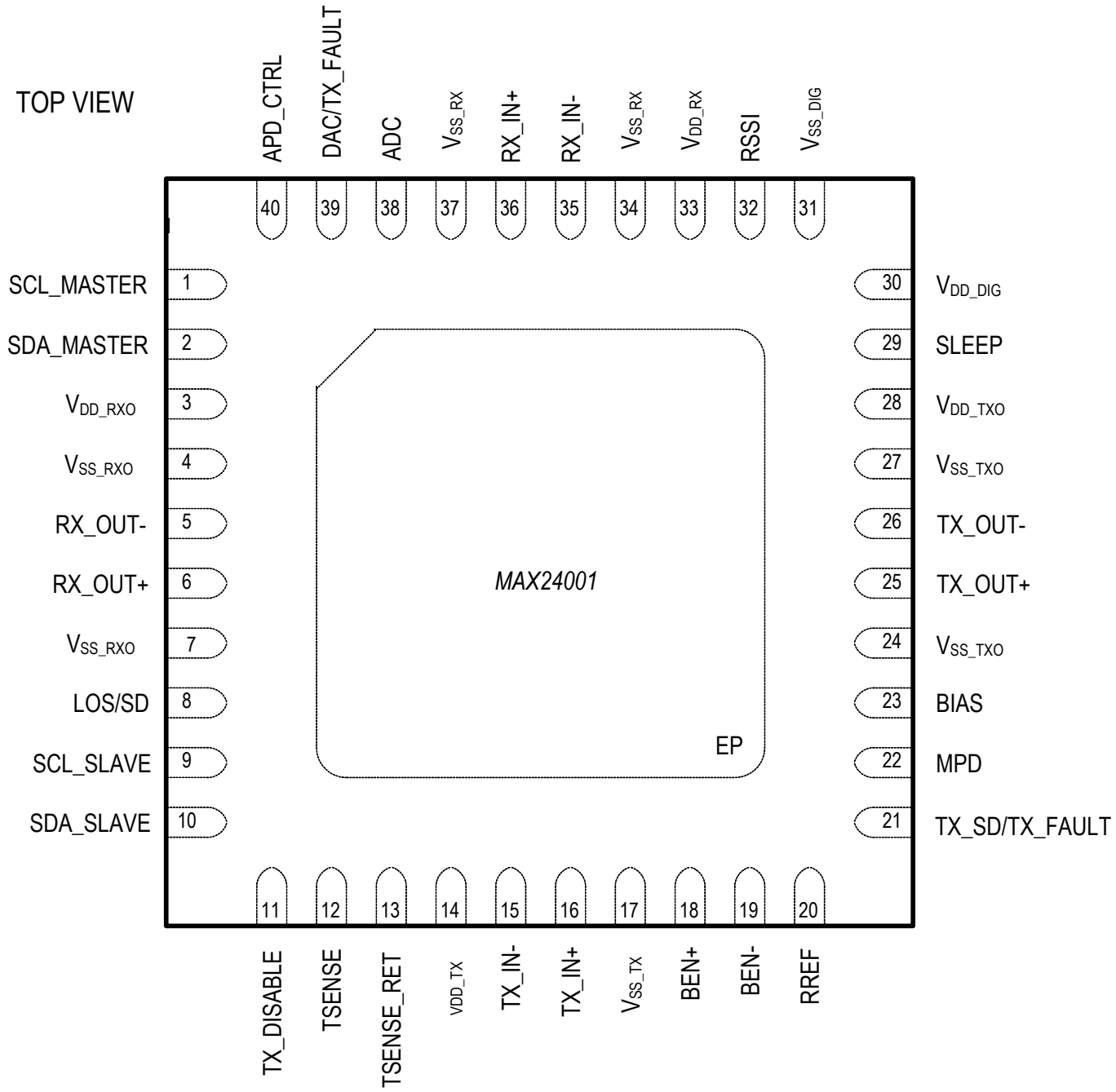


DIGITAL DIAGNOSTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TEMPERATURE						
Reporting Resolution		-40°C to +95°C range		0.85		°C/LSB
Maximum Inaccuracy		Single-point calibration, external mode		±2		°C
POWER SUPPLY						
Reporting Resolution		3.0V to 3.6V range		10		mV/LSB
Maximum Inaccuracy		Calibrated, within the supply reporting range		±3		%
TX BIAS						
Reporting Resolution		5mA to 90mA range		0.392		mA/LSB
Maximum Inaccuracy		Calibrated, within the Tx bias reporting range		±10		%
TX POWER						
MPD Current Reporting Resolution		**mpd_range** = 00, 40µA to 200µA		0.78		µA/LSB
		mpd_range = 01, 100µA to 800µA		3.125		µA/LSB
		mpd_range = 10, 400µA to 2000µA		12.5		µA/LSB
Maximum Inaccuracy		Calibrated, within the MPD operating range		±20		%
RX POWER						
RSSI Current Reporting Resolution		0 to 16µA (Note 4)		0.5		µA/LSB
		16µA to 206µA (Note 4)		2.0		µA/LSB
		206µA to 1000µA (Note 4)		8.0		µA/LSB
Maximum Inaccuracy		3µA to 25µA, calibrated (Note 4)		±25		%
		25µA to 1000µA, calibrated (Note 4)		±10		%

Note 4: rx_rssi_scale = 00 (x1 gain) range and resolution settings can be changed to improve accuracy.

Pin Configuration



TQFN
(5mm x 5mm)

Pin Description

PIN	NAME	DIR	TYPE	FUNCTION
1	SCL_MASTER	O/P	LVTTL	Two-Wire Interface Clock Connection To EEPROM, with Internal 10kΩ Pullup Resistor
2	SDA_MASTER	I/O	LVTTL	Two-Wire Interface Data Connection To EEPROM, with Internal 10kΩ Pullup Resistor
3	V_{DD_RXO}	Analog	+3.3V	Receiver Output Power Supply
4	V_{SS_RXO}	Analog	GND	Receiver Output Ground Connection
5	RX_OUT-	O/P	CML	Limiting Receiver Inverted Output. 50Ω to V_{DD_RXO}
6	RX_OUT+	O/P	CML	Limiting Receiver Noninverted Output. 50Ω to V_{DD_RXO}
7	V_{SS_RXO}	Analog	GND	Receiver Output Ground Connection
8	LOS/SD	O/P	LVTTL	Loss-Of-Signal Indication. Open drain with external 4.7kΩ to 10kΩ resistor.
9	SCL_SLAVE	I/P	LVTTL	Two-Wire Interface Clock Connection To Host. with external 10kΩ pullup resistor
10	SDA_SLAVE	I/O	LVTTL	Two-Wire Interface Data Connection To Host. with external 10kΩ pullup resistor
11	TX_DISABLE	I/P	LVTTL	Internally pulled high to V_{DD_TX} with a 7.5kΩ resistor
12	TSENSE	Analog	Analog	Temperature Sensor Current Force
13	TSENSE_RET	Analog	Analog	Temperature Sensor Current Return
14	V_{DD_TX}	Analog	+3.3V	Transmitter Power Supply
15	TX_IN-	I/P	High Speed	Transmitter Input Signal Inverted
16	TX_IN+	I/P	High Speed	Transmitter Input Signal Noninverted
17	V_{SS_TX}	Analog	GND	Transmitter Ground Connection
18	BEN+	I/P	High Speed	Burst-Enable Noninverted
19	BEN-	I/P	High Speed	Burst-Enable Inverted
20	RREF	Analog	Analog	Connects to External Precision Resistor
21	TX_SD/ TX_FAULT	O/P	LVTTL	Push-Pull Signal Detect Indication. Can be configured as open-drain TX_FAULT output, pulled high externally using a 4.7kΩ to 10kΩ resistor.
22	MPD	I/P	Analog	Monitor Photodiode Input
23	BIAS	Analog	Analog	Bias Current Sink
24	V_{SS_TXO}	Analog	GND	Transmitter Output Ground Connection
25	TX_OUT+	O/P	High Speed	Laser Data Differential Drive Output
26	TX_OUT-	O/P	High Speed	Laser Data Differential Drive Output
27	V_{SS_TXO}	Analog	GND	Transmitter Output Ground Connection
28	V_{DD_TXO}	Analog	+3.3V	Transmitter Output Power Supply
29	SLEEP	I/P	LVTTL	Sleep Mode Select
30	V_{DD_DIG}	Analog	+3.3V	Digital Power Supply
31	V_{SS_DIG}	Analog	GND	Digital Ground Connection
32	RSSI	I/P	Analog	Rx Photodiode Monitor (RSSI)
33	V_{DD_RX}	Analog	+3.3V	Receiver Power Supply
34	V_{SS_RX}	Analog	GND	Receiver Ground Connection
35	RX_IN-	I/P	CML	Receiver Input Signal. Differential 100Ω with RX_IN+.
36	RX_IN+	I/P	CML	Receiver Input Signal. Differential 100Ω with RX_IN-.
37	V_{SS_RX}	Analog	GND	Receiver Ground Connection
38	ADC	I/P	Analog	Voltage Input to On-Chip ADC
39	DAC/TX_FAULT	O/P	Analog	Current Output For APD Loop Control. Can be configured as open-drain TX_FAULT output, pulled high externally using a 4.7kΩ to 10kΩ resistor.
40	APD_CTRL	O/P	LVTTL	Open-Drain 1V2 or 3V3 Output. Externally pulled to power or ground depending on the application.
—	EP	Analog	GND	Exposed Pad. Solder to board to provide effective thermal connection to circuit board

Detailed Description

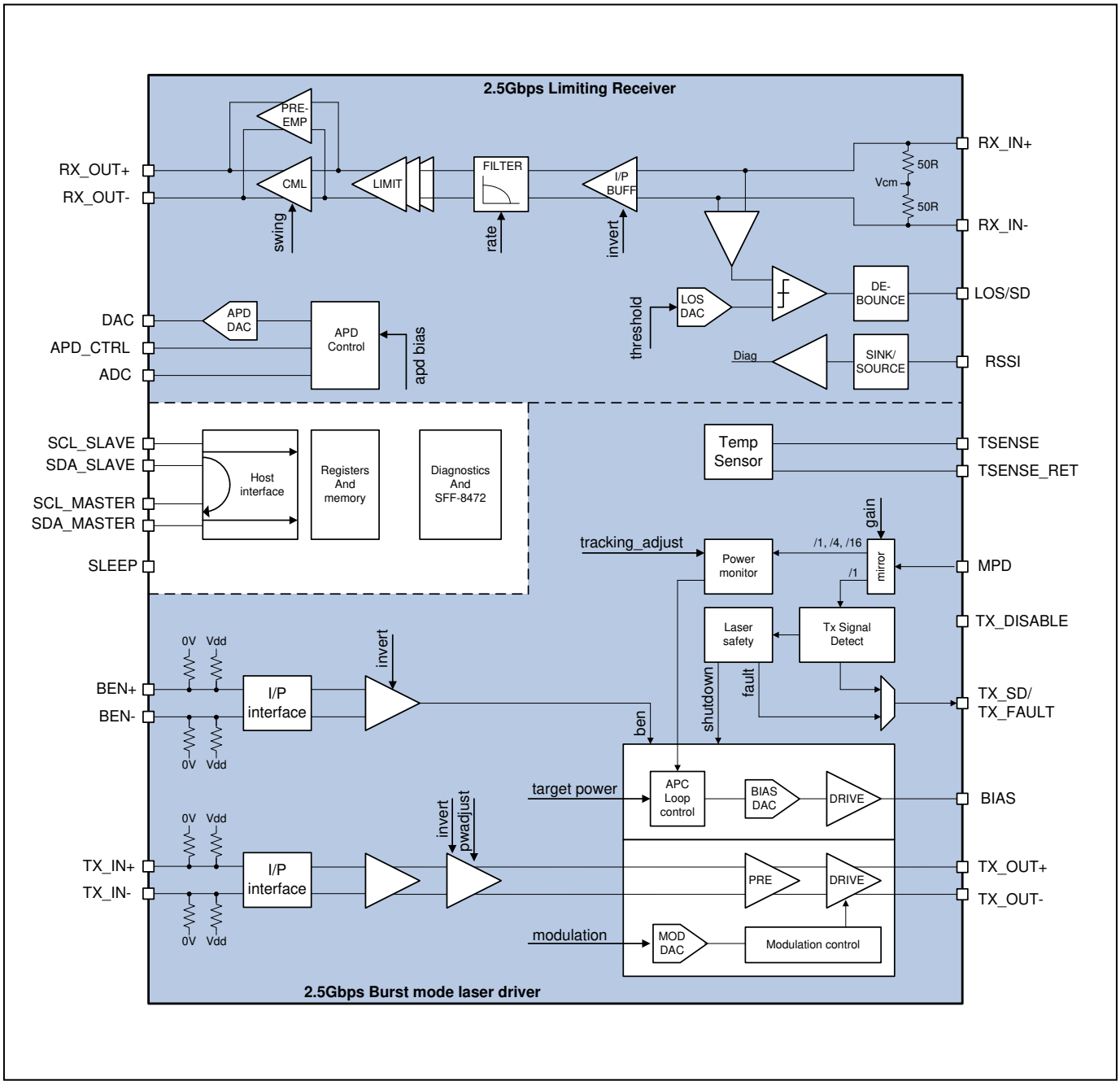


Figure 1. MAX24001 Block Diagram

Receiver Signal Path

[Control Register Address Range A4h: 90h to 93h]

The signal arriving at RX_IN is terminated with a 100Ω load to minimise return loss. An input buffer adds peaking to compensate for up to 10mm of FR4. The level of peaking is controlled by the ***rx_input_peak*** register. The signal can also be inverted using ***rx_invert***.

rx_ratesel0 or rx_ratesel1	BANDWIDTH (GHz)	BIT RATE (Gbps)
00	1	1.25
01	1.8	2.488

The received signal is then band limited to one of two rates selected by the **soft_rate_select** bit of the **system_control** register (A2h: 7Bh). If **soft_rate_select** = '0' then select **rx_ratesel0** else select **rx_ratesel1**. Filter bandwidths are nominally designed to be 0.7x the available data rates.

The CML output stage is a high-current driver that delivers a 200mV to 880mV signal from a low-impedance 50Ω output. The **rx_output_swing** register is used to control the signal at RX_OUT with 45mV resolution. Pre-emphasis may also be applied to the output signal using **rx_preemphasis**. The pre-emphasis (defined as ((B-A)/B) x 100) can be set to 0%, 2%, 6% or 10%. The pre-emphasis ratio remains relatively constant when A is adjusted.

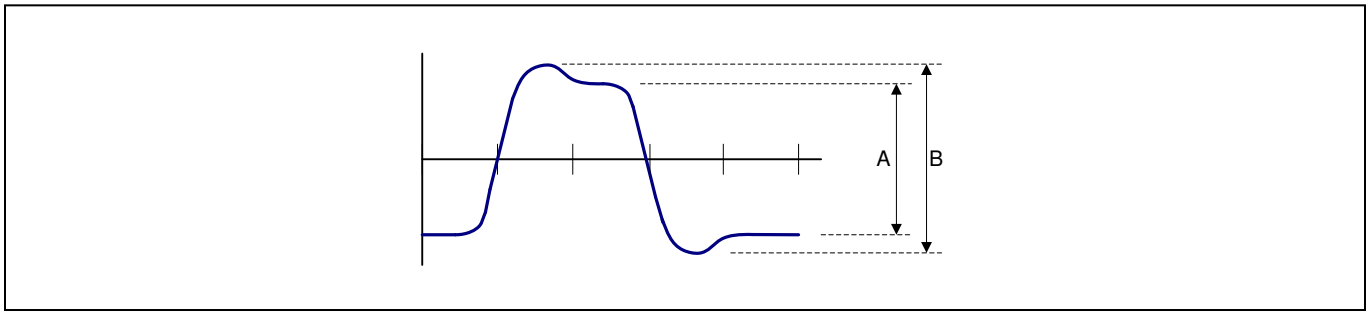


Figure 2. Rx Pre-Emphasis Control

The CML, pre-emphasis and limiting stages may be automatically powered down under loss-of-signal conditions (LOS = '1') by setting the **los_squelch** register. This feature uses the debounced LOS signal prior to any inversion caused by setting **los_invert**. Alternatively, the CML, pre-emphasis and limiting stages may be directly powered down by setting the **squelch** register.

Receiver Loss of Signal (LOS)

[Control Register Address Range A4h: 9Bh to 9Dh]

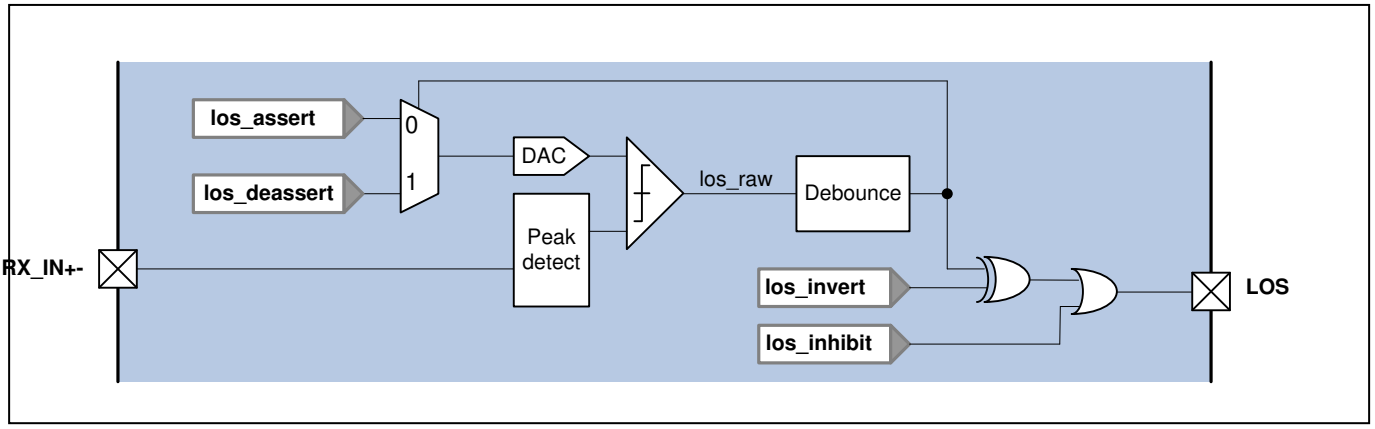


Figure 3. LOS Detection System

When the peak signal amplitude detected at RX_IN drops below the threshold level set by **los_assert** then a loss-of-signal condition is reported on the LOS pin and the **los_deassert** threshold is selected. The signal amplitude must then rise back above the threshold set by **los_deassert** before the loss-of-signal condition is removed and the **los_assert** threshold is re-selected. The two thresholds can be used to introduce a wide range of hysteresis into LOS detection. The deassert threshold level should be higher than the assert threshold for correct operation.

When the comparator output (`los_raw`) changes, the los debounce circuit holds the new value at its output for a programmable period of time controlled by **los_debounce**. Longer debounce timeout periods may be required to accommodate the much longer timeframe pulses caused by the response of the TIA AGC when the signal is suddenly interrupted. The decay of the differential signal is characterized by an unwanted signal crossover as shown in the diagram below. The unwanted pulse on `los_raw` is rejected by setting the debounce period to > 50µs.

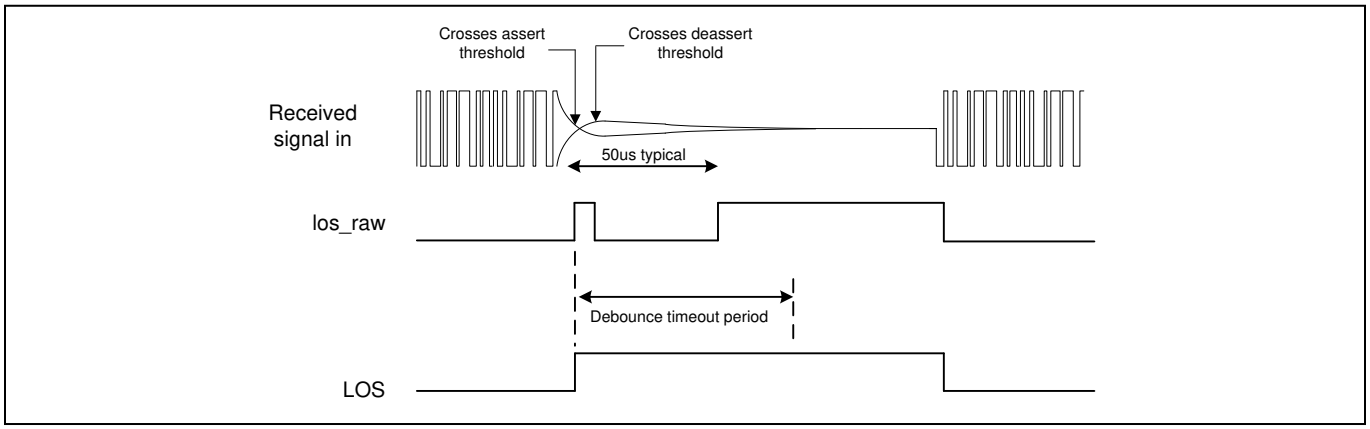


Figure 4. LOS Debounce Operation

The **los_invert** register is used to configure the pin for Signal Detect (SD) instead of LOS. An output mask (**los_inhibit**) holds the output to the LOS pin high after power-on reset until the configuration register load from EEPROM or microcontroller is complete. This avoids multiple transitions on the LOS pin during initialization, which can cause fault conditions to occur at the system level.

Transmitter Signal Path

[Control Register Address Range A4h: 9Eh to A1h]

The input to the transmitter signal path supports CML, LVPECL, HSTL, and SSTL electrical signalling schemes with a minimum of external components. The input may be either DC or AC coupled. An external 100Ω resistor provides differential termination. The internal potential dividers set the common mode level at 2.0V when the input is AC-coupled.

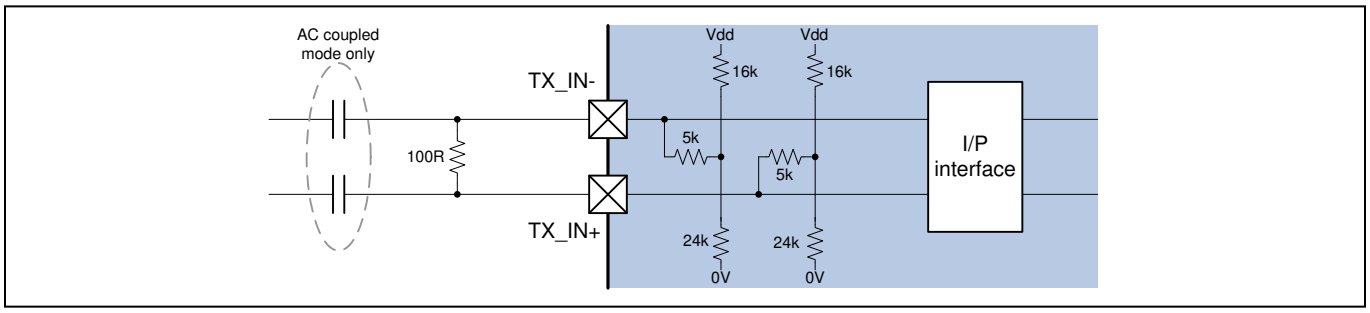


Figure 5. TX_IN and BEN Input Termination and Signal Conditioning

The laser modulation current is controlled by the **tx_moddac** register with a resolution of 375µA per LSB (nominally). This register may be set by the host, or alternatively set the **modlut_en** bit to cause the **tx_moddac** register to be automatically refreshed from the modulation lookup table (LUT) every 10ms. The modulation LUT is stored in external EEPROM at TWI slave address A6h, register address range 80h to FFh. It is indexed using the upper 7 bits of **temperature_uncal**.

If the **modramp_en** register is set then the value in **tx_moddac** ramps progressively from the old value to the new value by 1 LSB every cycle of the internal 64MHz clock. This prevents glitches from occurring in the DAC. If ramping is disabled then updates to **tx_moddac** are effective immediately. The modulation current is switched off between bursts and when the laser safety system asserts a shutdown. **burst_invert** is used to invert the differential signal on BEN±. **tx_invert** is used to invert the polarity of the transmit signal path.

Eye Optimization

The pulse width of the transmitted signal is adjusted by moving the crossing point of the eye up or down using **tx_pwadjust_dir**. Use the **tx_pwadjust_size** to control the amount of adjustment, in the direction set by **tx_pwadjust_dir**. At maximum adjustment, the zero crossing point (a) is moved by 40% of the 0-pk eye opening (b). The **tx_pwadjust_hires** register can be used to halve the adjustment step size and thus increase resolution (at the expense of halving the range).

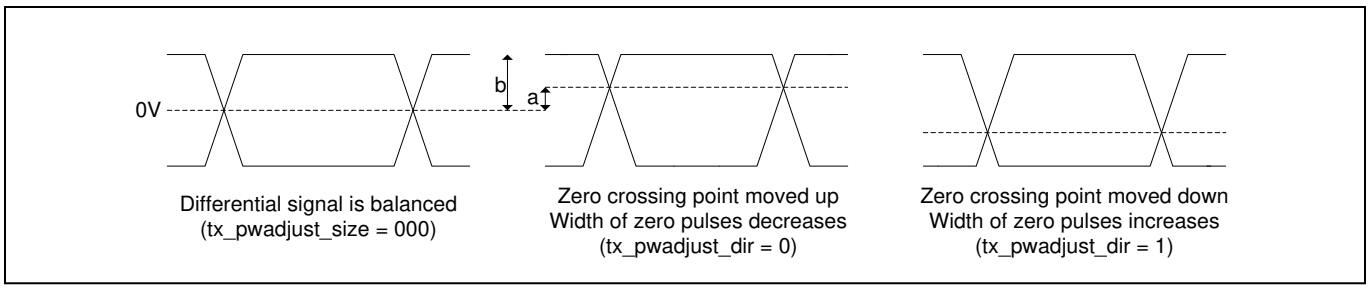


Figure 6. Crossing Point Adjustment

The **tx_snubber** register is used to snub out overshoot or undershoot in the output eye.

Tx Signal Detect

[Control Register Address Range A4h: ADh to AEh, BEh to BFh]

The Tx Signal Detect feature comprises two related areas of functionality:

For external signal and rogue ONU fault detect by the host, the MAX24001 controls the TX_SD pin as follows: TX_SD = '1' when there is light; TX_SD = '0' when there is no light from the laser.

For on-chip "Rogue ONU fault detect", the MAX24001 detects the presence of light during the burst gap. This fault condition is input to the laser safety system which can then optionally shut down the laser within 100µs of light being detected.

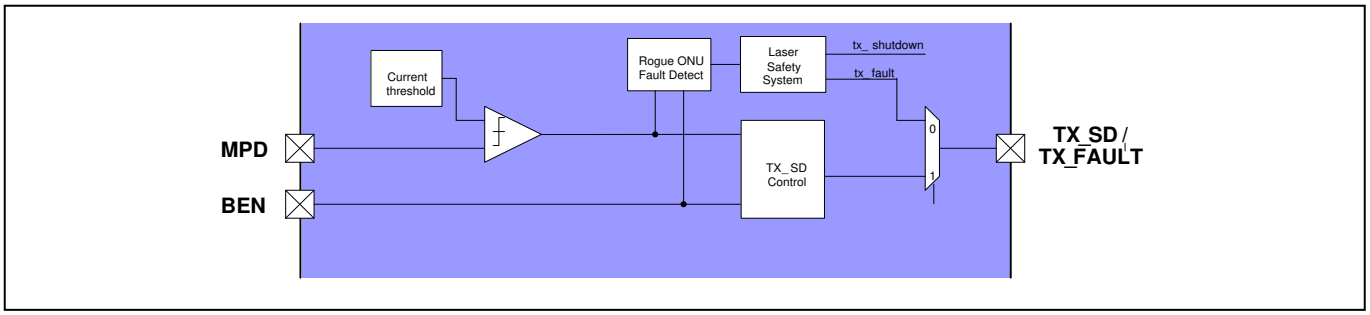


Figure 7. TX_SD Pin Signal Generation

The MPD current is compared with a threshold current set by the **txsd_threshold** register. This determines the MPD current level at which both TX_SD and rogue ONU are detected.

When BEN = '0' the TX_SD logic transfers the comparator output directly through to `tx_sd`. In addition, the Rogue ONU Fault Detect logic transfers the comparator output through to the laser safety system. The **txsd_rogueonu_delay** register specifies the delay (in cycles of the internal 64MHz clock) between the falling edge of BEN and testing for rogue ONU. The rogue_onu_fault condition is not generated during this time.

When BEN = '1' the TX_SD logic output goes high when the input from the comparator goes high. This state is latched. The `tx_sd` signal will then remain high until either the end of the burst, or until the comparator output remains low for a period of time exceeding the time defined by the **txsd_deglitch_period** register. This prevents `tx_sd` from toggling during a burst due to the pattern sensitivity of the MPD current. (During bias loop fast-start, `tx_sd` is held at '1')

Selection between TX_SD and TX_FAULT functionality is governed by the **txsd_select** register. The **txsd_allow** register holds the pin high until the configuration register load from EEPROM (or microcontroller) is complete. This avoids multiple transitions on the TX_SD pin during initialization.

Rogue ONU Behavior

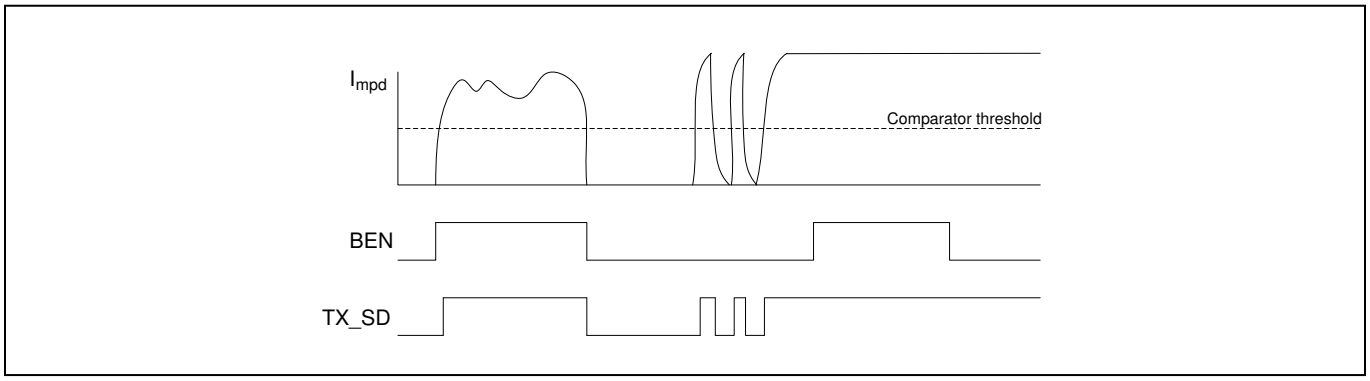


Figure 8. Rogue ONU Timing

TX_SD Behavior

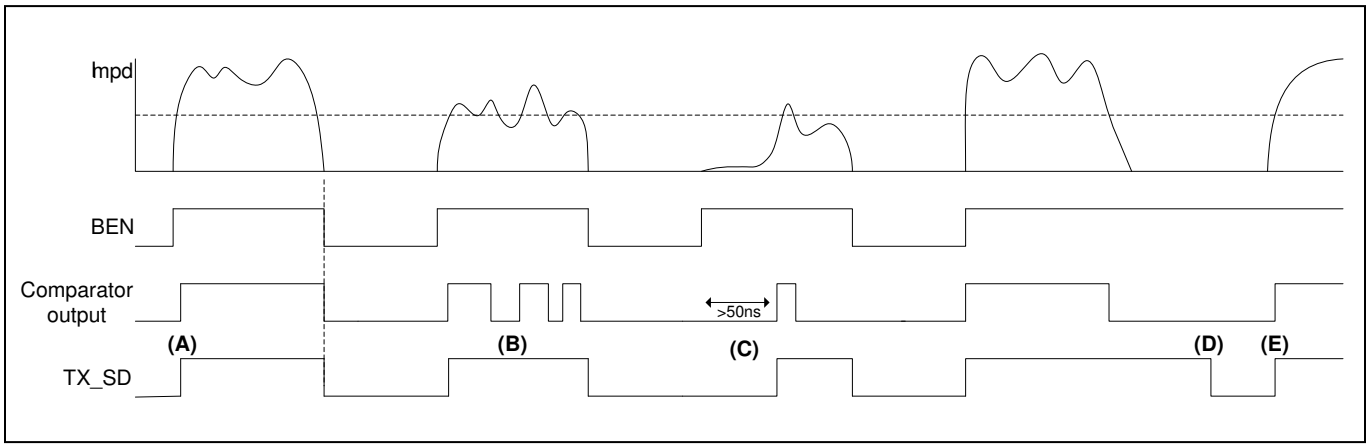


Figure 9. TX Signal Detect Timing

During the gaps the TX_SD logic is transparent and the comparator output is routed directly through to the TX_SD pin.

During the bursts:

(A) The TX_SD pin is asserted high when the MPD current first exceeds the threshold.
(B) The TX_SD pin will not toggle in response to short term fluctuations of the MPD current above and below the threshold (due to the pattern sensitivity of the MPD current).
(C) There is a requirement that the TX_SD pin responds within 50ns of the assertion of BEN. The MPD current is settled and the TX_SD circuitry can respond well within 50ns of the start of a burst. However, the MAX24001 will assert TX_SD high whenever a signal is detected during a long burst—even if the signal does not appear until well after the initial 50ns.
(D) If the laser stops outputting light during a burst, then there is a delay before TX_SD goes low. This is necessary in order to distinguish between the MPD current dipping below threshold due to a run of zeros, and the MPD current dropping below threshold due to a legitimate loss of signal. The delay is programmable using **txsd_deglitch_period**.
(E) If the signal is restored during a burst then TX_SD is asserted high again.

Laser Biasing

[Control Register Address Range A4h: A2h to A9h]

The bias current is controlled by the **tx_biasdac** register in one of six operating modes:

OPERATING MODE	DESCRIPTION	tx_biasmode <2:0>
Open loop, static	tx_biasdac only changes when it is written by the host	000
Open loop, LUT	tx_biasdac is constantly refreshed from values read from a temperature indexed lookup table (the bias LUT)	001
Closed loop, natural start	An automatic power control (APC) loop constantly adjusts tx_biasdac in order to maintain a target laser output power level. tx_biasdac defaults to near-zero after power-up and then converges naturally on the target level over a duration of time dictated by the loop bandwidth.	100
Closed loop, LUT start	The APC loop controls tx_biasdac, and tx_biasdac is preloaded from the bias LUT at power-up.	101
Closed loop, fast start	The APC loop controls tx_biasdac, and a fast-start algorithm is invoked at power-up to rapidly converge the loop on the target power level.	110
Closed loop, LUT fast start	The APC loop controls tx_biasdac. tx_biasdac is preloaded from the bias LUT at power up, and then a fast-start algorithm is invoked to rapidly converge the loop on the target power level.	111

Operational Overview

The **tx_biasmode<2:0>** register is a grouping of three individual controls registers:

tx_biasmode<0> : bias_lut_enable
tx_biasmode<1> : faststart_enable
tx_biasmode<2> : apc_enable

Open-Loop Operation

Clear the **apc_enable** register for open-loop operation.

The laser bias current is controlled by the **tx_biasdac** register with a resolution of 92.5µA per LSB (nominal). This register may be set by the host, or alternatively set the **bias_lut_enable** bit to cause the **tx_biasdac** register to be automatically refreshed from the bias lookup table (LUT) every 10ms. The bias LUT is stored in external EEPROM at TWI slave address A6h, register address range 00h to 7Fh. It is indexed using the upper 7 bits of **temperature_uncal**.

If the **biasramp_en** register is set then the value in **tx_biasdac** ramps progressively from the old value to the new by 1 LSB every cycle of the internal 64MHz clock. This prevents glitches from occurring in the DAC. If ramping is disabled then updates to **tx_biasdac** are effective immediately.

Closed-Loop Operation

Set the **apc_enable** register for closed-loop operation.

The automatic power control (APC) loop compares a value of laser output power produced by the power monitoring circuits with a target level set by **tx_apc_target**. This proportional error value is scaled using the **apc_loop_gain** and is then used to adjust the value of **tx_biasdac** (which has a number of internal precision extension bits). The **apc_loop_gain** register thus controls the bandwidth of the APC loop.

Since the bandwidth of the loop is not very high, it is desirable to set the **tx_biasdac** register to a point as close as possible to the target laser power level before the APC loop takes over. This is achieved by preloading the **tx_biasdac** register with a value from the bias LUT and/or running a search algorithm (referred to as fast-start). These actions are both triggered by the **bias_lut_enable** and **faststart_enable** bits. When these bits are set, then a table lookup or fast-start will occur at the next available opportunity. Once the lookup or fast-start has occurred then these bits are cleared. The host may therefore re-trigger fast/lut start by resetting **bias_lut_enable** and **faststart_enable** at any time. The bits are also set automatically as follows:

On power-up: **tx_biasmode** is configured from EEPROM

During SLEEP: The value in **faststart_after_sleep** is transferred to **faststart_enable**
The value in **bias_lut_after_sleep** is transferred to **bias_lut_enable**

During TX_DISABLE: The value in **faststart_after_txdisable** is transferred to **faststart_enable**
The value in **bias_lut_after_txdisable** is transferred to **bias_lut_enable**

Thus, the required loop behavior when the laser is enabled can be independently configured for reset, sleep mode and tx disable. This is further illustrated in the figure below:

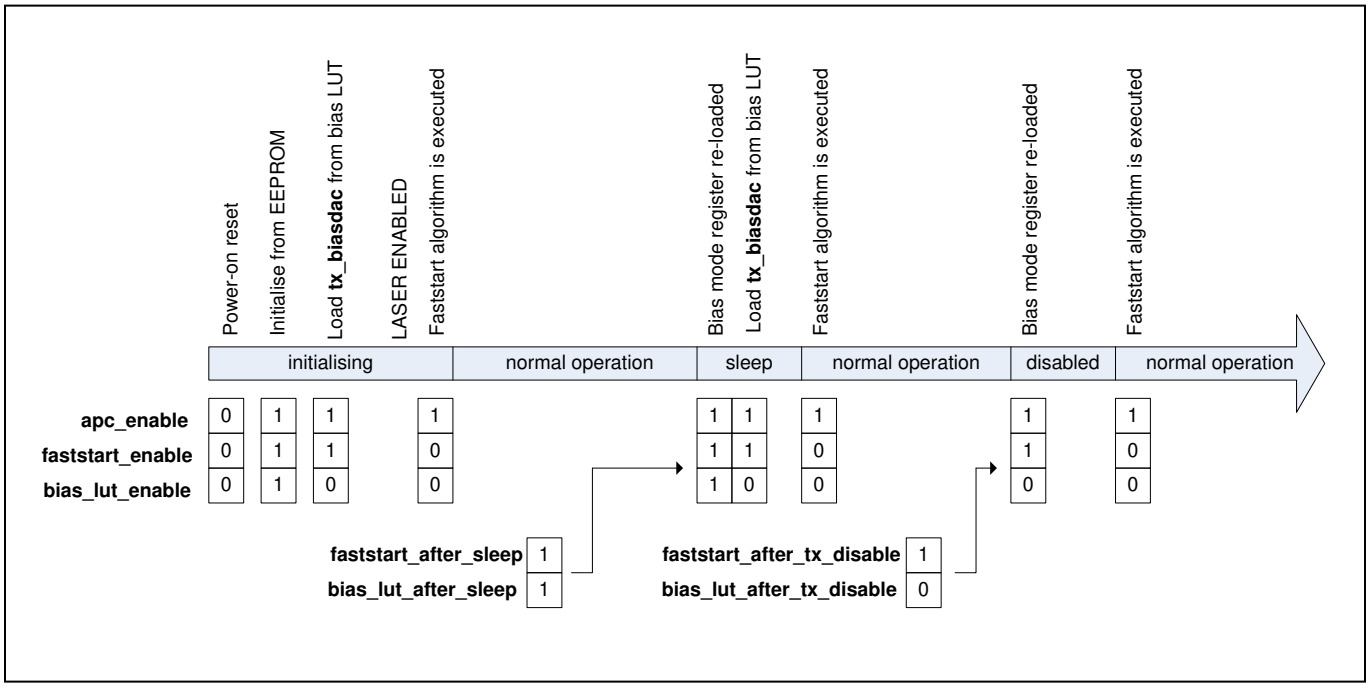


*Figure 10. Behavior of the **tx_biasmode** Register in Closed-Loop Mode*

Fast-Start Algorithm

[Control Register Address Range A4h: AAh to ACh]

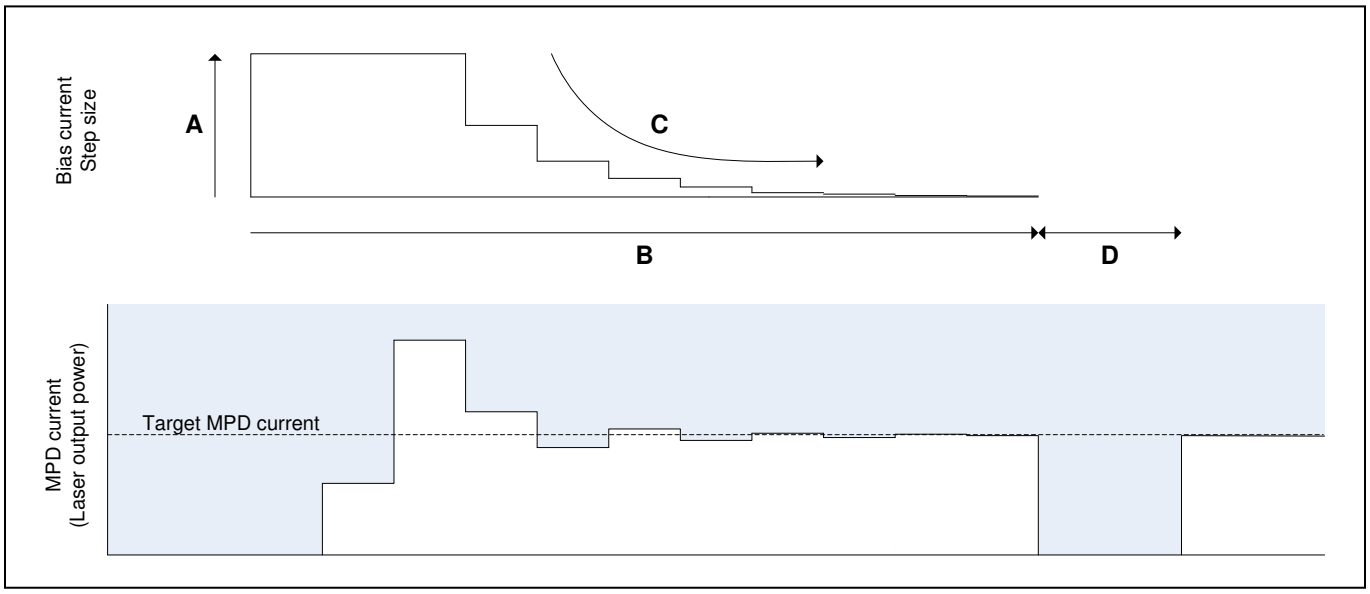


Figure 11. Fast-Start Algorithm Timing

During fast-start, the MAX24001 is temporarily reconfigured. The modulation driver sinks a constant current of $I_{MOD}/2$ on TX_OUT to represent the contribution made by the signal current to the average power. The power monitoring circuit is reconfigured to supply a direct comparison between the received MPD current and the target MPD current. The process of making a change to bias current and then a subsequent comparison of MPD current and target current is referred to as iteration. An iteration has a fixed duration (nominally 62ns).

Initially, the bias current is stepped up on every iteration until the MPD current exceeds the threshold. The initial bias current step size A is ideally ½ the modulation current, the rationale being that this is the largest step which can be taken whilst ensuring that the P1 power level is not exceeded. More generally, the initial step size is defined as A = (**tx_fstart_initial**/256) x I_{MOD}.

When the target level is exceeded the step size then decays (C). Halving the step size every iteration amounts to a binary search. In practice, incomplete settling of the loop can result in a small overshoot of the target current level. It is therefore recommended that each step is slightly more than 0.5x the previous step. This is configurable using the **fstart_decay** register. The **fstart_decay** register determines the multiplication factor applied to the step size on each subsequent iteration of the fast start algorithm.

fstart_decay	STEP DECAY MULTIPLIER
100000	32/64 = 0.5
100001	33/64 = 0.516
100010	34/64 = 0.531
100011	35/64 = 0.547
100100	36/64 = 0.563
100101	37/64 = 0.5785
..	..
101110	46/64 = 0.719
101111	47/64 = 0.734

The direction of each current step depends on whether the measured MPD current is above or below the target level. The number of iterations B is controlled by the **fstart_duration** register. The maximum number of iterations which can be guaranteed to complete within 3 x 400ns bursts is 15.

At the end of the fast-start algorithm, the laser output stage switches from sinking DC $I_{MON}/2$ on TX_OUT to full amplitude signal. This may result in a brief current spike. A facility is provided to optionally shut down the modulation current through the laser during this transition period (D). Use the **fstart_recovery_en** and **fstart_recovery_time** registers to shut down the modulation current for 0, 1 or 2 iterations.

APC Loop Bandwidth

The **apc_loop_gain** register adjusts the gain of the APC control loop. Loop bandwidth is calculated as a function of **apc_loop_gain**:

$$\text{Bandwidth} = \frac{2^{\text{apc\_loop\_gain - 15}} * k_{elec} * k_{mpd} * (\text{biasdac\_lsb} * 4) * f_{clock}}{2 * \pi * 16 * \text{mondac\_lsb}}$$

$$= 2^{\text{apc\_loop\_gain - 15}} * k_{elec} * k_{mpd} * 3.02\text{x}10^{6}$$

Where: mondac_lsb = 0.78µA
biasdac_lsb = 92.5µA
f_{CLOCK} = 64MHz (typical)
kmpd = 0.0625 when **mpd_range** = 10
0.25 when **mpd_range** = 01
1 when **mpd_range** = 00

apc_loop_gain	GAIN
0000	2^{-15}
0001	2^{-14}
0010	2^{-13}
:	:
1100	2^{-3}
1101	2^{-2}
1110	2^{-1}
1111	1

Power Monitoring

A power monitoring circuit generates a digital measure of MPD current (laser power) based on time-averaged samples taken during bursts when the laser is enabled. It has three settings in order to accommodate the wide range of monitor photodiode currents. The range setting (**mpd_range**) is chosen at the time that the module is calibrated, and does not change during normal operation of the APC loop. The unfiltered, 8-bit digital measure of MPD current is used internally by the APC loop.

mpd_range	PD MIRROR GAIN	I_{MON} OPERATING RANGE (µA)
00	1	40 to 200
01	1/4	100 to 800
10	1/16	400 to 2000

Tracking error in the TOSA means that the MPD current may vary over temperature in a nonlinear way for a given laser optical power. If the temperature-indexed tracking error lookup table (LUT) is enabled then the digital measure of MPD current is multiplied by the values read from the LUT. Each entry in the LUT represents a number in the range 0.5 (00h) to 1.5 (FFh), and 80h represents unity gain.

Set the **trackinglut_en** bit to enable this feature. A correction factor is retrieved from the tracking error LUT every 10ms. This LUT is stored in external EEPROM at TWI slave address A8h, register address range 80h to FFh. It is indexed using the upper 7 bits of **temperature_uncal**.

The digital measure of MPD current (including tracking error compensation) is used by the APC loop to control bias current.

Power Reporting

For power reporting purposes, the power monitor output is low-pass filtered to suppress the pattern sensitivity of the MPD current. This filter bandwidth is programmable using the mon_bandwidth register. Bandwidth = $64/(2\pi \times 2^{(15-n)})$ where n is the 4-bit integer mon_bandwidth value up to a maximum of 14. The filtered measure of laser power can be read from the txpower_uncal register.

mon_bandwidth	BANDWIDTH at f_{clock} = 64MHz
0000	311Hz
0001	622Hz
..	..
1000	80kHz
..	..
1110	5.1MHz
1111	No filtering

The **mpd_range** should be set at a level which accommodates the expected range of MPD current. The MAX24001 is not designed to automatically range switch during normal APC loop operation. However, if the APC loop fails and the power monitor saturates then the **mpd_range** will temporarily switch so that power reporting can cover the full 0 to 2mA range of photodiode current. The range then recovers back to the original setting if the power monitor value drops back below 64.

Power Leveling

The **power_levelling** register implements GPON power levelling. Set to 00, 01, or 1x to reduce the modulation amplitude set by **tx_moddac** by x1, x0.5 and x0.25, respectively. This register will also reduce the power level by having the same effect on the output of the **tx_apc_target** register. Power levelling does not affect the bias current in open-loop mode.

Laser Safety

[Control Register Address Range A4h: AFh to B3h]

The laser safety system generates two signals, `tx_fault_int` and `tx_shutdown_int`. `Tx_fault_int` is pure status. It reports via both register and TX_FAULT pin whether one or more enabled fault conditions have occurred. The TX_FAULT pin can be configured to appear at pin 21 or 39 using **pin_config0**. `Tx_shutdown_int` is a control signal. It disables the bias and modulation currents to the laser when one or more enabled fault conditions have occurred.

Fault Conditions

The fault conditions which affect `tx_fault_int` and `tx_shutdown_int` are:

Bias Fault	This occurs when the BIAS pin is shorted to ground.
APC Fault	This occurs when the MPD pin is shorted to ground.
VREF Fault	This occurs when the RREF pin is shorted to ground.
VDD Fault	This occurs when brownouts are detected on TX or TXO.
Tx Disable Fault	Is given by: (TX_DISABLE XOR **tx_disable_invert**) OR **soft_tx_disable** where TX_DISABLE is the pin value and **soft_tx_disable** is in SFF-8472 **status_control**.
Soft Tx Fault	This occurs when the **soft_tx_fault** bit in **software_faults** register is set.
RogueOnu Fault	If the laser is on during a gap between bursts then this fault condition is generated.

Alarm Fault	This occurs when one or more of the SFF-8472 DDM alarm flags are set to '1'. The flags which contribute to Alarm Fault are programmable via **ls_alarmflag_en**.

When the laser is in shutdown then the bias fault condition is ignored by the laser safety system. When `tx_shutdown` is deasserted there is a 250µs delay before the bias fault condition is used. This allows the circuit which detect a ground short on the bias pin time to settle before the bias fault condition is seen by the laser safety system.

Architecture

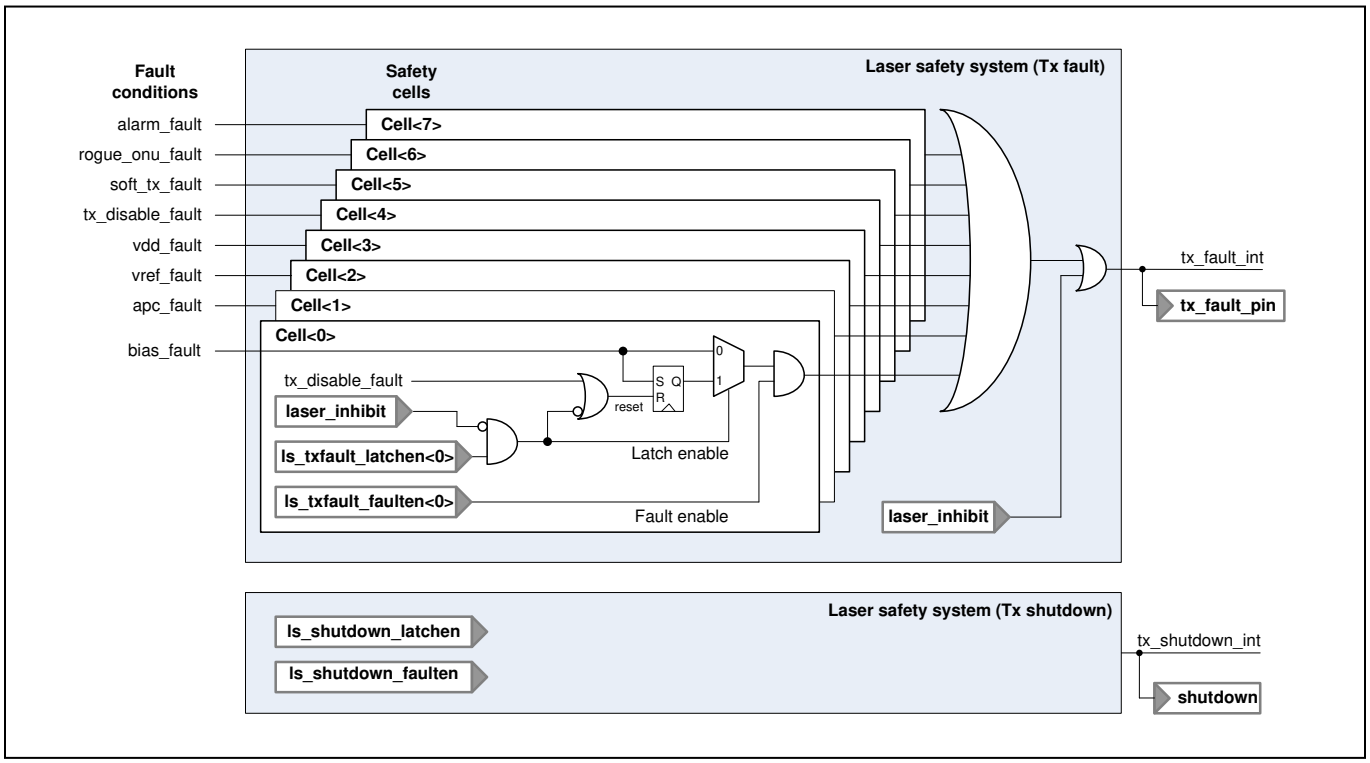


Figure 12. Laser Safety System

The laser safety system (Tx fault) generates the `tx_fault_int` signal. The status of this signal can be accessed in the SFF-8472 **status_control** register. The signal is also multiplexed onto the TX_FAULT/TX_SD pin.

Every safety cell has its own pair of latch enable and fault enable control register bits. The fault condition can only propagate through to the output when **_faulten** = '1'. When **_latchen** = '1' a latched version of the fault condition is used. The latch is held in reset when latching is disabled or when the `tx_disable_fault` signal is asserted. Note that `tx_disable_fault` is also a fault condition signal.

When it is asserted, the **laser_inhibit** signal holds all latches in reset and forces the `tx_fault_int` signal to '1'. Note that after the power-on reset, **laser_inhibit** is enabled. During initialization **pin_config** is the last configuration register to be loaded from EEPROM and therefore has the effect of clearing **laser_inhibit** and thus enabling the laser.

ls_fault_status reports the status of the fault conditions at the inputs to the safety cells.

The laser safety system is fully replicated for controlling laser shutdown. The system uses the **ls_shutdown_faulten** and **ls_shutdown_latchen** registers and produces the `tx_shutdown_int` signal for disabling the modulation and bias currents. The internal architecture is otherwise the same as the system for Tx Fault. The **shutdown** register can be found in **hardware_status**.

The module Tx supply (V_{CC_TX}) can be used in some applications to shut down the laser. This is supported in MAX24001 by detecting the removal of V_{CC_TX} on the V_{DD_TXO} pin. V_{CC_TX} is connected to V_{DD_TXO} as shown in Figure

13. A shutdown is then asserted if the voltage falls below 2.7V. If the connection between V_{CC_TX} and V_{DD_TXO} is not used, V_{DD_TXO} must be connected to another supply.

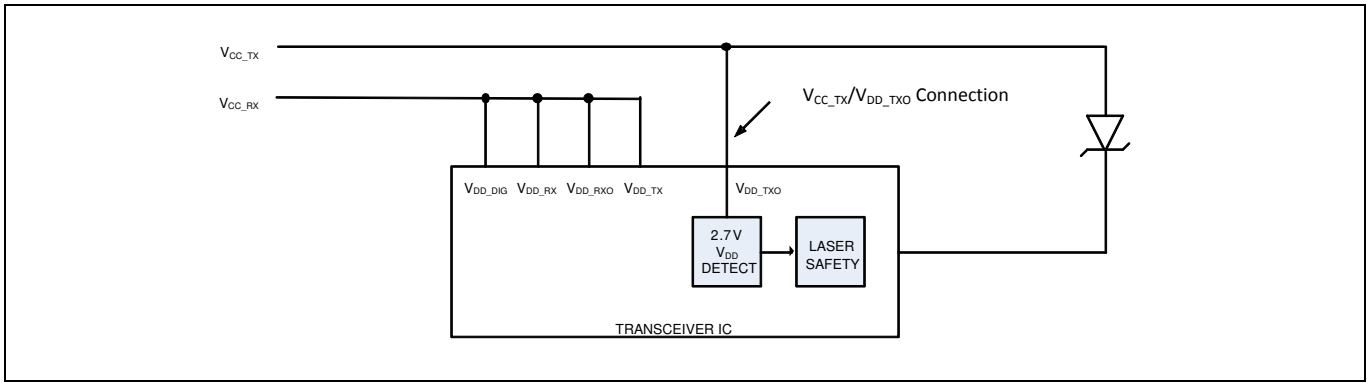


Figure 13. V_{DD_TXO} Configured to Assert Laser Shutdown

Temperature Sensor

[Control Register Address Range A4h: B6h, B9h, C1h]

The MAX24001 includes an integrated temperature sensor that reports the module temperature at the sensor transistor. The **temp_ext_sensor** register selects between an internal transistor or an external PNP transistor connected to the TSENSE and TSENSE_RET pins. If an external transistor is used then the PCB tracks connecting an external PNP transistor to the chip each have resistance << 1Ω. i.e. the tracks must be kept as short as possible. The temperature sensor reports a value in **temperature_uncal** once every 65ms. Resolution is approximately 0.8C per LSB of **temperature_uncal**. Part-to-part accuracy is optimized by adjusting **temp_calibrate** until each part reports the same value of **temperature_uncal** at a common temperature.

Setting **leave_pu** and **tempsense_pu** enables the temperature sensor to be in a power-saving mode by powering down between reads.

APD Controller

[Control register address range A4h: 94h]

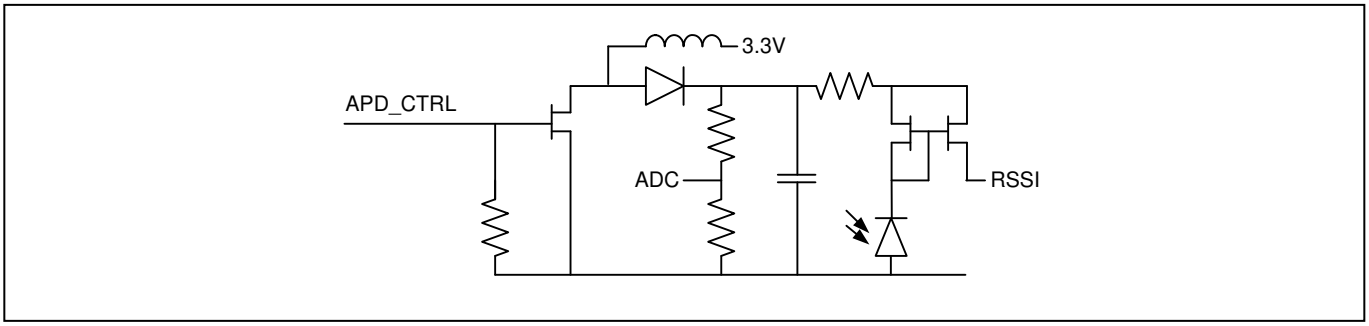


Figure 14. APD Biasing Application

Figure 14 shows a simplified arrangement for controlling the APD bias voltage, whereby the FET is switched by a pulse width modulated signal. The duty cycle can be used to control the voltage across the capacitor. This voltage can be sampled at the tap point of the potential divider. The MAX24001 provides functions which support this approach.

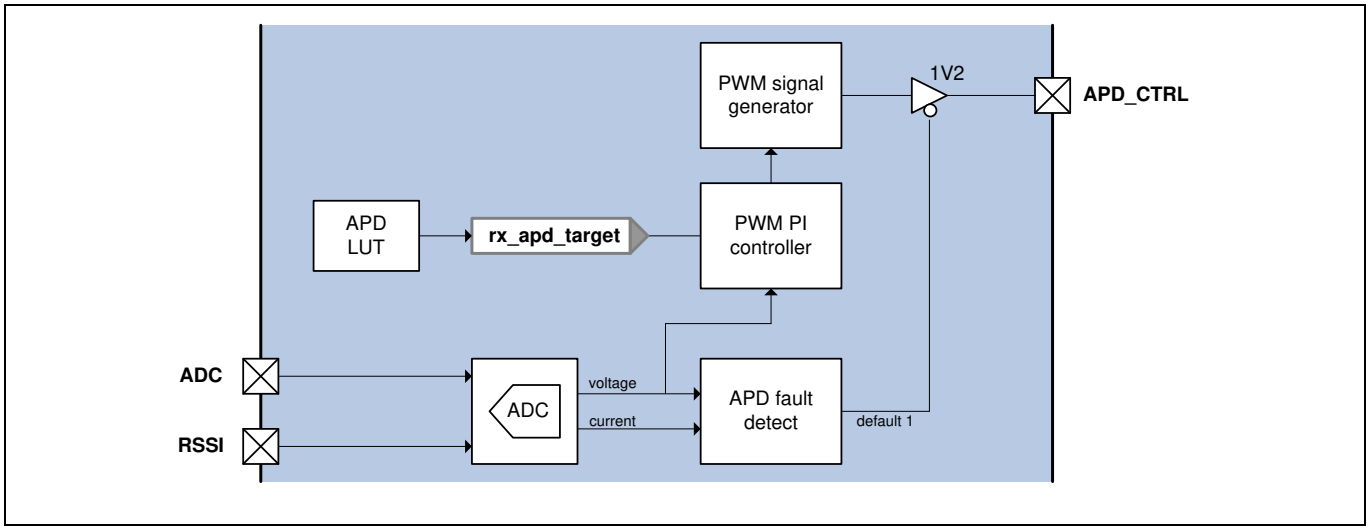


Figure 15. APD Biasing Control Loop Components

The PWM frequency can be configured to be 250kHz, 500kHz, 1MHz or 2MHz by **pwm_frequency**. The 8-bit value of **rx_apdpwm** adjusts the duty cycle from 0/256 to 255/256. **high_v** adjusts the drive level to 1.2V or 3.3V.

The APD controller adjusts the value of **rx_apdpwm** according to the proportional and integral gain setting of the loop in registers **k_proportional** and **k_integral** such that the voltage level sampled on the ADC pin converges on the target value **rx_apd_target**. The target value apdlut_en may be fixed, or it may be actively refreshed from the temperature indexed APD lookup table (LUT) when **target_lut_enable** is set. This LUT is stored in EEPROM at two-wire slave address A8h, register address range 00h to 7Fh. The LUT is indexed by **temperature_uncal**.

When the APD controller is active, a limit may be imposed on the maximum PWM duty using **max_duty**.

APD Controller—Additional features

APD safety features are also implemented. If the sampled value of RSSI current exceeds **rx_apd_i_threshold**, or the sampled voltage on the ADC pin exceeds **rx_apd_v_threshold** then the APC_CTRL pin driver is disabled (Hi-Z). Set the thresholds to FFh to disable this feature.

The APD controller is disabled when **k_proportional** and **k_integral** are both zero. The value in **rx_apdpwm** can be written directly, or will be periodically refreshed from the APD LUT if **pwm_lut_enable** is set. The polarity of the output on APD_CTRL can be inverted by setting **pwm_invert** to '1'.

If an external control loop is used (for example, using an external DC-DC converter) then this loop could be controlled by the DAC pin. The DAC is controlled from the **rx_apddac** register. This will be periodically refreshed from the APD LUT if **dac_lut_enable** is set. In this arrangement, the APD_CTRL pin can be used to control the shutdown input pin of the DC-DC converter.

Digital Diagnostics

Data Generation

[Control Register Address Range A4h: B4h to B5h, E6h to EAh]

Temperature, supply voltage, laser bias current, transmit power, and received power are all periodically sampled.

Temperature

The uncalibrated temperature can be read from the **temperature_uncal** register.

Supply Voltage

Select between Tx and Rx supply voltages using **adc_supplysel**, and adjust the sampling rate using **supply_bandwidth**. The uncalibrated supply voltage can be read from the **supply_uncal** register.

Tx Bias Current

The bias current measured during a burst will continue to be reported between bursts, irrespective of the length of the gap. If the laser is deliberately shutdown by the laser safety system or by asserting TX_DISABLE then Bias Current reports zero and the low alarm/warning flags are set. The uncalibrated bias current is read from the **bias_uncal** register.

Tx Power

The Tx Power measured during a burst will continue to be reported between bursts, irrespective of the length of the gap. If the laser is deliberately shutdown by the laser safety system or by asserting TX_DISABLE then Tx Power reports zero and the low alarm/warning flags are set. The uncalibrated Tx Power is read from the **txpower_uncal** register.

Rx Power

The RSSI pin can both source and sink a current (**rx_rssi_sink**) which is proportional to the optical power incident on the receiver. Resolution can be enhanced by applying additional gain (x1, x1.5 or x2) to the current at the RSSI pin using the **rx_rssi_scale** register (see **los_rssi_config**).

For Rx power measurement, the ADC is used in nonlinear “3-slope” mode. This provides both wide dynamic range and high resolution at low powers. The uncalibrated, 3-slope encoded value of Rx Power is read from the **rxpower_uncal** register.

RSSI CURRENT RANGE (µA)			***rxpower_uncal***
GAIN x1	**GAIN x1.5**	**GAIN x2**	
0 to 16 16 to 208 208 to 1232	0 to 11 11 to 139 139 to 821	0 to 8 8 to 104 104 to 616	0 to 32 32 to 128 128 to 255

Adjust the Rx Power sampling bandwidth using **rxpower_bandwidth**.