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Data Sheet
November 2016

MAX24287
1Gbps Parallel-to-Serial MII Converter

General Description

The MAX24287 is a flexible, low-cost Ethernet interface conversion IC. The parallel interface can be configured for GMII, RGMII, TBI, RTBI, or 10/100 MII, while the serial interface can be configured for 1.25Gbps SGMII or 1000BASE-X operation. In SGMII mode, the device interfaces directly to Ethernet switch ICs, ASIC MACs, and 1000BASE-T electrical SFP modules. In 1000BASE-X mode, the device interfaces directly to 1Gbps 1000BASE-X SFP optical modules. The MAX24287 performs automatic translation of link speed and duplex autonegotiation between parallel MII MDIO and the serial interface.

This device is ideal for interfacing single-channel GMII/MII devices such as microprocessors, FPGAs, network processors, Ethernet-over-SONET or -PDH mappers, and TDM-over-packet circuit emulation devices. The device also provides a convenient solution to interface such devices with electrical or optical Ethernet SFP modules.

Applications

Any System with a Need to Interface a Component with a Parallel MII Interface (GMII, RGMII, TBI RTBI, 10/100 MII) to a Component with an SGMII or 1000BASE-X Interface

Switches and Routers

Telecom Equipment

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX24287ETK+	-40°C to +85°C	68 TQFN-EP*
MAX24287ETK+T	-40°C to +85°C	68 TQFN-EP* Tape and Reel

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Block Diagram appears on page 7.

Register Map appears on page 42.

Highlighted Features

- **Bidirectional Wire-Speed Ethernet Interface Conversion**
- **Can Interface Directly to SFP Modules and SGMII PHY and Switch ICs**
- **Serial Interface Configurable as 1000BASE-X or SGMII Revision 1.8 (4-, 6-, or 8-Pin)**
- **Parallel Interface Configurable as GMII, RGMII, TBI, RTBI, or 10/100 MII**
- **Serial Interface Has Clock and Data Recovery Block (CDR) and Does Not Require a Clock Input**
- **Translates Link Speed and Duplex Mode Negotiation Between MDIO and SGMII PCS**
- **Supports 10/100 MII or RGMII Operation with SGMII Running at the Same Rate**
- **Configurable for 10/100 MII DTE or DCE Modes (i.e., Connects to PHY or MAC)**
- **Can Also Be Configured as General-Purpose 1:10 SerDes with Optional Comma Alignment**
- **Supports Synchronous Ethernet by Providing a 25MHz or 125MHz Recovered Clock and Accepting a Transmit Clock**
- **Can Provide a 125MHz Clock for the MAC to Use as GTXCLK**
- **Accepts 10MHz, 12.8MHz, 25MHz or 125MHz Reference Clock**
- **Software Control Through MDIO Interface**
- **GPIO Pins Can Be Configured as Clocks, Status Signals and Interrupt Outputs**
- **1.2V Operation with 3.3V I/O**
- **Small, 8mm x 8mm, 68-Pin TQFN Package**

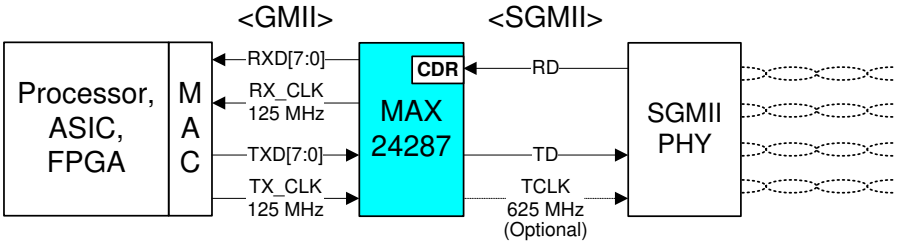
Table of Contents

List of Figures

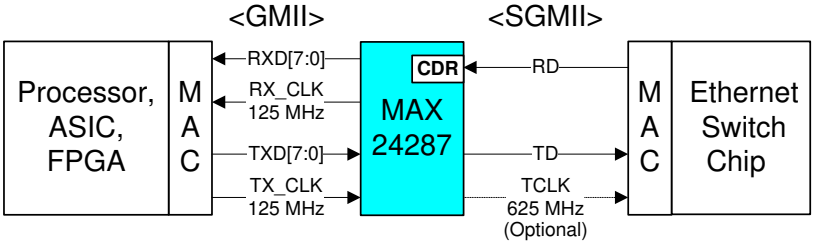
List of Tables

1. Application Examples

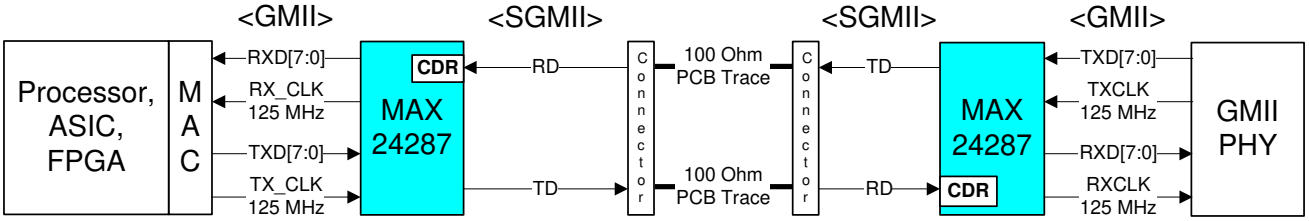
a) Copper Media



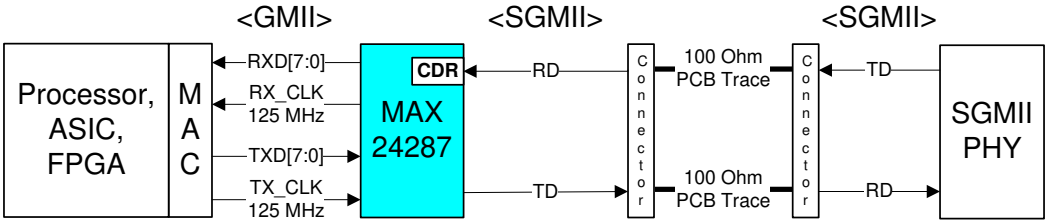
b) Connect Parallel MII Component to SGMII Component



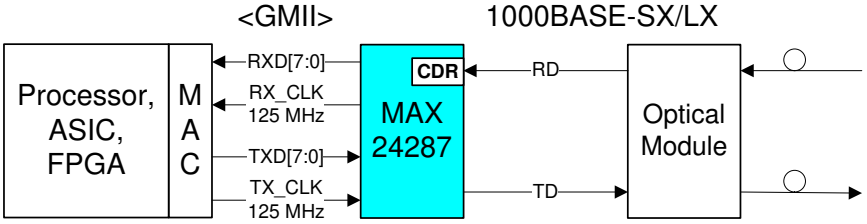
c1) Long PCB Trace Card-to-Card



c2)

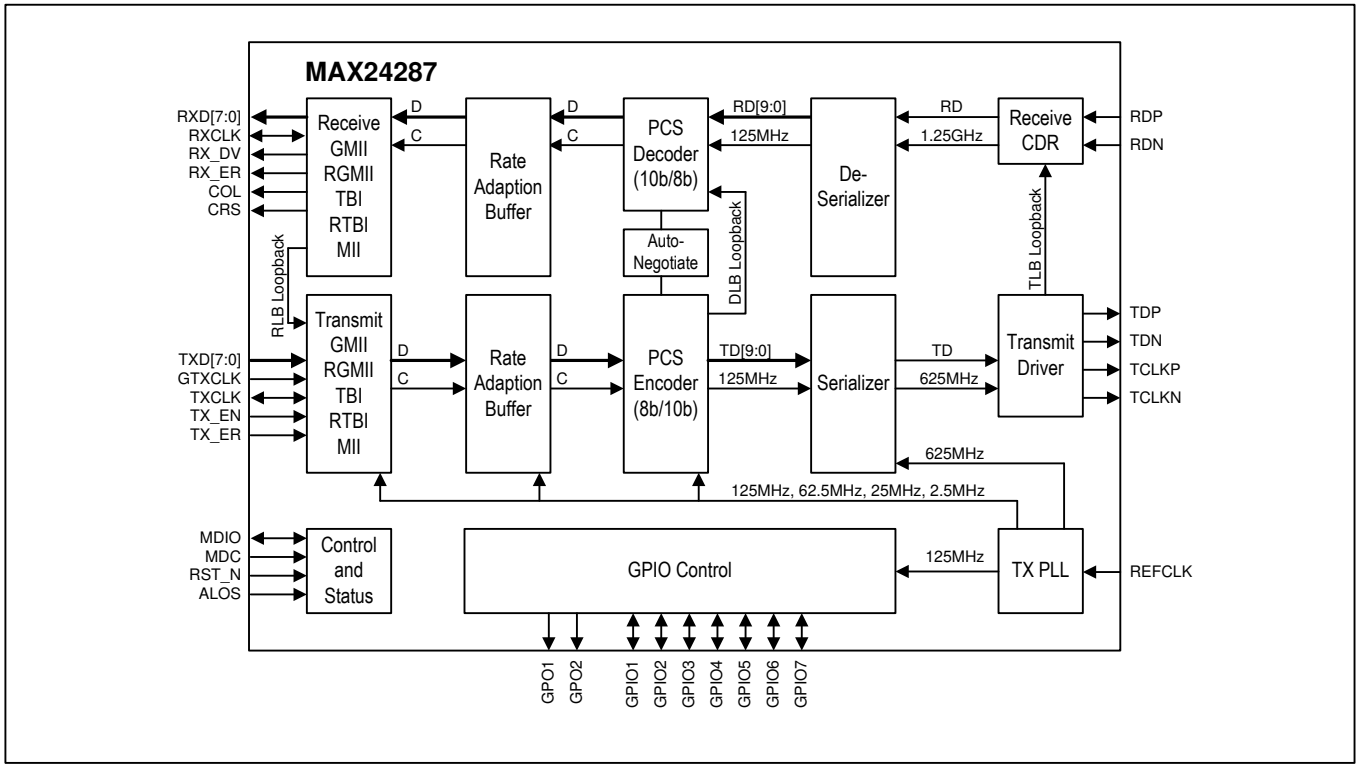


d) Fiber Module



2. Block Diagram

Figure 2-1. Block Diagram



3. Detailed Features

General Features

- High-speed MDIO interface (12.5MHz slave only) with optional preamble suppression
- Operates from a 10, 12.8, 20, 25, or 125MHz reference clock
- Optional 125MHz output clock for MAC to use as GTXCLK

Parallel-Serial MII Conversion Features

- Bidirectional wire-speed interface conversion
- Serial Interface: 1000BASE-X or SGMII revision 1.8 (4-, 6-, or 8-Pin)
- Parallel Interface: GMII, RGMII (10, 100 and 1000Mbps), TBI, RTBI or 10/100 MII (DTE or DCE)
- 8-pin source-clocked SGMII mode
- 4-pin 1000BASE-X SerDes mode to interface with optical modules
- Connects processors with parallel MII interfaces to 1000BASE-X SFP optical modules
- Connects processors with parallel MII interfaces to PHY or switch ICs with SGMII interfaces
- Interface conversion is transparent to MAC layer and higher layers
- Translates link speed and duplex mode between GMII/MII MDIO and SGMII PCS
- Configurable for 10/100 MII DTE or DCE Modes (i.e., connects to PHY or MAC)

Synchronous Ethernet Features

- Receive path bit clock can be output on a GPIO pin to line-time the system from the Ethernet port
- Transmit path can be frequency-locked to a system clock signal connected to the REFCLK pin

4. Acronyms, Abbreviations, and Glossary

- DCE Data Communication Equipment
- DDR Dual Data Rate (data driven and latched on both clock edges)
- DTE Data Terminating Equipment
- PCB Printed Circuit Board
- PHY Physical. Refers to either a transceiver device or a protocol layer

- Ingress The serial (SGMII) to parallel (GMII) direction
- Egress The parallel (GMII) to serial (SGMII) direction
- Receive The serial (SGMII) to parallel (GMII) direction
- Transmit The parallel (GMII) to serial (SGMII) direction

5. Pin Descriptions

Note that some pins have different pin names and functions under different configurations.

Table *5-1. Pin Type Definitions*

Type	Definition
I	Input
Idiff	Input, differential
Ipu	Input, with pullup
Ipd	Input, with pulldown
IO	Bidirectional
IOr	Bidirectional, sampled at reset
IOz	Bidirectional, can go high impedance
O	Output
Odiff	Output, differential (CML)
Oz	Output, can go high impedance

Table 5-2. Detailed Pin Descriptions – Global Pins (2 Pins)

Pin Name	PIN #	Type	Pin Description
RST_N	67	I	**Reset** (active low, asynchronous) This signal resets all logic, state machines and registers in the device. Pin states are sampled and used to set the default values of several register fields as described in 6.1. RST_N should be held low for at least 100µs. See section 6.3.1.
REFCLK	68	I	**Reference Clock** This signal is the reference clock for the device. The frequency can be 10MHz, 12.8MHz, 25MHz or 125MHz ± 100 ppm. At reset the frequency is specified using the RXD[3:2] pins (see section 6.1). The REFCLK signal is the input clock to the TX PLL. See section 6.9. Note: REFCLK frequency cannot be changed dynamically among the frequencies listed above. To change REFCLK frequency, (1) power down MAX24287, (2) change REFCLK frequency, then (3) power up MAX24287. REFCLK is an analog input that is internally biased with a 10kΩ resistor to 1.2V. This support AC-coupling if desired.

Pin Name	PIN #	Type	Pin Description
TEST0	45	I	**Factory Test.** Connect to DVDD33.
TEST1	64	I	**Factory Test.** Connect to DVDD33 or DVSS.
TEST2	63	I	**Factory Test.** Connect to DVDD33 or DVSS.
TEST3	62	I/O	**Factory Test.** Connect to DVDD33 or DVSS.

Table 5-3. Detailed Pin Descriptions – MDIO Interface (2 Pins)

Pin Name	PIN #	Type	Pin Description
MDC	41	I	**MDIO Clock.** MDC is the clock signal of the 2-wire MDIO interface. It can be any frequency up to 12.5MHz. See section 6.4.
MDIO	42	IOz	**MDIO Data.** This is the bidirectional, half-duplex data signal of the MDIO interface. It is sampled and updated on positive edges of MDC. IEEE 802.3 requires a 2kΩ±5% pulldown resistor on this signal at the MAC. See section 6.4.

Table 5-4. Detailed Pin Descriptions – JTAG Interface (5 pins)

Pin Name	PIN #	Type	Pin Description
JTRST_N	43	I	**JTAG Test Reset** (active low). Asynchronously resets the test access port (TAP) controller. JTRST_N should be held low during device power-up. If not used, JTRST_N can be held low or high after power-up. See section 7.2.18.
JTCLK	21	I	**JTAG Test Clock.** This clock signal can be any frequency up to 10MHz. JTDI and JTMS are sampled on the rising edge of JTCLK, and JTDO is updated on the falling edge of JTCLK. If not used, connect to DVDD33 or DVSS. See section 7.2.18.
JTMS	22	I	**JTAG Test Mode Select.** Sampled on the rising edge of JTCLK. Used to place the port into the various defined IEEE 1149.1 states. If not used, connect to DVDD33. See section 7.2.18.
JTDI	23	I	**JTAG Test Data Input.** Test instructions and data are clocked in on this pin on the rising edge of JTCLK. If not used, connect to DVDD33. See section 7.2.18.
JTDO	44	Oz	**JTAG Test Data Output.** Test instructions and data are clocked out on this pin on the falling edge of JTCLK. If not used leave unconnected. See section 7.2.18.

Table 5-5. Detailed Pin Descriptions – GPIO signals (5 dedicated pins, 4 shared pins)

Pin Name	PIN #	Type	Pin Description
GPO1	24	IOr	**General Purpose Output 1.** After reset, this pin can either be high impedance (TBI or RTBI mode) or an output that indicates link status, 0=link down, 1=link up. The function can be changed after reset. See section 6.2.
GPO2	25	IOr	**General Purpose Output 2.** After reset, this pin can either be high impedance (TBI or RTBI mode) or an output that indicates CRS (carrier sense). The function can be changed after reset. See section 6.2.

Pin Name	PIN #	Type	Pin Description
GPIO1	61	IOz	**General Purpose Input or Output 1.** After reset this pin can be either high impedance or generating a 125MHz clock signal. GPO1=0 at reset: After reset, GPIO1 is high impedance. GPO1=1 at reset: After reset, GPIO1 is 125MHz clock out The function can be changed after reset. See section 6.2.
GPIO2	60	IOz	**General Purpose Input or Output 2.** After reset this pin is high impedance. The function can be changed after reset. See section 6.2.
GPIO3	59	IOz	**General Purpose Input or Output 3.** After reset this pin is high impedance. The function can be changed after reset. See section 6.2.
GPIO4/TXD[4]	52	IOz	**General Purpose Input or Output 4.** Available for use as a GPIO pin when the parallel interface is configured for MII, RGMII or RTBI modes. After reset this pin is high impedance. The function can be changed after reset. See section 6.2.
GPIO5/TXD[5]	53	IOz	**General Purpose Input or Output 5.** Available for use as a GPIO pin when the parallel interface is configured for MII, RGMII or RTBI modes. After reset this pin is high impedance. The function can be changed after reset. See section 6.2.
GPIO6/TXD[6]	54	IOz	**General Purpose Input or Output 6.** Available for use as a GPIO pin when the parallel interface is configured for MII, RGMII or RTBI modes. After reset this pin is high impedance. The function can be changed after reset. See section 6.2.
GPIO7/TXD[7]	55	IOz	**General Purpose Input or Output 7.** Available for use as a GPIO pin when the parallel interface is configured for MII, RGMII or RTBI modes. After reset this pin is high impedance. The function can be changed after reset. See section 6.2.

Table 5-6. Detailed Pin Descriptions – SGMII/1000BASE-X Serial Interface (7 pins)

Pin Name	PIN #	Type	Pin Description
TDP, TDN	9 8	Odiff	**Transmit Data Output** These pins form a differential CML output for the 1.25Gbaud SGMII transmit signal to a neighboring 1000BASE-X optical module (SFP, etc.) or PHY with SGMII interface. See section 6.5.
TCLKP, TCLKN	6 5	Odiff	**Transmit Clock Output** These pins form a differential CML output for an optional 625MHz clock for the SGMII transmit signal on TDP/TDN. This output is disabled at reset but is enabled by setting CR.TCLK_EN=1. See section 6.5.
RDP, RDN	13 14	Idiff	**Receive Data Input** These pins form a differential input for the 1.25Gbaud SGMII receive signal from a neighboring 1000BASE-X optical module (SFP, etc.) or PHY with SGMII interface. A receive clock signal is not necessary because the device uses a built-in CDR to recover the receive clock from the signal on RDP/RDN. See section 6.5.
ALOS	19	I	**Analog Loss of Signal** This pin receives analog loss-of-signal from a neighboring optical transceiver module. If the optical module does not have an ALOS output, this pin should be connected to DVSS for proper operation. See section 6.5. 0 = ALOS not detected or not required, normal operation 1 = ALOS detected, loss of signal

Table 5-7. Detailed Pin Descriptions – Parallel Interface (25 pins)

Pin Name	PIN #	Type	Pin Description
RXCLK	40	IO	**Receive Clock** In all modes the frequency tolerance is ± 100 ppm. GMII Mode: RXCLK is the 125MHz receive clock. RGMII Modes: RXCLK is the 125MHz (RGMII-1000), 25MHz (RGMII-100) or 2.5MHz (RGMII-10) receive clock (DDR). TBI Mode: In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), RXCLK is the 62.5MHz receive clock for odd code groups and TXCLK/RCXCLK1 is the 62.5MHz receive clock for even code groups. In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset), RXCLK is the 125MHz receive clock. RTBI Mode: RXCLK is the 125MHz receive clock (DDR). MII Mode: RXCLK is the 25MHz (100Mbps MII) or 2.5MHz (10Mbps MII) receive clock. In DTE mode (DCE_DTE)=1, RXCLK is an input. In DCE mode (DCE_DTE)=0, RXCLK is an output.

Pin Name	PIN #	Type	Pin Description
RXD[0] RXD[1] RXD[2] RXD[3] RXD[4] RXD[5] RXD[6] RXD[7]	38 37 36 35 34 33 32 31	IOr	**Receive Data Outputs** During reset these pins are configuration inputs. See section 6.1. After reset they are driven as outputs. GMII Mode: receive_data[7:0] is output on RXD[7:0] on the rising edge of RXCLK. MII, RGMII-10 and RGMII-100 Modes: receive_data[3:0] is output on RXD[3:0] on the rising edge of RXCLK. RXD[7:4] are high impedance. RGMII-1000 Mode: receive_data[3:0] is output on RXD[3:0] on the rising edge of RXCLK, and receive_data[7:4] is output on the falling edge of RXCLK. RXD[7:4] are high impedance. TBI Mode: In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), receive_data[7:0] is output on RXD[7:0], receive_data[8] is output on RX_DV, and receive_data[9] is output on RX_ER on the rising edge of RXCLK and the rising edge of RXCLK1 (both 62.5MHz, 180 degrees out of phase). In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset), these same signals are output on the rising edge of RXCLK (125MHz). RTBI Mode: Receive_data[3:0] is output on RXD[3:0] and Receive_data[4] is output on RX_DV on the rising edge of RXCLK. Receive_data[8:5] is output on RXD[3:0] and receive_data[9] is output on RX_DV on the falling edge of RXCLK. RXD[7:4] are high impedance.
RX_DV	29	IOr	**Receive Data Valid** During reset this pin is a configuration input. See section 6.1. After reset it is driven as an output. MII Mode and GMII Mode: RX_DV is output on the rising edge of RXCLK. RGMII Modes: The RX_CTL signal is output on RX_DV on both edges of RXCLK. TBI Mode: In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), receive_data[8] is output on RX_DV on the rising edge of RXCLK and the rising edge of RXCLK1 (both 62.5MHz, 180 degrees out of phase). In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset), receive_data[8] is output on RX_DV on the rising edge of RXCLK (125MHz). RTBI Mode: Receive_data[4} is output on RX_DV on the rising edge of RXCLK. Receive_data[9] is output on RX_DV on the falling edge of RXCLK.
RX_ER	28	IOr	**Receive Error** During reset this pin is a configuration input. See section 6.1. After reset it is driven as an output. MII Mode and GMII Mode: RX_ER is output on the rising edge of RXCLK. RGMII Mode and RTBI Mode: RX_ER pin is high impedance. TBI Mode: In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), receive_data[9] is output on RX_ER on the rising edge of RXCLK and the rising edge of RXCLK1 (both 62.5MHz, 180 degrees out of phase). In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset), receive_data[9] is output on the rising edge of RXCLK (125MHz).

Pin Name	PIN #	Type	Pin Description
COL	27	IOr	**Collision Detect** During reset this pin is a configuration input. See section 6.1. After reset it is driven as an output. MII Mode. GMII Mode and RGMII Modes: COL indicates that a Tx/Rx collision is occurring. It is meaningful only in half duplex operation. It is asynchronous to any of the clocks. COL is driven low at all times when BMCR.DLB=1 and BMCR.COL_TEST=0. When BMCR.DLB=1 and BMCR.COL_TEST=1, COL behaves as described in the COL_TEST bit description. 1 = Collision is occurring 0 = Collision is not occurring TBI Mode and RTBI Mode: This pin is high impedance.
CRS/COMMA	26	IOr	**Carrier Sense / Comma Detect** During reset this pin is a configuration input. See section 6.1. After reset it is driven as an output. MII Mode. GMII Mode and RGMII Modes: CRS is asserted by the device when either the transmit data path or the receive data path is active. This signal is asynchronous to any of the clocks. TBI Mode and RTBI Mode: COMMA is asserted by the device when a comma pattern is detected in the receive data stream. In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), COMMA is updated on the rising edge of RXCLK and the rising edge of RXCLK1 (both 62.5MHz, 180 degrees out of phase). In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset) and RTBI mode, COMMA is updated on the rising edge of RXCLK (125MHz).
TXCLK/ RXCLK1	46	IO	**MII Transmit Clock** When TXCLK is an input, frequency tolerance is ±100ppm. MII Mode: TXCLK is the 25MHz (100Mbps MII) or 2.5MHz 10Mbps MII) transmit clock. In DTE mode (DCE_DTE)=1, TXCLK is an input. In DCE mode (DCE_DTE)=0, TXCLK is an output. GMII Mode, RGMII Mode and RTBI Mode: TXCLK can output a 125MHz clock for use by neighboring components (e.g. a MAC) when GMIICR.TXCLK_EN=1 (or TXCLK=1 at reset). TBI Mode: In normal TBI mode (GMIICR.TBI_RATE=1 or RX_DV=1 at reset), this pin becomes the 62.5MHz RXCLK1 output for even code groups. In one-clock TBI mode (GMIICR.TBI_RATE=0 or RX_DV=0 at reset), TXCLK can output a 125MHz clock for use by neighboring components (e.g. a MAC) when GMIICR.TXCLK_EN=1 (or TXCLK=1 at reset).

Pin Name	PIN #	Type	Pin Description
GTXCLK	66	I	**GMII/RGMII Transmit Clock** In all modes the frequency tolerance is ± 100ppm. GMII Mode: GTXCLK is the 125MHz transmit clock. RGMII Modes: GTXCLK is the 125MHz (RGMII-1000), 25MHz (RGMII-100) or 2.5MHz (RGMII-10) transmit clock (DDR). TBI Mode: GTXCLK is the 125MHz transmit clock. RTBI Mode: GTXCLK is the 125MHz transmit clock (DDR). MII Mode: This pin is not used and should be pulled low. See the TXCLK pin description.
TXD[0] TXD[1] TXD[2] TXD[3] TXD[4]/GPIO4 TXD[5]/GPIO5 TXD[6]/GPIO6 TXD[7]/GPIO7	48 49 50 51 52 53 54 55	I I I I IOz IOz IOz IOz	**Transmit Data Inputs** Depending on the parallel MII interface mode, four or eight of these pins are used to accept transmit data from a neighboring component. GMII Mode: The rising edge of GTXCLK latches transmit_data[7:0] from TXD[7:0]. MII, RGMII-10 and RGMII-100 Modes: The rising edge of TXCLK (MII) or GTXCLK (RGMII) latches transmit_data[3:0] from TXD[3:0]. TXD[7:4] become GPIO7 – GPIO4. RGMII-1000 Mode: The rising edge of GTXCLK latches transmit_data[3:0] from TXD[3:0]. The falling edge of GTXCLK latches transmit_data[7:4] from TXD[3:0]. TXD[7:4] become GPIO7 – GPIO4. TBI Mode: The rising edge of GTXCLK latches transmit_data[7:0] from TXD[7:0], transmit_data[8] from TX_EN and transmit_data[9] from TX_ER. RTBI Mode: The rising edge of GTXCLK latches transmit_data[3:0] from TXD[3:0] and transmit_data[4] from TX_EN. The falling edge of GTXCLK latches transmit_data[8:5] from TXD[3:0] and transmit data[9] from TX_EN. TXD[7:4] become GPIO7 – GPIO4.
TX_EN	57	I	**Transmit Enable** MII Mode and GMII Mode: The rising edge of TXCLK (MII) or GTXCLK (GMII) latches the TX_EN signal from this pin. RGMII Modes: Both edges of GTXCLK latch the TX_CTL signal from this pin. TBI Mode: The rising edge of GTXCLK latches transmit_data[7:0] from TXD[7:0], transmit_data[8] from TX_EN and transmit_data[9] from TX_ER. RTBI Mode: The rising edge of GTXCLK latches transmit_data[3:0] from TXD[3:0] and transmit_data[4] from TX_EN. The falling edge of GTXCLK latches transmit_data[8:5] from TXD[3:0] and transmit data[9] from TX_EN.

Pin Name	PIN #	Type	Pin Description
TX_ER	58	I	**Transmit Error** MII Mode and GMII Mode: The rising edge of TXCLK (MII) or GTXCLK (GMII) latches the TX_ER signal from this pin. RGMII Modes: This pin is not used. TBI Mode: The rising edge of GTXCLK latches transmit_data[7:0] from TXD[7:0], transmit_data[8] from TX_EN and transmit_data[9] from TX_ER. RTBI Mode: This pin is not used.

Table 5-8. Detailed Pin Descriptions – Power and Ground Pins (17 pins)

Pin Name	PIN #	Pin Description
DVDD12	30, 56	Digital Power Supply, 1.2V (2 pins)
DVDD33	20, 39, 65	Digital Power Supply, 3.3V
DVSS	47	Return for DVDD12 and DVDD33
RVDD12	16	1.25G Receiver Analog Power Supply, 1.2V
RVDD33	12	1.25G Receiver Analog Power Supply, 3.3V
RVSS	15	Return for RVDD12 and RVDD33
TVDD12	11	1.25G Transmitter Analog Power Supply, 1.2V
TVDD33	7	1.25G Transmitter Analog Power Supply, 3.3V
TVSS	10	Return for TVDD12 and TVDD33
CVDD12	3	TX PLL Analog Power Supply, 1.2V
CVDD33	2	TX PLL Analog Power Supply, 3.3V
CVSS	4	Return for CVDD12 and CVDD33
GVDD12	18	Analog Power Supply, 1.2V
GVSS	1	Return for GVDD12.
Exposed Pad	EP	Exposed pad (die paddle). Connect to ground plane. EP also functions as a heatsink. Solder to the circuit-board ground plane to maximize thermal dissipation.

6. Functional Description

6.1 Pin Configuration During Reset

The MAX24287 initial configuration is determined by pins that are sampled at reset. The values on these pins are used to set the reset values of several register bits. Note that the behavior described in this section cannot be used for “hardware-only” operation. Some register accesses through the MDIO interface are required for proper operation as described in section 6.14.

The pins that are sampled at reset to pin-configure the device are listed described in Table 6-1. During reset these pins are high-impedance inputs and require 10kΩ pullup or pulldown resistors to set pin-configuration values. After reset, the pins can become outputs if configured to do so and operate as configured. There are two pin configuration modes: 15-pin mode and 3-pin mode.

In 15-pin mode (COL=0 during reset, see Table 6-1) all major settings associated with the PCS block are configurable. In addition, the input reference clock frequency on the REFCLK pin is configured during reset using the RXD[3:2] pins.

Table 6-1. Reset Configuration Pins, 15-Pin Mode (COL=0)

Pin	Function	Register Bit Affected	Notes
CRS	Double Date Rate	GMIICR:DDR=CRS	See Table 6-2.
GPO2	10/100 MII: DTE or DCE	10/100 MII: GMIICR:DTE_DCE	0=DCE, 1=DTE (serial interface is configured for SGMII mode, PCSCR:BASEX=0)
	Other: Serial Interface	Other: PCSCR:BASEX	0=SGMII, 1=1000BASE=X
GPO1	GPIO1 Configuration	GPIOCR1.GPIO1_SEL[2]	0=high impedance 1=125MHz from TX PLL
RXD[1:0]	Parallel Interface Speed	GMIICR:SPD[1:0]	See Table 6-2.
RXD[3:2]	REFCLK Frequency	None	00=10MHz, 01=12.8MHz, 10=25MHz, 11=125MHz
RXD[7:4]	MDIO PHYAD[3:0].	Internal MDIO PHYAD register (device address on MDIO bus).	Note: PHYAD[4:0]=11111 enables factory test mode. Do not use.
RX_ER	MDIO PHYAD[4].		
RX_DV	TBI Mode	GMIICR:TBI_RATE	0=one-clock mode (125MHz) 1=normal mode (62.5MHz x 2)
	Other: Auto-negotiation	BMCR:AN_EN	0=Disable, 1=Enable
TXCLK	TXCLK Enable	GMIICR:TXCLK_EN	0=high impedance 1=125MHz from TX PLL Ignored in MII mode and TBI with two 62.5MHz Rx clocks

Table 6-2. Parallel Interface Configuration

SPD[1]	SPD[0]	Speed	DDR=0	DDR=1
0	0	10Mbps	MII	RGMII-10
0	1	100Mbps	MII	RGMII-100
1	0	1000Mbps	GMII	RGMII-1000
1	1	1000Mbps	TBI	RTBI

In 3-pin mode (COL=1 during reset, see Table 6-3) the device is configured for a 1000Mbps RGMII or GMII parallel interface. This mode is targeted to the application of connecting an ASIC, FPGA or processor with an RGMII or GMII interface to a switch device with an SGMII interface or to a 1000BASE-X optical interface. In 3-pin mode, the REFCLK pin is configured for 25MHz, the PHY address is set to 0x04, 1000BASE-X auto-negotiation (or automatic transmission of SGMII control information) is enabled, TXCLK is configured to output a 125MHz clock, and the

TCLKP/TCLKN differential pair is disabled. Note: if RX_ER and RXD[7:4] are all high when the device exits reset then the device enters factory test mode; for normal operation set these pins to any other combination of values.

Table 6-3. Reset Configuration Pins, 3-Pin Mode (COL=1)

Pin	Function	Register Bit Affected	Notes
CRS	Double Date Rate	GMIICR:DDR=CRS	0=GMII, 1=RGMII
GPO2	Serial Interface	PCSCR:BASEX	0=SGMII, 1=1000BASE=X

Note: In 3-pin mode register fields are automatically set as follows: REFCLK clock rate to 25MHz, GMIICR:SPD[1:0]=10, MDIO PHYAD is set to 0x04, BMCR:AN_EN=1, GMIICR:TXCLK_EN=1, GPIOCR1=0 and GPIOCR2=0. All other registers are reset to normal defaults listed in the register descriptions.

6.2 General-Purpose I/O

The MAX24287 has two general-purpose output pins, GPO1, GPO2, and seven general-purpose input/output pins, GPIO1 through GPIO7. Each pin can be configured to drive low or high or be in a high-impedance state. Other uses for the GPO and GPIO pins are listed in Table 6-4 through Table 6-6. The GPO and GPIO pins are each configured using a GPxx_SEL field in registers GPIOCR1 or GPIOCR2 with values as indicated in the tables below.

When a GPIO pin is configured as high impedance it can be used as an input. The real-time state of GPIOx can be read from GPIOSR.GPIOx. In addition, a latched status bit GPIOSR.GPIOxL is available for each GPIO pin. This latched status bit is set when the transition specified by GPIOCR2.GPIO13_LSC (for GPIO1 through GPIO3) or by GPIOCR2.GPIO47_LSC (for GPIO4 through GPIO7) occurs on the pin.

Note that GPIO4 through GPIO7 are alternate pin functions to TXD[7:4] and therefore are only available when the parallel MII is configured for MII, RGMII or RTBI.

Table 6-4. GPO1, GPIO1 and GPIO3 Configuration Options

GPxx_SEL	Description
000	High impedance, not driven, can be an used as an input
001	Drive logic 0
010	Drive logic 1
011	Interrupt output, active low. GPO1 drives low and high, GPIO1 and GPIO3 are open-drain.
100	Output 125MHz from the TX PLL
101	Output 25MHz or 125MHz from receive clock recovery PLL. Not squelched. Frequency specified by CR.RCFREQ.
110	Output real-time link status, 0=link down, 1=link up
111	reserved value, do not use

Table 6-5. GPO2 and GPIO2 Configuration Options

GPxx_SEL	Description
000	High impedance, not driven, can be an used as an input
001	Drive logic 0
010	Drive logic 1
011	reserved value, do not use
100	Output 125MHz from TX PLL
101	Output 25MHz or 125MHz from receive clock recovery PLL. The frequency is specified by CR.RCFREQ. Signal is automatically squelched (driven low) when CR.RCSQL=1 and any of several conditions occur. See section 6.2.1.
110	Output CRS (carrier sense) status
111	reserved value, do not use

Table 6-6. GPIO4, GPIO5, GPIO6 and GPIO7 Configuration Options

GPxx_SEL	Description
000	High impedance, not driven, can be an used as an input
001	Drive logic 0
010	Drive logic 1
011	reserved value, do not use
100	Output 125MHz from TX PLL
101	Output 25MHz or 125MHz from receive clock recovery PLL. The frequency is specified by CR.RCFREQ. Signal is automatically squelched (driven low) when CR.RCSQL=1 and any of several conditions occur. See section 6.2.1.
110	reserved value, do not use
111	reserved value, do not use

6.2.1 Receive Recovered Clock Squelch Criteria

A 25MHz or 125MHz clock from the receive clock recovery PLL can be output on any of GPO2, GPIO2 and GPIO4-7. When CR.RCSQL=1, this clock is squelched (driven low) when any of the following conditions occur:

- IR.ALOS=1 (analog loss-of-signal occurred)
- IR.RLOS=1 (CDR loss-of-signal occurred))
- IR.RLOL=1 (CDR PLL loss-of-lock occurred)
- IR.LINK_ST=0 (auto-negotiation link down occurred, latched low)

Since each of these criteria is a latched status bit, the output clock signal remains squelched until all of these latched status bits go inactive (as described in section 7.2).

6.3 Reset and Processor Interrupt

6.3.1 Reset

The following reset functions are available in the device:

1. Hardware reset pin (RST_N): This pin asynchronously resets all logic, state machines and registers in the device except the JTAG logic. When the RST_N pin is low, all internal registers are reset to their default values. Pin states are sampled and used to set the default values of several register fields as described in section 6.1. RST_N should be asserted for at least 100µs.

2. Global reset bit, GPIOCR1.RST: Setting this bit is equivalent to asserting the RST_N pin. This bit is self-clearing.

3. Datapath reset bit, BMCR.DP_RST. This bit resets the entire datapath from parallel MII interface through PCS encoder and decoder. It also resets the deserializer. It does not reset any registers, GPIO logic, or the TX PLL. The DP_RST bit is self-clearing.

4. JTAG reset pin JTRST_N. This pin resets the JTAG logic. See section 7.2.18 for details about JTAG operation.

6.3.2 Processor Interrupts

Any of pins GPO1, GPIO1 and GPIO3 can be configured as an active low interrupt output by setting the appropriate field in GPIOCR1 to 011. GPO1 drives high and low while GPIO1 and GPIO3 are open-drain and require pullup resistors.

Status bits than can cause an interrupt are located in the IR register. The corresponding interrupt enable bits are also located in the IR register. The PAGESEL register has a top-level IR status bit to indicate the presence of

active interrupt sources. The PAGESEL register is available on all pages through the MDIO interface, allowing the interrupt routine to read the register without changing the MDIO page.

6.4 MDIO Interface

6.4.1 MDIO Overview

The MAX24287's MDIO interface is compliant to IEEE 802.3 clause 22. MAX24287 always behaves as a PHY on the MDIO bus. Because MAX24287 is not a complete PHY but rather a device that sits between a MAC and a PHY, it implements only a subset of the registers and register fields specified in 802.3 clause 22 as shown in the table below.

MDIO Address	802.3 Name	MAX24287 Name
0	Control	BMCR
1	Status	BMSR
2, 3	PHY Identifier	ID1, ID2
4	Auto-Negotiation Advertisement	AN_ADV
5	Auto-Negotiation Link Partner Base Page Ability	AN_RX
6	Auto-Negotiation Expansion	AN_EXP
15	Extended Status	EXT_STAT

The MDIO consists of a bidirectional, half-duplex serial data signal (MDIO) and a ≤12.5MHz clock signal (MDC) driven by a bus master, usually a MAC. The format of management frames transmitted over the MDIO interface is shown below (see IEEE 802.3 clause 22.2.4.5 for more information). MDIO DC electrical characteristics are listed in section 9.2.1. AC electrical characteristics are listed in section 9.3.6. The MAX24287's MDIO slave state machine is shown in Figure 6-1.

	Management Frame Fields							
	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
READ Command	32 ‘1’s	01	10	AAAAA	RRRRR	Z0	16-bit	Z
WRITE Command	32 ‘1’s	01	01	AAAAA	RRRRR	10	16-bit	Z

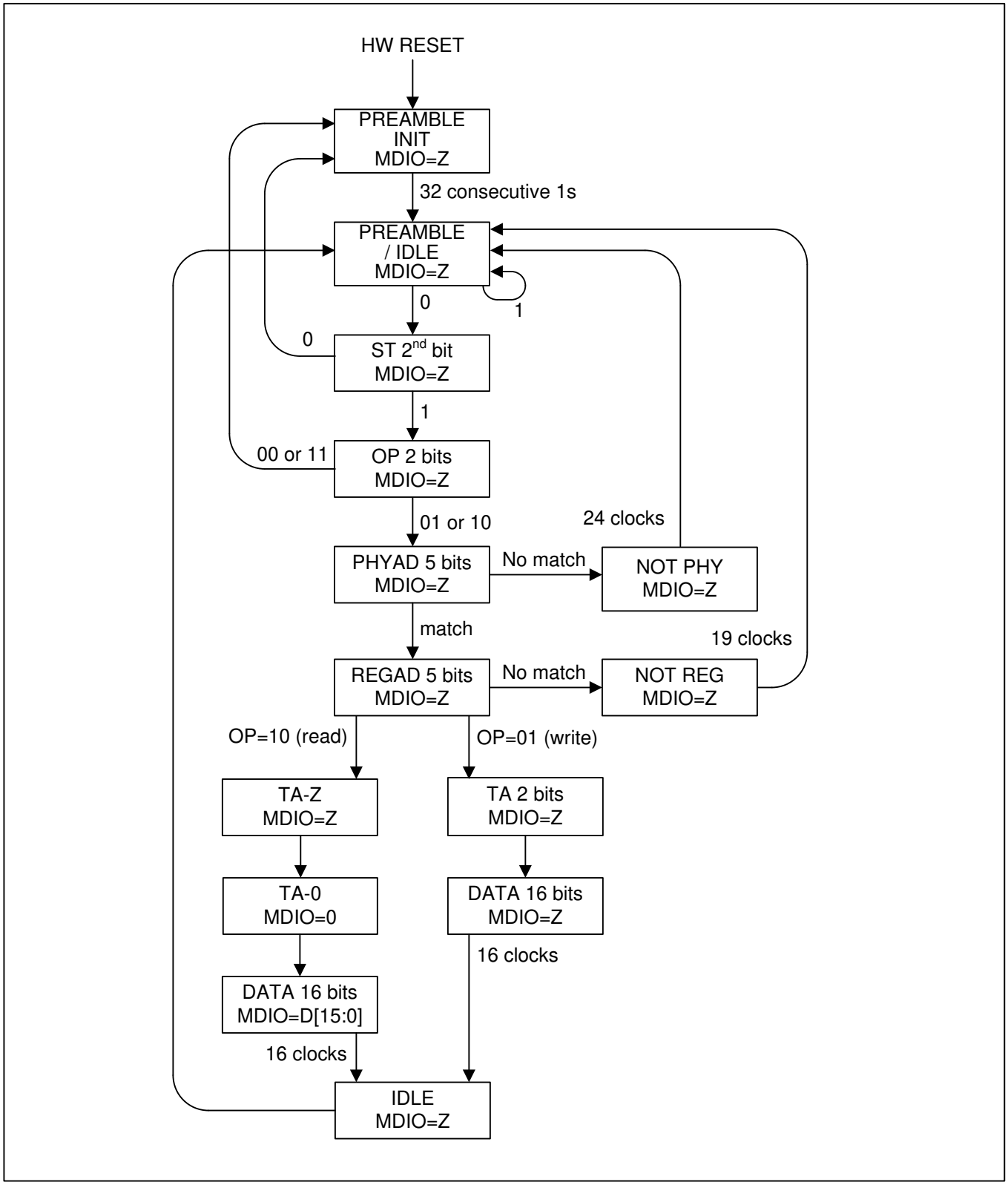
The transmission and reception bit order is MSB first for the PHYAD, REGAD and DATA fields

MAX24287 supports preamble suppression. This allows quicker bursts of read and write transfers to occur by shortening the minimum transfer cycle time from 65 clock periods to 33 clock periods. There must be at least a 32-bit preamble on the first transfer after reset, but on subsequent transfers the preamble can be suppressed or shortened. When the preamble is completely suppressed the 0 in the ST symbol follows the single IDLE Z, which is one clock period duration.

Like any MDIO slave, MAX24287 only performs the read or write operation specified if the PHYAD bits of the MDIO command match the device PHY address. The device PHY address is latched during device reset from the RXD[7:4] and RX_ER pins. See section 6.1.

The MAX24287 does not support the 802.3 clause 45 MDIO extensions. Management frames with ST bits other than 01 or OP bits other than 01 or 10 are ignored and put the device in a state where it ignores the MDIO traffic until it sees a full preamble (32 ones). If Clause 45 ICs and the MAX24287 are connected to the same MDIO management interface, the station management entity must put a full preamble on the bus after communicating with clause 45 ICs before communicating with the MAX24287.

Figure 6-1. MDIO Slave State Machine

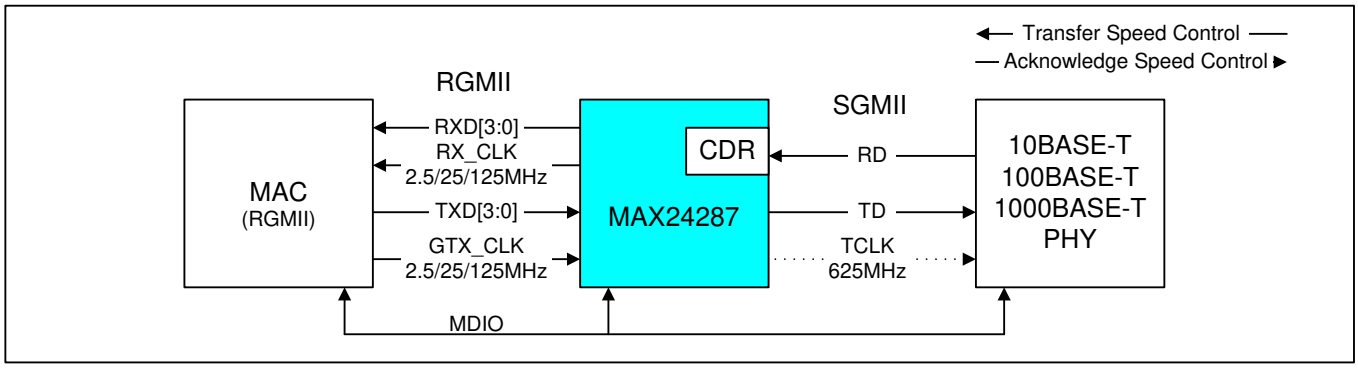


6.4.2 Examples of MAX24287 and PHY Management Using MDIO

The MDIO interface is typically provided by the MAC function within a neighboring processor, ASIC or FPGA component. It can be used to configure the registers in the MAX24287 and/or the registers in a PHY or switch chip connected to the MAX24287 via the SGMII interface.

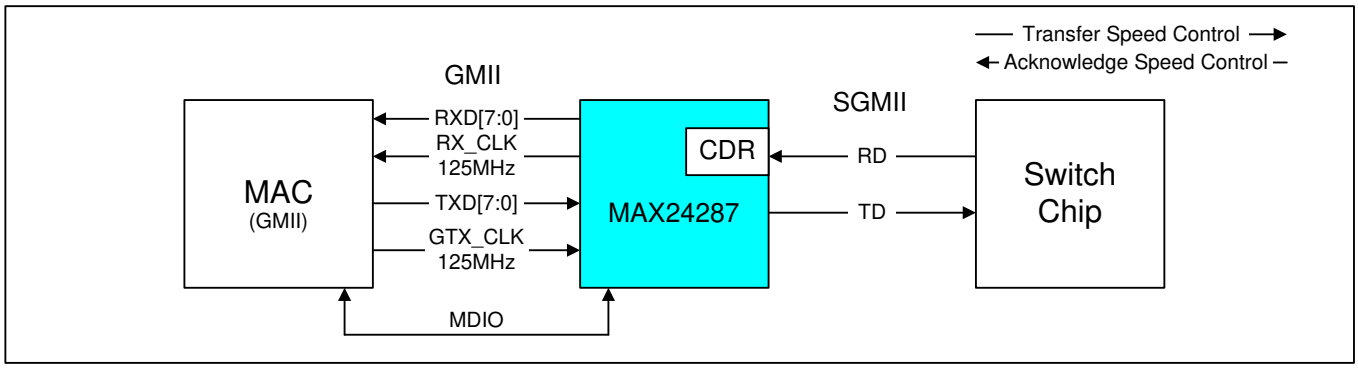
Case 1 in Figure 6-2 shows a typical application where the MAX24287 connects a MAC with a 3-speed RGMII interface to a 3-speed PHY with an SGMII interface. Through the MDIO interface, system software configures the MAX24287 and optionally the PHY. (The PHY may not need to be configured if it is operating in a hardware-only auto-negotiation 1000BASE-T mode). After initial configuration and after the PHY auto-negotiates link details with its 1000BASE-T link partner, the speed and mode are transferred to the MAX24287 over the SGMII interface as specified in the SGMII specification and are available in the MAX24287 AN_RX register. The processor reads this information and configures the MAC and the MAX24287 to match the mode the PHY is in.

Figure 6-2. Management Information Flow Options, Case 1,Tri-Mode PHY



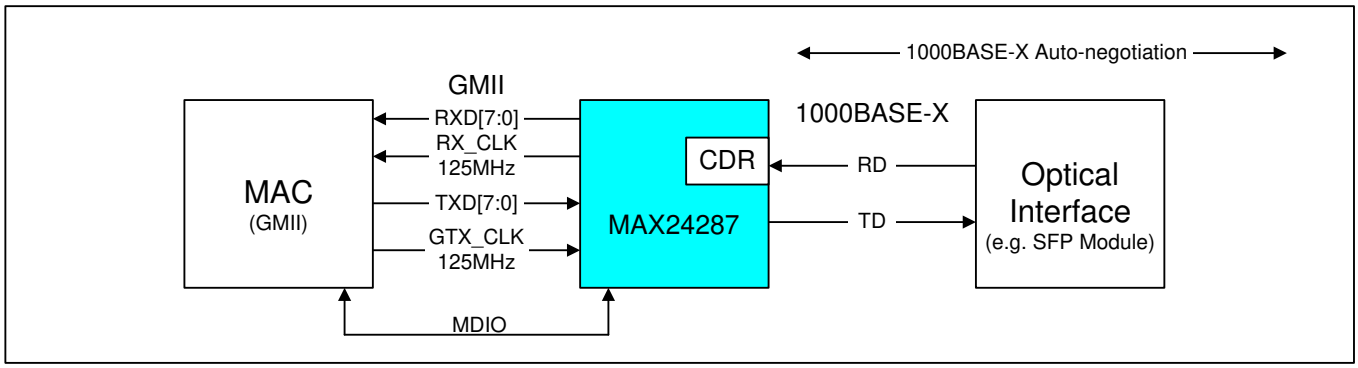
Case 2 in Figure 6-3 shows a typical application where the MAX24287 connects a MAC with a GMII interface to an SGMII switch chip. Through the MDIO interface, system software configures the MAX24287 to match the MAC mode and writes the MAX24287's AN_ADV register to also match the MAC mode. The MAX24287 then transfers the speed and mode over the SGMII interface as specified in the SGMII specification. The switch chip receives this information and configures its port to match.

Figure 6-3. Management Information Flow Options, Case 2, SGMII Switch Chip



Case 3 in Figure 6-4 shows a typical application where the MAX24287 connects a MAC with a GMII interface to an optical interface. In this case the MAX24287 provides the 1000BASE-X PCS and PMA functions for the optical interface. Through the MDIO interface, system software configures the MAX24287 to match the MAC mode, both of which need to be 1000 Mbps speed. The MAX24287 then auto-negotiates with its link partner. This 1000BASE-X auto-negotiation is primarily to establish the pause functionality of the link. The MAX24287's auto-negotiation support is described in section 6.7.

Figure 6-4. Management Information Flow Options, Case 3, 1000BASE-X Interface



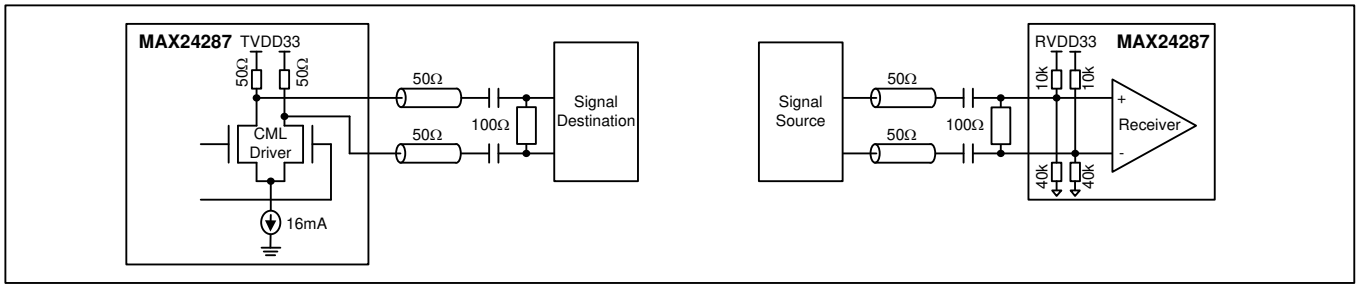
6.5 Serial Interface – 1000BASE-X or SGMII

The high-speed serial interface is compatible with the specification of the 1000BASE-CX PMD service interface TP1 as defined in 802.3 clause 39. It is also compatible with the specification of the SGMII interface and can connect to optical PMD modules in 1000BASE-SX/LX interfaces.

On this interface the MAX24287 transmits a 1250Mbaud differential signal on the TDP/TDN output pins. DDR clocking is used, and the transmit interface outputs a 625MHz differential clock signal on the TCLKP/TCLKN output pins. In the receive direction the clock and data recovery (CDR) block recovers both clock and data from the incoming 1250Mbaud signal on RDP/RDN. A separate receive clock signal is not needed.

Signal Format, Coupling, Termination. The serial interface passes data at 1.25 Gbaud using a CML differential output and an any-format differential input. The CML TDP/TDN outputs have internal 50Ω pullup resistors to TVDD33. The differential input RDP/RDN does not have internal termination, and an external 100Ω termination resistor between RDP and RDN is recommended. The high-speed serial interface pins are typically connected with neighboring components using AC coupling as shown in Figure 6-5.

Figure 6-5. Recommended External Components for High-Speed Serial Interface



Receive Loss-of-Signal. The device's receiver logic has an ALOS input pin through which analog loss-of-signal (ALOS) can be received from a neighboring optical transceiver module, if the high-speed serial signal is transmitted/received optically. The IR.ALOS bit is set when the ALOS pin goes high. ALOS can cause an interrupt if enabled by IR.ALOS_IE.

In addition, the clock-and-data recovery block (CDR) indicates loss-of-signal when it does not detect any transitions in 24 bit times. The IR.RLOS latched status bit is set when the CDR indicates loss-of-signal. RLOS can cause an interrupt if enabled by IR.RLOS_IE.

Receive Loss-of-Lock. The receive clock PLL in the CDR locks to the recovered clock from the RDP/RDN pins and produces several receive-side clock signals. If the receive clock PLL loses lock, it sets IR.RLOL, which can cause an interrupt if enabled by IR.RLOL_IE.

Transmit Clock. The TCLKP/TCLKN differential output can be enabled and disabled using CR.TCLK_EN. Disabled means the output drivers for TCLKP and TCLKN are disabled (high impedance) and the internal 50Ω termination resistors pull both TCLKP and TCLKN up to 3.3V.

DC Electrical Characteristics. See section 9.2.2.

AC Electrical Characteristics. See section 9.3.3.

6.6 Parallel Interface – GMII, RGMII, TBI, RTBI, MII

The parallel interface can be configured as GMII, MII or TBI compliant to IEEE 802.3 clauses 35, 22 and 36, respectively. It can also be configured as reduced pin count RGMII or RTBI compliant to the HP document RGMII Version 1.3 12/10/2000. A summary of the parallel interface modes is show in Table 6-7 below.

Table 6-7. Parallel Interface Modes

Mode	Baud Rate, Mbps	Data Transfer Per Cycle, # of Wires Per Direction	Transmit Clock	Receive Clock	Full Duplex	Half Duplex
TBI, normal	1250	10-bit codes, 10 wires	Input, 125MHz	Output, 2 62.5MHz	Yes	No
TBI, 1 Rx clock	1250	10-bit codes, 10 wires	Input, 125MHz	Output, 1 125MHz	Yes	No
RTBI	1250	10-bit codes, 5 wires, DDR	Input, 125MHz	Output, 125MHz	Yes	No
GMII	1000	8-bit data, 8 wires	Input, 125MHz	Output, 125MHz	Yes	No
RGMII-1000	1000	8-bit data, 4 wires, DDR	Input, 125MHz	Output, 125MHz	Yes	No
RGMII-100	100	4-bit data, 4 wires	Input, 25MHz	Output 25MHz	Yes	Yes
RGMII-10	10	4-bit data, 4 wires	Input, 2.5MHz	Output, 2.5MHz	Yes	Yes
MII-100 DCE	100	4-bit data, 4 wires	Output, 25MHz	Output, 25MHz	Yes	Yes
MII-10 DCE	10	4-bit data, 4 wires	Output, 2.5MHz	Output, 2.5MHz	Yes	Yes
MII-100 DTE	100	4-bit data, 4 wires	Input, 25MHz	Input, 25MHz	Yes	Yes
MII-10 DTE	10	4-bit data, 4 wires	Input ,2.5MHz	Input, 2.5MHz	Yes	Yes

The parallel interface mode is controlled by GMIICR.SPD[1:0]. TBI and MII options are specified by GMIICR.TBI_RATE and GMIICR.DTE_DCE, respectively.

6.6.1 GMII Mode

The MAX24287's GMII interface is compliant to IEEE 802.3 clause 35 but only operates full duplex. Half duplex operation is not supported, and the TX_ER pin is ignored. The PHY therefore does not receive the following from the MAC: carrier extend, carrier extend error, and transmit error propagation as described in 802.3 section 35.2.1.6, section 35.2.2.5 and Table 35-1. These features are not needed for full duplex operation.

The parallel interface can be configured for GMII mode using software configuration or pin configuration at reset. For pin configuration (see section 6.1) one of the following combinations of pin states must be present during device reset:

- COL=0, RXD[1:0]=10, CRS=0
- COL=1, CRS=0

For software configuration, the following register fields must be set: GMIICR.SPD[1:0]=10 and GMIICR.DDR=0.

See IEEE 802.3 clause 35 for functional timing diagrams. GMII DC electrical characteristics are listed in section 9.2.1. AC electrical characteristics are listed in section 9.3.4 and 9.3.5.

Table 6-8. GMII Parallel Bus Pin Naming

Pin Name	802.3 Pin Name	Function
RXCLK	RX_CLK	Receive 125MHz clock output
RXD[7:0]	RXD[7:0]	Receive data output
RX_DV	RX_DV	Receive data valid output
RX_ER	RX_ER	Receive data error output
CRS	CRS	Receive carrier sense
COL	COL	Receive collision (held low in GMII mode)
TXCLK	---	Outputs 125MHz from the TX PLL for MAC when GMIICR.TXCLK_EN=1.
GTXCLK	GTX_CLK	Transmit 125MHz clock input
TXD[7:0]	TXD[7:0]	Transmit data input
TX_EN	TX_EN	Transmit data enable input
TX_ER	TX_ER	Transmit data error input (not used - ignored)