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REFERENCE DESIGN AVAILABLE

MAX2552

Band III, IV, IX, and X WCDMA Femtocell Transceiver with GSM Monitoring

General Description

The MAX2552 is a complete single-chip RF-to-bits and bits-to-RF radio transceiver. This device is in compliance with the 3GPP TS25.104 femtocell standard for Band III, IV, IX, and X. It is equipped with multiple receive inputs and transmit outputs for low band, high band, and macro-cell monitoring (Table 1).

This fully integrated transceiver facilitates compact radio designs for dongle and stand-alone femtocell products by minimizing external component count. Maxim's MAX-PHY serial interface is used to drastically reduce IC pin count, while worldwide field-proven architecture accelerates time to product deployment.

The device features unparalleled receive blocker performance and the industry's lowest noise figure for higher data rates and range. Low-power operational modes are available to minimize power consumption. The transmitter is designed to deliver EVM far exceeding the standard requirement at 0dBm.

The MAX2552/MAX2553 is a family of pin-compatible transceivers that cover all major WCDMA and cdma2000® bands. All parts are controlled by a 4-wire interface.

The MAX2552 is packaged in a compact 7mm x 7mm TQFN and specified over the -40°C to +85°C extended temperature range. A complete radio reference design is available to facilitate custom designs.

Applications

WCDMA Band III, IV, IX, and X Femtocells

***Ordering Information* and *Simplified Block Diagram* appear at end of data sheet.**

*For related parts and recommended products to use with this part, refer to **www.maximintegrated.com/MAX2552.related**.*

Features

- **Single-Chip Femtocell Radio Transceiver**
- **WCDMA/HSPA+ Band III, IV, IX, and X Operation**
- **TS25.104 Standard Compliant**
- **Multiple LNA Inputs for WCDMA, PCS, and GSM Macrocell Monitoring (Bands II, III, IV, V, IX, and X)**
- **High Level of Integration**
  - **On-Chip Fractional-N Frequency Synthesizers for LO Generation**
  - **No Tx SAW Filters Required**
  - **Integrated PA Drivers for Lower-Cost Power Amplifier Designs**
  - **12-Bit AFC DAC to Control TCXO**
  - **On-Chip Temperature Sensor**
  - **Three General-Purpose Outputs**
  - **Reference Clock with Selectable CMOS and Low Swing Output**
  - **PLL Lock-Detect Output Through GPO3**
- **Optimized Receiver Performance**
  - **Exceptional Receive Sensitivity**
  - **High Dynamic Range Sigma-Delta ADCs Allow Simple AGC Implementation with Switched Gain States**
- **Optimized Transmitter Performance**
  - **Factory Calibrated for Gain, Carrier Leakage, and Sideband Suppression**
  - **10-Bit Gain-Control Resolution for Better Power Accuracy**
  - **60dB Gain-Control Range**
- **Loopback Operating Mode from Tx Baseband Input to Rx Baseband Output**
- **MAX-PHY Serial Digital Interface**
- **SPI Read/Write Functionality**
- **Operation Controlled by 4-Wire Serial Interface**
- **Low-Cost, 7mm x 7mm TQFN Package**

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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6678; Rev 0; 4/13

MAX2552

Band III, IV, IX, and X WCDMA Femtocell Transceiver with GSM Monitoring

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ABSOLUTE MAXIMUM RATINGS

$V_{CC\_}$ to GND_ ..... -0.3V to +3.9V
RXIN_, MIXIN_, LNAOUT_ to GND_ ..... -0.3V to +1.2V
All Pins Except $V_{CC\_}$ to GND_ ..... -0.3V to ($V_{CC\_}$ + 0.3V)
AC Input Signals ..... 1.0V Peak
Digital Input Current ..... ±10mA
Maximum VSWR Without Damage 8:1

Continuous Power Dissipation (T_A = +70°C)
TQFN Multilayer Board (derate 40mW/°C above +70°C) ... 3.2W
Junction Temperature ..... +150°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance (θ_{JA}) ..... 25°C/W

Junction-to-Case Thermal Resistance (θ_{JC}) ..... 1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC ELECTRICAL CHARACTERISTICS

($V_{CC\_}$ = 3.0V to 3.6V, 50Ω system, f_{REFIN} = 19.2MHz. T_A = -40 to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C, unless otherwise noted. Register settings as defined in tables following the specification tables.) (Note 2)

SPEC NO.	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC1	Supply Voltage	$V_{CC\_}$		3.0	3.3	3.6	V
DC19	Operating Supply Current WCDMA	$I_{CC\_}$	Full-duplex high band		300	419	mA
DC20			RXIN2 monitor		78	110	
DC21			RXIN4 monitor		70	100	
DC22			RXIN5 monitor		71	100	
DC23			Tx only		250	360	
DC24			Idle Rx		36		
DC25			Idle Tx		40		
DC3	Operating Supply Current AFC-Only Mode	$I_{CC\_}$	AFC DAC and SPI only		190	1000	µA
DC5	Operating Supply Current Reference Buffer Mode	$I_{CC\_}$	REFOUT = 500Ω ll 22pF, all else = off		6	7.5	mA
DC6	Operating Supply Current Sleep Mode	$I_{CC\_}$	All functions off		18	1000	µA
DC11	Digital Input Logic-High			1.3			V
DC12	Digital Input Logic-Low					0.4	V
DC13	Input Current for Digital Control Pins					10	lµAl
DC16	GPO Sink Current		V_{OUT} = 0.35V, DOUT_DRV = 01	1.0	1.8		mA
DC17	GPO Source Current		V_{OUT} = $V_{CC\_}$ - 0.3V, DOUT_DRV = 01	1.0	1.9		mA

AC ELECTRICAL CHARACTERISTICS

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band III, IV, IX, and X Duplexer Specifications

(Diplexer between antenna and duplexer loss: 0.3dB (applies to all Rx modes).)

Antenna—Uplink Port (Applies to Uplink WCDMA Rx Mode on RXIN1)

BAND (MHz)	Uplink 1710 to 1785	1 to 1660	1660 to 1710	1785 to 1825	1825 to 2200	2200 to 2500	2500 to 4500	4500 to 12750
ATTENUATION (dB)	Attenuation	Minimum Attenuation						
	2	32	12	12	37	27	12	7
Rx SAW FILTER RESPONSE								
BAND (MHz)	Out of band							
ATTENUATION (dB)	Required minimum attenuation relative to in-band							
	25							

Band III, IV, IX, and X Uplink WCDMA Rx Mode on RXIN1 (Full Duplex)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb4fu-0	Frequency Band	WCDMA FDD Band III uplink (lowest to highest channel center frequency)	1712.4		1782.4	MHz
		WCDMA FDD Band IV uplink (lowest to highest channel center frequency)	1712.4		1752.6	
		WCDMA FDD Band IX uplink (lowest to highest channel center frequency)	1752.4		1782.4	
		WCDMA FDD Band X uplink (lowest to highest channel center frequency)	1712.4		1767.6	
Wb4fu-1	Sensitivity 3GPP TS25.104 Section 7.2.1	Tx on at -27dBm, LNA gain mid-gain, PGA gain register set to 9, assumed SNDR > -17.5dB at sensitivity, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-117	-107	dBm
Wb4fu-1a	Sensitivity with LNA in High-Gain Mode	Tx on at -27dBm, LNA gain high, PGA gain register set to 6, assumed SNDR > -17.5dB at sensitivity, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-119	-107	dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band III, IV, IX, and X Uplink WCDMA Rx Mode on RXIN1 (Full Duplex) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb4fu-3	High-Level EVM WCDMA	P_{IN} = -20dBm, LNA gain low, PGA gain register set to 1		3.8		%
Wb4fu-4	Sensitivity with Adjacent Channel Interference 3GPPP TS25.104 Section 7.4.1	Tx on -27dBm, LNA gain high, PGA gain register set to 3, assumed SNDR > -17.5dB at sensitivity, inferring signals at front-end input -28dBm, at 5MHz offset and -10MHz offset and modulated as in 3GPP, using UL reference measurement channel, (12.2kbps) as specified in A.2 3GPP 25.104, Production tested by measurement if SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-100		dBm
Wb4fu-5	Sensitivity with In-Band Blocking Interference 3GPPP TS25.104 Section 7.5.1	Tx on -27dBm, LNA gain high, PGA gain register set to 6, assumed SNDR > -17.5dB at sensitivity, inferring signals at front-end input -30dBm, at 10MHz offset and -10MHz offset and modulated as in 3GPPP, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, production tested by measurement if SNDR at output on CW input signal at -90dBm test only worst case in production, SNDR at MAX-PHY filter output established with FFT		-115	-101	dBm
Wb4fu-6	Sensitivity with Out-of-Band Blocking Interference 3GPP TS25.104 Section 7.5.1	Front-end assumed response as above, Tx on at -27dBm, LNA high gain, PGA gain register set to 6, assumed SNDR > -17.5dB at sensitivity, interfering signal at front-end input -15dBm CW, 1MHz to 1690MHz and 1805MHz to 12750MHz using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT (Note 3)		-116	-101	dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band III, IV, IX, and X Uplink WCDMA Rx Mode on RXIN1 (Full Duplex) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb4fu-8	Sensitivity with Intermodulation Interference 3GPP TS25.104 Section 7.6.1	Tx on at -27dBm, LNA gain high, PGA gain register set to 6, assumed SNDR > -17.5dB at sensitivity; interfering signals at front-end input -38dBm, at 10MHz offset (CW) and 20MHz offset (modulated) as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in A.2 3GPP 25.104, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT (Note 3)		-116	-101	dBm
Wb4fu-10	Spurious Emissions Out-of-Band 3GPP TS25.104 Section 7.7.1	30MHz to 1GHz, measured in 100kHz BW		-100	-60	dBm
		1GHz to 12.75GHz, measured in 1MHz BW, with the exception of frequencies between 12.5MHz below the first carrier frequency and 12.5MHz above the last carrier frequency used by the BS (Note 3)		-75	-50	
Wb4fu-11	Spurious Emissions in Receive Bands 3GPP TS25.104 Section 7.9.2	Front-end assumed response as above, 1710MHz to 1785MHz (Note 3)		-95	-80	dBm
Wb4fu-12	Conversion Gain High LNA Gain	LNA high gain, PGA gain register set to 6, tested on CW input signal at -90dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	23	31	36	dB
Wb4fu-13	Conversion Gain Mid LNA Gain	LNA mid gain, PGA gain register set to 9, tested on CW input signal at -90dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	23	31	36	dB
Wb4fu-14	Conversion Gain Low LNA Gain	LNA gain low, PGA gain register set to 1, tested on CW input signal at -20dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	-13	-6.5	-3	dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Antenna—Downlink Port (Applies to Downlink WCDMA Rx Mode on RXIN5)

BAND (MHz)	Downlink 2110 to 2170	1 to 2025	2025 to 2050	2050 to 2095	2185 to 2230	2230 to 2255	2255 to 12750
ATTENTUATION (dB)	Attenuation	Minimum Attenuation					
	2	15	10	0	0	10	15

Band IV and X Downlink WCDMA Rx Mode on RXIN5 (Monitor)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb4fd-0	Frequency Band		2112.4		2167.6	MHz
Wb4fd-1	Sensitivity 3GPP TS25.101 Section 7.3.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, using UL reference measurement channel, (12.2kbps) as specified in C.3.1 3GPP 25.101, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-109	-101	dBm
Wb4fd-4	Sensitivity with Adjacent Channel Interference 3GPP TS25.101 Section 7.5.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, interfering signals at front-end input -52dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-103		dBm
Wb4fd-4a	Sensitivity with Adjacent Channel Interference 3GPP TS25.101 Section 7.5.1 CASE 2	LNA gain medium, PGA gain register set to 6, tested SNDR at output, interfering signals at front-end input -25dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -69dBm, SNDR at MAX-PHY filter output established with FFT		-92		dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band IV and X Downlink WCDMA Rx Mode on RXIN5 (Monitor) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb4fd-8	Sensitivity with Intermodulation Interference 3GPP TS25.101 Section 7.8.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, interfering signals at front-end input -46dBm, at 10MHz offset (CW) and 20MHz offset (modulated) as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-109		dBm
Wb4fd-10	Spurious Emissions Out-of-Band 3GPP TS25.101 Section 7.9.1	30MHz to 12750MHz in 100kHz bandwidth (Note 3)		-80	-60	dBm
Wb4fd-11	Spurious Emissions in Receive Bands 3GPP TS25.101 section 7.9.2	Front-end assumed response as above, 1710MHz to 1785MHz and 2110MHz to 2170MHz (Note 3)		-93	-80	dBm
Wb4fd-12	Conversion Gain High LNA Gain	LNA gain high, PGA gain register set to 11, tested on CW input signal at -90dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	34	42		dB
Wb4fd-13	Conversion Gain Low LNA Gain	LNA gain low, PGA gain register set to 0, tested on CW input signal at -20dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output		-12	-8	dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Downlink WCDMA RX MODE on RXIN2 (Monitor)

Assumed External Front-End Filtering Characteristics Between Antenna and LNA:

BAND (MHz)	Downlink 1800 to 1880	1 to 1750	1750 to 1770	1770 to 1815	1864 to 1930	1930 to 1950	1950 to 12750
ATTENUATION (dB)	Attenuation	Minimum Attenuation (dB)					
	2	15	10	0	0	10	15

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb9fd-0	Frequency Band		1807.4		1877.4	MHz
Wb9fd-1	Sensitivity 3GPP TS25.101 Section 7.3.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, using UL reference measurement channel, (12.2kbps) as specified in C.3.1 3GPP, 25.101, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-110	-101	dBm
Wb9fd-4	Sensitivity with Adjacent Channel Interference 3GPP TS25.101 Section 7.5.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, interfering signals at front-end input -52dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-109		dBm
Wb9fd-4a	Sensitivity with Adjacent Channel Interference 3GPP TS25.101 Section 7.5.1 CASE 2	LNA gain medium, PGA gain register set to 6, tested SNDR at output, interfering signals at front-end input -25dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -69dBm, SNDR at MAX-PHY filter output established with FFT		-94		dBm

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Downlink WCDMA RX MODE on RXIN2 (Monitor) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb9fd-8	Sensitivity with Intermodulation Interference 3GPP TS25.101 Section 7.8.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, interfering signals at front-end input -46dBm, at 10MHz offset (CW) and 20MHz offset (modulated) as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, production tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-109		dBm
Wb9fd-10	Spurious Emissions Out-of-Band 3GPP TS25.101 Section 7.9.1	30MHz to 12750MHz in 100kHz bandwidth (Note 3)		-60	-55	dBm
Wb9fd-11	Spurious Emissions in Receive Bands 3GPP TS25.101 section 7.9.2	Front-end assumed response as above, 1750MHz to 1785MHz and 1845MHz to 1880MHz (Note 3)		-97	-80	dBm
Wb9fd-12	Conversion Gain High LNA Gain	LNA gain high, PGA gain register set to 11, tested on CW input signal at -90dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	37	45		dB
Wb9fd-13	Conversion Gain Low LNA Gain	LNA gain low, PGA gain register set to 0, tested on CW input signal at -20dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output		-12.5	-8	dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

PCS Band GMSK Rx Mode on RXIN2

Assumed External Front-End Filtering Characteristics Between Antenna and LNA

BAND (MHz)	In-Band 1930 to 1990	(a) 1 to 1910	(b) 2010 to 2050	(c) 2230 to 2255	(d) 2255 to 12750
ATTENUATION (dB)	Attenuation	Minimum Attenuation			
	3.5	15	6	6	15

DCS Band Rx Mode on RXIN2

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
pcs-0	RF Frequency	At pin RXIN2, 200kHz channel raster, lowest to highest channel center frequency	1930.2		1994.8	MHz
pcs-1	Sensitivity 3GPP TS100.910 Section 6.2	LNA gain high, PGA gain register set to 12, assumed SNDR > 7dB at sensitivity, using static E-TCH/F as specified in 3GPP TS 100.910, production tested by measurement of SNDR at output on CW input signal at -102dBm, SNDR at MAX-PHY filter output established with FFT		-109	-101	dBm
pcs-10	Conversion Gain High LNA Gain	LNA gain high, PGA gain register set to 12, production tested on CW input signal at -102dBm, calculated by subtracting the FE input signal in dBm from the output signal in dBFS at digital filter outputs, includes digital gain to the16-bit output	45	50		dB

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Antenna—Downlink Port (Applies to Downlink WCDMA Rx Mode on RXIN4)

BAND (MHz)	Downlink 869 to 894	1 to 804	914 to 2200	2230 to 2255	2255 to 12750
ATTENUATION (dB)	Attenuation	Minimum Attenuation			
	2.5	32	32	6	15

Band V Downlink WCDMA Rx Mode on RXIN4 (Monitor)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb5fd-0	Frequency Band		867.4		891.6	MHz
Wb5fd-1	Sensitivity 3GPP TS25.101 Section 7.3.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-111.5	-104.7	dBm
Wb5fd-4	Sensitivity with Adjacent Channel Interference 3GPP TS25.101 Section 7.5.1	LNA gain high, PGA gain register set to 11, assumed SNDR > -7dB at sensitivity; interfering signals at front-end input -52dBm, at 5MHz offset and -5MHz offset and modulated as in 3GPP, using UL reference measurement channel (12.2kbps) as specified in C.3.1 3GPP 25.101, tested by measurement of SNDR at output on CW input signal at -90dBm, SNDR at MAX-PHY filter output established with FFT		-111	-101	dBm
Wb5fd-9	Spurious Emissions Out-of-Band 3GPP TS25.101 Section 7.9.1 (Note 3)	30MHz to 1000MHz, 100kHz bandwidth (Note 3)		-100	-60	dBm
		1000MHz to 12750MHz, 1MHz bandwidth (Note 3)		-90	-50	

AC ELECTRICAL CHARACTERISTICS (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

Band V Downlink WCDMA Rx Mode on RXIN4 (Monitor) (continued)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Wb5fd-10	Spurious Emissions in Receive Bands 3GPP TS25.101 Section 7.9.2	Front-end assumed response as above, 824MHz to 849MHz and 869MHz to 894MHz (Note 3)		-100	-80	dBm
Wb5fd-11	Conversion Gain High LNA Gain	LNA gain high, PGA gain register set to 11, tested on CW input signal at -90dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the 16-bit output	40	45		dB
Wb5fd-12	Conversion Gain Low LNA Gain	LNA gain low, PGA gain register set to 0, tested on CW input signal at -20dBm, calculated by subtracting the FE input signal in dBm from the ADC output signal in dBFS at digital filter outputs, includes digital gain to the16-bit output		-13	-8.5	dB

GSM850 Band RX Mode

The signal shares the same path as WCDMA Band V downlink. Losses applied are:

1) Diplexer: 0.3dB
2) Band V duplexer, antenna to downlink port (same as WCDMA table)
3) SPDT: 0.3dB

GSM850 Band GMSK Monitor on RXIN4

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
G850-0	RF Frequency		865.2		893.8	MHz
G850-1	Sensitivity 3GPP TS100.910 Section 6.2	LNA gain high, PGA gain register set to 12, assumed SNDR > 7dB at sensitivity;,using static E-TCH/F as specified in 3GPP TS 100.910, production tested by measurement of SNDR at output on CW input signal at -102dBm;,SNDR at MAX-PHY filter output established with FFT		-110		dBm

Tx MODE AC ELECTRICAL CHARACTERISTICS

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
W1	RF Frequency Range	Center of the WCDMA signal, Bands IV and X output (TXOUT)	2112.4		2167.6	MHz
		Center of the WCDMA signal, Bands III and IX output (TXOUT)	1807.4		1877.4	
W2	Linear Output Power	TX_GAIN = 1023	0			dBm
W3	Adjacent Channel Power Ratio	Offset frequency = ±5MHz in 3.84MHz BW		-55		dBc
W4	Alternate Channel Power Ratio	Offset frequency = ±10MHz in 3.84MHz BW		-70		dBc
W5	Rx Band Noise Power, $P_{OUT} \leq$ 0dBm (Note 3)	Noise measured at -400MHz offset in 3.84MHz BW, then convert to per Hz, Band IV and X output		-149	-142	dBm/Hz
		Noise measured at -95MHz offset in 3.84MHz BW, then convert to per Hz, Band III and IX output		-145	-139	
W6	EVM	P_{OUT} = 0dBm		3.8		%
W6a	RCDE	TM6, 8 channels at 0dBm		-28		dB
W7	Minimum Output Power	TX_GAIN = 0		-62	-47	dBm
W8	Output Power Deviation from T_A = +25°C to -40°C (Note 3)	TX_GAIN = 1023		0.8	2.9	dB
W9	Output Power Deviation from T_A = +25°C to +85°C (Note 3)	TX_GAIN = 1023	-3	-0.7		dB
W10	Power Control Step Size Accuracy (1dB)	Five calibration points over the power control range to create four linear regions, any linearly interpolated 1dB TX_GAIN step over the specified power range (W2 and W7) produces 1dB output power step within this error range		±0.25		dB
W11	Power Control Step Size Accuracy (10dB)	Five calibration points over the power control range to create four linear regions, any linearly interpolated 10dB TX_GAIN step over the specified power range (W2 and W7) produces 10dB output power step within this error range		±0.75		dB

AC ELECTRICAL CHARACTERISTICS: GENERAL

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE FREQUENCY INPUT						
R1	Input Level	Test condition	125		600	mV_{P-P}
R2	Input Frequency	Reference divider set to divide-by-2 for frequencies higher than 26MHz	13	19.2	40	MHz
REFERENCE FREQUENCY OUTPUT						
RO1a	REFOUT Output Level, AC	500Ω ll 22pF load, REFOUT_LV_CMOS_SEL = 1	110	320	500	mV_{P-P}
RO1b	REFOUT Output Level, DC			0.8		V
RO2	REFOUT Output Amplitude	500Ω ll 22pF load, REFOUT_LV_CMOS_SEL = 0	2.25	2.7		V_{P-P}
RO4	REFOUT Output Frequency	Matches REFIN frequency (FREF)	13	19.2	40	MHz
Rx DIGITAL LOW-VOLTAGE DIFFERENTIAL SIGNALING OUTPUT INTERFACE						
LV0	Output Bit Rate on Each I and Q	Test condition		153.6		Mbps
LV1	Output Common Mode Voltage			1.2		V
LV3	Output Differential Swing on Load (Note 3)	120Ω differential output load (Note 3)	100	140	220	mV_{PEAK}
LV4	Differential Output Resistance			670		Ω
Tx BASEBAND INTERFACE						
Bb1	Input Bit Rate, on Each I and Q	Test condition		153.6		Mbps
Bb8	Common-Mode Input Voltage			1.25		V
Bb9	Differential Input Swing		112	140	500	mV_{P-P}
Bb10	Differential Input Resistance (Note 3)	Bit TXINDACZI = 1	55	100	140	Ω
Bb11		Bit TXINDACZI = 0	140	220	340	
Rx RF PLL						
RS1	Valid RF Main Division Ratio Range		65		169	
RS3	Valid Main Fractional Divider Programming Value	20-bit resolution	00000		FFFFF	hex
RS5	Charge-Pump Current Gain	Using 800µA setting	0.5	0.82	1.0	mA
RS6a	VCO Tuning Gain	RXVCO, high band	38	127	216	MHz/V
RS6b		RXVCO, low band	21	65	111	
RS9	PLL Settling Time	50kHz loop bandwidth		30		µs

AC ELECTRICAL CHARACTERISTICS: GENERAL (continued)

(MAX2552 EV kit, registers set as described in Table 19 to Table 48, $V_{CC\_}$ = 3.0V to 3.6V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred, T_A = -40°C to +85°C. Typical values are at $V_{CC\_}$ = 3.3V, T_A = +25°C and mid-band, unless otherwise noted. Tx specifications are referred to the output pin of the chip.) (Note 2)

SPEC NO.	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Tx RF PLL						
TS2	Valid RF Main Division Ratio Range		69		167	
TS3	Valid Reference Division Ratios	Division ratios are 1 or 2	1		2	
TS4	Valid Main Fractional Divider Programming Value	20-bit resolution	00000		FFFFF	hex
TS5	Charge-Pump Current CP	800µA	0.5	0.82	1.0	mA
TS9	PLL Settling Time	50kHz loop bandwidth		30		µs
DAC1	Resolution	Monotonicity is production tested		12		Bits
AFC DAC						
DAC3	Output-Voltage High	Load > 200kΩ to GND, AFCDAC = all 1	2.55	2.68		V
DAC4	Output-Voltage Low	Load > 200kΩ to $V_{CC\_}$, AFCDAC = all 0		0.37	0.45	V
DAC6	Settling Time	Step from 0.6V to 2V, settling to ±10mV		1		µs
DIGITAL TEMPERATURE SENSOR						
T1	Output Code vs. Temperature	T_A = -40°C		5		°/code
T2		T_A = +25°C		17		
T3		T_A = +85°C		27		°/code
T5	Code Slope	T_A = -20°C to +70°C		5		
ISOLATION						
M1	RXIN_ Pin-to-Pin Isolation	Between any RXIN_ pins, with one of the two ports disabled		30		dB
M2	TXOUT_ to RXIN_ Isolation	Between any TXOUT and RXIN_, with both ports on		60		dB

Note 2: Production tested at T_A = +25°C. Cold and hot are guaranteed by design and characterization.
Note 3: Guaranteed by design and characterization.

Band III, IV, IX, and X WCDMA Femtocell Transceiver with GSM Monitoring

General Comments

MAX-PHY

MAX-PHY is Maxim's solution for the digital interface system between the radio IC and the baseband/DSP. It is a multimode, software-programmable, digital signal post-processing engine that processes the data out of the radio IC and produces the digital filtered outputs for use in the DSP. It enables multimode operation of the radio through software control. Maxim offers an evaluation kit for the MAX2552 along with an FPGA-based MAX-PHY evaluation platform. The FPGA includes the recommended digital channel-selection filters. The Verilog code for these filters is also available for integration into the DSP. Contact Maxim for further information.

Additional Information

The specifications in the following pages calculate sensitivity with a specified front-end loss from a measured signal-to-noise and distortion ratio (SNDR) and an assumed minimum output $SNDR_{SENS}$ needed for demodulation at sensitivity. The sensitivity values can be related to noise figure by the formula:

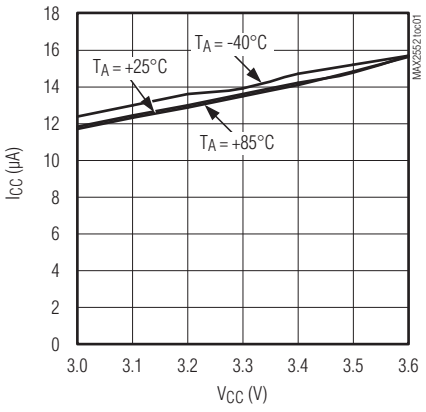
Noise Figure of MAX2552 (dB) = Sensitivity (dBm) - Front-End Loss (dB) - $SNDR_{SENS}$ (dB) + 174dBm/Hz - 10 x LOG(bandwidth in Hz)

Low-noise amplifier (LNA) and programmable-gain amplifier (PGA) gain are set according to the Conditions column in the *Electrical Characteristics* tables. The output SNDR is measured using MAX-PHY and the bandwidth of the measurement is defined by the digital filters in MAX-PHY. DC at the output is excluded from the SNDR measurement. SNDR is calculated using an FFT of the output bytes with a typical FFT length of 2^{14} output samples.

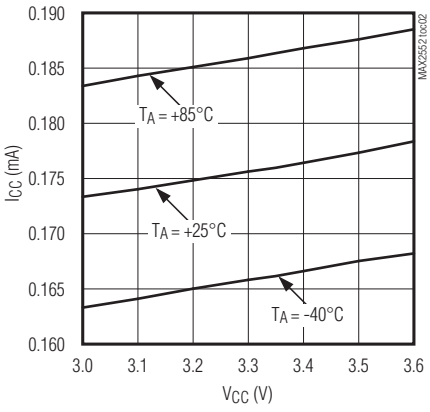
Typical Operating Characteristics

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

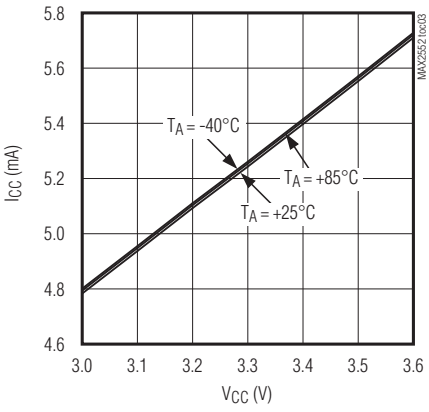
SLEEP MODE I_{CC}



AFC-ONLY MODE I_{CC}



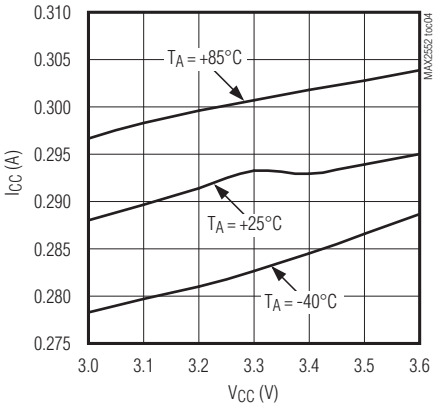
REFERENCE BUFFER MODE I_{CC}



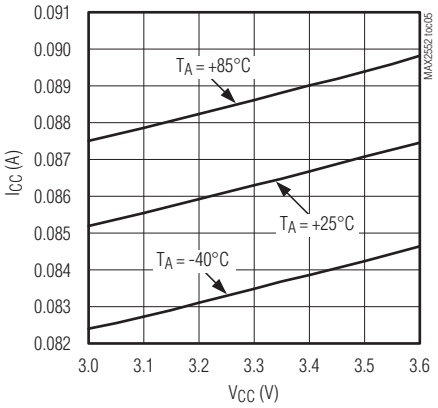
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

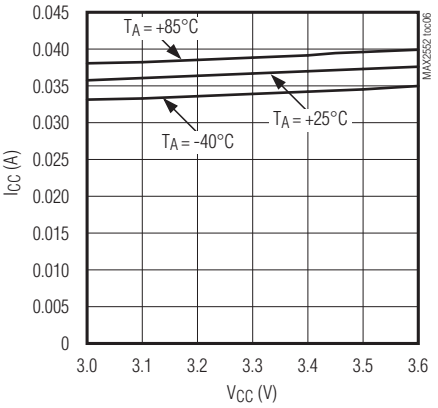
BAND4 FULL DUPLEX MODE I_{CC}



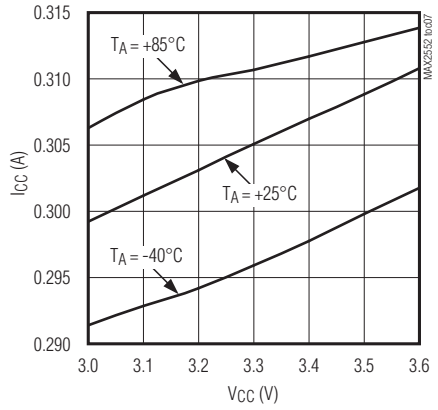
BAND4 RX ONLY MODE I_{CC}



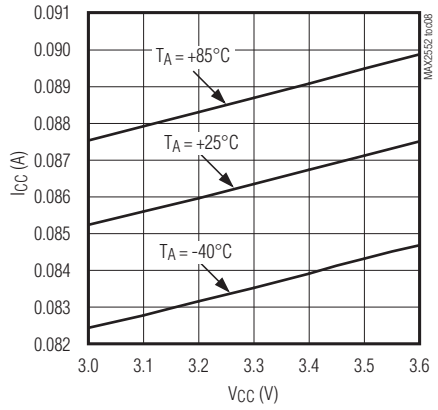
BAND4 RX IDLE MODE I_{CC}



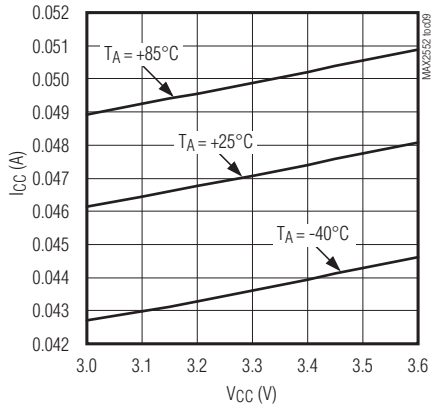
BAND9 FULL DUPLEX MODE I_{CC}



BAND9 RX ONLY MODE I_{CC}



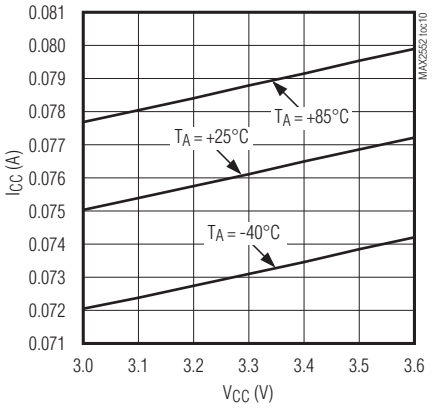
BAND9 RX IDLE MODE I_{CC}



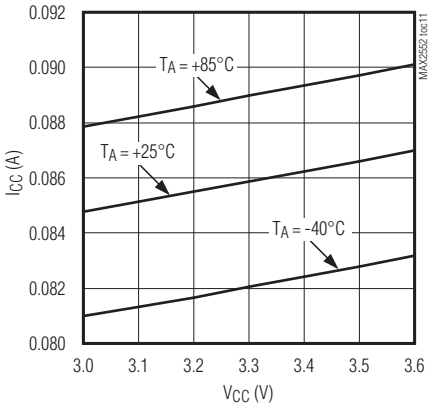
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

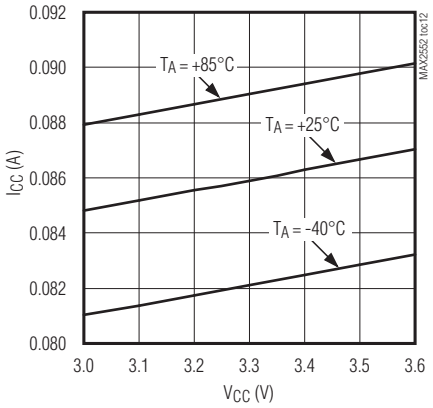
BAND4 RX MONITOR MODE I_{CC}



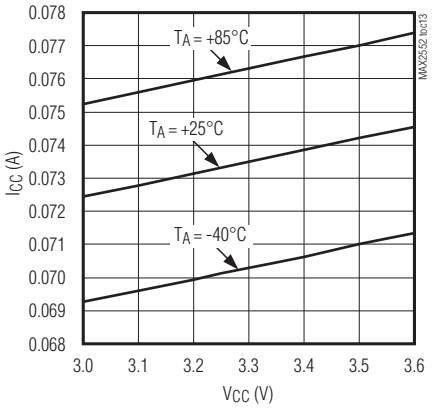
BAND9 RX MONITOR MODE I_{CC}



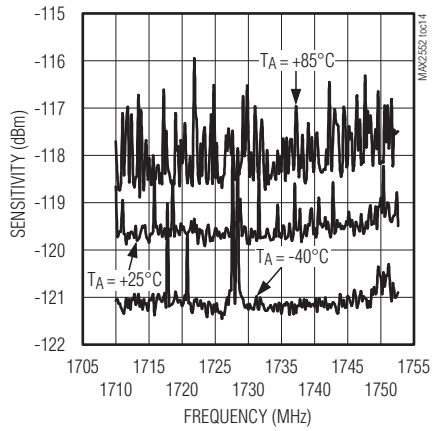
PCS MONITOR MODE I_{CC}



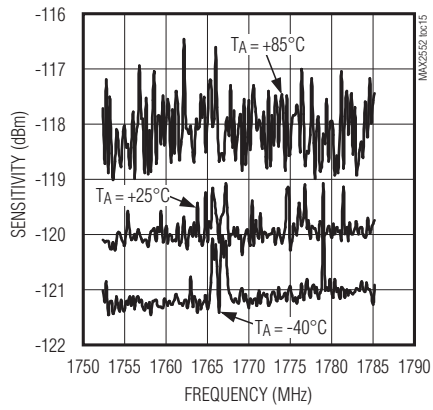
GSM MONITOR MODE I_{CC}



BAND4 UPLINK RX1 SENSITIVITY



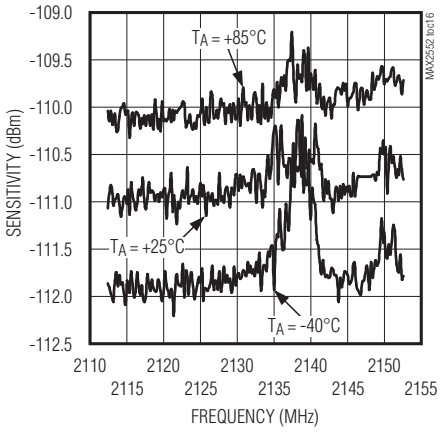
BAND9 UPLINK RX1 SENSITIVITY



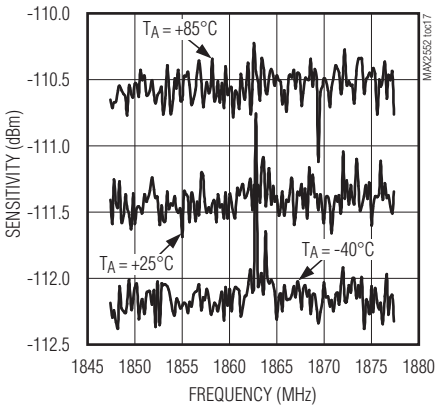
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

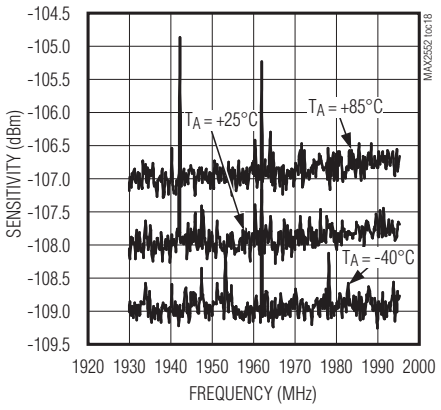
BAND4 DOWNLINK RX5 SENSITIVITY



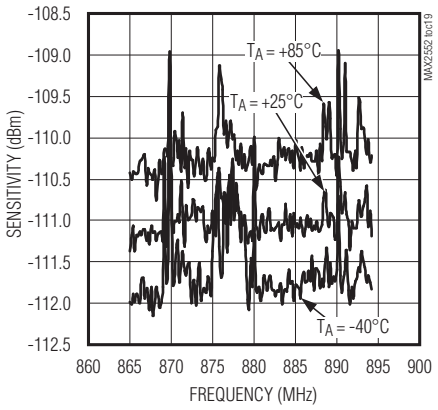
BAND9 DOWNLINK RX2 SENSITIVITY



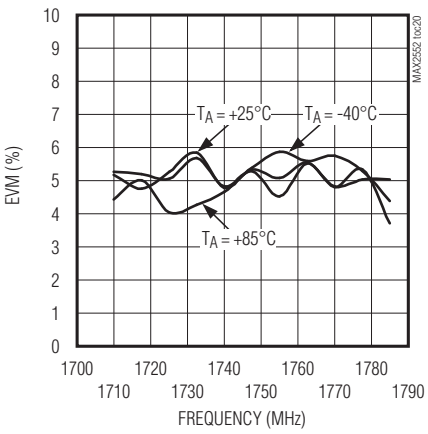
PCS RX2 SENSITIVITY



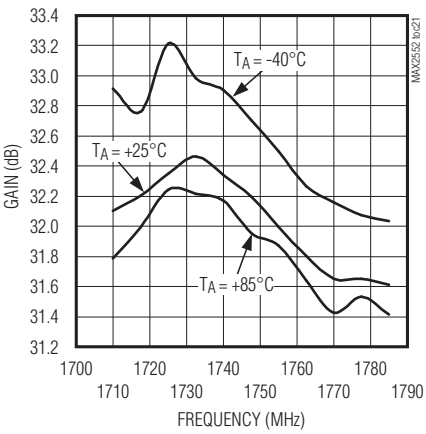
GSM RX4 SENSITIVITY



BAND#4 AND BAND#9 UPLINK RX1 EVM



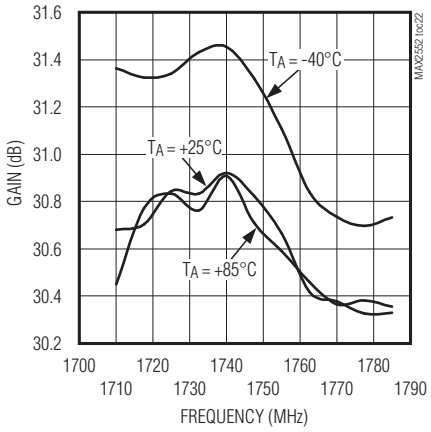
RX1 GAIN, LNA = HIGH, PGA = 6



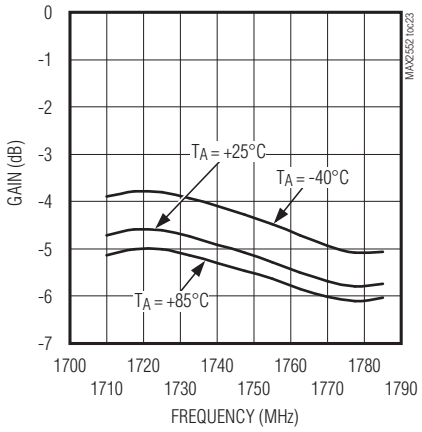
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

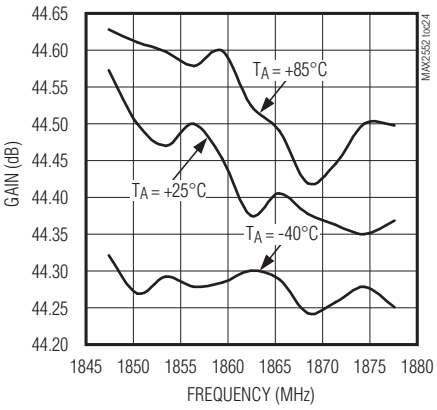
RX1 GAIN, LNA = MID, PGA = 9



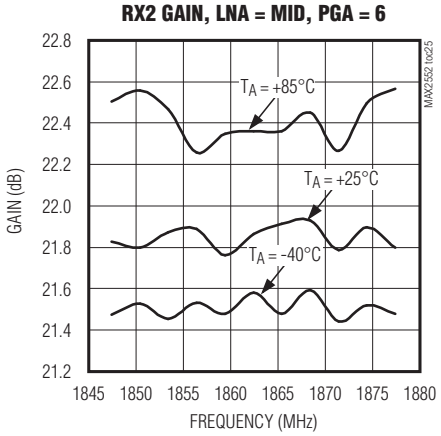
RX1 GAIN, LNA = LOW, PGA = 1



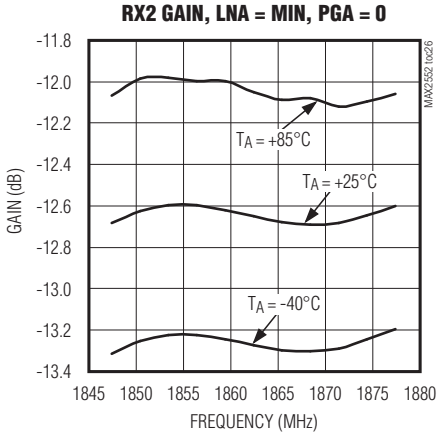
RX2 GAIN, LNA = HIGH, PGA = 11



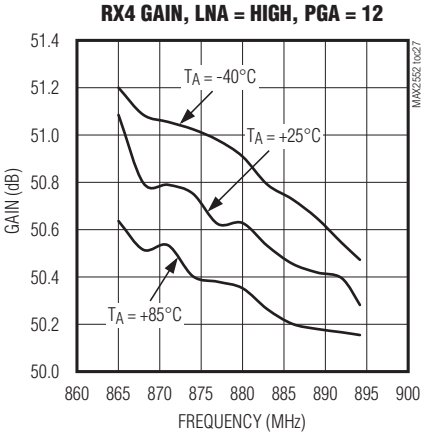
RX2 GAIN, LNA = MID, PGA = 6



RX2 GAIN, LNA = MIN, PGA = 0



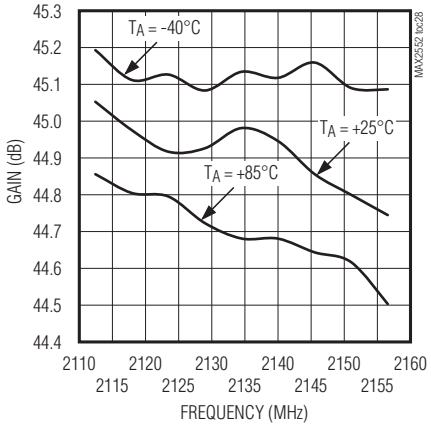
RX4 GAIN, LNA = HIGH, PGA = 12



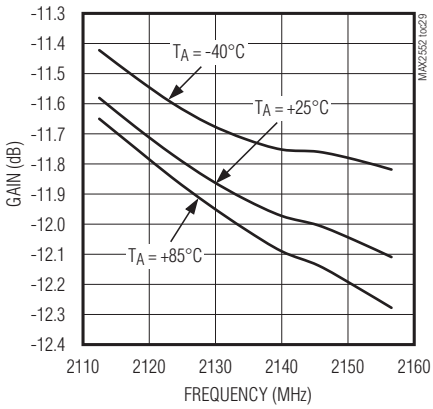
Typical Operating Characteristics (continued)

(MAX2552 EV kit and MAX-PHY FPGA evaluation platform, T_A = +25°C, unless otherwise noted. Registers set as described in Table 19 and Table 20, $V_{CC\_}$ = 3.3V, f_{REFIN} = 19.2MHz, all sensitivity levels and blocker levels are antenna referred.)

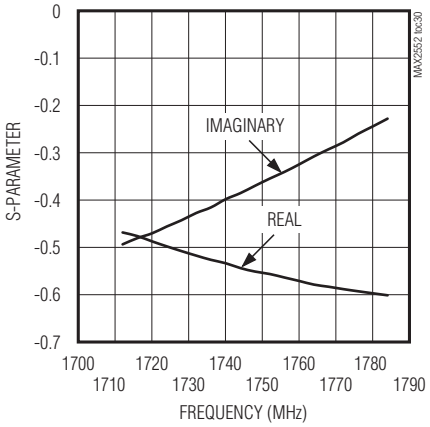
RX5 GAIN, LNA = HIGH, PGA = 11



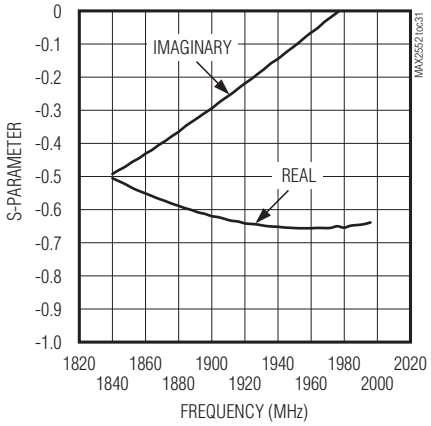
RX5 GAIN, LNA = LOW, PGA = 0



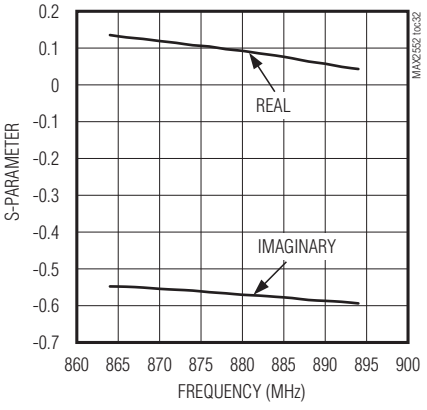
RXIN1 PIN S-PARAMETER



RXIN2 PIN S-PARAMETER



RXIN4 PIN S-PARAMETER



RXIN5 PIN S-PARAMETER