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19-0363; Rev 2; 3/11

EVALUATION KIT AVAILABLE

2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

General Description

The MAX2831/MAX2832 direct conversion, zero-IF, RF transceivers are designed specifically for 2.4GHz to 2.5GHz 802.11g/b WLAN applications. The MAX2831 completely integrates all circuitry required to implement the RF transceiver function, providing an RF power amplifier (PA), RF-to-baseband receive path, baseband-to-RF transmit path, VCO, frequency synthesizer, crystal oscillator, and baseband/control interface. The MAX2832 integrates the same functional blocks except for the PA. Both devices include a fast-settling sigma-delta RF synthesizer with smaller than 20Hz frequency steps and a digitally tuned crystal oscillator allowing use of a low-cost crystal. The devices also integrate on-chip DC-offset cancellation and I/Q errors and carrier leakage-detection circuits. Only an RF bandpass filter (BPF), crystal, RF switch, and a small number of passive components are needed to form a complete 802.11g/b WLAN RF front-end solution.

The MAX2831/MAX2832 completely eliminate the need for an external SAW filter by implementing on-chip monolithic filters for both the receiver and transmitter. The baseband filters are optimized to meet the IEEE 802.11g standard and proprietary turbo modes up to 40MHz channel bandwidth. These devices are suitable for the full range of 802.11g OFDM data rates (6Mbps to 54Mbps) and 802.11b QPSK and CCK data rates (1Mbps to 11Mbps). The ICs are available in a small, 48-pin TQFN package measuring only 7mm x 7mm x 0.8mm.

Applications

Wi-Fi, PDA, VOIP, and Cellular Handsets

Wireless Speakers and Headphones

General 2.4GHz ISM Radios

Features

- **2.4GHz to 2.5GHz ISM Band Operation**
- **IEEE 802.11g/b Compatible (54Mbps OFDM and 11Mbps CCK)**
- **Complete RF Transceiver, PA, and Crystal Oscillator (MAX2831)**
  - **Best-in-Class Transceiver Performance**
  - **62mA Receiver Current**
  - **2.6dB Rx Noise Figure**
  - **-76dBm Rx Sensitivity (54Mbps OFDM)**
  - **No I/Q Calibration Required**
  - **0.1dB/0.35° Rx I/Q Gain/Phase Imbalance**
  - **33dB RF and 62dB Baseband Gain Control Range**
  - **60dB Range Analog RSSI per RF Gain Setting**
  - **Fast Rx I/Q DC-Offset Settling**
  - **Programmable Baseband Lowpass Filter**
  - **20-Bit Sigma-Delta Fractional-N PLL with < 20Hz Step Size**
  - **Digitally Tuned Crystal Oscillator**
  - **+18.5dBm Transmit Power (5.6% EVM with 54Mbps OFDM)**
  - **31dB Tx Gain Control Range**
  - **Integrated Power Detector (MAX2831)**
  - **Serial or Parallel Gain-Control Interface**
  - **> 40dB Tx Sideband Suppression without Calibration**
  - **Tx/Rx I/Q Error Detection**
- **Transceiver Operates from +2.7V to +3.6V**
- **PA Operates from +2.7V to +4.2V (MAX2831)**
- **Low-Power Shutdown Mode**
- **Small 48-Pin TQFN Package (7mm x 7mm x 0.8mm)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX2831ETM+T	-40°C to +85°C	48 TQFN-EP*
MAX2832ETM+T	-40°C to +85°C	48 TQFN-EP*

**EP = Exposed pad.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Pin Configuration appears at end of data sheet.

2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

ABSOLUTE MAXIMUM RATINGS

V_{CCTXPA}, V_{CCPA} and TXRF_ to GND ....-0.3V to +4.5V
V_{CCLNA}, V_{CCTXMX}, V_{CCPLL}, V_{CCCP}, V_{CCXTAL}, V_{CCVCO}, $V_{CCRXVGA}$, V_{CCRXFL}, and $V_{CCRXMX\_}$ to GND....-0.3V to +3.9V
B6, B7, B3, B2, $\overline{SHDN}$, B5, $\overline{CS}$, SCLK, DIN, B1, TUNE, B4, TXBBI_, TXBBQ_, RXHP, RXTX, RXBBI_, RXBBQ_, RSSI, BYPASS, CPOUT, LD, CLOCKOUT, XTAL, CTUNE, RXRF_ to GND ....-0.3V to (Operating V_{CC} + 0.3V)
RXBBI_, RXBBQ_, RSSI, BYPASS, CPOUT, LD, CLOCKOUT Short-Circuit Duration 10s
RF Input Power ....+10dBm
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFN (derates 27.8mW/°C above +70°C) 2.22W
Operating Temperature Range ....-40°C to +85°C
Junction Temperature ....+150°C
Storage Temperature Range ....-65°C to +160°C
Lead Temperature (soldering, 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION! ESD SENSITIVE DEVICE

DC ELECTRICAL CHARACTERISTICS

(MAX2831 EV kit: $V_{CC\_}$ = 2.7V to 3.6V, V_{CCPA} = V_{CCTXPA} = 2.7V to 4.2V, T_A = -40°C to +85°C, Rx set to the maximum gain. $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RSSI and clock output buffer are off, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open. 100mV_{RMS} differential I and Q signals (54Mbps IEEE 802.11g OFDM) applied to I/Q baseband inputs of transmitter in transmit mode, f_{REF} = 40MHz, and registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at V_{CC} = 2.8V, V_{CCPA} = 3.3V, and T_A = +25°C, LO frequency = 2.437GHz, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETERS	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage	$V_{CC\_}$		2.7		3.6	V
	V_{CCPA}, V_{CCTXPA}		2.7		4.2	
Supply Current	Shutdown mode, B7: B1 = 0000000, reference oscillator not applied	T_A = +25°C		20		μA
	Standby mode	T_A = +25°C		28	35	mA
		T_A = -40°C to +85°C			35	
	Rx mode	T_A = +25°C		62	78	
		T_A = -40°C to +85°C			82	
	Tx mode, T_A = +25°C, V_{CC} = 2.8V, V_{CCPA} = 3.3V, (Note 2)	MAX2831, transmit section		82	104	
		MAX2831, PA, P_{OUT} = +18.2dBm		209	258	
		MAX2832		86		
	Rx calibration mode	T_A = +25°C		101		
	Tx calibration mode	T_A = +25°C		78		
Rx I/Q Output Common-Mode Voltage	T_A = +25°C at default common-mode setting		0.98	1.2	1.33	V
Rx I/Q Output Common-Mode Voltage Variation	T_A = -40°C (relative to T_A = +25°C)			-17		mV
	T_A = +85°C (relative to T_A = +25°C)			15		
Tx Baseband Input Common-Mode Voltage Operating Range	DC-coupled		0.9		1.3	V
Tx Baseband Input Bias Current	Source current				22	μA

DC ELECTRICAL CHARACTERISTICS (continued)

(MAX2831 EV kit: $V_{CC\_}$ = 2.7V to 3.6V, V_{CCPA} = V_{CCTXPA} = 2.7V to 4.2V, T_A = -40°C to +85°C, Rx set to the maximum gain. $\overline{CS}$ = high, RXHP = SCLK = DIN = low, RSSI and clock output buffer are off, no signal at RF inputs, all RF inputs and outputs terminated into 50Ω, receiver baseband outputs are open. 100mV$_{RMS}$ differential I and Q signals (54Mbps IEEE 802.11g OFDM) applied to I/Q baseband inputs of transmitter in transmit mode, f_{REF} = 40MHz, and registers set to recommended settings and corresponding test mode, unless otherwise noted. Typical values are at V_{CC} = 2.8V, V_{CCPA} = 3.3V, and T_A = +25°C, LO frequency = 2.437GHz, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS: $\overline{SHDN}$, RXTX, SCLK, DIN, $\overline{CS}$, B7:B1, RXHP					
Digital Input-Voltage High, V_{IH}		V_{CC} - 0.4			V
Digital Input-Voltage Low, V_{IL}				0.4	V
Digital Input-Current High, I_{IH}		-1		+1	µA
Digital Input-Current Low, I_{IL}		-1		+1	µA
LOGIC OUTPUTS: LD, CLOCKOUT					
Digital Output-Voltage High, V_{OH}	Sourcing 100µA	V_{CC} - 0.4			V
Digital Output-Voltage Low, V_{OL}	Sinking 100µA			0.4	V

AC ELECTRICAL CHARACTERISTICS—Rx Mode

(MAX2831 EV kit: $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A =+25°C, f_{RF} = 2.439GHz, f_{LO} = 2.437GHz; receiver baseband I/Q outputs at 112 mV$_{RMS}$ (-19dBV), f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXTX = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications which normally apply over the entire operating conditions, unless otherwise indicated. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER SECTION: LNA RF INPUT-TO-BASEBAND I/Q OUTPUTS						
RF Input Frequency Range			2.4		2.5	GHz
RF Input Return Loss	High RF gain			18		dB
	Mid RF gain			11		
	Low RF gain			14		
Total Voltage Gain	Maximum gain, B7:B1 = 1111111	T_A = +25°C	86	98		dB
		T_A = -40°C to +85°C	83			
	Minimum gain, B7:B1 = 0000000	T_A = +25°C		3	8	
RF Gain Steps (Note 3)	From high-gain mode (B7:B6 = 11) to medium-gain mode (B7:B6 = 10)			-16		dB
	From high-gain mode (B7:B6 = 11) to low-gain mode (B7:B6 = 0X)			-33		
RF Gain-Change Settling Time	Gain change from high gain to medium gain, high gain to low, or medium gain to low gain; gain settling to within ±2dB of steady state; RXHP = 1			0.2		µs

AC ELECTRICAL CHARACTERISTICS—Rx Mode (continued)

(MAX2831 EV kit: $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A =+25°C, f_{RF} = 2.439GHz, f_{LO} = 2.437GHz; receiver baseband I/Q outputs at 112 mV_{RMS} (-19dBV), f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXTX = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications which normally apply over the entire operating conditions, unless otherwise indicated. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Baseband Gain Range	From maximum baseband gain (B5:B1 = 11111) to minimum baseband gain (B5:B1 = 00000)		55	62	67	dB
DSB Noise Figure	Voltage gain = maximum with B7:B6 = 11			2.6		dB
	Voltage gain = 50dB with B7:B6 = 11			3.2		
	Voltage gain = 45dB with B7:B6 = 10			16		
	Voltage gain = 15dB with B7:B6 = 0X			34		
In-Band Compression Point Based on EVM	$-19dBV_{RMS}$ baseband output EVM degrades to 9%	B7:B6 = 11		-41		dBm
		B7:B6 = 10		-24		
		B7:B6 = 0X		-6		
In-Band Output P-1dB	Voltage gain = 90dB, with B7:B6 = 11			2.5		V_{P-P}
Out-of-Band Input IP3 (Note 4)	B7:B6 = 11			-12		dBm
	B7:B6 = 10			-4		
	B7:B6 = 0X			24		
I/Q Phase Error	1σ variation (without calibration)			±0.35		Degrees
I/Q Gain Imbalance	1σ variation (without calibration)			±0.1		dB
RX I/Q Output Load Impedance (R ll C)	Minimum differential resistance			10		kΩ
	Maximum differential capacitance			10		pF
Tx-to-Rx Conversion Gain for Rx I/Q Calibration	For receiver gain, B7:B1 = 1101111 (Note 5)			0.5		dB
Baseband VGA Settling Time	Gain change from B5:B1 = 10111 to B5:B1 = 00111; gain settling to within ±2dB of steady state			0.1		µs
I/Q Output DC Step when RXHP Transitions from 1 to 0 in Presence of 802.11g Short Sequence	After switching RXHP to logic 0 from initial logic 1, during ideal short sequence data at -55dBm input in AWGN channel, for -19dBV output; normalized to RMS signal on I and Q outputs; transition point varied from 0 to 0.8µs in steps of 0.1µs			-5		dBc
I/Q Output DC Droop	After switching RXHP to 0, D13:D12, Register 7 (A3:A0 = 0111)			±1		V/s
I/Q Static DC Offset	RXHP = 1, B7:B1 = 1101110, 1σ variation			±1		mV
Spurious Signal Emissions from LNA input	RF = 1GHz to 26.5GHz			-51		dBm
RECEIVER BASEBAND FILTERS						
Gain Ripple in Passband	10kHz to 8.5MHz at baseband			±1.3		DB_{P-P}
Group-Delay Ripple in Passband	10kHz to 8.5MHz at baseband			±45		ns_{P-P}

AC ELECTRICAL CHARACTERISTICS—Rx Mode (continued)

(MAX2831 EV kit: $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A =+25°C, f_{RF} = 2.439GHz, f_{LO} = 2.437GHz; receiver baseband I/Q outputs at 112 mV_{RMS} (-19dBV), f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXTX = SCLK = DIN = low, with power matching for the differential RF pins using the typical applications and registers set to default settings and corresponding test mode, unless otherwise noted. Unmodulated single-tone RF input signal is used with specifications which normally apply over the entire operating conditions, unless otherwise indicated. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Baseband Filter Rejection (Nominal Mode)	At 8.5MHz			3.2		dB
	At 15MHz			27		
	At 20MHz			50		
	At > 40MHz			80		
RSSI						
RSSI Minimum Output Voltage	R_{LOAD} ≥ 10kΩ ll 5pF			0.4		V
RSSI Maximum Output Voltage	R_{LOAD} ≥ 10kΩ ll 5pF			2.4		V
RSSI Slope				30		mV/dB
RSSI Output Settling Time	To within 3dB of steady state	+32dB signal step		200		ns
		-32dB signal step		600		

AC ELECTRICAL CHARACTERISTICS—Tx Mode

(MAX2831 EV kit: $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{RF} = 2.439GHz , f_{LO} = 2.437GHz. f_{REF} = 40MHz, $\overline{SHDN}$ = RXTX = $\overline{CS}$ = high, and SCLK = DIN = low, with power matching for the differential RF pins using the typical applications circuit. 100mV$_{RMS}$ sine and cosine signal (or 100mV$_{RMS}$ 54Mbps IEEE 802.11g I/Q signals wherever OFDM is mentioned) applied to baseband I/Q inputs of transmitter (differential DC-coupled). Registers set to recommend settings and corresponding test mode, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
TRANSMIT SECTION: Tx BASEBAND I/Q INPUTS TO RF OUTPUTS							
RF Output Frequency Range				2.4		2.5	GHz
Output Power	MAX2831	54Mbps 802.11g OFDM signal	Output power adjusted to meet 5.6% EVM, and spectral mask		18.5		dBm
			B6:B1 = 000000		-7.5		
		802.11b signal, 141mV$_{RMS}$, IEEE802.11b I/Q signals	Output power adjusted to meet spectral mask		21		
	MAX2832	-3dB VGA back off			-5.3		
		B6:B1 = 000000			-31.5		
Unwanted Sideband Suppression	Without I/Q calibration, B6:B1 = 100001				-42		dBc
Carrier Leakage at Center Frequency of Channel	Without DC offset correction				-30		dBc
Transmitter Spurious Signal Emissions (MAX2831)	B6:B1 = 111000, OFDM signal		1/3 x f_{LO}		-67		dBm/MHz
			< 1GHz		-36		
			> 1GHz		-47		
			2/3 x f_{LO}		-64		
			4/3 x f_{LO}		-42		
			5/3 x f_{LO}		-65		
			8/3 x f_{LO}		-51		
			2 x f_{LO}		-33		
			3 x f_{LO}		-54		
Transmitter Spurious Signal Emissions (MAX2832)	B6:B1 = 111111, OFDM signal		1/3 x f_{LO}		-78		dBm/MHz
			< 1GHz		-65		
			> 1GHz		-72		
			2/3 x f_{LO}		-78		
			4/3 x f_{LO}		-46		
			5/3 x f_{LO}		-72		
			8/3 x f_{LO}		-46		
			2 x f_{LO}		-60		
			3 x f_{LO}		-75		

AC ELECTRICAL CHARACTERISTICS—Tx Mode (continued)

(MAX2831 EV kit: $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{RF} = 2.439GHz , f_{LO} = 2.437GHz. f_{REF} = 40MHz, $\overline{SHDN}$ = RXTX = $\overline{CS}$ = high, and SCLK = DIN = low, with power matching for the differential RF pins using the typical applications circuit. 100mV$_{RMS}$ sine and cosine signal (or 100mV$_{RMS}$ 54Mbps IEEE 802.11g I/Q signals wherever OFDM is mentioned) applied to baseband I/Q inputs of transmitter (differential DC-coupled). Registers set to recommend settings and corresponding test mode, unless otherwise noted. RF inputs/outputs specifications are referenced to device pins and do not include 1dB loss from EV kit PCB, balun, and SMA connectors.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
RF Output Return Loss	Off-chip balun + match, single-ended	MAX2831		-20		dB
		MAX2832		-10		
Tx I/Q Input Load Impedance (R ll C)	Minimum differential resistance			20		kΩ
	Maximum differential capacitance			0.7		pF
Baseband -3dB Corner Frequency	D1:D0 = 01, Register 8 (A3:A0 = 1000)	Nominal mode		11		MHz
Baseband Filter Rejection	At 30MHz, in nominal mode			62		dB
Minimum Power Detector Output Voltage	Short sequence transmitter power = +9dBm			0.3		V
Maximum Power Detector Output Voltage	Short sequence transmitter power = +19dBm			1.2		V
RF Power Detector Response Time				0.3		µs
TRANSMITTER LO LEAKAGE AND I/Q CALIBRATION USING LO LEAKAGE AND SIDEBAND DETECTOR (see the *Tx/Rx Calibration Mode* section)						
Tx BASEBAND I/Q INPUTS TO RECEIVER OUTPUTS						
LO Leakage and Sideband Detector Output	Calibration register, D12:D11 = 00, A3:A0 = 0110	Output at 1 x f_{TONE} (for LO leakage = -29dBc), f_{TONE} = 2MHz, 100mV$_{RMS}$		-34		dBV$_{RMS}$
		Output at 2 x f_{TONE} (for LO leakage = -240dBc), f_{TONE} = 2MHz, 100mV$_{RMS}$		-44		
Amplifier Gain Range	D12:D11 = 00 to D12:D11 = 11, A3:A0 = 0110			30		dB
Lower -3dB Corner Frequency				1		MHz

2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

AC ELECTRICAL CHARACTERISTICS—Frequency Synthesis

(MAX2831 EV kit: $V_{CC\_}$ = 2.7V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 150kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
FREQUENCY SYNTHESIZER						
RF Channel Center Frequency			2.4		2.5	GHz
Channel Center Frequency Programming Minimum Step Size				20		Hz
Charge-Pump Comparison Frequency				20		MHz
Reference Frequency Range			20		44	MHz
Reference Frequency Input Levels	AC-coupled to XTAL pin		800			mV_{P-P}
Reference Frequency Input Impedance (R ll C)	Resistance (XTAL)			5		kΩ
	Capacitance (XTAL)			4		pF
Closed-Loop Phase Noise	f_{OFFSET} = 1kHz			-86		dBc/Hz
	f_{OFFSET} = 10kHz			-94		
	f_{OFFSET} = 100kHz			-94		
	f_{OFFSET} = 1MHz			-110		
	f_{OFFSET} = 10MHz			-120		
Closed-Loop Integrated Phase Noise	RMS phase jitter; integrate from 10kHz to 10MHz offset			0.9		Degrees
Charge-Pump Output Current				1		mA
Reference Spurs	20MHz offset			-55		dBc
VCO Frequency Error	Measured from Tx-Rx or Rx-Tx transition	3µs to 9µs		50		kHz
		> 9µs		1		
VOLTAGE-CONTROLLED OSCILLATOR						
Pushing	Referred to 2400MHz LO, V_{CC} varies by 0.3V			210		kHz
VCO Tuning Voltage Range			0.5		2.2	V
LO Tuning Gain	V_{TUNE} = 0.5V			103		MHz/V
	V_{TUNE} = 2.2V			86		

AC ELECTRICAL CHARACTERISTICS—Miscellaneous Blocks

(MAX2831 EV kit: $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, f_{LO} = 2.437GHZ, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CRYSTAL OSCILLATOR						
On-Chip Tuning Capacitance Range	Maximum capacitance, A3:A0 = 1110, D6:D0 = 1111111			15.4		pF
	Minimum capacitance, A3:A0 = 1110, D6:D0 = 0000000			0.5		
On-Chip Tuning Capacitance Step Size				0.12		pF
ON-CHIP TEMPERATURE SENSOR						
Output Voltage	A3:A0 = 1000, D9:D8 = 01	T_A = -40°C		0.35		V
		T_A = +25°C		1		
		T_A = +85°C		1.6		

AC ELECTRICAL CHARACTERISTICS—Timing

(MAX2831 EV kit: $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A =+25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 150kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SYSTEM TIMING (See Figure 3)						
Turn-On Time	From $\overline{SHDN}$ rising edge to LO settled within 1kHz using external reference frequency input			60		µs
Crystal Oscillator Turn-On Time	90% of final output amplitude level			1		ms
Channel Switching Time	Loop BW = 150kHz, f_{RF} = 2.5GHz to 2.4GHz			25		µs
Rx/Tx Turnaround Time	Measured from Tx or Rx enable rising edge; signal settling to within ±2dB of steady state	Rx to Tx		2		µs
		Tx to Rx, RXHP = 1		2		
Tx Turn-On Time (from Standby Mode)	From Tx-enable active rising edge; signal settling to within ±2dB of steady state			1.5		µs
Tx Turn-Off Time (from Standby Mode)	From Tx-enable inactive rising edge			1		µs
Rx Turn-On Time (from Standby Mode)	From Rx-enable active rising edge; signal settling to within ±2dB of steady state			1.9		µs
Rx Turn-Off Time (from Standby Mode)	From Rx-enable inactive rising edge			0.1		µs

2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

AC ELECTRICAL CHARACTERISTICS—Timing (continued)

(MAX2831 EV kit: $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A =+25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, SCLK = DIN = low, PLL loop bandwidth = 150kHz, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
3-WIRE SERIAL-INTERFACE TIMING (See Figure 2)					
SCLK Rising Edge to $\overline{CS}$ Falling Edge Wait Time, t_{CSO}			6		ns
Falling Edge of $\overline{CS}$ to Rising Edge of First SCLK Time, t_{CSS}			6		ns
DIN to SCLK Setup Time, t_{DS}			6		ns
DIN to SCLK Hold Time, t_{DH}			6		ns
SCLK Pulse-Width High, t_{CH}			6		ns
SCLK Pulse-Width Low, t_{CL}			6		ns
Last Rising Edge of SCLK to Rising Edge of $\overline{CS}$ or Clock to Load Enable Setup Time, t_{CSH}			6		ns
$\overline{CS}$ High Pulse Width, t_{CSW}			20		ns
Time Between the Rising Edge of $\overline{CS}$ and the Next Rising Edge of SCLK, t_{CS1}			6		ns
Clock Frequency, f_{CLK}			20		MHz
Rise Time, t_R			2		ns
Fall Time, t_F			2		ns

Note 1: Min and max limits are guaranteed by test at T_A = +25°C and +85°C and guaranteed by design and characterization at T_A = -40°C. The power-on register settings are not production tested. Recommended register setting must be loaded after V_{CC} is supplied.

Note 2: Guaranteed by design and characterization.

Note 3: The nominal part-to-part variation of the RF gain step is ±1dB.

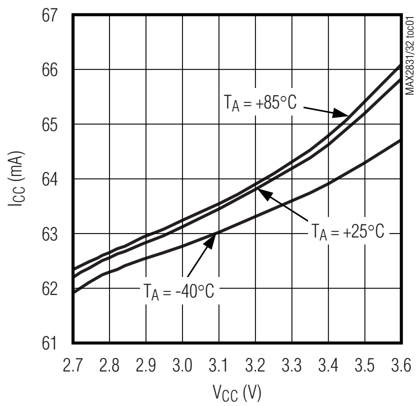
Note 4: Two tones at +25MHz and +48MHz offset with -35dBm/tone. Measure IM3 at 2MHz.

Note 5: Tx I/Q inputs = $100mV_{RMS}$.

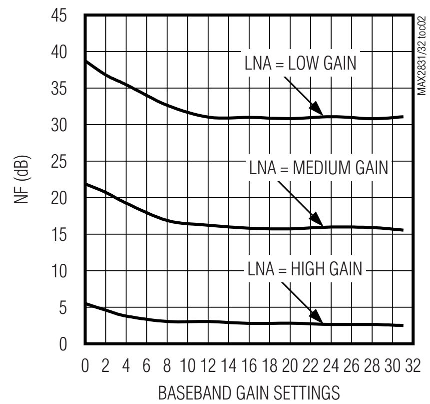
Typical Operating Characteristics

(MAX2831 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

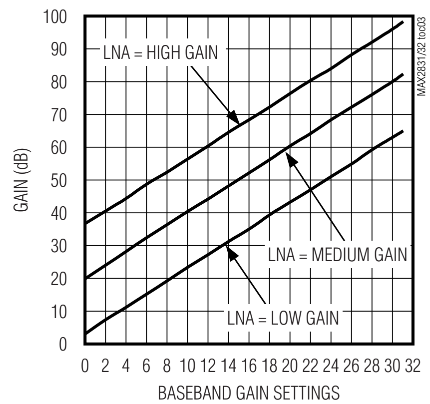
Rx I_{CC} vs. V_{CC}



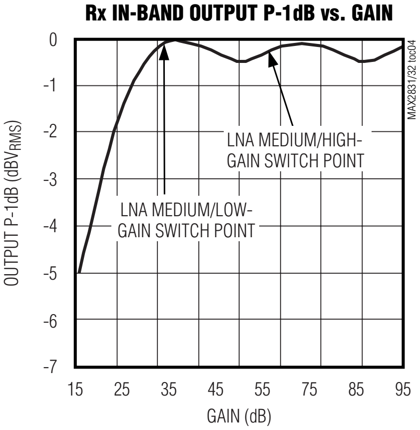
NOISE FIGURE vs. BASEBAND GAIN SETTINGS



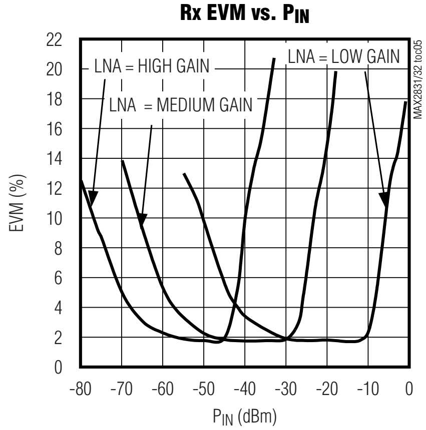
Rx VOLTAGE GAIN vs. BASEBAND GAIN SETTING



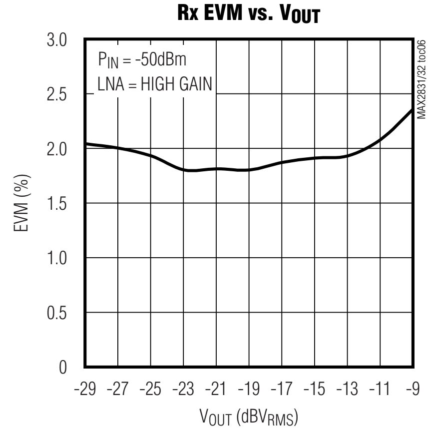
Rx IN-BAND OUTPUT P-1dB vs. GAIN



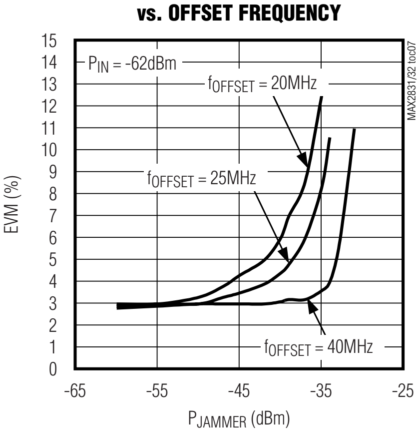
Rx EVM vs. P_{IN}



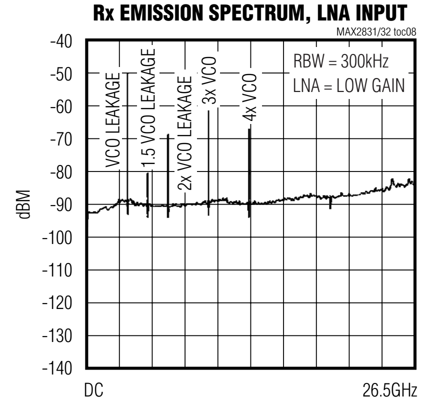
Rx EVM vs. V_{OUT}



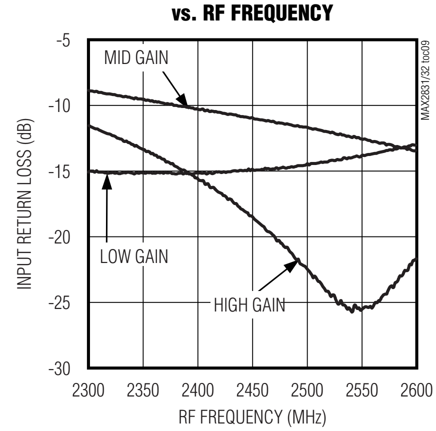
OFDM EVM WITH OFDM JAMMER vs. OFFSET FREQUENCY



Rx EMISSION SPECTRUM, LNA INPUT



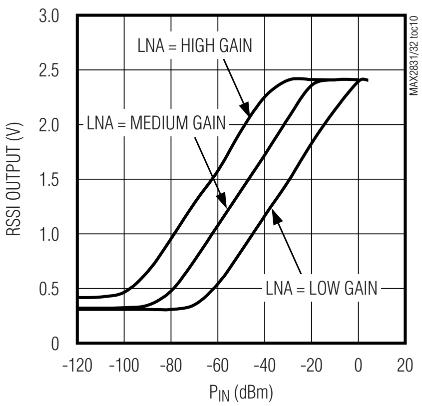
LNA INPUT RETURN LOSS vs. RF FREQUENCY



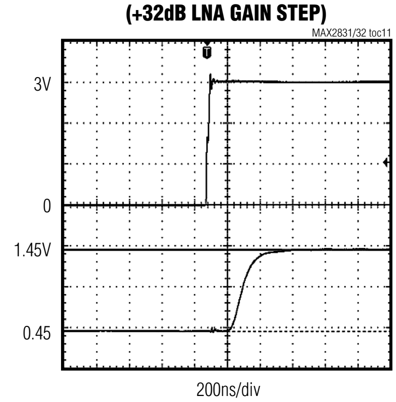
Typical Operating Characteristics (continued)

(MAX2831 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

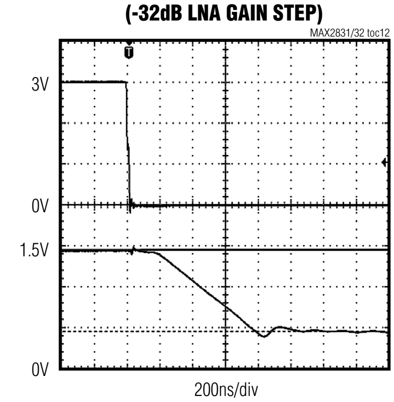
Rx RSSI OUTPUT vs. INPUT POWER



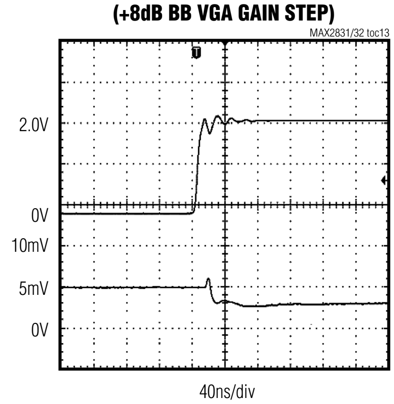
Rx RSSI STEP RESPONSE (+32dB LNA GAIN STEP)



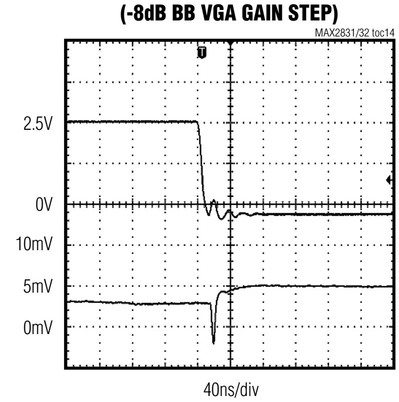
Rx RSSI STEP RESPONSE (-32dB LNA GAIN STEP)



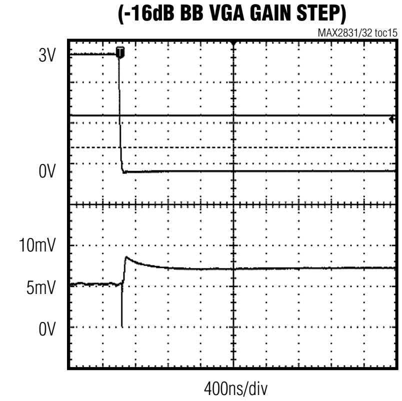
Rx I/Q DC OFFSET SETTLING RESPONSE (+8dB BB VGA GAIN STEP)



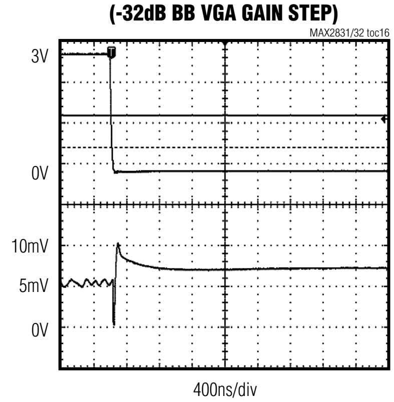
Rx I/Q DC OFFSET SETTLING RESPONSE (-8dB BB VGA GAIN STEP)



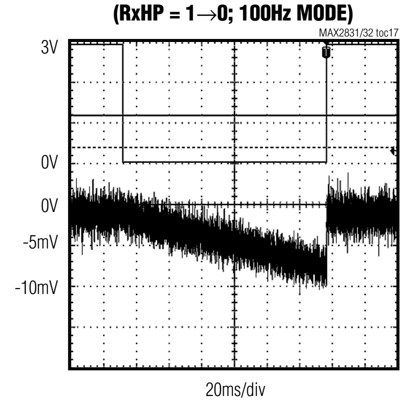
Rx I/Q DC OFFSET SETTLING RESPONSE (-16dB BB VGA GAIN STEP)



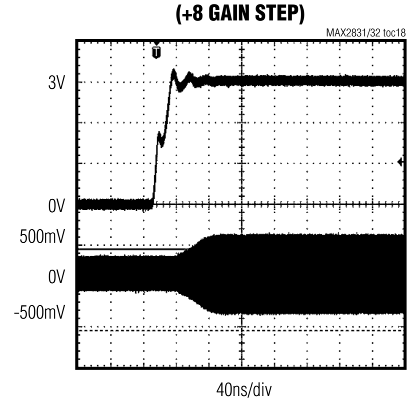
Rx I/Q DC OFFSET SETTLING RESPONSE (-32dB BB VGA GAIN STEP)



I/Q OUTPUT DC ERROR DROOP (RxHP = 1→0; 100Hz MODE)



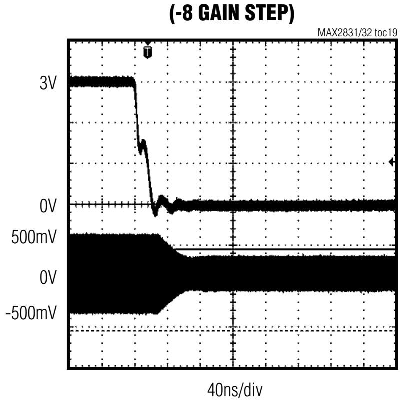
Rx BB VGA SETTLING RESPONSE (+8 GAIN STEP)



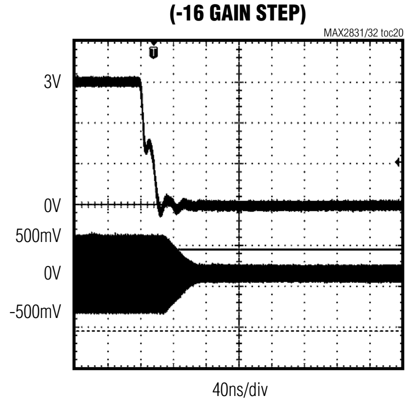
Typical Operating Characteristics (continued)

(MAX2831 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

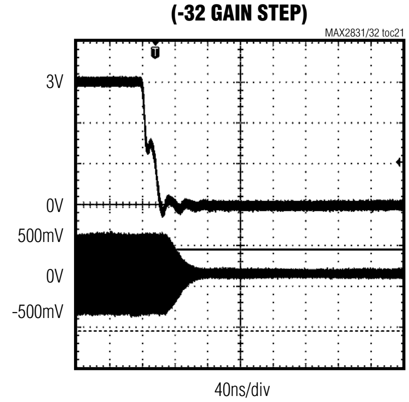
Rx BB VGA SETTLING RESPONSE (-8 GAIN STEP)



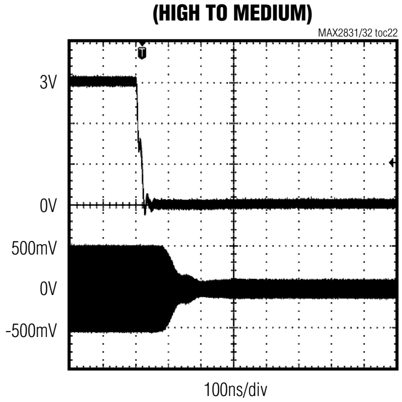
Rx BB VGA SETTLING RESPONSE (-16 GAIN STEP)



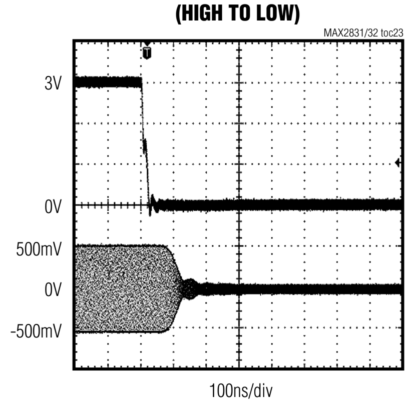
Rx BB VGA SETTLING RESPONSE (-32 GAIN STEP)



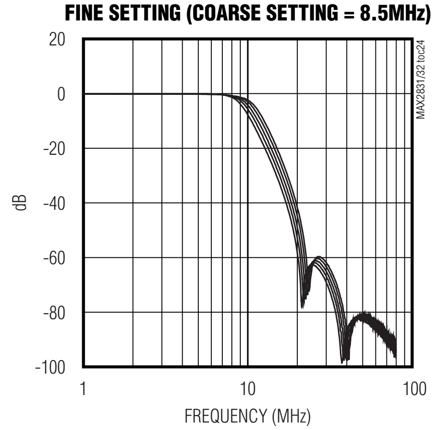
RF LNA SETTLING RESPONSE (HIGH TO MEDIUM)



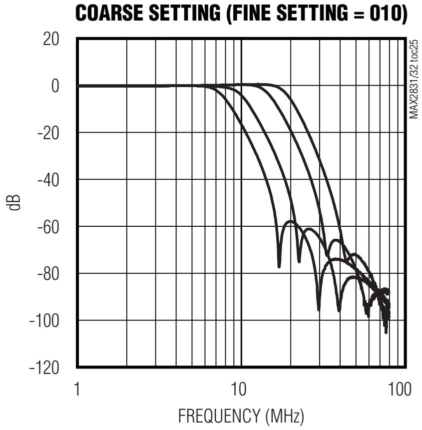
RF LNA SETTLING RESPONSE (HIGH TO LOW)



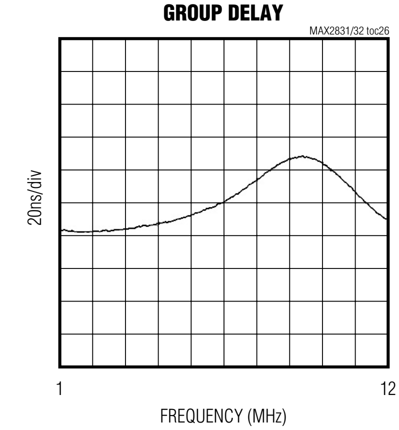
Rx BB FREQUENCY RESPONSE vs. FINE SETTING (COARSE SETTING = 8.5MHz)



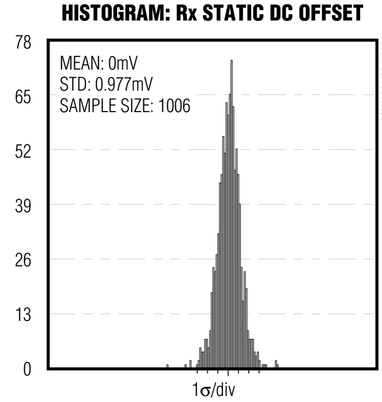
Rx BB FREQUENCY RESPONSE vs. COARSE SETTING (FINE SETTING = 010)



RX BASEBAND FILTER GROUP DELAY



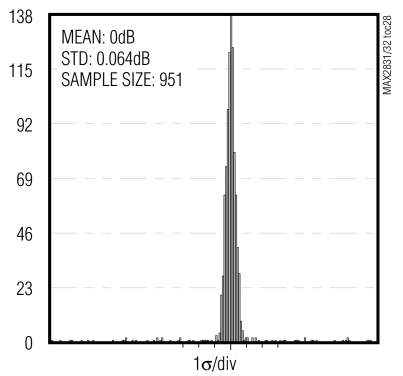
HISTOGRAM: Rx STATIC DC OFFSET



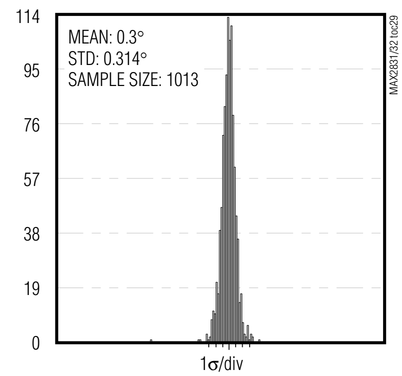
Typical Operating Characteristics (continued)

(MAX2831 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

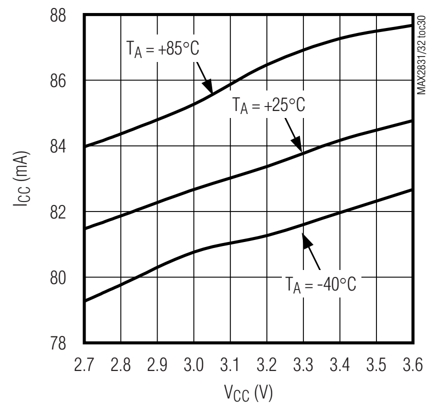
HISTOGRAM: Rx GAIN IMBALANCE



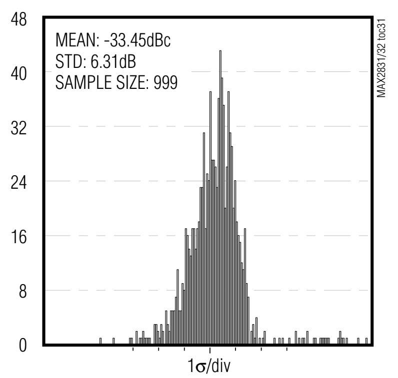
HISTOGRAM: Rx PHASE IMBALANCE



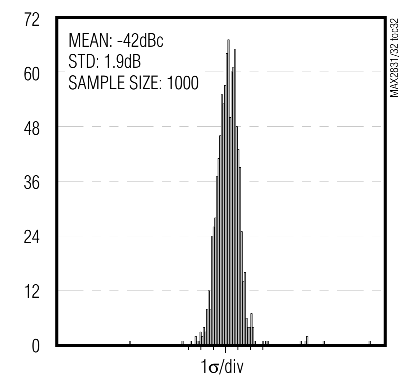
Tx I_{CC} vs. V_{CC}



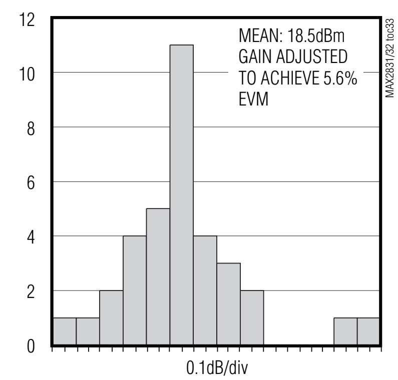
HISTOGRAM: Tx LO LEAKAGE



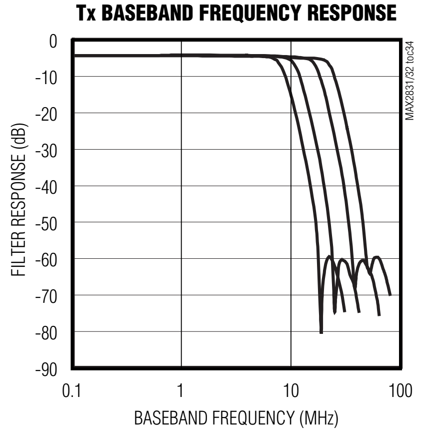
HISTOGRAM: Tx SIDEBAND SUPPRESSION



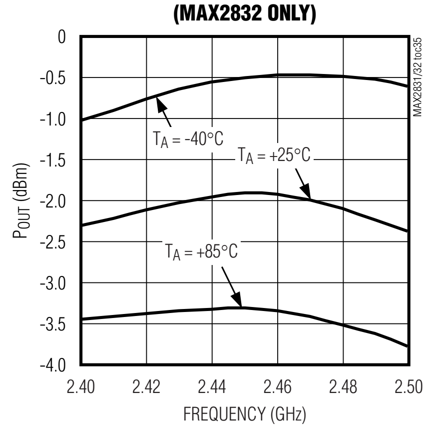
HISTOGRAM: Tx OUTPUT POWER VARIATION



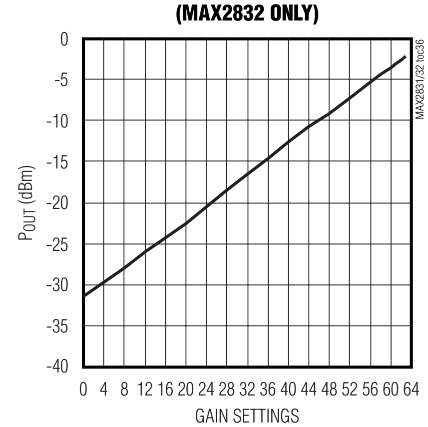
Tx BASEBAND FREQUENCY RESPONSE



Tx OUTPUT POWER vs. FREQUENCY (B6:B1 = 111111) (MAX2832 ONLY)



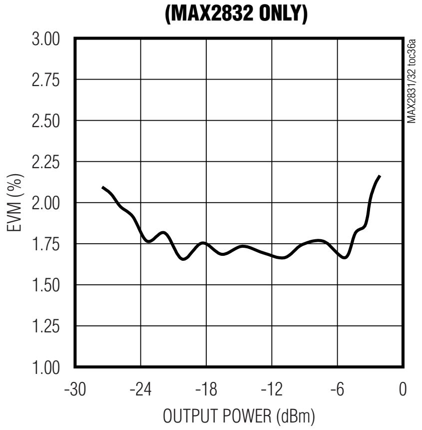
Tx OUTPUT POWER vs. GAIN SETTING (MAX2832 ONLY)



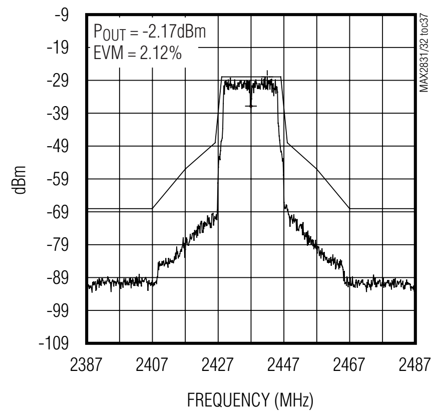
Typical Operating Characteristics (continued)

(MAX2831 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

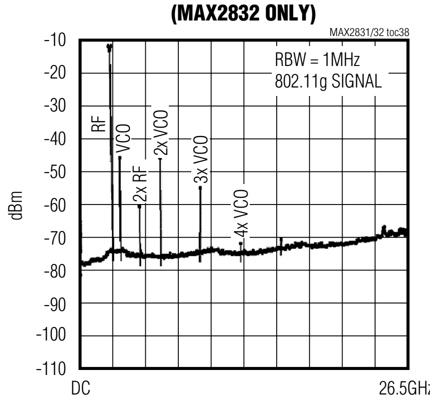
EVM vs. Tx OUTPUT POWER (MAX2832 ONLY)



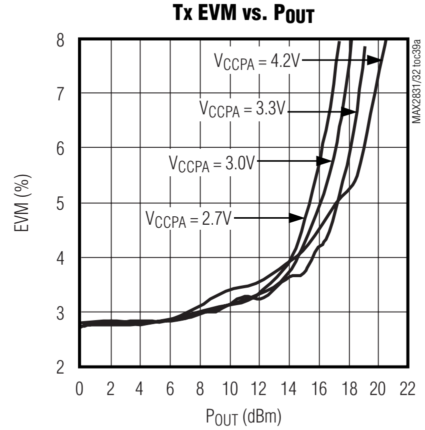
11g SPECTRAL MASK (MAX2832 ONLY)



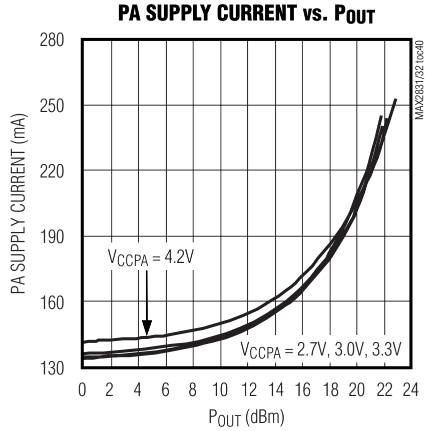
Tx OUTPUT SPURS (MAX2832 ONLY)



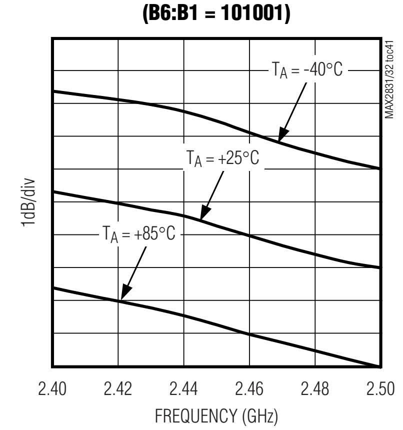
Tx EVM vs. P_{OUT}



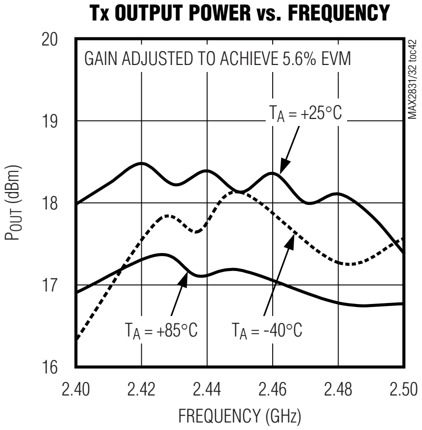
PA SUPPLY CURRENT vs. P_{OUT}



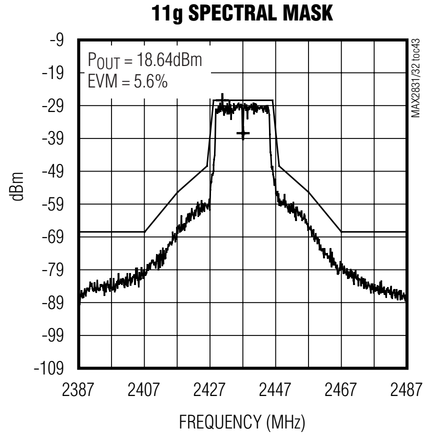
Tx GAIN VARIATION vs. FREQUENCY (B6:B1 = 101001)



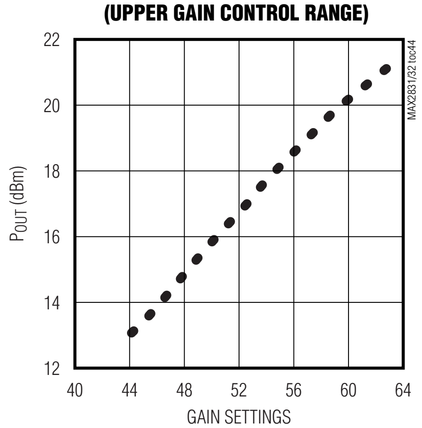
Tx OUTPUT POWER vs. FREQUENCY



11g SPECTRAL MASK



802.11g P_{OUT} vs. GAIN SETTING (UPPER GAIN CONTROL RANGE)

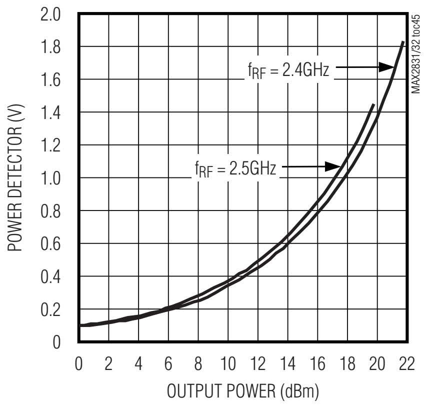


2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

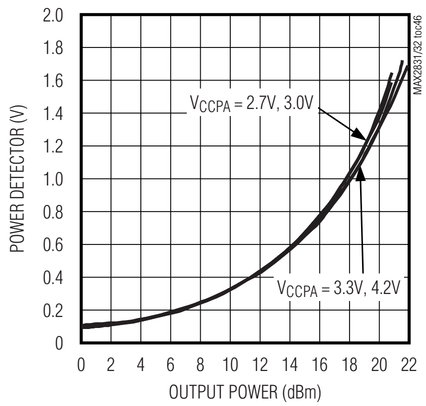
Typical Operating Characteristics (continued)

(MAX2831 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

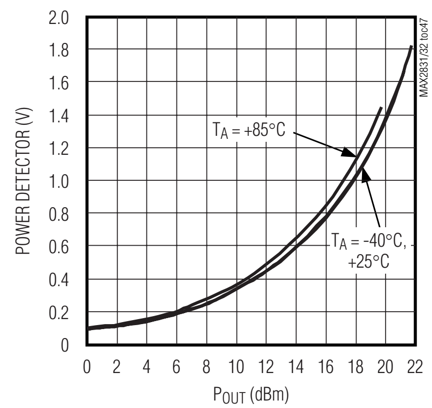
POWER DETECTOR OVER FREQUENCY



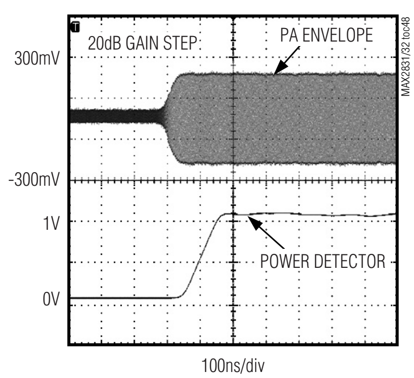
POWER DETECTOR OVER SUPPLY VOLTAGE



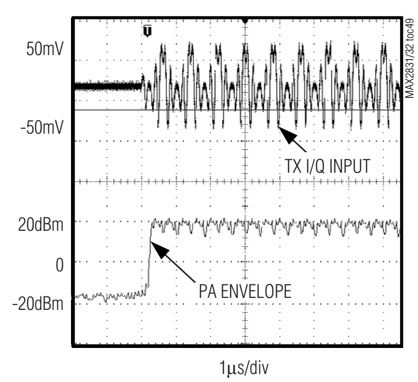
POWER DETECTOR OVER TEMPERATURE



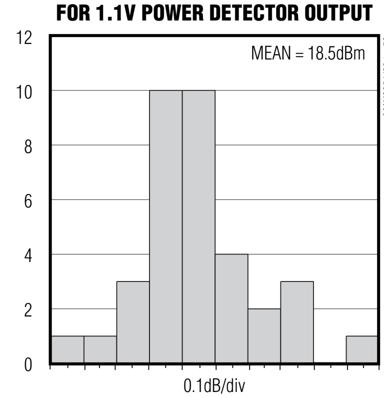
POWER-DETECTOR OUTPUT



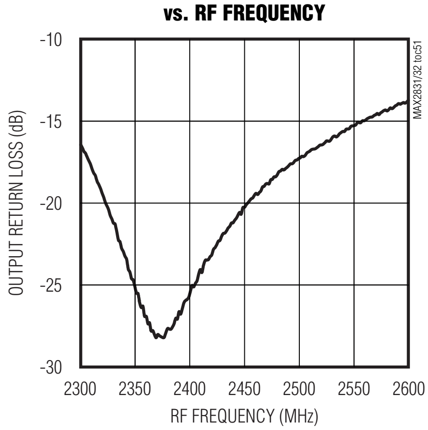
PA OUTPUT ENVELOPE RESPONSE



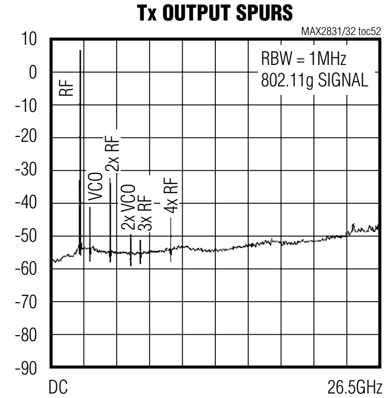
PA OUTPUT POWER HISTORGRAM FOR 1.1V POWER DETECTOR OUTPUT



PA OUTPUT RETURN LOSS vs. RF FREQUENCY



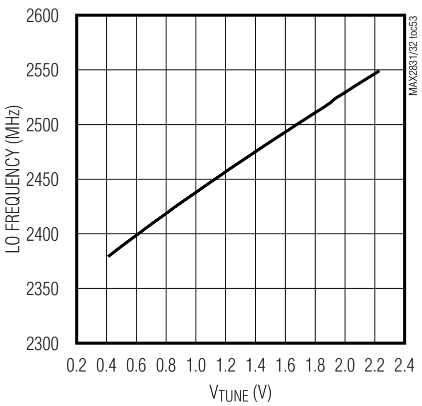
Tx OUTPUT SPURS



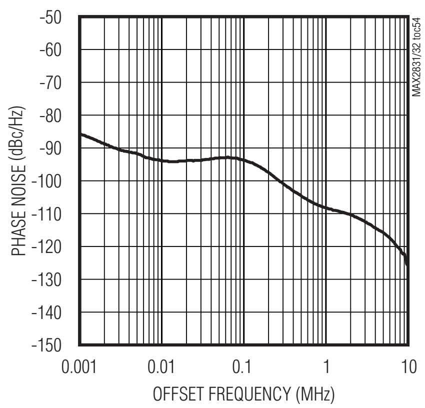
Typical Operating Characteristics (continued)

(MAX2831 EV kit, $V_{CC\_}$ = 2.8V, V_{CCPA} = V_{CCTXPA} = 3.3V, T_A = +25°C, f_{LO} = 2.437GHz, f_{REF} = 40MHz, $\overline{SHDN}$ = $\overline{CS}$ = high, RXHP = SCLK = DIN = low.)

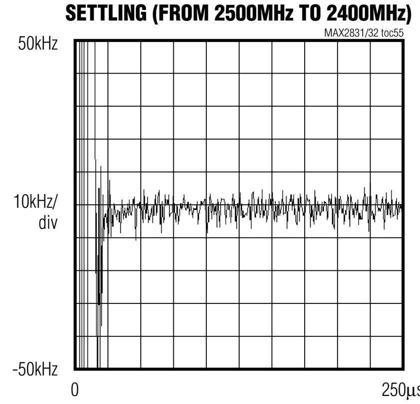
LO FREQUENCY vs. V_{TUNE}



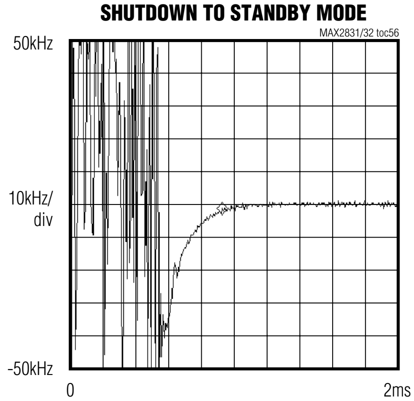
LO PHASE NOISE vs. OFFSET FREQUENCY



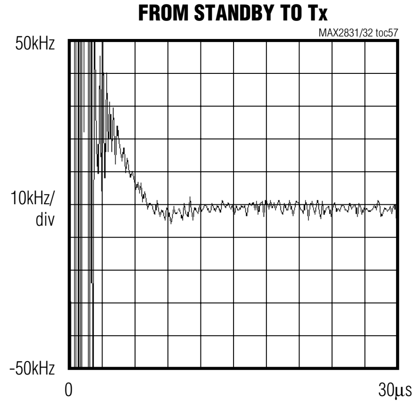
CHANNEL SWITCHING FREQUENCY SETTLING (FROM 2500MHz TO 2400MHz)



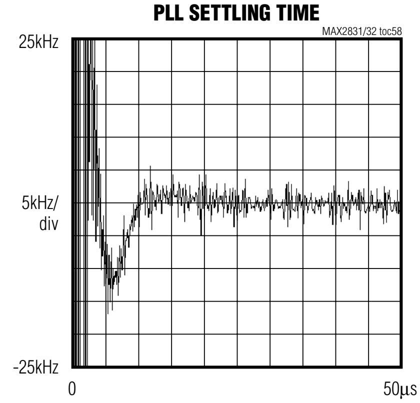
PLL SETTLING TIME FROM SHUTDOWN TO STANDBY MODE



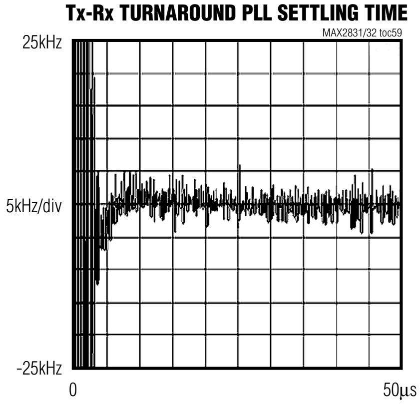
PLL SETTLING TIME FROM STANDBY TO Tx



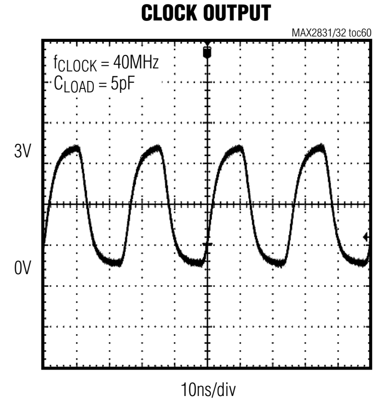
Rx TO Tx TURNAROUND PLL SETTLING TIME



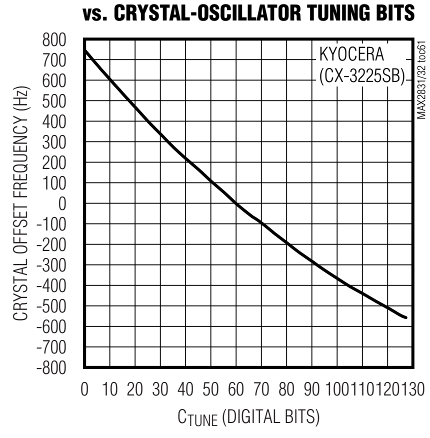
Tx-Rx TURNAROUND PLL SETTLING TIME



CLOCK OUTPUT

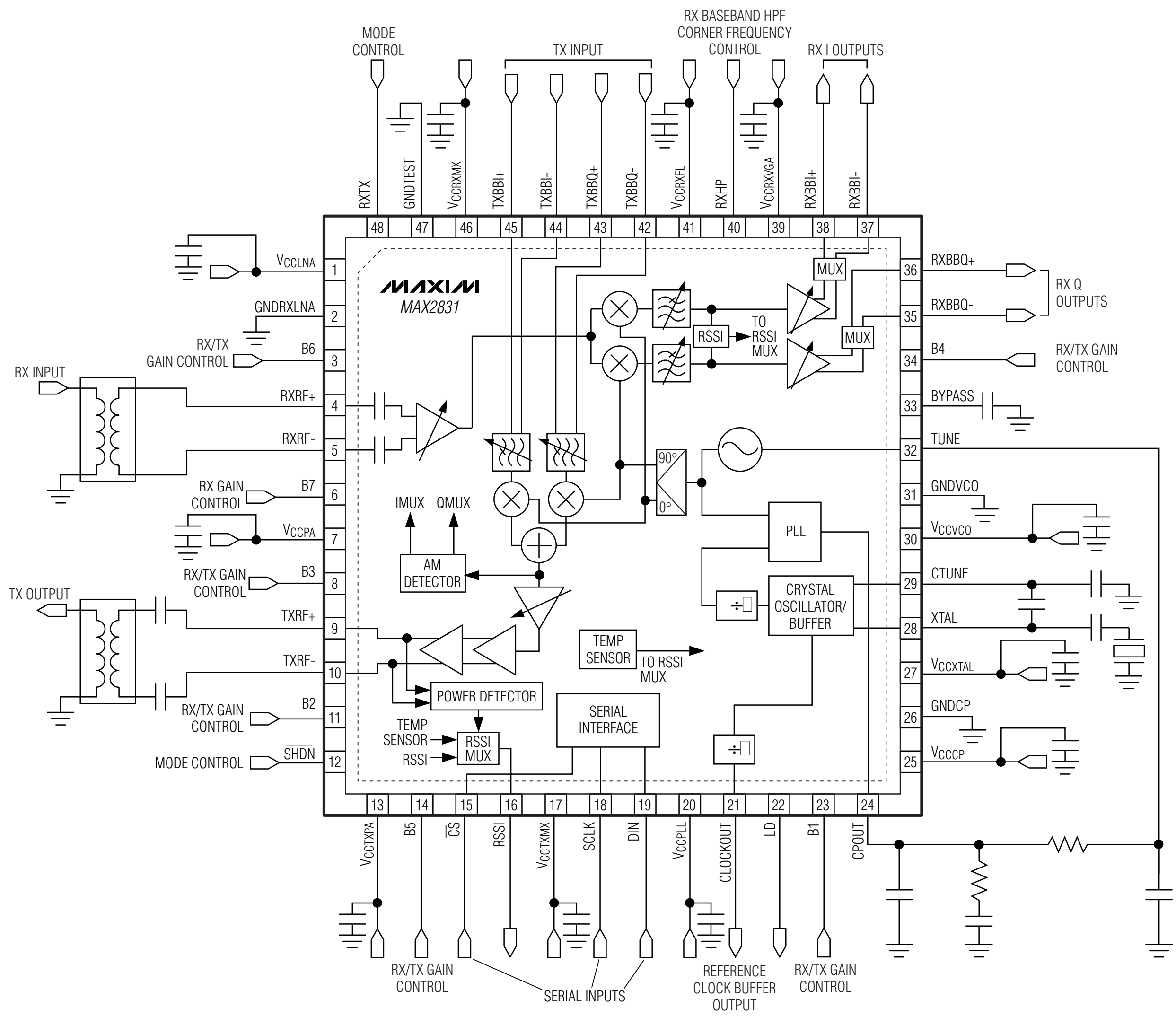


CRYSTAL-OSCILLATOR OFFSET FREQUENCY vs. CRYSTAL-OSCILLATOR TUNING BITS



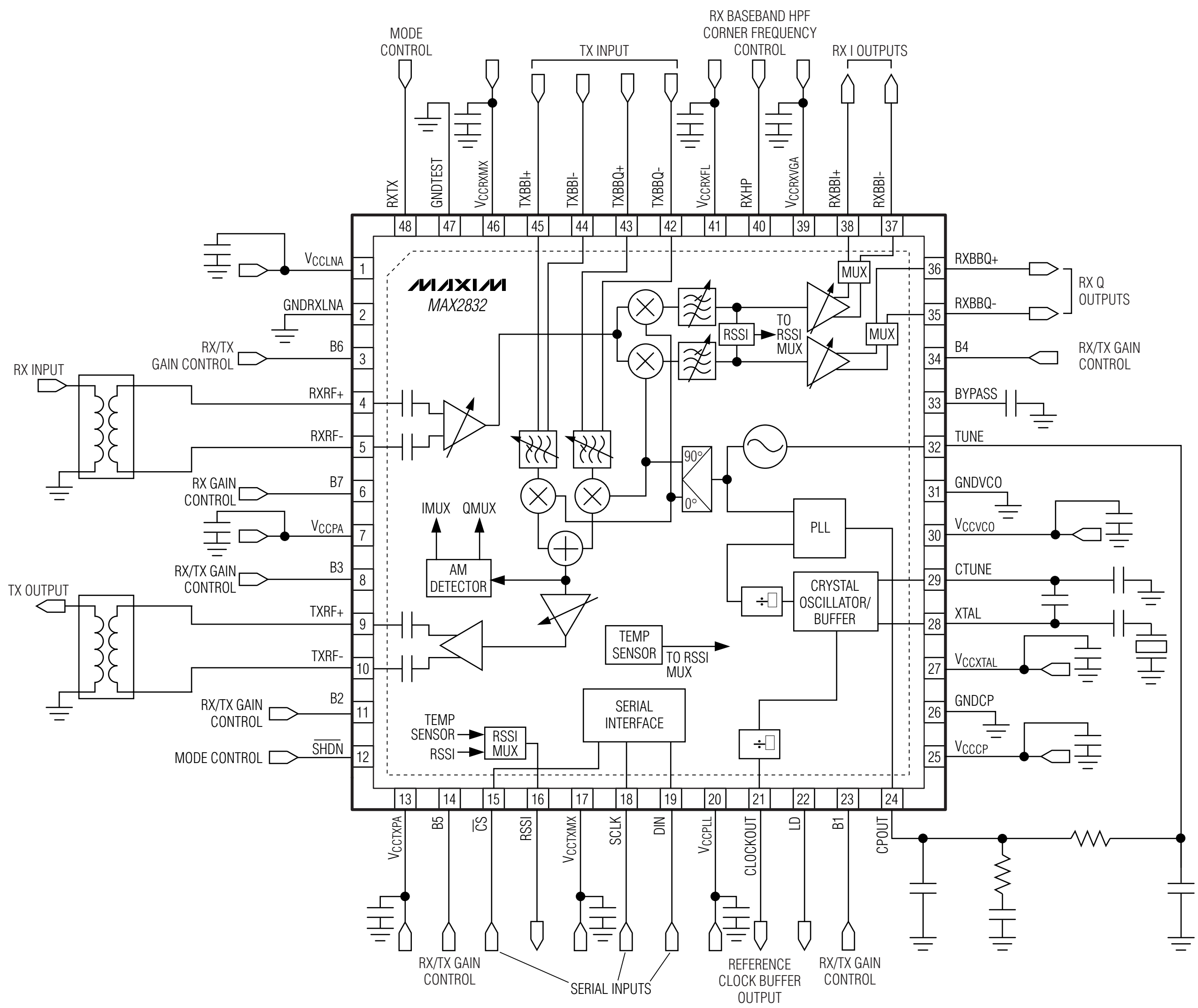
2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

Block Diagrams/Typical Operating Circuits



NOTE: ALL GROUND (PINS 2, 26, AND 31) AND BYPASS CAPACITORS' GROUND REQUIRE THEIR OWN VIAS TO GROUND.
DO NOT CONNECT THEM TO THE EXPOSED PADDLE GROUND.

Block Diagrams/Typical Operating Circuits (continued)



NOTE: ALL GROUND (PINS 2, 26, AND 31) AND BYPASS CAPACITORS' GROUND REQUIRE THEIR OWN VIAS TO GROUND. DO NOT CONNECT THEM TO THE EXPOSED PADDLE GROUND.

Pin Description

PIN	NAME	FUNCTION
1	V_{CCLNA}	LNA Supply Voltage
2	GNDRXLNA	LNA Ground
3	B6	Receiver and Transmitter Gain-Control Logic-Input Bit 6
4	RXRF+	LNA Differential Input. Input is internally AC-coupled and matched to 100Ω differential. Connect directly to a 2:1 balun.
5	RXRF-	
6	B7	Receiver Gain-Control Logic-Input Bit 7
7	V_{CCPA}	Supply Voltage for Second Stage of Power Amplifier
8	B3	Receiver and Transmitter Gain-Control Logic-Input Bit 3
9	TXRF+	Power-Amplifier Differential Output for the MAX2831. PA output must be AC-coupled. PA driver internally AC-coupled differential outputs and matched to 100Ω differential for the MAX2832. Connect directly to a 2:1 balun.
10	TXRF-	
11	B2	Receiver and Transmitter Gain-Control Logic-Input Bit 2
12	$\overline{SHDN}$	Active-Low Shutdown and Standby Logic Input. See Table 31 for operating modes.
13	V_{CCTXPA}	Supply Voltage for First-Stage of PA and PA Driver
14	B5	Receiver and Transmitter Gain-Control Logic-Input Bit 5
15	$\overline{CS}$	Active-Low Chip-Select Logic Input of 3-Wire Serial Interface (See Figure 2)
16	RSSI	RSSI, PA Power Detector (MAX2831 Only) or Temperature-Sensor Multiplexed Analog Output
17	V_{CCTXMX}	Transmitter Upconverter Supply Voltage
18	SCLK	Serial-Clock Logic Input of 3-Wire Serial Interface (See Figure 2)
19	DIN	Data Logic Input of 3-Wire Serial Interface (See Figure 2)
20	V_{CCPLL}	PLL and Registers Supply Voltage. Connect to the supply voltage to retain the register settings.
21	CLOCKOUT	Reference Clock Buffer Output
22	LD	Lock-Detect Logic Output of Frequency Synthesizer. Output high indicates that the frequency synthesizer is locked. Output programmable as CMOS or open-drain output. (See Tables 16 and 20.)
23	B1	Receiver and Transmitter Gain-Control Logic-Input Bit 1
24	CPOUT	Charge-Pump Output. Connect the frequency synthesizer's loop filter between CPOUT and TUNE (see the *Block Diagrams/Typical Operating Circuits*).
25	V_{CCCP}	PLL Charge-Pump Supply Voltage
26	GNDCP	Charge-Pump Circuit Ground
27	V_{CCXTAL}	Crystal Oscillator Supply Voltage
28	XTAL	Crystal or Reference Clock Input. AC-couple a crystal or a reference clock to this analog input.
29	CTUNE	Connection for Crystal Oscillator Off-Chip Capacitors. When using an external reference clock input, leave CTUNE unconnected.
30	V_{CCVCO}	VCO Supply Voltage
31	GNDVCO	VCO Ground
32	TUNE	VCO TUNE Input (see the *Block Diagrams/Typical Operating Circuits*)
33	BYPASS	On-Chip VCO Regulator Output Bypass. Bypass with a 0.1µF to 1µF capacitor to GND. Do not connect other circuitry to this point.
34	B4	Receiver and Transmitter Gain-Control Logic-Input Bit 4

Pin Description (continued)

PIN	NAME	FUNCTION
35	RXBBQ-	Receiver Baseband Q-Channel Differential Outputs. In TX calibration mode, these pins are the LO leakage and sideband detector outputs.
36	RXBBQ+	
37	RXBBI-	Receiver Baseband I-Channel Differential Outputs. In TX calibration mode, these pins are the LO leakage and sideband detector outputs.
38	RXBBI+	
39	$V_{CCRXVGA}$	Receiver VGA Supply Voltage
40	RXHP	Receiver Baseband AC-Coupling High-Pass Corner Frequency Control Logic Input
41	V_{CCRXFL}	Receiver Baseband Filter Supply Voltage
42	TXBBQ-	Transmitter Baseband I-Channel Differential Inputs
43	TXBBQ+	
44	TXBBI-	Transmitter Baseband Q-Channel Differential Inputs
45	TXBBI+	
46	V_{CCRXMX}	Receiver Downconverters Supply Voltage
47	GNDTEST	Connect to Ground
48	RXTX	RX/TX Mode Control Logic Input. See Table 31 for operating modes.
—	EP	Exposed Paddle. Connect to the ground plane with multiple vias for proper operation and heat dissipation. Do not share with any other pin grounds and bypass capacitors' ground.

Detailed Description

The MAX2831/MAX2832 single-chip, low-power, direct conversion, zero-IF transceivers are designed to support 802.11g/b applications operating in the 2.4GHz to 2.5GHz band. The fully integrated transceivers include a receive path, transmit path, voltage-controlled oscillator (VCO), sigma-delta fractional-N synthesizer, crystal oscillator, RSSI, PA power detector (MAX2831), temperature sensor, Rx and Tx I/Q error-detection circuitry, baseband-control interface and linear power amplifier (MAX2831). The only additional components required to implement a complete radio front-end solution are a crystal, a pair of baluns, a BPF, a switch, and a small number of passive components (RCs, no inductors required).

Receiver

The fully integrated receiver achieves a noise figure of 2.6dB in high-gain mode, and an input compression point of -6dBm in low-gain mode, while consuming only 62mA of supply current. The receiver integrates an LNA and VGA with a 95dB digitally programmable gain control range, direct-conversion downconverters, I/Q baseband lowpass filters with programmable LPF corner frequencies, analog RSSI and integrated DC-offset correction circuitry. A logic-low on the RXTX input (pin 48) and a logic-high on the $\overline{SHDN}$ input (pin 12) enable the receiver.

LNA Input Matching

The LNA features a differential input that is internally AC-coupled and internally matched to 100Ω. Connect a 2:1 balun transformer directly to the RXRF+ (pin 4) and RXRF- (pin 5) ports to convert the differential 100Ω input impedance to a single-ended 50Ω input. Provide electrically symmetrical input traces from the LNA input to the balun to maintain IP2 performance and RF common-mode noise rejection.

LNA Gain Control

The LNA has three gain modes: max gain, max gain - 16dB, and max gain - 33dB. The three LNA gain modes can be serially programmed through the SPI™ interface by programming bits D6:D5 in Register 11 (A3:A0 = 1011) or programmed in parallel through the digital logic gain-control pins, B7 (pin 6) and B6 (pin 3). Set bit D12 = 1 in Register 8 (A3:A0 = 1000) to enable programming through the SPI interface, or set bit D12 = 0 to enable parallel programming. See Table 1 for LNA gain-control settings.

Table 1. LNA Gain-Control Settings (Pins B7:B6 or Register A3:A0 = 1011, D6:D5)

B7 OR D6	B6 OR D5	NAME	DESCRIPTION
1	1	High	Max gain
1	0	Medium	Max gain - 16dB (typ)
0	X	Low	Max gain - 33dB (typ)

SPI is a trademark of Motorola, Inc.

Baseband Variable-Gain Amplifier

The receiver baseband variable-gain amplifiers provide 62dB of gain control range programmable in 2dB steps. The VGA gain can be serially programmed through the SPI interface by setting bits D4:D0 in Register 11 (A3:A0 = 1011) or programmed in parallel through the digital logic gain-control pins, B5 (pin 14), B4 (pin 34), B3 (pin 8), B2 (pin 11), and B1 (pin 23). Set bit D12 = 1 in Register 8 (A3:A0 = 1000) to enable serial programming through the serial interface or set bit D12 = 0 to enable parallel programming through the external logic pins. See Table 2 for the gain-step value and Table 3 for baseband VGA gain-control settings.

Receiver Baseband Lowpass Filter

The receiver integrates lowpass filters that provide an upper -3dB corner frequency of 8.5MHz (nominal mode) with 50dB of attenuation at 20MHz, and 45ns of group delay ripple in the passband (10kHz to 8.5MHz). The upper -3dB corner frequency is tightly controlled on-chip and does not require user adjustment. However, provisions are made to allow fine tuning of the upper -3dB corner frequency. In addition, coarse frequency tuning allows the -3dB corner frequency to be set to 7.5MHz (11b mode), 8.5MHz (11g mode), 15MHz (turbo 1 mode), and 18MHz (turbo 2 mode) by programming bits D1:D0 in Register 8 (A3:A0 = 1000). See Table 4. The coarse corner frequency can be fine-tuned approximately ±10% in 5% steps by programming bits D2:D0 in Register 7 (A3:A0 = 0111). See Table 5 for receiver LPF fine -3dB corner frequency adjustment.

Table 2. Receiver Baseband VGA Gain-Step Value (Pins B5:B1 or Register D4:D0, A3:A0 = 1011)

PIN/BIT	GAIN STEP (dB)
B1/D0	2
B2/D1	4
B3/D2	8
B4/D3	16
B5/D4	32

Table 3. Baseband VGA Gain-Control Settings in Receiver Gain-Control Register (Pin B5:B1 or Register D4:D0, A3:A0 = 1011)

B5:B1 OR D4:D0	GAIN
11111	Max
11110	Max - 2dB
11101	Max - 4dB
:	:
00000	Min

Baseband Highpass Filter and DC Offset Correction

The receiver implements programmable AC and near-DC coupling of I/Q baseband signals. Temporary AC-coupling is used to quickly remove LO leakage and other DC offsets that could saturate the receiver outputs. When DC offsets have settled, near DC-coupling is enabled to avoid attenuation of the received signal. AC-coupling is set (-3dB highpass corner frequency of 600kHz) when a logic-high is applied to RXHP (pin 40). Near DC-coupling is set (-3dB highpass corner frequency of 100Hz nominal) when a logic-low is applied to RXHP. Bits D13:D12 in Register 7 (A3:A0 = 0111) allow the near DC-coupling -3B highpass corner frequency to be set to 100Hz (D13:D12 = 00), 4kHz (D13:D12 = X1), or 30kHz (D13:D12 = 10). See Table 6.

Table 4. Receiver LPF Coarse -3dB Corner Frequency Settings in Register (A3:A0 = 1000)

BITS (D1:D0)	-3dB CORNER FREQUENCY (MHz)	MODE
00	7.5	11b
01	8.5	11g
10	15	Turbo 1
11	18	Turbo 2

Table 5. Receiver LPF Fine -3dB Corner Frequency Adjustment in Register (A3:A0 = 0111)

BITS (D2:D0)	% ADJUSTMENT RELATIVE TO COARSE SETTING
000	90
001	95
010	100
011	105
100	110

Table 6. Receiver Highpass Filter -3dB Corner Frequency Programming

RXHP	A3:A0 = 0111, D13:D12	-3dB HIGHPASS CORNER FREQUENCY (Hz)
1	XX	600k
0	00	100 (recommended)
0	X1	4k
0	10	30k

X = Don't care.

Receiver I/Q Baseband Outputs

The differential outputs (RXBBI+, RXBBI-, RXBBQ+, RXBBQ-) of the baseband amplifiers have a differential output impedance of ~300Ω, and are capable of driving differential loads up to 10kΩ || 10pF. The outputs are internally biased to a common-mode voltage of 1.1V and are intended to be DC-coupled to the in-phase (I) and quadrature (Q) analog-to-digital data converter inputs of the accompanying baseband IC. Additionally, the common-mode output voltage can be adjusted from 1.1V to 1.4V through programming bits D11:D10 in Register 15 (A3:A0 = 1111).

Received Signal-Strength Indicator (RSSI)

The RSSI output (pin 16) can be programmed to multiplex an analog output voltage proportional to the received signal strength, the PA output power (MAX2831), or the die temperature. Set bits D9:D8 = 00 in Register 8 (A3:A0 = 1000) to enable the RSSI output in receive mode (off in transmit mode). Set bit D10 = 1 to enables the RSSI output when RXHP = 1, and disable the RSSI output when RXHP = 0. Set bit D10 = 0 to enable the RSSI output independent of RXHP. See Table 7 for a summary of the RSSI output versus register programming and RXHP.

The received signal strength indicator provides an analog voltage proportional to the log of the sum of the squares of the I and Q channels, measured after the receive baseband filters and before the variable-gain amplifiers. The RSSI analog output voltage is proportional to the RF input signal level and LNA gain state over a 60dB range, and is not dependent upon VGA gain. See the graph RX RSSI Output vs. Input Power in the *Typical Operating Characteristics* for further details.

Transmitter

The transmitter integrates baseband lowpass filters, direct-upconversion mixers, a VGA, a PA driver, and a linear RF PA with a power detector (MAX2831). A logic-high on the RXTX input (pin 48) and a logic-high on the $\overline{SHDN}$ input (pin 12) enable the transmitter.

Transmitter I/Q Baseband Inputs

The differential analog inputs of the transmitter baseband amplifier I/Q inputs (TXBBI+, TXBBI-, TXBBQ+, TXBBQ-) have a differential impedance of 20kΩ || 1pF. The inputs require an input common-mode voltage of 0.9V to 1.3V, which is provided by the DC-coupled I and Q DAC outputs of the accompanying baseband IC.

Transmitter Baseband Lowpass Filtering

The transmitter integrates lowpass filters that can be tuned to -3dB corner frequencies of 8MHz (11b), 11MHz (11g), 16.5MHz (turbo 1 mode), and 22.5MHz (turbo 2 mode) through programming bits D1:D0 in Register 8 (A3:A0 = 1000) and bit D5:D3 in Register 7 (A3:A0 = 0111). The -3dB corner-frequency is tightly controlled on-chip and does not require user adjustment. Additionally, provisions are made to fine tune the -3dB corner frequency through bits D5:D3 in the Filter Programming register (A3:A0 = 0111). See Tables 8 and 9.

Table 7. RSSI Pin Truth Table

INPUT CONDITIONS			RSSI OUTPUT
A3:A0 = 1000, D9:D8	A3:A0 = 1000, D10	RXHP	
X	0	0	No signal
00	0	1	RSSI
01	0	1	Temperature sensor
10	0	1	Power detector (MAX2831)
00	1	X	RSSI
01	1	X	Temperature sensor
10	1	X	Power detector (MAX2831)

X = Don't care.

Table 8. Transmitter LPF Coarse -3dB Corner Frequency Settings in Register (A3:A0 = 1000)

BITS (D1:D0)	-3dB CORNER FREQUENCY (MHz)	MODE
00	8	11b
01	11	11g
10	16.5	Turbo 1
11	22.5	Turbo 2

Table 9. Transmitter LPF Fine -3dB Corner Frequency Adjustment in Register (A3:A0 = 0111)

BITS (D5:D3)	% ADJUSTMENT RELATIVE TO COARSE SETTING
000	90
001	95
010	100
011	105
100	110 (11g)
101	115
101–111	Not used

2.4GHz to 2.5GHz 802.11g/b RF Transceivers with Integrated PA

Transmitter Variable-Gain Amplifier

The variable-gain amplifier of the transmitter provides 31dB of gain control range programmable in 0.5dB steps over the top 8dB of the gain control range and in 1dB steps below that. The transmitter gain can be programmed serially through the SPI interface by setting bits D5:D0 in Register 12 (A3:A0 = 1100) or in parallel through the digital logic gain-control pins B6:B1 (pins 3, 6, 8, 11, 14, 23, and 34, respectively). Set bit D10 = 0 in Register 9 (A3:A0 = 1001) to enable parallel programming, and set bit D10 = 1 to enable programming through the 3-wire serial interface. See Table 10 for the transmitter VGA gain-control settings.

Table 10. Transmitter VGA Gain-Control Settings

NUMBER	D5:D0 Or B6:B1	OUTPUT SIGNAL POWER
63	111111	Max
62	111110	Max - 0.5dB
61	111101	Max - 1.0dB
:	:	:
49	110001	Max - 7dB
48	110000	Max - 7.5dB
47	101111	Max - 8dB
46	101110	Max - 8dB
45	101101	Max - 9dB
44	101100	Max - 9dB
:	:	:
5	000101	Max - 29dB
4	000100	Max - 29dB
3	000011	Max - 30dB
2	000010	Max - 30dB
1	000001	Max - 31dB
0	000000	Max - 31dB

Power-Amplifier Driver Output Matching (MAX2832)

The PA driver of the MAX2832 has a 100Ω differential output with on-chip AC-coupling capacitors. Provide electrically symmetrical traces to present a balanced load to the PA driver output to help maintain driver linearity and RF common-mode rejection.

Power-Amplifier Bias, Enable Delay and Output Matching (MAX2831)

The MAX2831 integrates a 2-stage PA, providing +18.5dBm of output power at 5.6% EVM (54Mbps OFDM signal) in 802.11g mode while exceeding the 802.11g spectral mask requirements. The first and second stage PA bias currents are set through programming bits D2:D0 and bits D6:D3 in Register 10 (A3:A0 = 1010), respectively. An adjustable PA enable delay, relative to the transmitter enable (RXTX low-to-high transition), can be set from 200ns to 7µs through programming bits D13:D10 in Register 10 (A3:A0 = 1010).

The PA of the MAX2831 has a 100Ω differential output that is internally matched. The output has to be AC-coupled using two off-chip 1.5pF capacitors to a 100Ω:50Ω balun. Provide electrically symmetrical traces from the PA output to the balun to present a balanced load and to reduce out-of-band spurs.

Power Detector (MAX2831)

The MAX2831 integrates a voltage-peak detector at the PA output and provides an analog voltage proportional to PA output power. See the Power Detector Over Frequency and Power Detector Over Supply Voltage graphs in the *Typical Operating Characteristics*. Set bits D9:D8 = 10 in Register 8 (A3:A0 = 1000) to multiplex the power-detector analog output voltage to the RSSI output (pin 16).

Synthesizer Programming

The MAX2831/MAX2832 integrate a 20-bit sigma-delta fractional-N synthesizer, allowing the device to achieve excellent phase-noise performance (0.9° RMS from 10kHz to 10MHz), fast PLL settling times, and an RF frequency step-size of 20Hz. The synthesizer includes a divide-by-1 or a divide-by-2 reference frequency divider, an 8-bit integer portion main divider with a divisor range programmable from 64 to 255, and a 20-bit fractional portion main-divider. Bit D2 in Register 5 (A3:A0 = 0101) sets the reference oscillator divider ratio to 1 or 2. Bits D7:D0 in Register 3 (A3:A0 = 0011) set the integer portion of the main divider. The 20-bit fractional portion of the main-divider is split between two registers. The 14 MSBs of the fractional portion are set in Register 4 (A3:A0 = 0100), and the 6 LSBs of the fractional portion of the main divider are set in Register 3 (A3:A0 = 0011). See Tables 11 and 12.

Calculating Integer and Fractional Divider Ratios

The desired integer and fractional divider ratios can be calculated by dividing the RF frequency (f_{RF}) by f_{COMP}. For nominal 802.11g/b operation, a 40MHz reference oscillator is divided by 2 to generate a 20MHz comparison frequency (f_{COMP}). The following method can be used when calculating divider ratios supporting various reference and comparison frequencies:

LO Frequency Divider = f_{RF} / f_{COMP} = 2437MHz / 20MHz = 121.85

Integer Divider = 121 (d) = 0111 1001 (binary)

Fractional Divider = 0.85 x (2^{20} - 1) = 891289 (decimal) = 1101 1001 1001 1001 1001

See Table 13 for integer and fractional divider ratios for 802.11g/b systems using a 20MHz comparison frequency.

Table 11. Integer Divider Register (A3:A0 = 0011)

BIT	RECOMMENDED	DESCRIPTION
D13:D8	00000	6 LSBs of 20-Bit Fractional Portion of Main Divider
D7:D0	01111001	8-Bit Integer Portion of Main Divider. Programmable from 64 to 255.

Table 12. Fractional Divider Register (A3:A0 = 0100)

BIT	RECOMMENDED	DESCRIPTION
D13:D0	11011001100110	14 MSBs of 20-Bit Fractional Portion of Main Divider

Table 13. IEEE 802.11g/b Divider-Ratio Programming Words

f_{RF} (MHz)	(f_{RF} / f_{COMP})	INTEGER DIVIDER	FRACTIONAL DIVIDER	
		A3:A0 = 0011, D7:D0	A3:A0 = 0100, D13:D0	A3:A0 = 0011, D13:D8
2412	120.6	0111 1000b	2666h	1Ah
2417	120.85	0111 1000b	3666h	1Ah
2422	121.1	0111 1001b	0666h	1Ah
2427	121.35	0111 1001b	1666h	1Ah
2432	121.6	0111 1001b	2666h	1Ah
2437	121.85	0111 1001b	3666h	1Ah
2442	122.1	0111 1010b	0666h	1Ah
2447	122.35	0111 1010b	1666h	1Ah
2452	122.6	0111 1010b	2666h	1Ah
2457	122.85	0111 1010b	3666h	1Ah
2462	123.1	0111 1011b	0666h	1Ah
2467	123.35	0111 1011b	1666h	1Ah
2472	123.6	0111 1011b	2666h	1Ah
2484	124.2	0111 1100b	0CCCh	33h